

N-Channel Power MOSFET

700V, 8A, 0.6Ω

FEATURES

- Super-Junction technology
- High performance, small $R_{DS(on)} \cdot Q_g$ figure of merit (FOM)
- High ruggedness performance
- 100% UIS and R_g tested
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

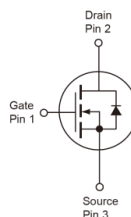
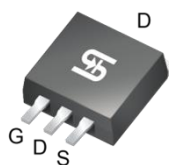
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	700	V
$R_{DS(on)}$ (max)	0.6	Ω
Q_g	12.6	nC

APPLICATIONS

- Power Supply
- AC/DC LED Lighting



TO-262S (I²PAK SL)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	700	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	8	A
	$T_C = 100^\circ\text{C}$		4.6	A
Pulsed Drain Current (Note 2)		I_{DM}	24	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$		P_D	83	W
Single Pulse Avalanche Energy (Note 3)		E_{AS}	100	mJ
Single Pulse Avalanche Current (Note 3)		I_{AS}	2	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.5	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	700	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.0	2.9	4.0	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 700V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	V _{GS} = 10V, I _D = 2.4A	R _{DS(on)}	--	0.53	0.6	Ω
Dynamic (Note 5)						
Total Gate Charge	V _{DS} = 380V, I _D = 8A, V _{GS} = 10V	Q _g	--	12.6	--	nC
Gate-Source Charge		Q _{gs}	--	2.9	--	
Gate-Drain Charge		Q _{gd}	--	4.5	--	
Input Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	743	--	pF
Output Capacitance		C _{oss}	--	63	--	
Gate Resistance	f = 1.0MHz	R _g	--	3.6	7.2	Ω
Switching (Note 6)						
Turn-On Delay Time	V _{DD} = 380V, R _{GEN} = 25Ω, I _D = 8A, V _{GS} = 10V	t _{d(on)}	--	36	--	ns
Turn-On Rise Time		t _r	--	21	--	
Turn-Off Delay Time		t _{d(off)}	--	95	--	
Turn-Off Fall Time		t _f	--	21	--	
Source-Drain Diode						
Forward On Voltage (Note 4)	I _S = 8A, V _{GS} = 0V	V _{SD}	--	--	1.4	V
Reverse Recovery Time	V _R =200V, I _S = 4A dI _F /dt = 100A/μs	t _{rr}	--	187.9	--	ns
Reverse Recovery Charge		Q _{rr}	--	1.4	--	μC

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 50mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

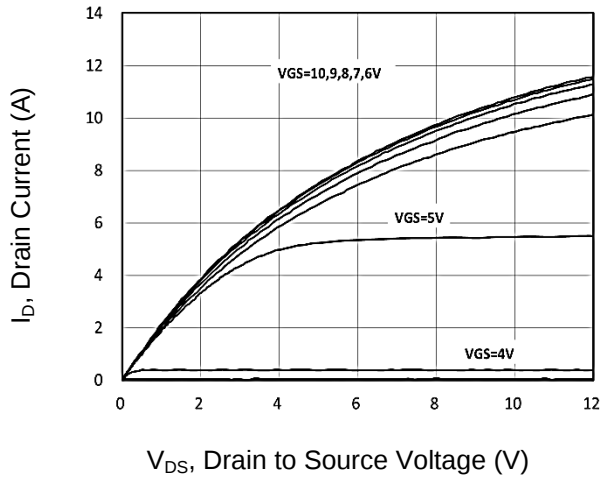
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM70N600ACL X0G	TO-262S (I ² PAK SL)	50pcs / Tube

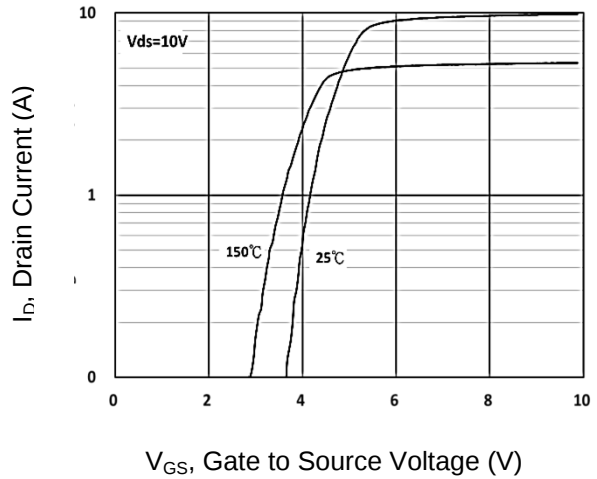
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

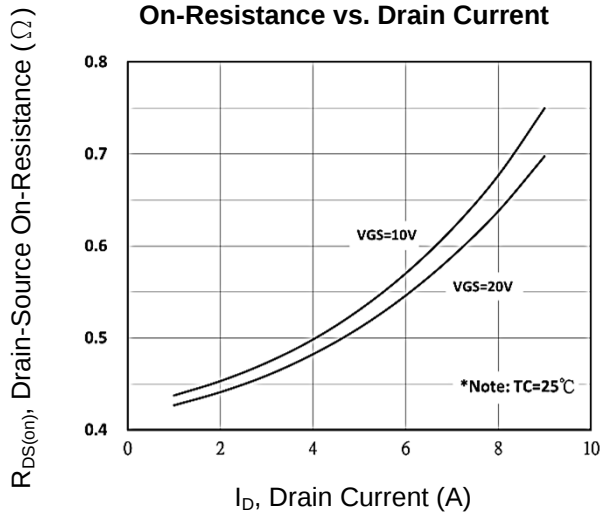
Output Characteristics



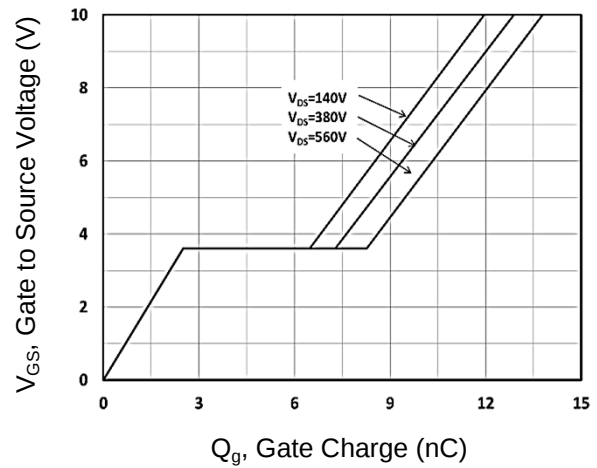
Transfer Characteristics



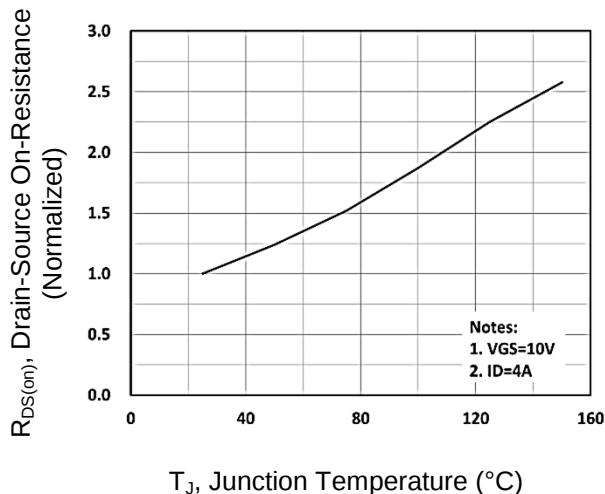
On-Resistance vs. Drain Current



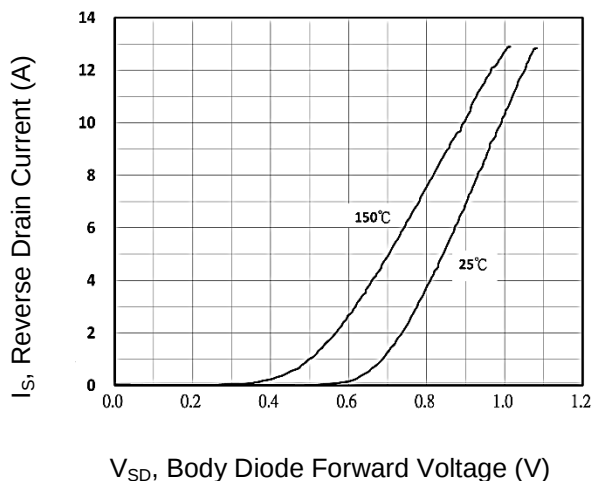
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



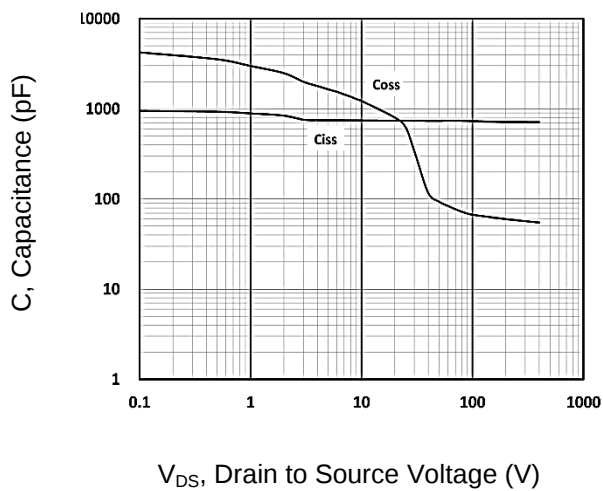
Source-Drain Diode Forward Current vs. Voltage



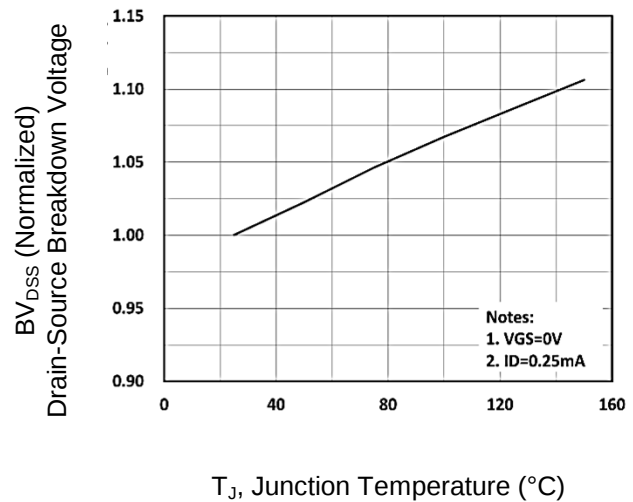
CHARACTERISTICS CURVES

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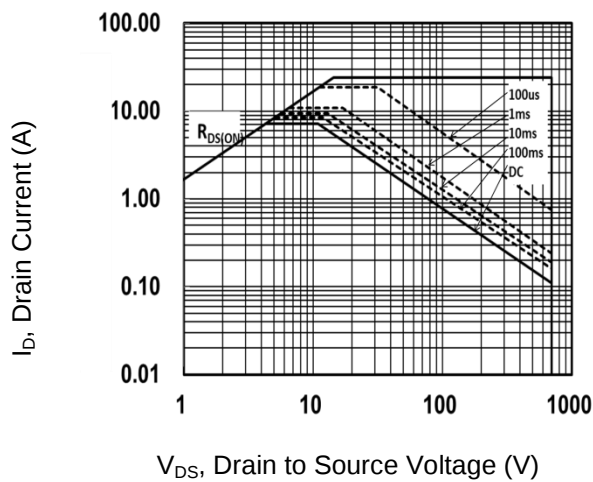
Capacitance vs. Drain-Source Voltage



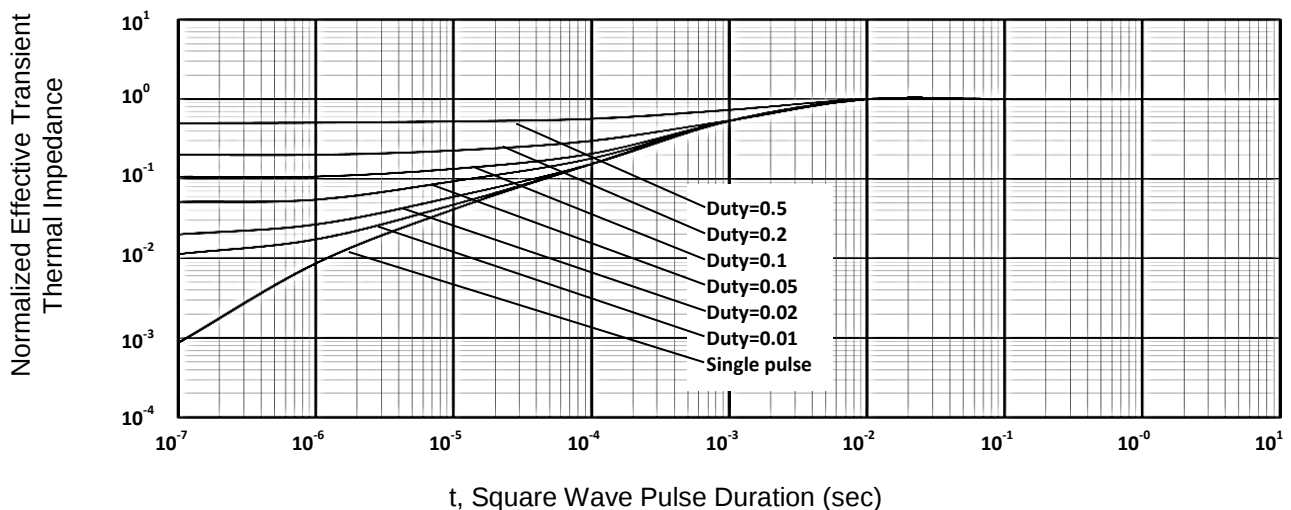
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area, Junction-to-Case

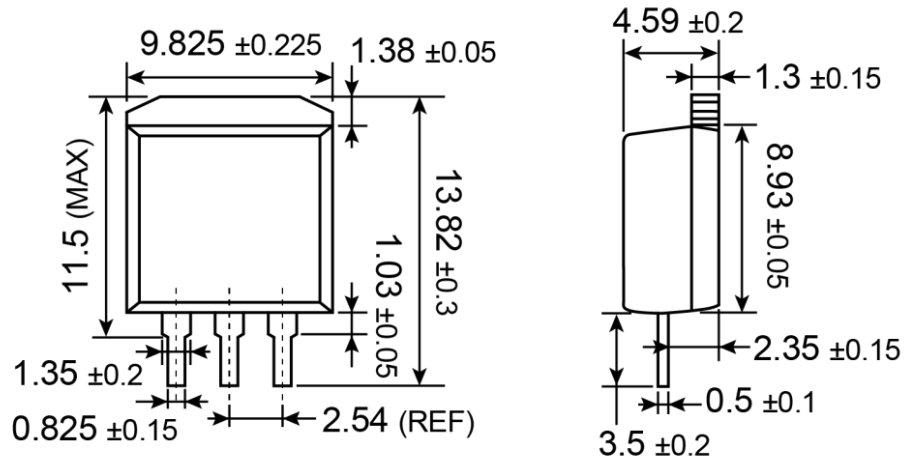


Normalized Thermal Transient Impedance, Junction-to-Case

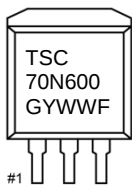


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-262S



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9