

# nanoSmart® Ultra-Low-Power Linear Regulator

## DESCRIPTIONS

The TS14001 linear regulator is an ultra-low-power circuit which draws low nA level quiescent current at light load, but has the capability to regulate current loads as high as 200mA.

## APPLICATIONS

- Portable electronics
- RFID
- Industrial
- Medical
- Energy harvesting systems
- SmartCard

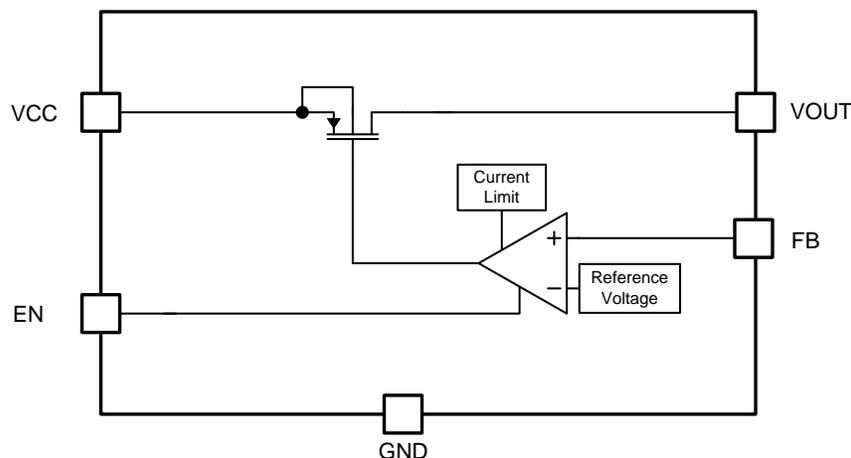
## FEATURES

- **Ultra-low nA operating current at light load**
- **Best-in-class quiescent current of 20nA at  $I_{load}=0$**
- **Best-in-class quiescent current of 100pA in disable mode**
- **Output voltage options of 1.2V - 4.2V in 100mV steps (programmed at manufacturing)**
- Accurate output regulation
- Over-current protection

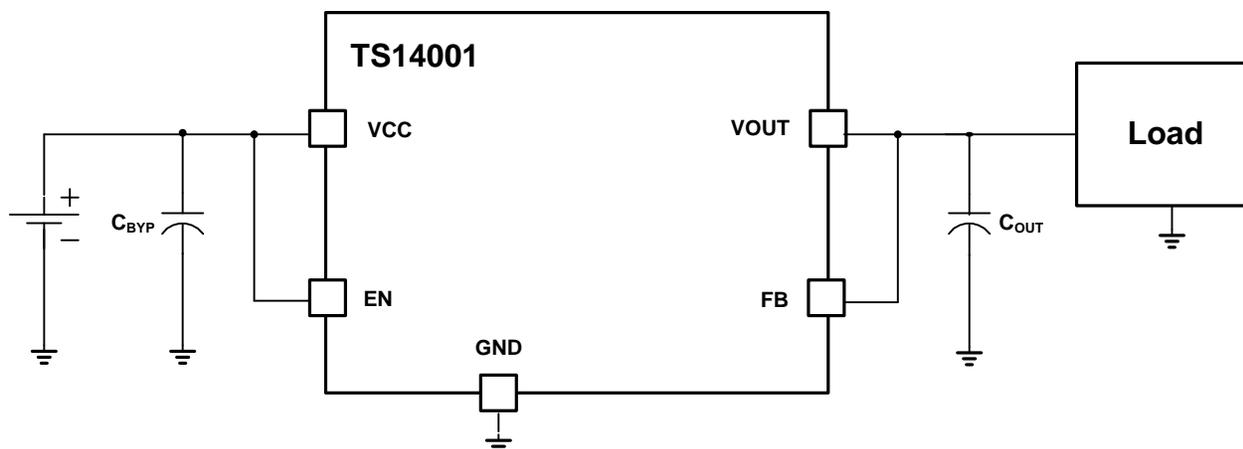
## SUMMARY SPECIFICATIONS

- Low input operating voltage of 2.5V to 5.5V
- Packaged in a 8pin VDFN (2x2)

## Block Diagram



## TYPICAL APPLICATION



## PIN-OUT CONFIGURATION

PIN #	NAME	I/O/P	DESCRIPTION
1	GND	P	Ground
2	V <sub>OUT</sub>	O	Regulated Output Voltage
3	NC		No Connect (connect to GND or float)
4	NC		No Connect (connect to GND or float)
5	NC		No Connect (connect to GND or float)
6	FB	I	Feedback Input
7	V <sub>CC</sub>	P	Input Power
8	EN	I	Enable Input

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted<sup>(1,2,3)</sup>

PIN / PARAMETER	VALUE	UNIT
V <sub>CC</sub> , V <sub>OUT</sub> , EN, FB	-0.3 to 6.0	V
Electrostatic Discharge (Human Body Model)	2	kV
Operating Junction Temperature Range, T <sub>J</sub>	-20 to 85	°C
Storage Temperature Range, T <sub>STG</sub>	-65 to 150	°C
Lead Temperature (soldering, 10 seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: All voltage values are with respect to network ground terminal.

Note 3: ESD testing is performed according to the respective JEDEC standard.

## THERMAL CHARACTERISTICS

Package DFN	$\theta_{JA}$ (°C/W) (See Note 4)	$\theta_{JC}$ (°C/W) (See Note 5)
8 pin	73.1	10.7

Note 4: This assumes a FR4 board only.

Note 5: This assumes a 1oz. Copper JEDEC standard board with thermal vias. See Exposed Pad section and application note for more information.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Unregulated Supply Input Voltage ( $V_{CC}$ )	2.5		5.5	V
Enable Input (EN)	0		5	V
Regulated Supply Output Voltage ( $V_{OUT}$ ) typical	1.2		4.2	V
Operating Ambient Temperature, $T_A$ (Note 6)	-40		55	°C
Operating Junction Temperature, $T_J$	-40		85	°C
Input Bypass Capacitor ( $C_{BYP}$ )		2.2		uF
Output Bypass Capacitor ( $C_{OUT}$ )	1	2.2	4.7	uf

Note 6:  $T_A$  Max shown here is a guideline. Higher  $T_A$  can be tolerated if  $T_J$  does not exceed the Absolute Maximum Rating.

## CHARACTERISTICS

Electrical characteristics,  $V_{CC} = 2.5V$  to  $5V$ ,  $T_J = 25C$ , unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBAT	Input Supply Voltage		2.5		5.5	V
$V_{iL_{EN}}$	Input Low Logic Level				$0.3 \cdot V_{CC}$	V
$V_{iH_{EN}}$	Input High Logic Level		$0.7 \cdot V_{CC}$			V
$I_{qq}$	Quiescent Current	$V_{CC} = 2.5V$ to $5.5V$ , $I_{OUT} = 0$		20		nA
$I_{qq-disable}$	Quiescent Current: Disable Mode	$I_{OUT} = 0$ , $EN = 0$		100		pA
$I_{op-gnd}$	Operating Current	$V_{CC} = V_{CC\_MIN}$ , $I_{OUT} = 200mA$ (Note 7)		200		uA
		$V_{CC} = V_{CC\_NOM}$ , $I_{OUT} = 200mA$ (Note 7)		200		uA
		$V_{CC} = V_{CC\_MAX}$ , $I_{OUT} = 200mA$ (Note 7)		200		uA
$I_{out}$	Load Capability	$V_{out\_nominal}$ from 1.2V to 3.5V	0		200	mA
		$V_{out\_nominal} > 3.5V$	0		100	

Note 7: If  $V_{out\_nominal} < 2.5V$ , then  $V_{CC\_MIN} = 2.5V$ , otherwise  $V_{CC\_MIN} = V_{out} + 0.3V$ .  $V_{CC\_MAX}$  is always 5.5V.  $V_{CC\_NOM}$  is the average of  $V_{CC\_MAX}$  and  $V_{CC\_MIN}$ .

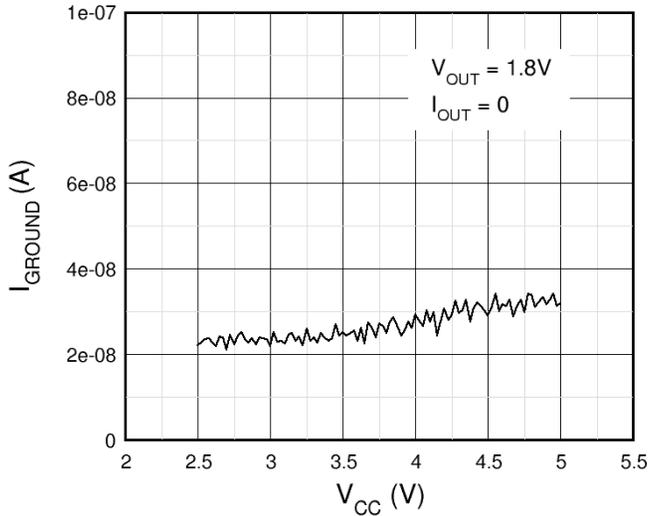
## CHARACTERISTICS CONTINUED

Electrical characteristics,  $V_{CC} = 2.5V$  to  $5V$ ,  $T_J = 25C$ , unless otherwise noted

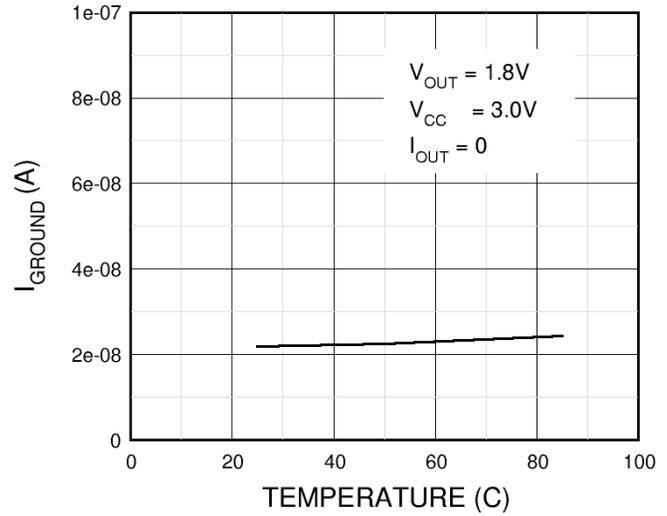
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{Line}$	DC Line Regulation	$V_{CC} = V_{CC\_MIN}$ to $V_{CC\_MAX}$ , $V_{OUT} = 1.8V$ to $4.2V$ , $I_{OUT} = 50mA$		0.5	4	%
		$V_{CC} = V_{CC\_MIN}$ to $V_{CC\_MAX}$ , $V_{OUT} < 1.8V$ , $I_{OUT} = 50mA$			4	%
$V_{Load}$	DC Load Regulation	$V_{CC} = V_{CC\_NOM}$ , $I_{OUT} = 0.02mA$ to $200mA$ ,		1	3	%
$I_{limit}$	Current Limit	$I_{OUT}$ measured at $V_{OUT} = 0.9 * V_{out\_nominal}$ ; $V_{out\_nominal}$ from $1.2V$ to $3.5V$		250		mA
		$I_{OUT}$ measured at $V_{OUT} = 0.9 * V_{out\_nominal}$ ; $V_{out\_nominal} > 3.5V$		175		

## TYPICAL CHARACTERISTICS

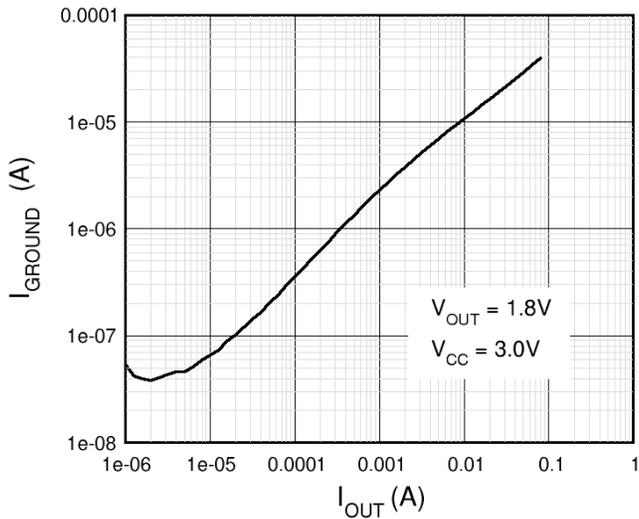
$I_{qq}$  Performance



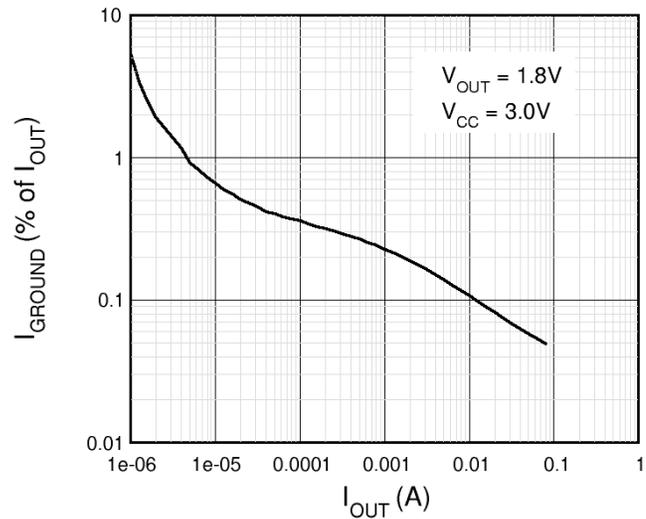
$I_{qq}$  Performance



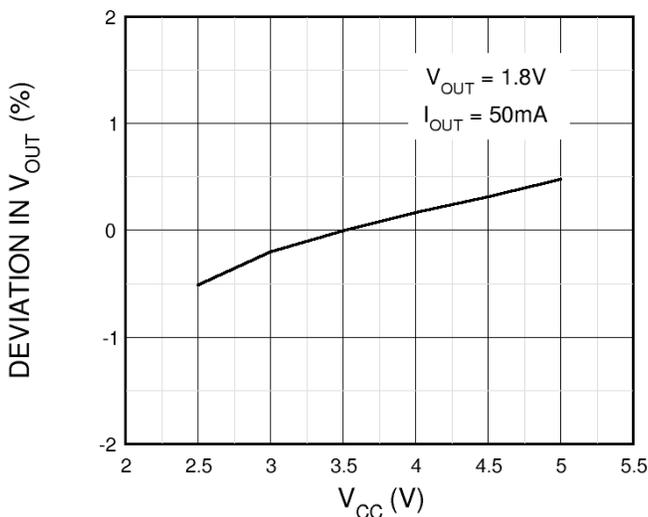
$I_{qq}$  Performance vs. Load Current



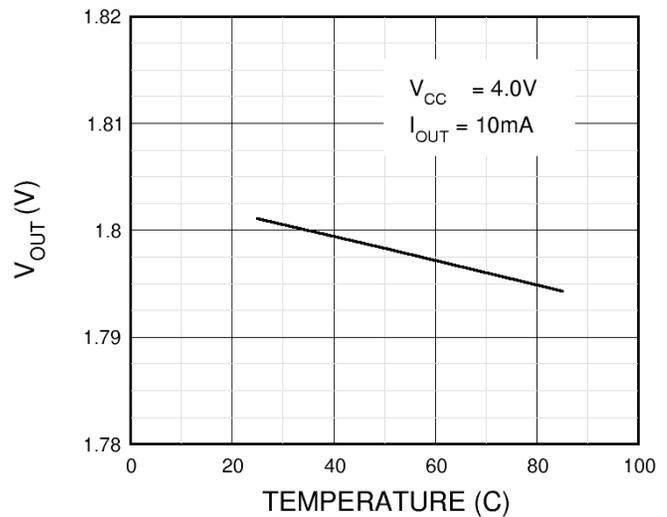
$I_{qq}$  Performance vs. Load Current

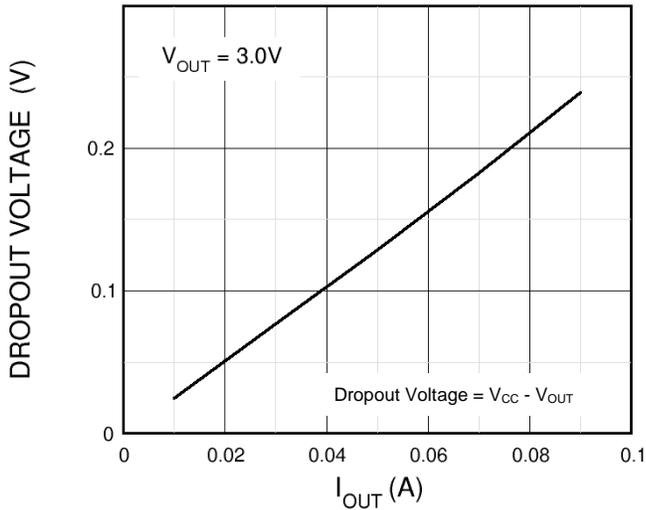
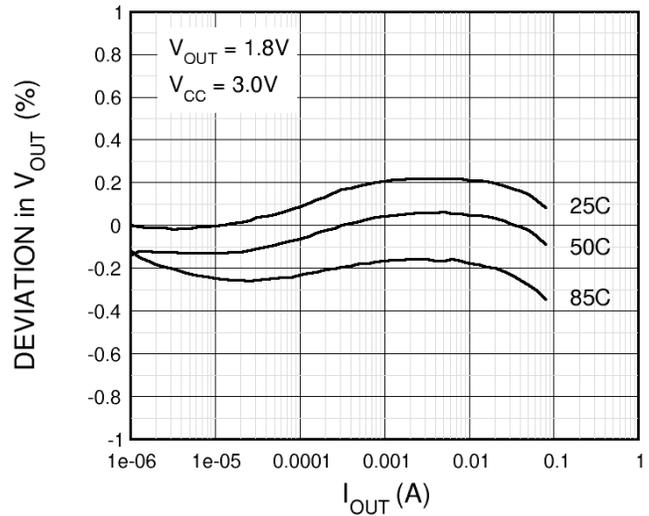
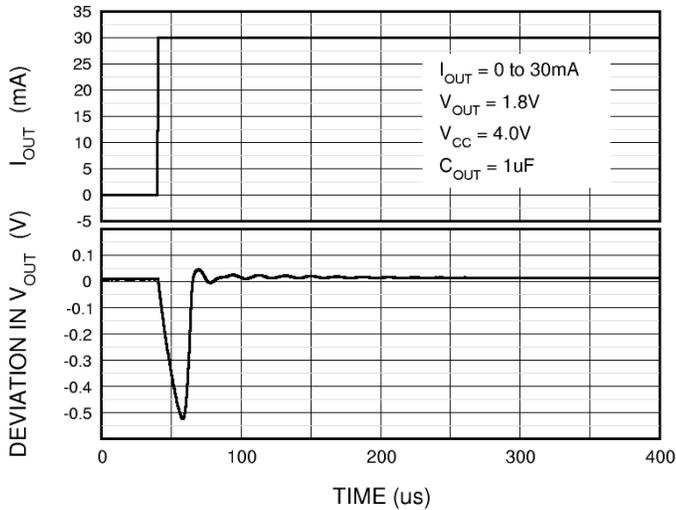
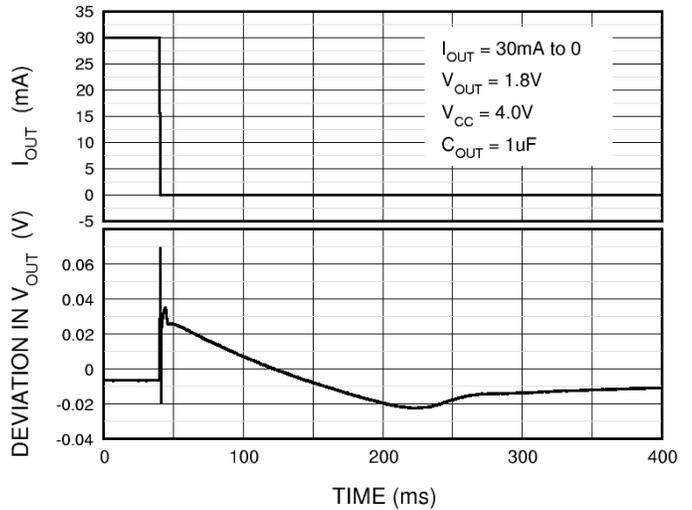
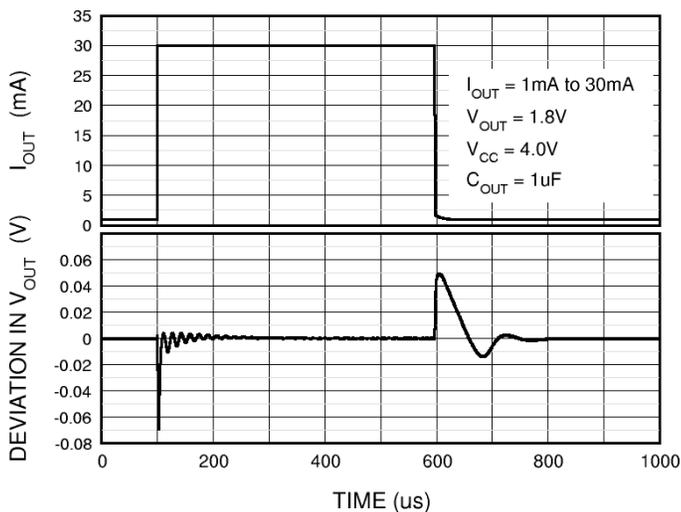
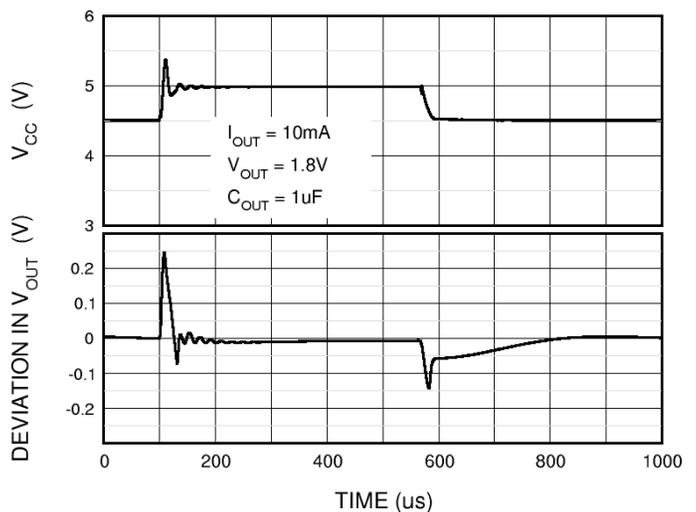


Line Regulation Performance

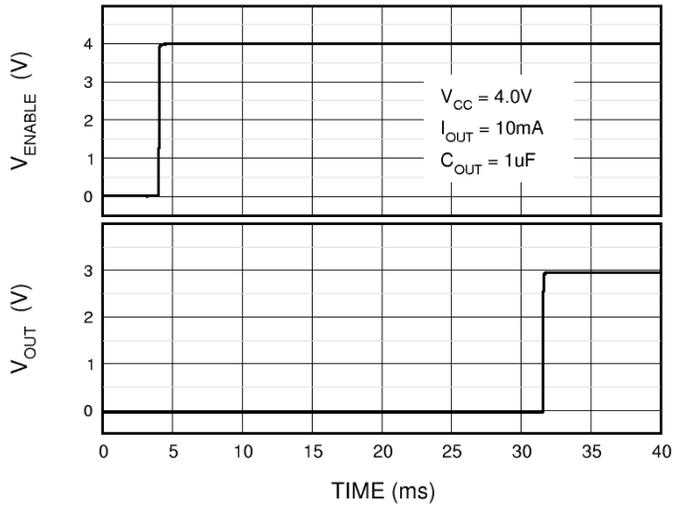


$V_{OUT}$  Performance vs. Temperature



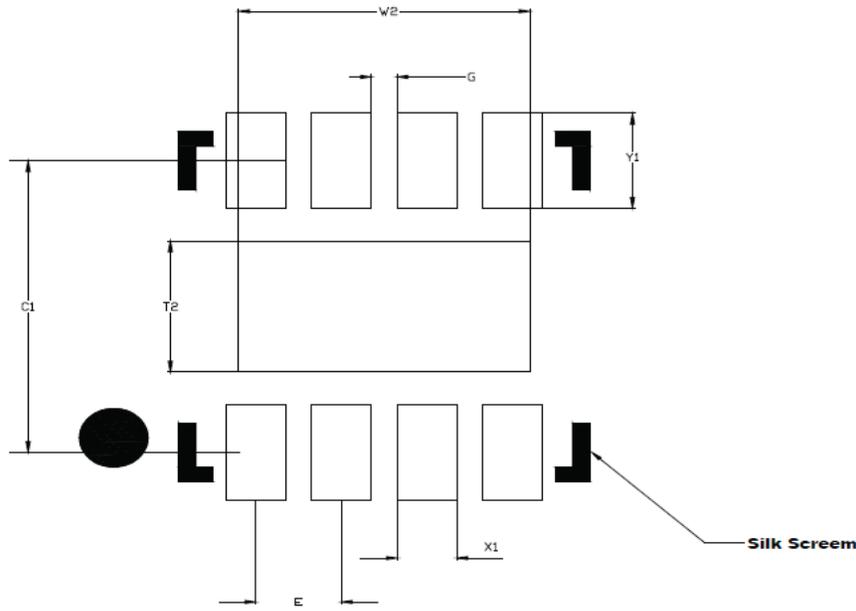
**Dropout Voltage When  $V_{OUT}$  Drops By 3%**

**Load Regulation Performance**

**Load Step Response**

**Load Step Response**

**Load Step Response**

**Line Step Response**


Output Enable Timing





## RECOMMENDED PCB LAND PATTERN



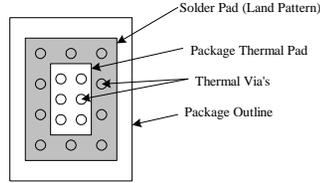
**RECOMMENDED  
LAND PATTERN**

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	0.90
Contact Pad Spacing	C1	-	2.00	-
Contact Pad Width (X8)	X1	-	-	0.35
Contact Pad Length (X8)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

## APPLICATION USING A MULTI-LAYER PCB

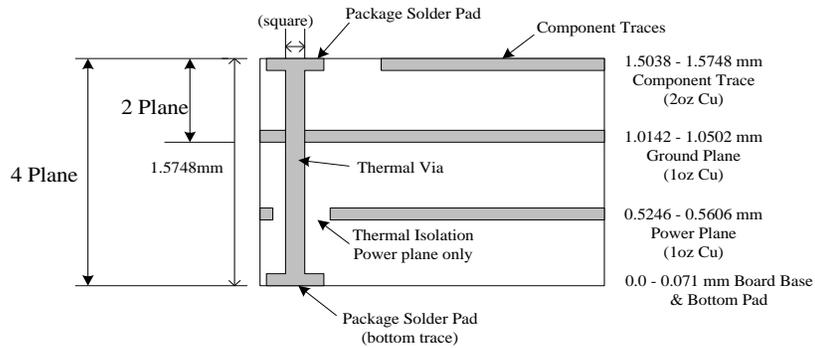
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with ground a plane.



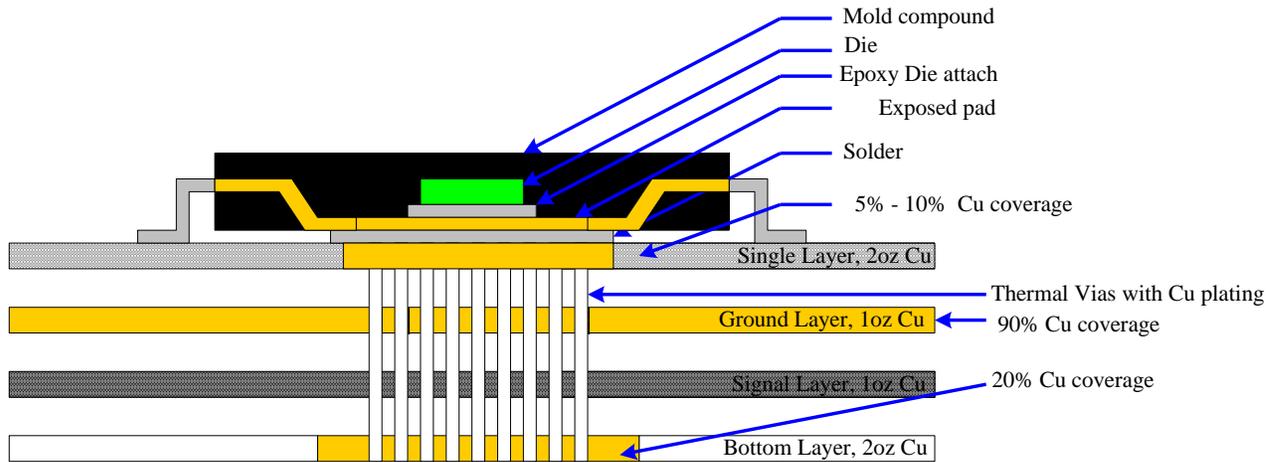
Package and PCB Land Configuration  
For a Multi-Layer PCB

### JEDEC standard FR4 PCB Cross-section:



Multi-Layer Board (Cross-sectional View)

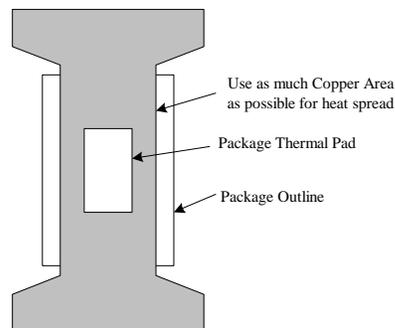
In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.



Note: NOT to Scale

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

## APPLICATION USING A SINGLE LAYER PCB



Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

## IMPORTANT:

**If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.**

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**ORDERING INFORMATION****TS14001-CvvvDFNR**

vvv	Output Voltage*
012	1.2 V
018	1.8 V
025	2.5 V
033	3.3 V
042	4.2 V

\* Custom values also available (1.2V - 4.2V typical in 100mV increments)

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