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October 2015

## FDN86501LZ

# N-Channel Shielded Gate PowerTrench® MOSFET 60 V, 2.6 A, 116 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 116 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 2.6 A
- Max  $r_{DS(on)}$  = 173 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 2.1 A
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

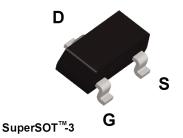


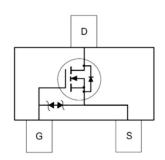
### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

#### **Applications**

- Primary DC-DC Switch
- Load Switch





## **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted.

Symbol	Parameter		Ratings	Units
$V_{DS}$	Drain to Source Voltage		60	V
$V_{GS}$	Gate to Source Voltage		±20	V
	-Continuous	(Note 1a)	2.6	^
ID	-Pulsed	(Note 4)	24	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	6	mJ
В	Power Dissipation	(Note 1a)	1.5	W
$P_{D}$	Power Dissipation	(Note 1b)	0.6	T VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{ heta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	80	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8650	FDN86501LZ	SSOT-3	7 "	8 mm	3000 units

### **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	octeristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		68		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μА

#### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	1.9	2.4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-5		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A		89	116	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 2.1 \text{ A}$		121	173	mΩ
		$V_{GS}$ = 10 V, $I_D$ = 2.6 A, $T_J$ = 125 °C		152	198	1
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.6 A		8		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 20 V V - 0 V		236	335	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz		77	110	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12		4.9	10	pF
$R_a$	Gate Resistance		0.1	8.0	2.0	Ω

#### **Switching Characteristics**

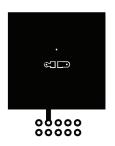
t <sub>d(on)</sub>	Turn-On Delay Time		4.4	10	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.6 A,	1.2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	9.6	20	ns
t <sub>f</sub>	Fall Time		1.2	10	ns
Qg	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	3.8	5.4	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V} V_{DD} = 30 \text{ V},$	1.9	2.7	nC
$Q_{gs}$	Gate to Source Gate Charge	I <sub>D</sub> = 2.6 A	0.7		nC
Q <sub>qd</sub>	Gate to Drain "Miller" Charge		0.6		nC

#### **Drain-Source Diode Characteristics**

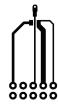
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.6 \text{ A}$ (Note 2)	0.9	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 2.6 A, di/dt = 100 A/μs	31	50	ns
Q <sub>rr</sub>	Reverse Recovery Charge		19	31	nC

#### Notes:

<sup>1.</sup> R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a) 80 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 180 °C/W when mounted on a minimum pad.

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 6 mJ is based on starting  $T_J$  = 25 °C, L = 3 mH,  $I_{AS}$  = 2 A,  $V_{DD}$  = 60 V,  $V_{GS}$  = 10 V. 100% test at L = 0.1 mH,  $I_{AS}$  = 9 A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

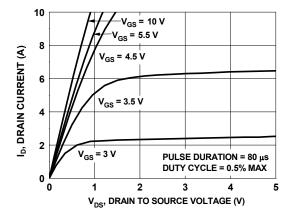


Figure 1. On Region Characteristics

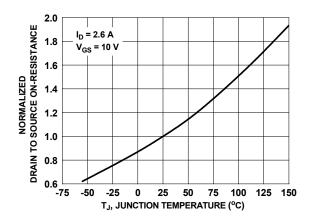


Figure 3. Normalized On Resistance vs. Junction Temperature

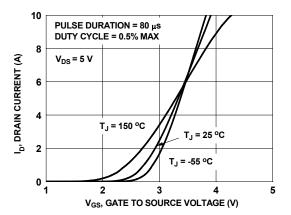


Figure 5. Transfer Characteristics

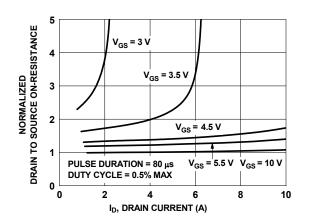


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

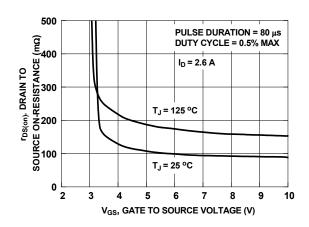


Figure 4. On-Resistance vs. Gate to Source Voltage

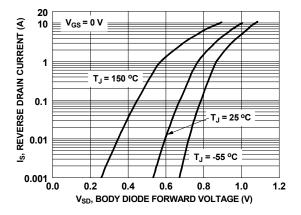


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# Typical Characteristics $T_J$ = 25 °C unless otherwise noted.

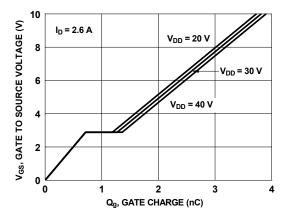


Figure 7. Gate Charge Characteristics

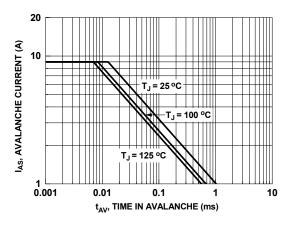


Figure 9. Unclamped Inductive Switching Capability

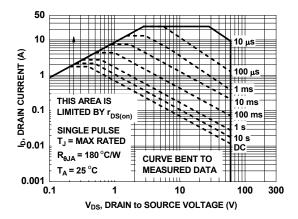


Figure 11. Forward Bias Safe Operating Area

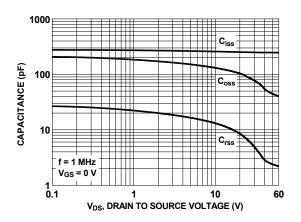


Figure 8. Capacitance vs. Drain to Source Voltage

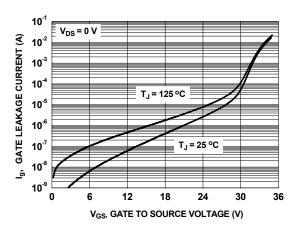


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

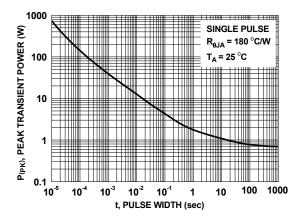


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted.

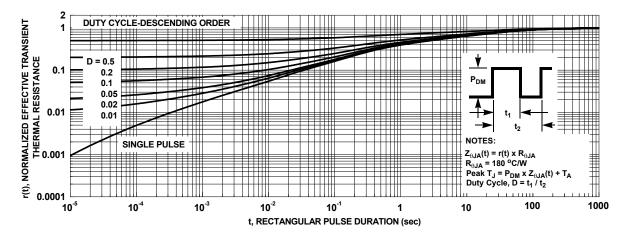
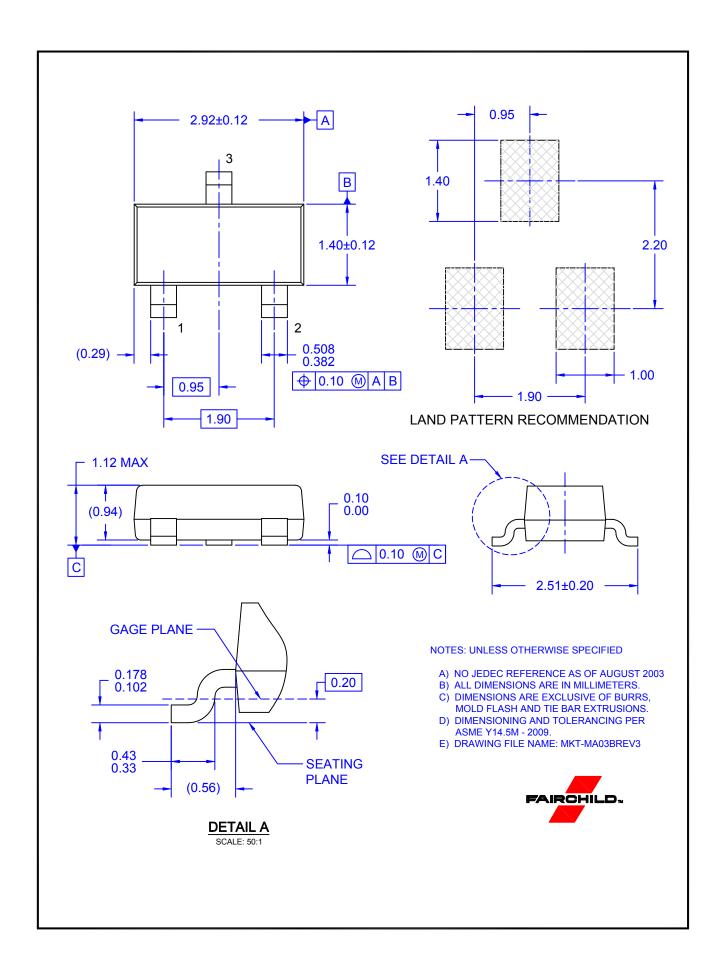


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9