2N5655, 2N5657

Plastic NPN Silicon High-Voltage Power Transistor

These devices are designed for use in line−operated equipment such as audio output amplifiers; low−current, high−voltage converters; and AC line relays.

Features

- Excellent DC Current Gain –
    $h_{FE} = 30-250$ @ $I_C = 100$ mAdc
- Current−Gain − Bandwidth Product –
    $f_T = 10$ MHz (Min) @ $I_C = 50$ mAdc
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	2N5655	2N5657	Unit
Collector−Emitter Voltage	V_{CEO}	250	350	Vdc
Collector−Base Voltage	V_{CB}	275	375	Vdc
Emitter−Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous Peak	I_C	0.5 1.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	20 0.16		W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	6.25	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC registered data.

Publication Order Number:
2N5655/D

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0.5 AMPERE POWER TRANSISTORS NPN SILICON 250–350 VOLTS, 20 WATTS
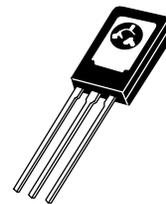
TO−225AA CASE 77−09 STYLE 1

MARKING DIAGRAM

YWW
2
N565xG
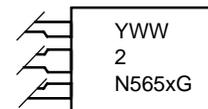
Y	= Year
WW	= Work Week
2N565x	= Device Code
	x = 5 or 7
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
2N5655	TO−225	500 Units / Bulk
2N5655G	TO−225 (Pb−Free)	500 Units / Bulk
2N5657	TO−225	500 Units / Bulk
2N5657G	TO−225 (Pb−Free)	500 Units / Bulk

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted) (Note 2)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage ($I_C = 100$ mAdc (inductive), $L = 50$ mH)	2N5655 2N5657	$V_{CEO(sus)}$	250 350	– –	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	2N5655 2N5657	$V_{(BR)CEO}$	250 350	– –	Vdc
Collector Cutoff Current ($V_{CE} = 150$ Vdc, $I_B = 0$) ($V_{CE} = 250$ Vdc, $I_B = 0$)	2N5655 2N5657	I_{CEO}	– –	0.1 0.1	mAdc
Collector Cutoff Current ($V_{CE} = 250$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 350$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 150$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 100°C$) ($V_{CE} = 250$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 100°C$)	2N5655 2N5657 2N5655 2N5657	I_{CEX}	– – – –	0.1 0.1 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CB} = 275$ Vdc, $I_E = 0$) ($V_{CB} = 375$ Vdc, $I_E = 0$)	2N5655 2N5657	I_{CBO}	– –	10 10	μAdc
Emitter Cutoff Current ($V_{EB} = 6.0$ Vdc, $I_C = 0$)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3) ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc) ($I_C = 100$ mAdc, $V_{CE} = 10$ Vdc) ($I_C = 250$ mAdc, $V_{CE} = 10$ Vdc) ($I_C = 500$ mAdc, $V_{CE} = 10$ Vdc)		h_{FE}	25 30 15 5.0	– 250 – –	–
Collector–Emitter Saturation Voltage (Note 3) ($I_C = 100$ mAdc, $I_B = 10$ mAdc) ($I_C = 250$ mAdc, $I_B = 25$ mAdc) ($I_C = 500$ mAdc, $I_B = 100$ mAdc)		$V_{CE(sat)}$	– – –	1.0 2.5 10	Vdc
Base–Emitter Voltage ($I_C = 100$ mAdc, $V_{CE} = 10$ Vdc) (Note 3)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc, $f = 10$ MHz) (Note 4)		f_T	10	–	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 100$ kHz)		C_{ob}	–	25	pF
Small–Signal Current Gain ($I_C = 100$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)		h_{fe}	20	–	–

2. Indicates JEDEC registered data for 2N5655 Series.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle $\leq 2.0\%$.
4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.
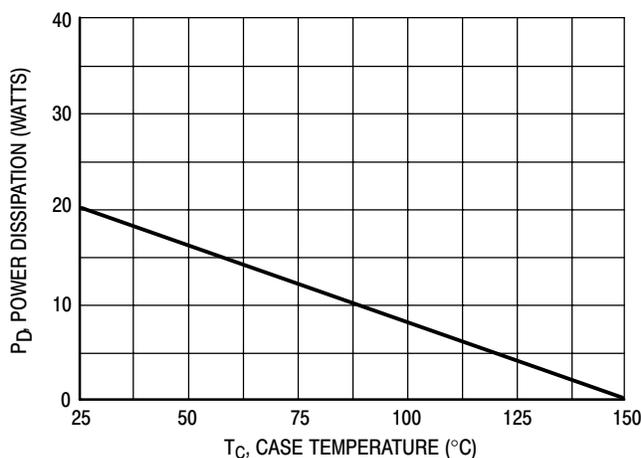

Figure 1. Power Derating
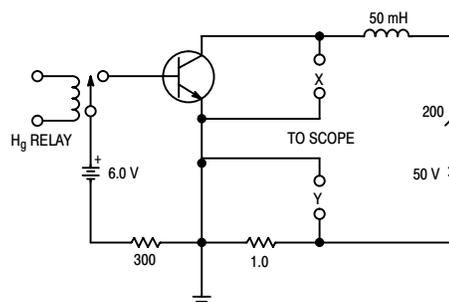
Figure 2. Sustaining Voltage Test Circuit

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

2N5655, 2N5657
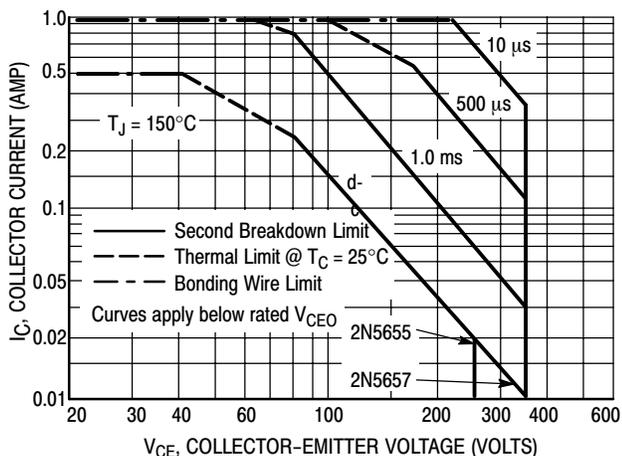
Figure 3. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.
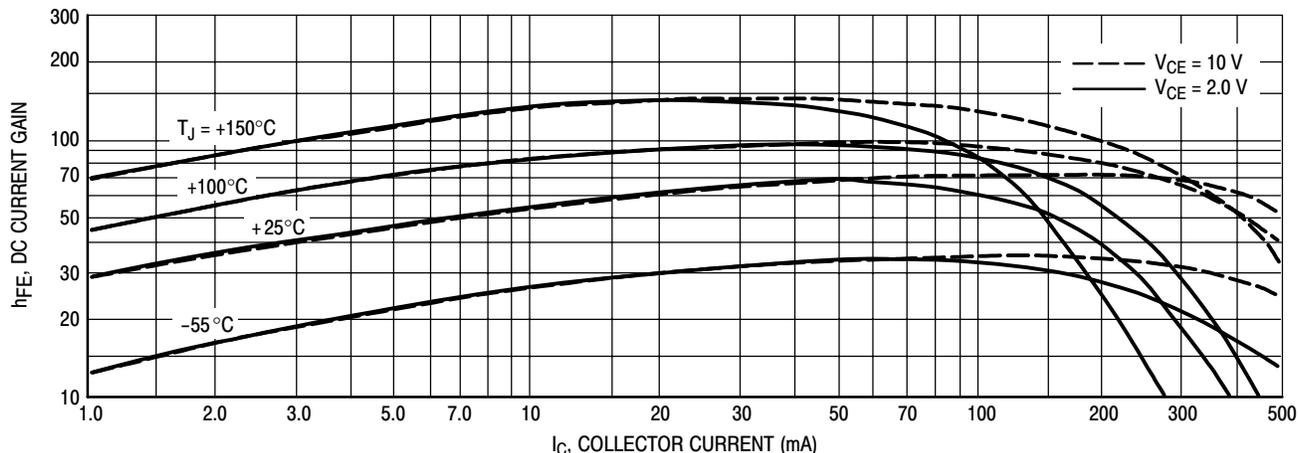
Figure 4. Current Gain
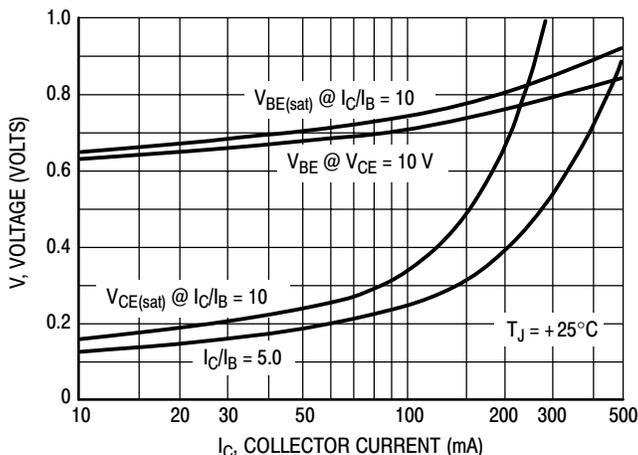
Figure 5. "On" Voltages

**2N5655, 2N5657**
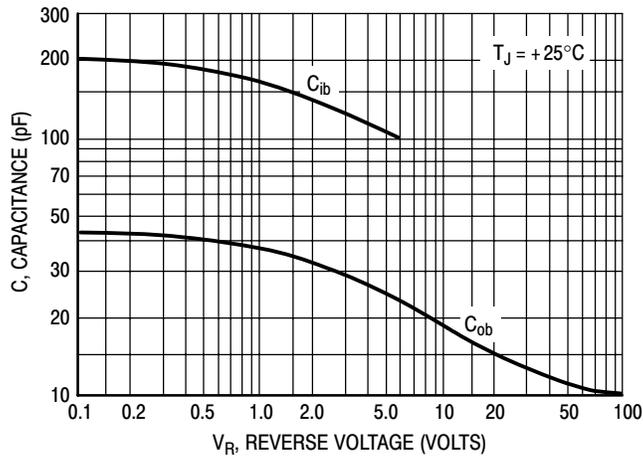
Figure 6. Capacitance
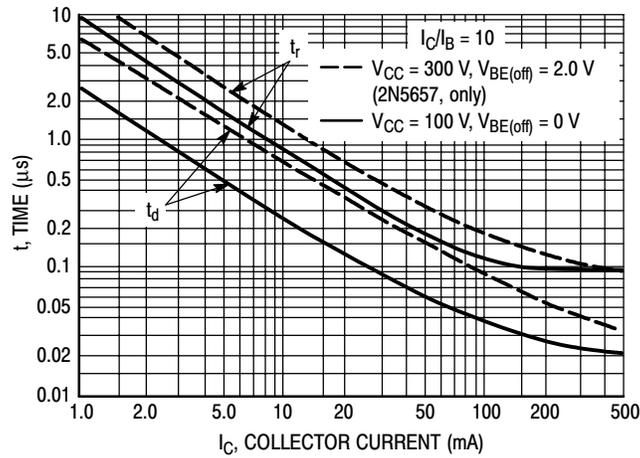
Figure 7. Turn−On Time
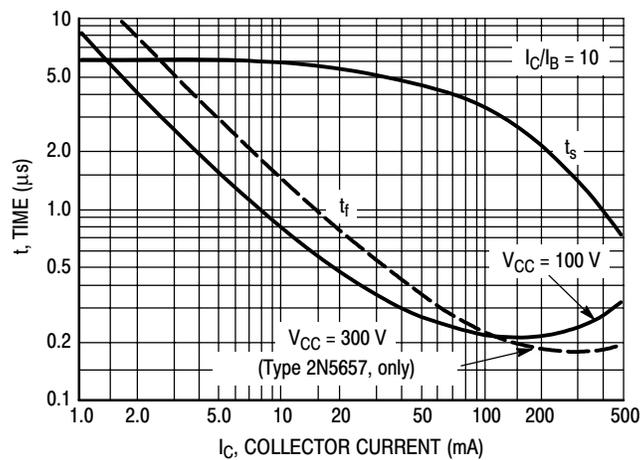
Figure 8. Turn−Off Time

PACKAGE DIMENSIONS

TO–225
CASE 77–09
ISSUE Z
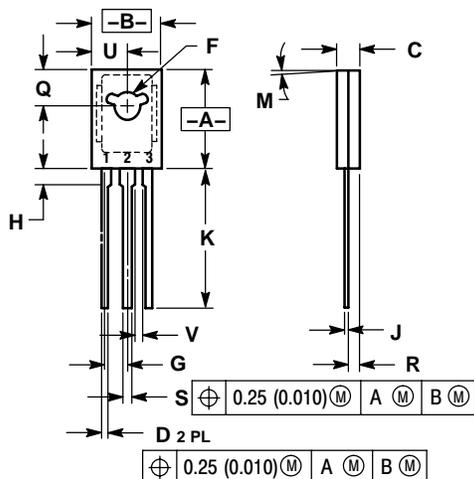
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077–01 THRU –08 OBSOLETE, NEW STANDARD 077–09.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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