EVALUATION KIT AVAILABLE

MAX15048/MAX15049

Triple-Output Buck Controllers with Tracking/Sequencing

General Description

The MAX15048/MAX15049 are triple-output pulse-width modulated (PWM), step-down, DC-DC controllers with tracking (MAX15048) and sequencing (MAX15049) options. The devices operate over the 4.7V to 23V input-voltage range. Each PWM controller provides an adjustable output down to 0.6V and delivers up to 15A of load current with excellent load and line regulation. The MAX15049 can start into prebiased outputs. The MAX15048/MAX15049 are optimized for high-performance, small-size power-management solutions.

The options of coincident or ratiometric tracking (MAX15048) or output sequencing (MAX15049) allow the tailoring of the power-up/power-down sequence depending on the system requirements. Each of the MAX15048/MAX15049 PWM sections utilizes a voltage-mode control scheme with external compensation, allowing for good noise immunity and maximum flexibility with a wide selection of inductor values and capacitor types. Each PWM section operates at the same fixed switching frequency that is programmable from 200kHz to 1.2MHz. Each converter, operating at up to 1.2MHz with 120° out-of-phase, increases the input capacitor ripple frequency up to 3.6MHz, reducing the RMS input ripple current and thus the size of the input bypass capacitor significantly. The MAX15048/MAX15049 integrate boost diodes for additional system cost savings.

The MAX15048/MAX15049 include internal undervoltage lockout (UVLO) with hysteresis and digital soft-start (MAX15048/MAX15049)/soft-stop (MAX15048) for glitch-free power-up and power-down of the converter. The power-good circuitry (PGOOD) monitors all three outputs and provides a power-good signal to the system control/processor when all outputs are within regulation. Protection features include lossless valley-mode current limit, hiccup mode output short-circuit protection, and thermal shutdown.

The MAX15048/MAX15049 are available in space-saving, 5mm x 5mm, lead-free, 32-pin TQFN-EP packages and are specified for operation over the -40°C to +85°C extended temperature range.

Applications

Point-of-Load DC-DC Converters

ASIC/CPU/DSP Core and I/O Voltages

DDR Power Supply

Base-Station Power Supplies

Telecom and Networking Power Supplies

RAID Control Power Supplies

Set-Top Boxes

Features

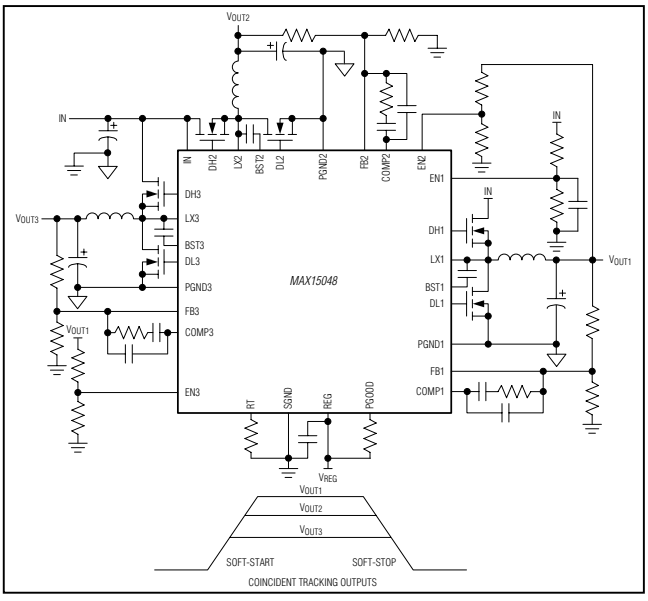
- **4.7V to 23V or 5V ±10% Input Voltage Range**
- **Triple-Output Synchronous Buck Controllers with 120° Out-of-Phase Operation**
- **Prebias Power-Up (MAX15049)**
- **Output Voltage Adjustable Down to 0.6V**
- **Coincident/Ratiometric Tracking (MAX15048)**
- **Accurate Sequencing Through Enable Threshold (MAX15049)**
- **External Compensation for Maximum Flexibility**
- **Digital Soft-Start (MAX15048/MAX15049) and Soft-Stop (MAX15048)**
- **Lossless Valley-Mode Current Sensing Using $R_{DS(ON)}$ of the Low-Side MOSFET**
- **PGOOD Output**
- **Integrated Bootstrap Diodes**
- **Programmable Switching Frequency from 200kHz to 1.2MHz**
- **Thermal Shutdown and Hiccup Mode Short-Circuit Protection**
- **Space-Saving (5mm x 5mm), 32-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15048ETJ+	-40°C to +85°C	32 TQFN-EP*
MAX15049ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Typical Operating Circuit (Coincident Tracking)



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5110; Rev 0; 1/10

ABSOLUTE MAXIMUM RATINGS

IN, LX_ to SGND .....-0.3V to +30V
BST_ to SGND.....-0.3V to +30V
BST_ to LX_.....-0.3V to +6V
REG, DREG_, EN_, RT to SGND.....-0.3V to +6V
PGOOD, FB_, COMP_ to SGND .....-0.3V to +6V
DL_ to PGND_.....-0.3V to ($V_{DREG_}$ + 0.3V)
DH_ to LX_ .....-0.3V to ($V_{BST_}$ + 0.3V)
PGND to SGND, PGND_
to Any Other PGND_.....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) ...2758.6mW
Junction-to-Case Thermal Resistance (θ_{JC})
(Note 1) .....2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) .....29°C/W
Operating Junction Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering (reflow) ....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V or V_{IN} = V_{REG} = 5V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		4.7		23	V
		V_{IN} = V_{REG} = $V_{DREG_}$ (Note 3)	4.5		5.5	
Input Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising	4.0	4.2	4.4	V
Input Undervoltage-Lockout Hysteresis				0.3		V
Operating Supply Current		V_{IN} = 12V, $V_{FB_}$ = 0.8V		6	9	mA
Shutdown Supply Current		V_{IN} = 12V, EN_ = 0, PGOOD unconnected		100	200	µA
VOLTAGE REGULATOR (REG)						
Output-Voltage Set Point	V_{REG}	V_{IN} = 6V to 23V	4.75		5.25	V
Load Regulation		I_{REG} = 0 to 60mA, V_{IN} = 6V			0.2	V
BOOTSTRAP SWITCH						
Internal Boost Switch Resistance		$V_{BST,LX}$ = 5V		3		Ω
TRANSCONDUCTANCE ERROR AMPLIFIER/DIGITAL SOFT-START/-STOP						
FB_ Input Bias Current			-1		+1	µA
FB_ Voltage Set Point	$V_{FB_}$		0.594	0.600	0.606	V
FB_ to COMP_ Transconductance				2.0		mS
COMP_ Output Swing			0.75		3.5	V
Open-Loop Gain				80		dB
Unity-Gain Bandwidth				10		MHz
Soft-Start/-Stop Duration				2048		Clocks
Reference Voltage Steps				64		Steps

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V or V_{IN} = V_{REG} = 5V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Switching Frequency Range (Each Converter)	f_{SW}	f_{SW} minimum, V_{RT} = 0.5V		200		kHz
		f_{SW} maximum, V_{RT} = 3V		1200		
Switching Frequency Accuracy (Each Converter)		f_{SW} = 500kHz	-4		+4	%
Phase Delay		DH1 rising to DH2 rising and DH2 rising to DH3 rising		120		Degrees
RT Current		V_{RT} = 0.5V to 3V	31.5	32	32.5	µA
Minimum Controllable On-Time	$t_{ON(MIN)}$			75		ns
Minimum Off-Time	$t_{OFF(MIN)}$			300		ns
PWM Ramp Amplitude (P-P)				1.0		V
PWM Ramp Valley				1.2		V
DRIVERS						
DL_, DH_ Break-Before-Make Time		C_{LOAD} = 2nF		35		ns
DH1 On-Resistance		Low, sinking 100mA		0.8		Ω
		High, sourcing 100mA		2.4		
DH2 On-Resistance		Low, sinking 100mA		0.8		Ω
		High, sourcing 100mA		2.4		
DH3 On-Resistance		Low, sinking 100mA		0.8		Ω
		High, sourcing 100mA		2.4		
DL1 On-Resistance		Low, sinking 100mA		0.6		Ω
		High, sourcing 100mA		2.4		
DL2 On-Resistance		Low, sinking 100mA		0.6		Ω
		High, sourcing 100mA		2.4		
DL3 On-Resistance		Low, sinking 100mA		0.6		Ω
		High, sourcing 100mA		2.4		
CURRENT-LIMIT AND HICCUP MODE						
Cycle-by-Cycle Valley Current-Limit Threshold	V_{LIM}	T_A = T_J = +25°C		69		mV
Threshold Temperature Coefficient				3333		ppm/°C
Number of Cumulative Current-Limit Events to Hiccup	N_{CL}			8		Events
Number of Consecutive Noncurrent-Limit Cycles to Clear N_{CL}	N_{CLR}			3		Events
Hiccup Timeout	N_{HT}			4096		Clock periods

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V or V_{IN} = V_{REG} = 5V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/PGOOD						
EN_ Threshold	V_{EN-TH}	EN_ rising	0.57	0.60	0.63	V
EN_ Threshold Hysteresis				46		mV
EN_ Input Bias Current			-1		+1	µA
PGOOD Threshold		FB_ rising	0.545	0.550	0.555	V
PGOOD Hysteresis				30		mV
PGOOD Output Low Level		Sinking 3mA			0.1	V
PGOOD Leakage		V_{PGOOD} = 5V	-1		+1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature		Temperature rising		+160		°C
Thermal-Shutdown Hysteresis				20		°C

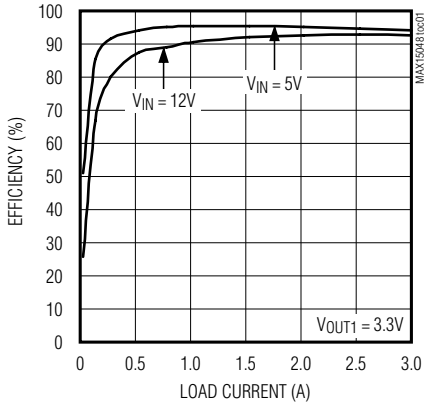
Note 2: 100% production tested at T_A = T_J = +25°C and T_A = T_J = +85°C. Limits at other temperatures are guaranteed by design.

Note 3: For 5V applications, connect REG directly to IN.

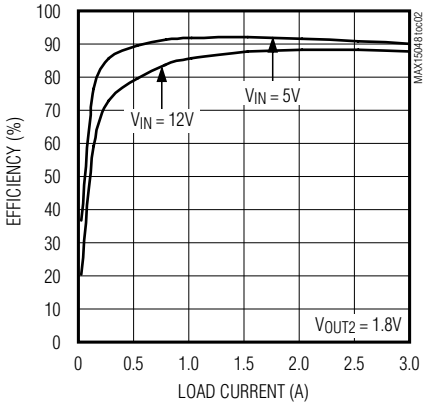
Typical Operating Characteristics

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

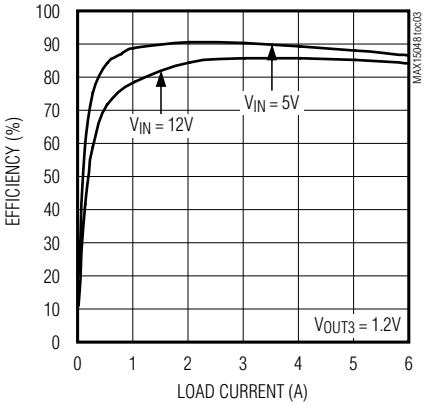
CONVERTER 1 EFFICIENCY vs. LOAD CURRENT



CONVERTER 2 EFFICIENCY vs. LOAD CURRENT



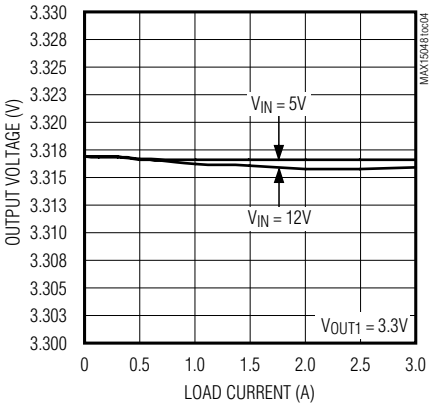
CONVERTER 3 EFFICIENCY vs. LOAD CURRENT



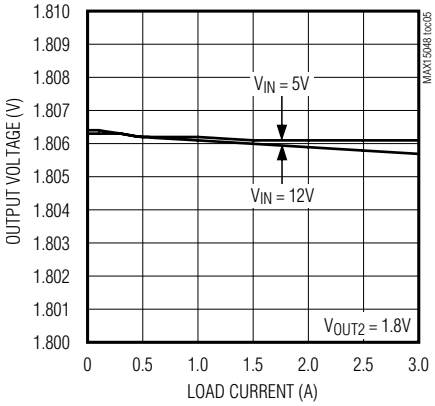
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

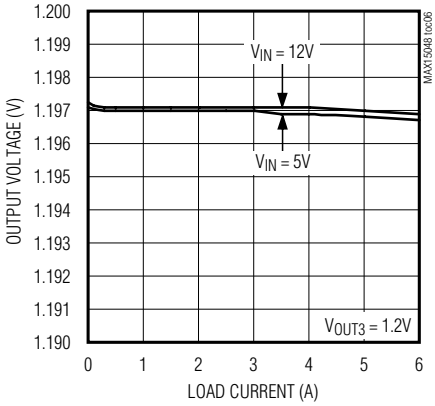
CONVERTER 1 OUTPUT VOLTAGE vs. LOAD CURRENT



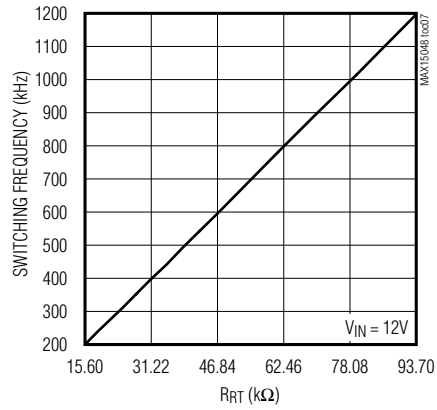
CONVERTER 2 OUTPUT VOLTAGE vs. LOAD CURRENT



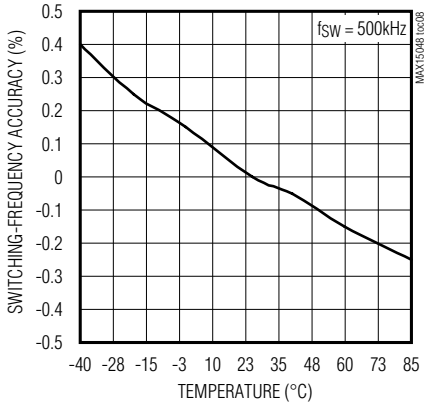
CONVERTER 3 OUTPUT VOLTAGE vs. LOAD CURRENT



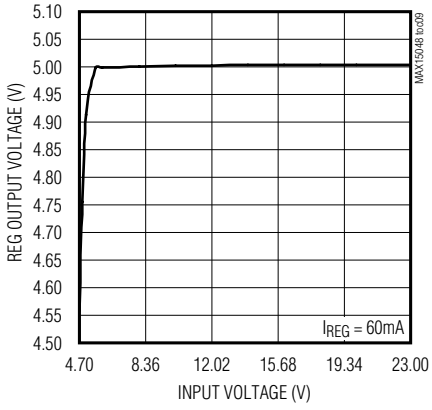
SWITCHING FREQUENCY vs. R_{RT}



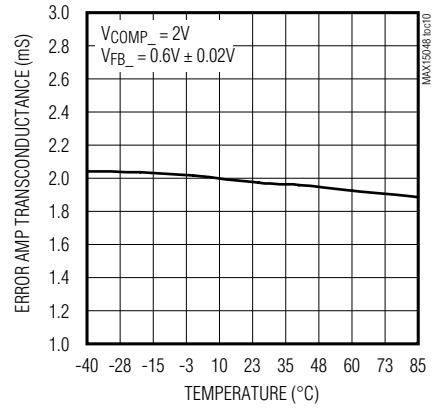
SWITCHING-FREQUENCY ACCURACY vs. TEMPERATURE



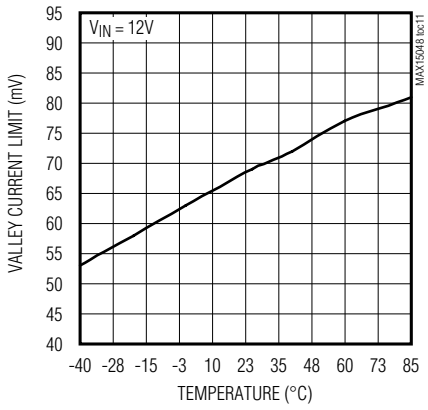
REG OUTPUT VOLTAGE vs. INPUT VOLTAGE



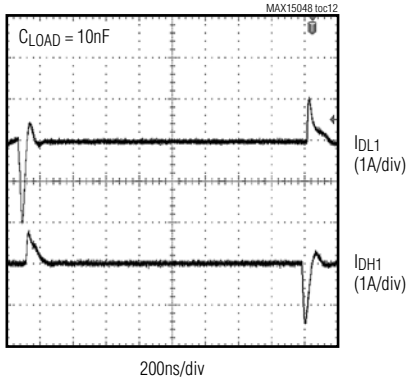
ERROR AMP TRANSCONDUCTANCE vs. TEMPERATURE



VALLEY CURRENT LIMIT vs. TEMPERATURE



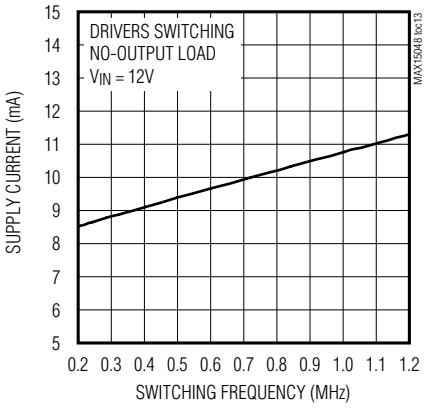
DL1 AND DH1 PEAK SOURCE-AND-SINK CURRENT



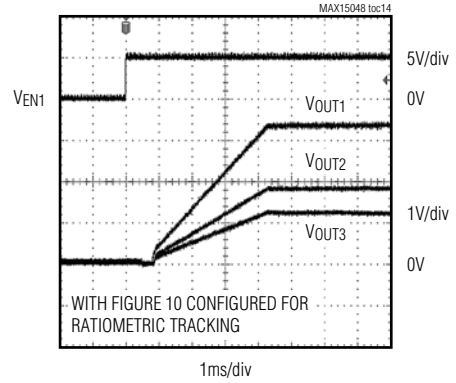
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

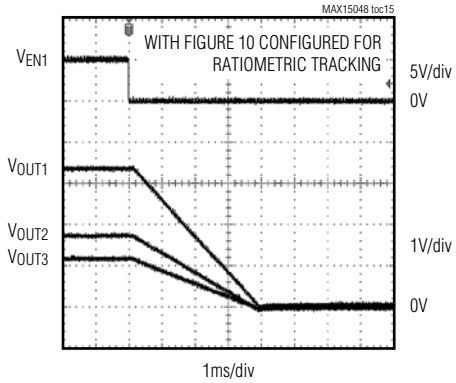
OPERATING SUPPLY CURRENT vs. SWITCHING FREQUENCY



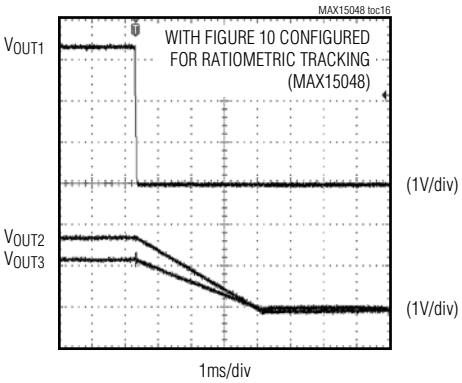
RATIOMETRIC STARTUP (MAX15048)



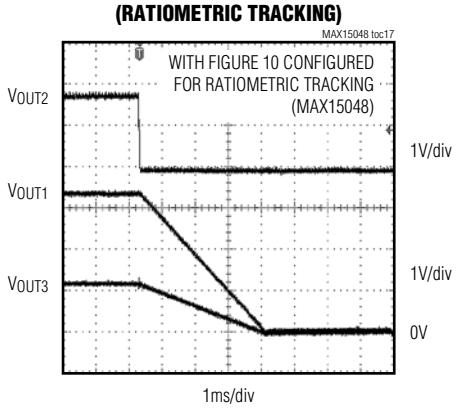
RATIOMETRIC SHUTDOWN (MAX15048)



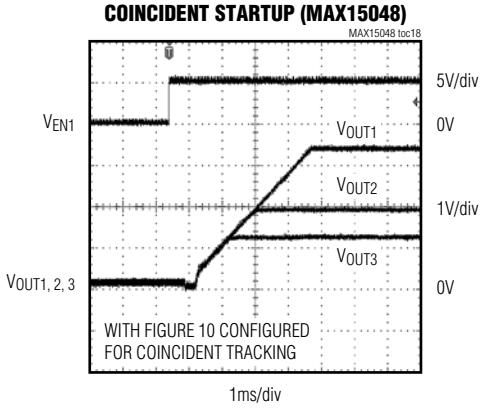
CHANNEL 1 SHORT CIRCUIT (RATIOMETRIC TRACKING)



CHANNEL 2 SHORT CIRCUIT (RATIOMETRIC TRACKING)



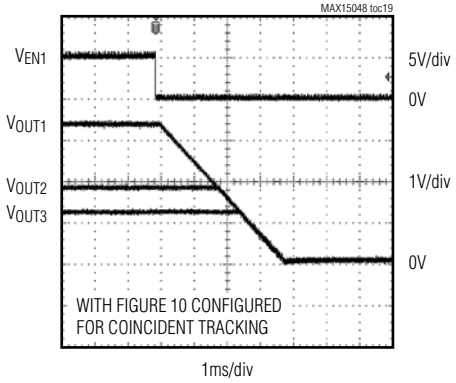
COINCIDENT STARTUP (MAX15048)



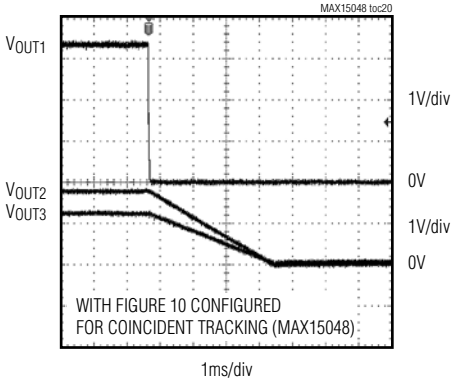
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

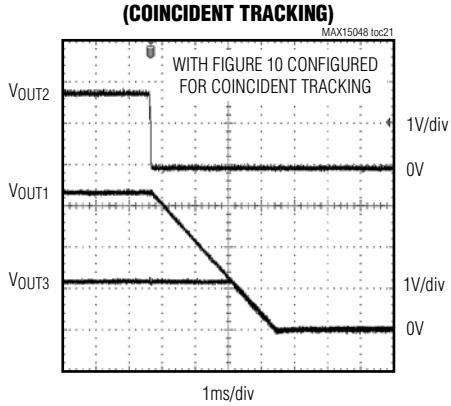
COINCIDENT SHUTDOWN (MAX15048)



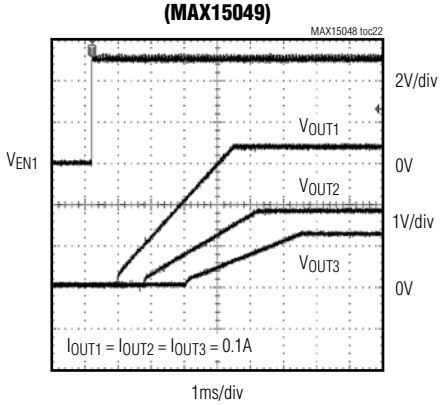
CHANNEL 1 SHORT CIRCUIT (COINCIDENT TRACKING)



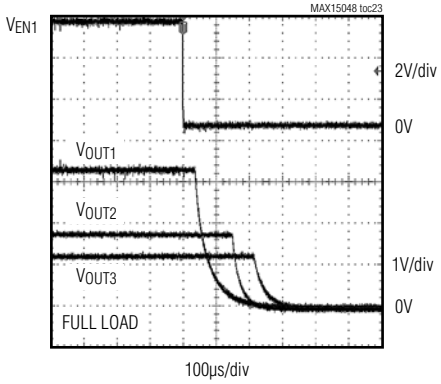
CHANNEL 2 SHORT CIRCUIT (COINCIDENT TRACKING)



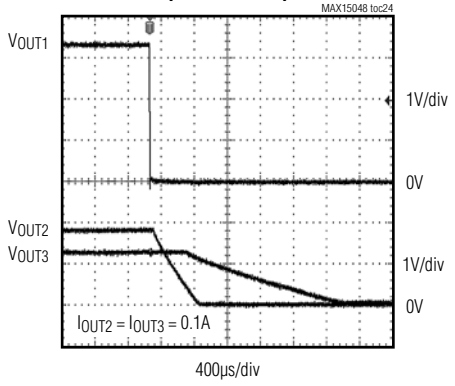
SEQUENCING STARTUP (MAX15049)



SEQUENCING SHUTDOWN



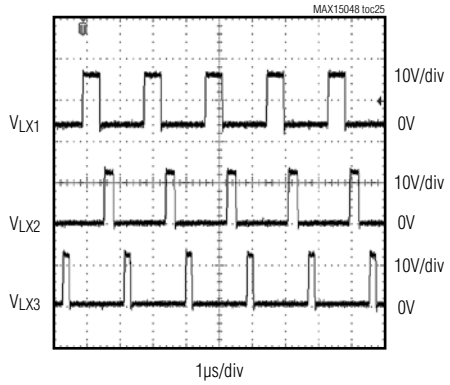
CHANNEL 1 SHORT CIRCUIT (SEQUENCING)



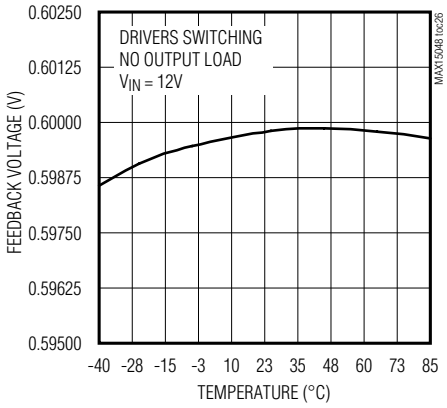
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

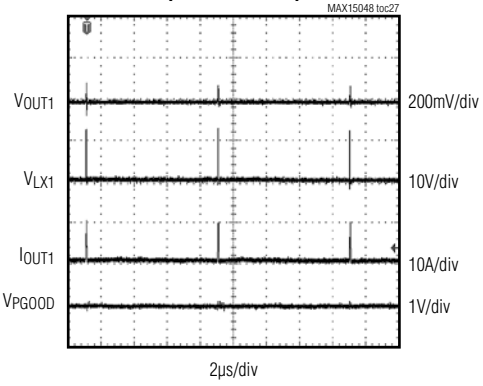
120° OUT-OF-PHASE OPERATION



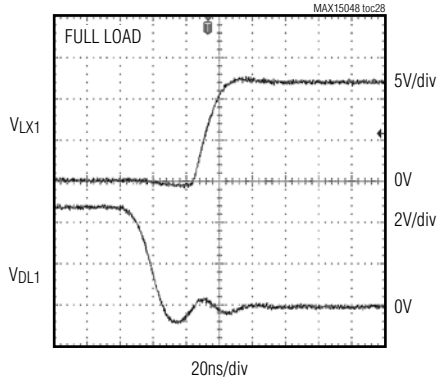
$V_{FB_}$ vs. TEMPERATURE



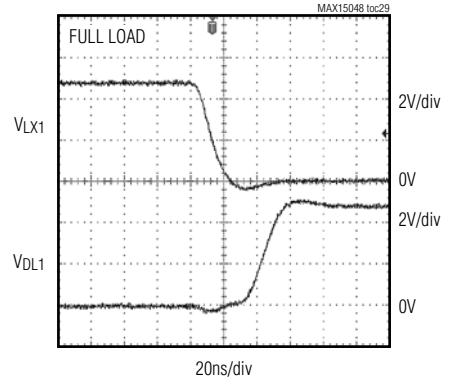
CONVERTER 1 SHORT-CIRCUIT CONDITION (HICCUP MODE)



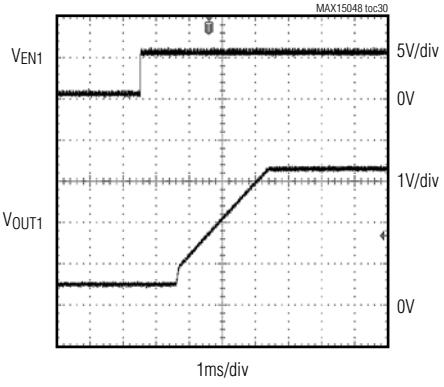
BREAK-BEFORE-MAKE TIMING



BREAK-BEFORE-MAKE TIMING



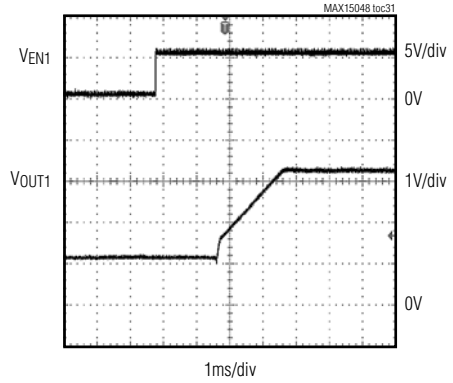
STARTUP INTO PREBIASED OUTPUT (0.5V PREBIASED)



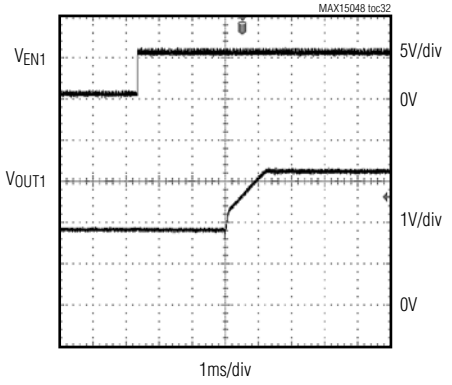
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{DREG_}$ = V_{REG}, $V_{PGND_}$ = 0V, C_{REG} = 2.2µF, R_{RT} = 39.2kΩ, T_A = +25°C, unless otherwise noted. See Figure 10.)

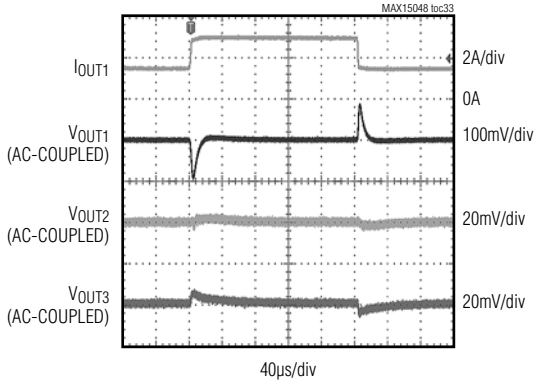
STARTUP INTO PREBIASED OUTPUT (1.2V PREBIASED)



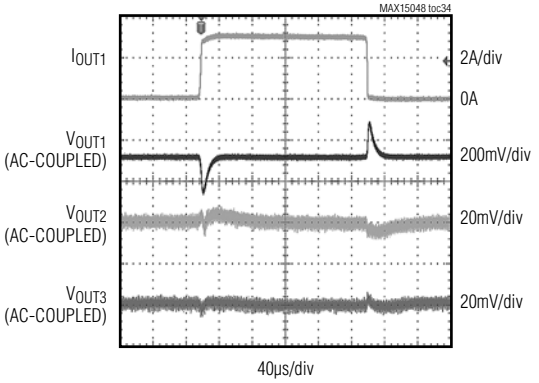
STARTUP INTO PREBIASED OUTPUT (1.8V PREBIASED)



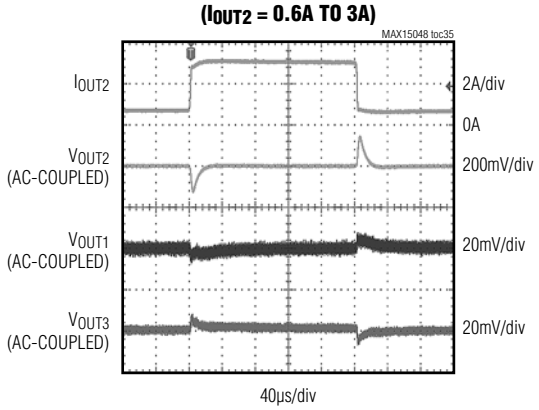
LOAD-TRANSIENT RESPONSE (I_{OUT1} = 1.5A TO 3A)



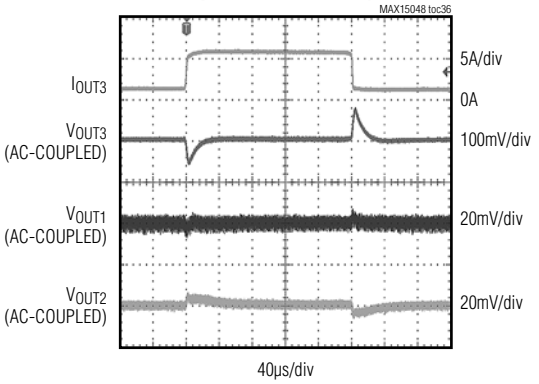
LOAD-TRANSIENT RESPONSE (I_{OUT1} = 0.1A TO 3A)



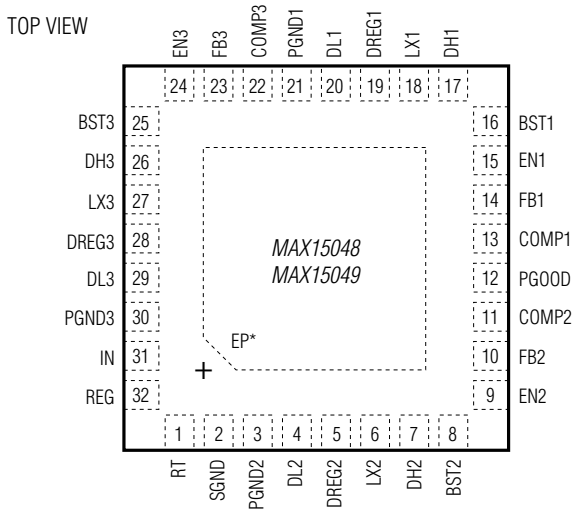
LOAD-TRANSIENT RESPONSE (I_{OUT2} = 0.6A TO 3A)



LOAD-TRANSIENT RESPONSE (I_{OUT3} = 1.2A TO 6A)



Pin Configuration



TQFN
(5mm × 5mm)

*EXPOSED PAD.

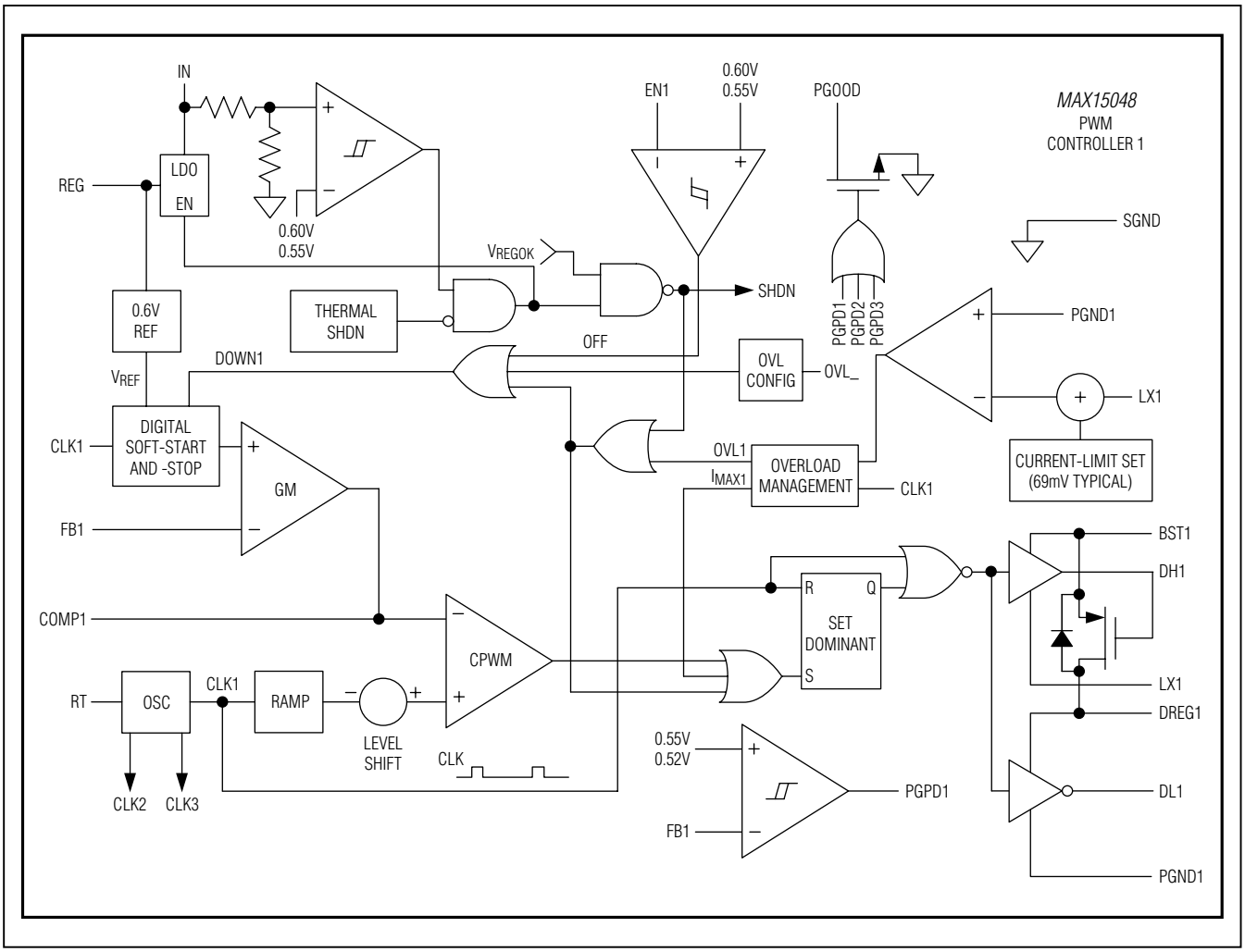
Pin Description

PIN	NAME	FUNCTION
1	RT	Oscillator Timing Resistor Connection. Connect a 15.6kΩ to 93.75kΩ resistor from RT to SGND to program the switching frequency from 200kHz to 1.2MHz.
2	SGND	Analog Ground. Connect SGND and PGND_ together at one point near the input bypass capacitor return terminal.
3	PGND2	Controller 2 Power Ground. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND2.
4	DL2	Controller 2 Low-Side Gate-Driver Output. DL2 is the gate-driver output for the synchronous MOSFET.
5	DREG2	Controller 2 Low-Side Gate-Driver Supply. Connect externally to REG through a 1Ω to 4.7Ω resistor. Connect a minimum of 0.22µF ceramic capacitor from DREG2 to PGND2.
6	LX2	Controller 2 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX2.
7	DH2	Controller 2 High-Side Gate-Driver Output. DH2 drives the gate of the high-side MOSFET.
8	BST2	Controller 2 High-Side Gate-Driver Supply. Connect a 0.1µF ceramic capacitor from BST2 to LX2.
9	EN2	Controller 2 Enable/Tracking Input. See Figure 2. When tracking (MAX15048), connect the same resistive voltage-divider used for FB2 from output 1 to EN2 to SGND for coincident tracking. Connect EN2 to analog ground for ratiometric tracking. When sequencing (MAX15049), EN2 must be above 0.6V for PWM controller 2 to start.
10	FB2	Controller 2 Feedback Regulation Point. Connect to the center tap of a resistive voltage-divider from the converter output to SGND to set the output voltage. The FB2 voltage regulates to 0.6V (typ).
11	COMP2	Controller 2 Transconductance Error-Amplifier Output. Connect COMP2 to the compensation feedback network of output 2.

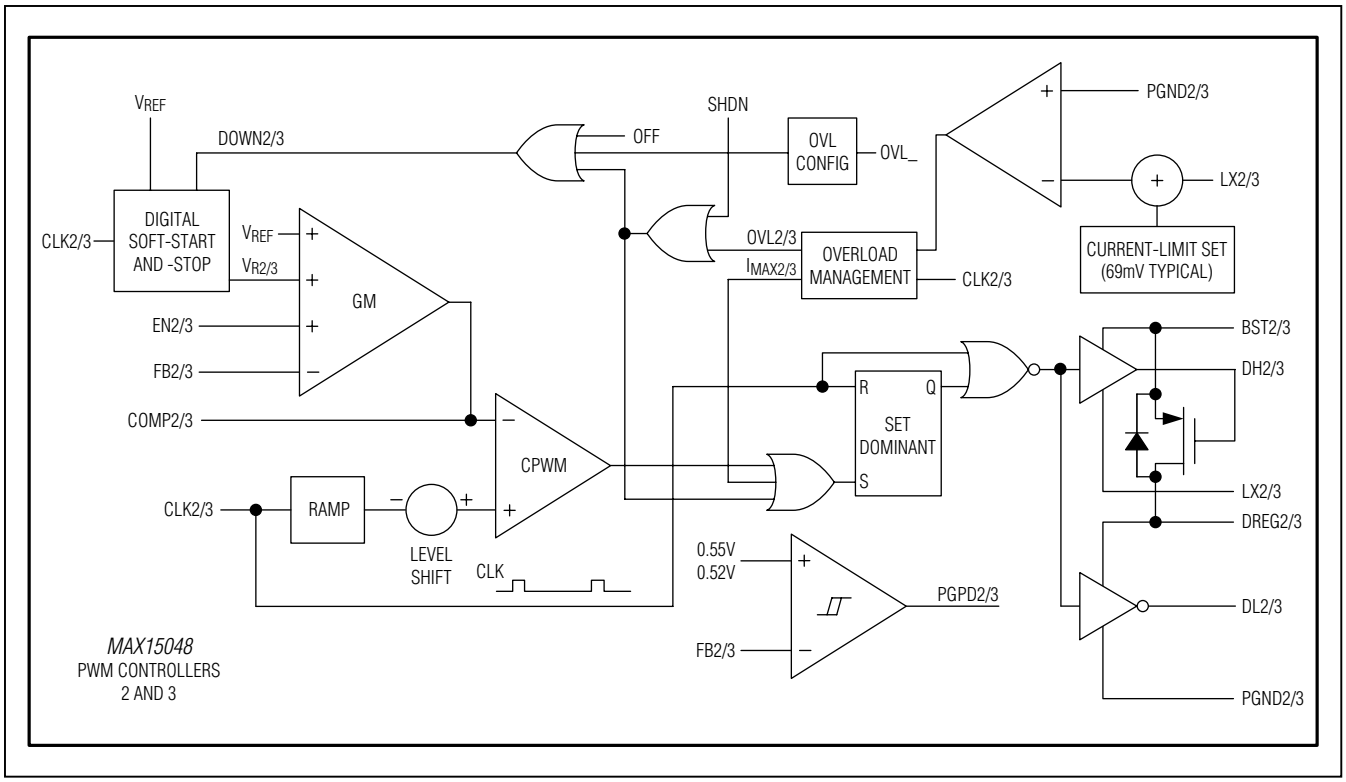
Pin Description (continued)

PIN	NAME	FUNCTION
12	PGOOD	Controller Power-Good Output. Pull up PGOOD with a resistor to a positive voltage below 5.5V. For the MAX15048, PGOOD output releases when all three $V_{FB_}$ voltages are above 0.55V. For the MAX15049, PGOOD output releases when all three controllers are out of prebias and all three $V_{FB_}$ voltages are above 0.55V.
13	COMP1	Controller 1 Transconductance Error-Amplifier Output. Connect COMP1 to the compensation feedback network of output 1.
14	FB1	Controller 1 Feedback Regulation Point. Connect to the center tap of a resistive voltage-divider from the converter output to SGND to set the output voltage. The FB1 voltage regulates to 0.6V (typ).
15	EN1	Controller 1 Enable Input. For tracking (MAX15048), EN1 must be above 0.6V, V_{EN-TH}, for the PWM controller to start outputs 1, 2, and 3. Controller 1 is the master. Use the master as the highest output voltage in a coincident tracking configuration. For the MAX15049, EN1 must be above 0.6V for the PWM controller to start output 1.
16	BST1	Controller 1 High-Side Gate-Driver Supply. Connect a 0.1µF ceramic capacitor from BST1 to LX1.
17	DH1	Controller 1 High-Side Gate-Driver Output. DH1 drives the gate of the high-side MOSFET.
18	LX1	Controller 1 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX1.
19	DREG1	Controller 1 Low-Side Gate-Driver Supply. Connect externally to REG through a 1Ω to 4.7Ω resistor. Connect a minimum of 0.22µF ceramic capacitor from DREG1 to PGND1.
20	DL1	Controller 1 Low-Side Gate-Driver Output. DL1 is the gate-driver output for the synchronous MOSFET.
21	PGND1	Controller 1 Power Ground. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND1. Connect to SGND at a single point near the input capacitor return terminal.
22	COMP3	Controller 3 Transconductance Error-Amplifier Output. Connect COMP3 to the compensation feedback network of output 3.
23	FB3	Controller 3 Feedback Regulation Point. Connect to the center tap of a resistive voltage-divider from the converter output to SGND to set the output voltage. The FB3 voltage regulates to 0.6V (typ).
24	EN3	Controller 3 Enable/Tracking Input. See Figure 2. When tracking (MAX15048), connect the same resistive voltage-divider used for FB3 from output 1 to EN3 to SGND for coincident tracking. Connect EN3 to analog ground for ratiometric tracking. When sequencing (MAX15049), EN3 must be above 0.6V for PWM controller 3 to start.
25	BST3	Controller 3 High-Side Gate-Driver Supply. Connect a 0.1µF ceramic capacitor from BST3 to LX3.
26	DH3	Controller 3 High-Side Gate-Driver Output. DH3 drives the gate of the high-side MOSFET.
27	LX3	Controller 3 High-Side MOSFET Source Connection/Synchronous MOSFET Drain Connection. Connect the inductor and the negative side of the boost capacitor to LX3.
28	DREG3	Controller 3 Low-Side Gate-Driver Supply. Connect externally to REG through a 1Ω to 4.7Ω resistor. Connect a minimum of 0.22µF ceramic capacitor from DREG3 to PGND3.
29	DL3	Controller 3 Low-Side Gate-Driver Output. DL3 is the gate-driver output for the synchronous MOSFET.
30	PGND3	Controller 3 Power Ground. Connect the input filter capacitor's negative terminal, the source of the synchronous MOSFET, and the output filter capacitor's return to PGND3.
31	IN	Supply Input Connection. Connect to an external voltage source from 4.7V to 23V. For 4.5V to 5.5V input applications, connect IN and REG together.
32	REG	5V Regulator Output. Bypass with a 2.2µF ceramic capacitor to SGND.
—	EP	Exposed Pad. Solder the exposed pad to a large SGND plane to improve thermal dissipation.

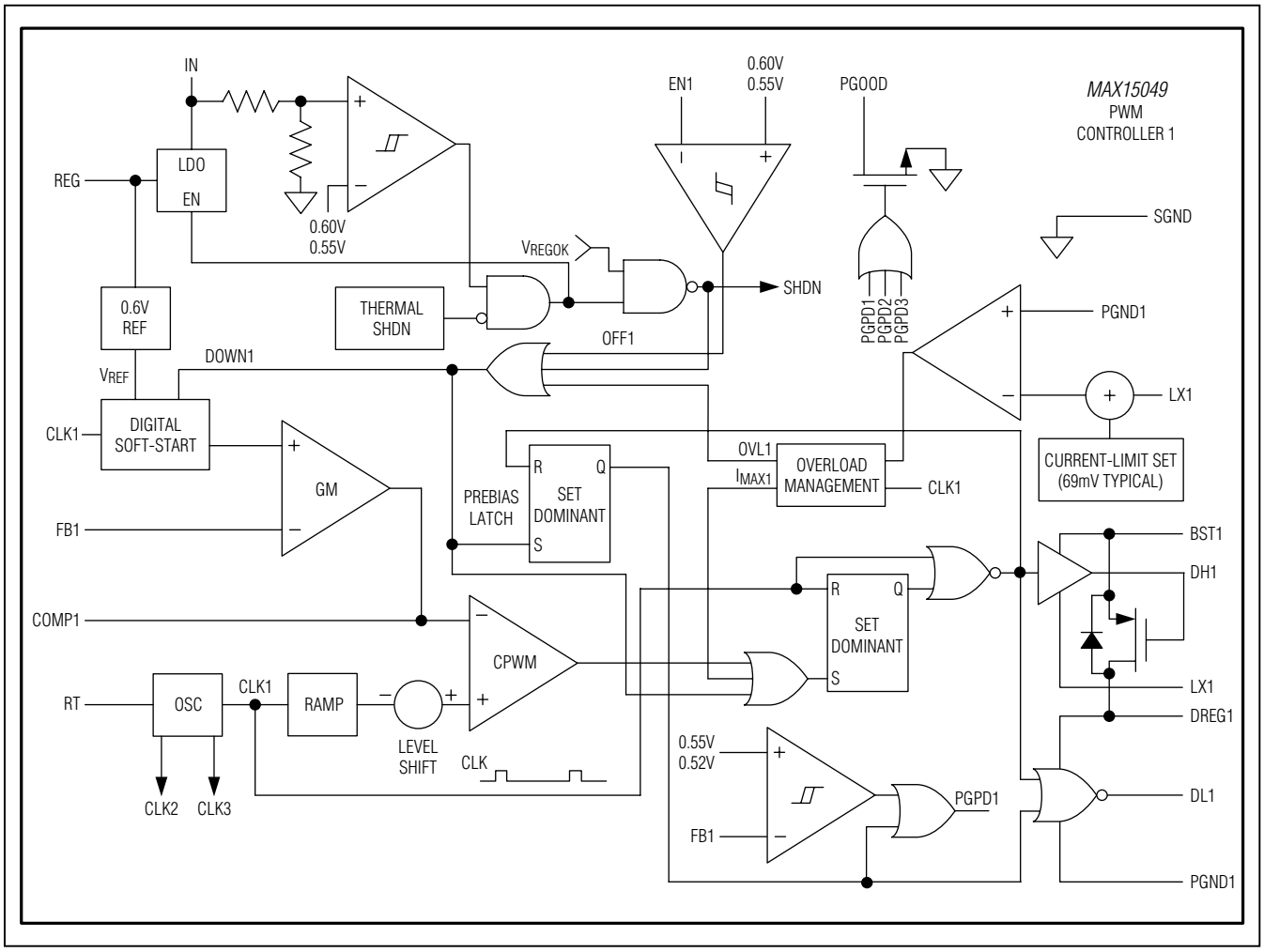
Functional Diagrams



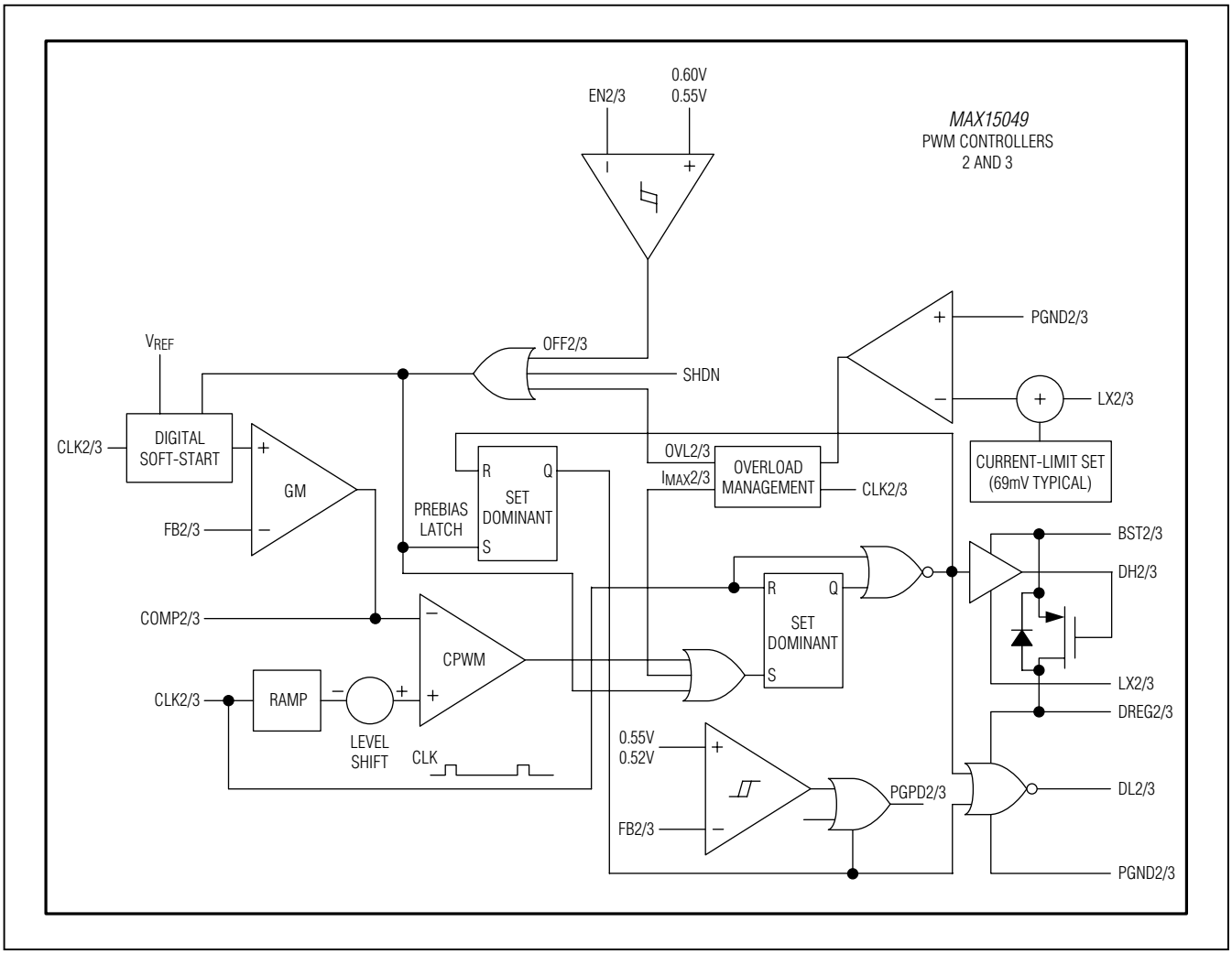
Functional Diagrams (continued)



Functional Diagrams (continued)



Functional Diagrams (continued)



Detailed Description

The MAX15048/MAX15049 are triple-output, PWM, step-down, DC-DC controllers with tracking and sequencing options. The devices operate over the 4.7V to 23V or 5V ±10% input voltage range. Each PWM controller provides an adjustable output down to 0.6V and delivers up to 15A of load current with excellent load and line regulation. The MAX15049 can start into prebiased outputs. This ensures the glitch-free output voltage power-up in the case of parallel power modules. The MAX15048/MAX15049 are optimized for high performance, small-size power-management solutions.

Each of the MAX15048/MAX15049 PWM sections utilizes a voltage-mode control scheme for good noise immunity and offer external compensation, allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The devices operate at a fixed switching frequency that is programmable from 200kHz to 1.2MHz. Each converter, operating at up to 1.2MHz with 120° out-of-phase, increases the input capacitor ripple frequency up to 3.6MHz, reducing the RMS input-ripple current and the size of the input bypass capacitor requirement significantly.

The MAX15048 provides either coincident tracking or ratiometric tracking, and the MAX15049 provides sequencing. This allows tailoring of the power-up/power-down sequence depending on the system requirements. The MAX15048/MAX15049 integrate boost diodes for additional system cost savings.

The MAX15048/MAX15049 feature lossless valley-mode current-limit protection through monitoring the voltage drop across the synchronous MOSFET's on-resistance. The internal current source of these devices exhibits a positive temperature coefficient to help compensate for the MOSFET's temperature coefficient.

The MAX15048/MAX15049 include internal UVLO with hysteresis, digital soft-start, and soft-stop (the MAX15048 only) for glitch-free power-up and power-down of the converter. The power-good circuitry (PGOOD) monitors all three outputs and provides a PGOOD signal to a system controller/processor indicating when all outputs are within regulation. Protection features include lossless valley-mode current limit, hiccup mode output short-circuit protection, and thermal shutdown.

Internal Undervoltage Lockout (UVLO)

V_{IN} must exceed the default UVLO threshold before any operation can commence. The UVLO circuitry keeps the MOSFET drivers, oscillator, and all the internal circuitry shut down to reduce current consumption. The UVLO rising threshold is 4.2V with 300mV hysteresis.

Digital Soft-Start (MAX15048/MAX15049)/ Soft-Stop (MAX15048)/ Prebiased Output (MAX15049)

The soft-start feature of the MAX15048/MAX15049 allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after V_{IN} exceeds the UVLO threshold and the enable input is above 0.6V. The soft-start circuitry gradually ramps up the reference voltage. This controls the rate of rise of the output voltage and reduces input surge currents during startup. The soft-start duration is 2048 clock cycles. The output voltage is incremented through 64 equal steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

For the MAX15048, soft-stop commences when the enable input falls below 0.55V. The soft-stop circuitry ramps down the reference voltage controlling the output voltage rate of fall. The output voltage is decremented through 64 equal steps in 2048 clock cycles.

The MAX15049 can start into a prebiased load. During soft-start, both switches are kept off until the PWM comparator commands the first PWM pulse. Until then, the converters do not sink current from the outputs. The first PWM pulse occurs when the ramping reference voltage increases above the FB_ voltage.

Internal Linear Regulator (REG)

REG is the output terminal of a 5V LDO powered from IN, which provides power to the IC. Connect REG externally to DREG_ to provide power for the low-side MOSFET gate drivers. Bypass REG to SGND with a minimum 2.2µF ceramic capacitor. Place the capacitor physically close to the MAX15048/MAX15049 to provide good bypassing. REG is intended for powering only the internal circuitry and should not be used to supply power to external loads. REG can source up to 60mA. This current, I_{REG}, includes quiescent current (I_Q) and gate-drive current ($I_{DREG_}$):

$$I_{REG} = I_Q + [f_{SW} \times \Sigma(Q_{GHS_} + Q_{GLS_})]$$

where $Q_{GHS_}$ and $Q_{GLS_}$ equal the total gate charge of each of the respective high- and low-side external MOSFETs at V_{GATE} = 5V, f_{SW} is the switching frequency of the converter, and I_Q is the quiescent current of the device at the switching frequency.

MOSFET Gate Drivers and Internal Boost Switch

DREG_ is the supply input for the low-side MOSFET driver. Connect DREG_ to REG externally. Every time the low-side MOSFET switches on, high peak current is drawn from DREG_ for a short time. Adding an RC filter (1Ω to 4.7Ω and 220nF ceramic capacitors are typical) from REG to DREG_ filters out these high-peak currents. Alternatively, DREG_ can be connected to an external source ($V_{DREG-EXT}$). Note that the DREG_ voltage should be high enough to fully enhance the low-side MOSFET. To avoid partial enhancing of the MOSFETs, use $V_{DREG-EXT}$ to set the UVLO externally using EN1.

BST_ supplies the power for the high-side MOSFET drivers. The MAX15048/MAX15049 consist of an internal switch between DREG_ and BST_ to boost DH_ voltage above V_{IN}, providing the necessary gate-to-source voltage to turn on the high-side MOSFET. Connect a bootstrap 0.1µF or higher ceramic capacitor between BST_ and LX_.

The high-side (DH_) and low-side (DL_) drivers drive the gates of the external n-channel MOSFETs. The drivers' 1A peak source-and-sink-current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced switching losses.

The gate-driver circuitry also provides a break-before-make time (35ns typ) to prevent shoot-through currents during transition.

MAX15048 Coincident/ Ratiometric Tracking (EN_)

The enable input (EN_) in conjunction with digital soft-start and soft-stop provide coincident/ratiometric tracking. Track an output voltage by connecting a resistive voltage-divider from the output being tracked to the enable/tracking input. For example, for V_{OUT2} to coincidentally track V_{OUT1}, connect the same resistive voltage-divider used for FB2 from OUT1 to EN2 to SGND. See Figure 2 and the *Typical Operating Characteristics* (Coincident Tracking).

Track ratiometrically by connecting EN_ to SGND. This synchonizes the soft-start and soft-stop of all the controllers' references, and hence their respective output voltages track ratiometrically. See Figure 2 and the *Typical Operating Characteristics* (Ratiometric Tracking).

For the MAX15048, the output short-circuit fault situations at master or slave outputs are handled carefully so that either the master or slave output does not stay on when the other outputs are shorted to ground. When the slave is shorted and enters in hiccup mode, both the master and the other slave soft-stop. When the master is shorted and the part enters hiccup mode, the slaves ratiometrically soft-stop. Coming out of the hiccup, all outputs soft-start coincidently or ratiometrically depending on their initial configuration. See the *Typical Operating Characteristics* for the output behavior during the fault conditions. During the thermal shutdown or power-off when the input falls below its UVLO, the output voltages fall down at a rate depending on the respective output capacitor and load.

See Figure 1 for a graphical representation of coincident/ratiometric tracking (MAX15048) or sequencing (MAX15049).

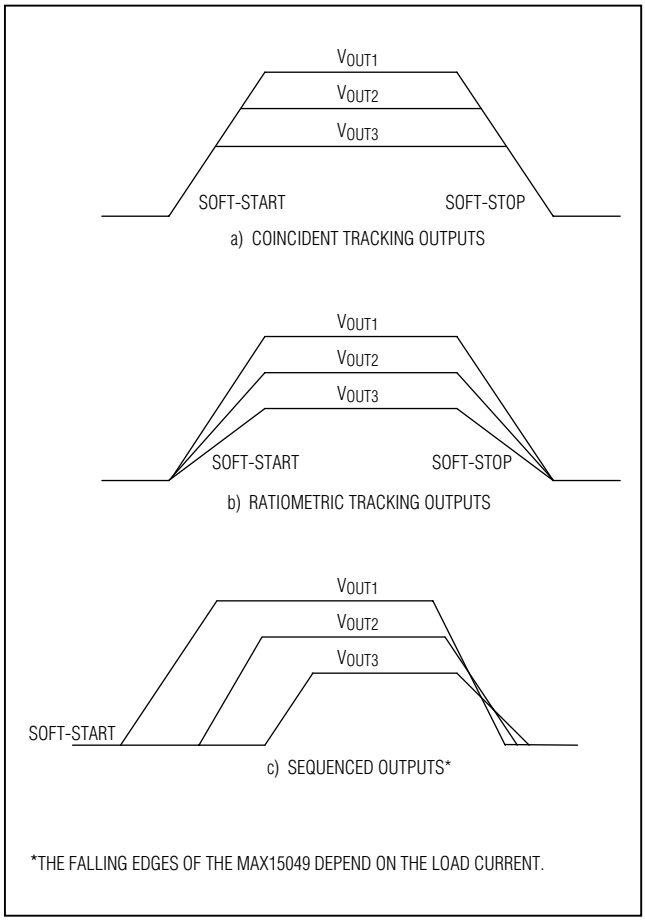


Figure 1. Graphical Representation of Coincident Tracking, Ratiometric Tracking (MAX15048), or Sequencing (MAX15049)

MAX15049 Output-Voltage Sequencing (EN_)

In Figure 1c, when sequencing, the enable input must be above 0.6V for each PWM controller to start. The $V_{OUT_}$ outputs and EN_ inputs can be daisy-chained to generate power sequencing. See Figure 2 and the *Typical Operating Characteristics* ($V_{OUT_}$ to EN_ Sequencing). Alternately, connect a resistive voltage-divider from the voltage to be sequenced from the enable input to SGND to set when each controller should start.

Error Amplifier

The output of the internal transconductance error amplifier (COMP_) is provided for frequency compensation (see the *Compensation Design Guidelines* section). FB_ is the inverting input and COMP_ is the output of the error amplifier. The error transamplifier has an 80dB open-loop gain and a 10MHz GBW product. See the *Typical Operating Characteristics* for a plot of gain and phase vs. frequency.

Output Short-Circuit Protection (Hiccup Mode)

The current-limit circuit employs a valley current-limiting algorithm that uses the synchronous MOSFET's on-resistance as the current-sensing element. The current-limit threshold is internally set at 69mV (typ). Once the high-side MOSFET turns off, the voltage across the current-sensing element is monitored. If this voltage does not exceed the current-limit threshold, the high-side MOSFET turns on normally at the start of the next cycle. If the voltage exceeds the current-limit threshold

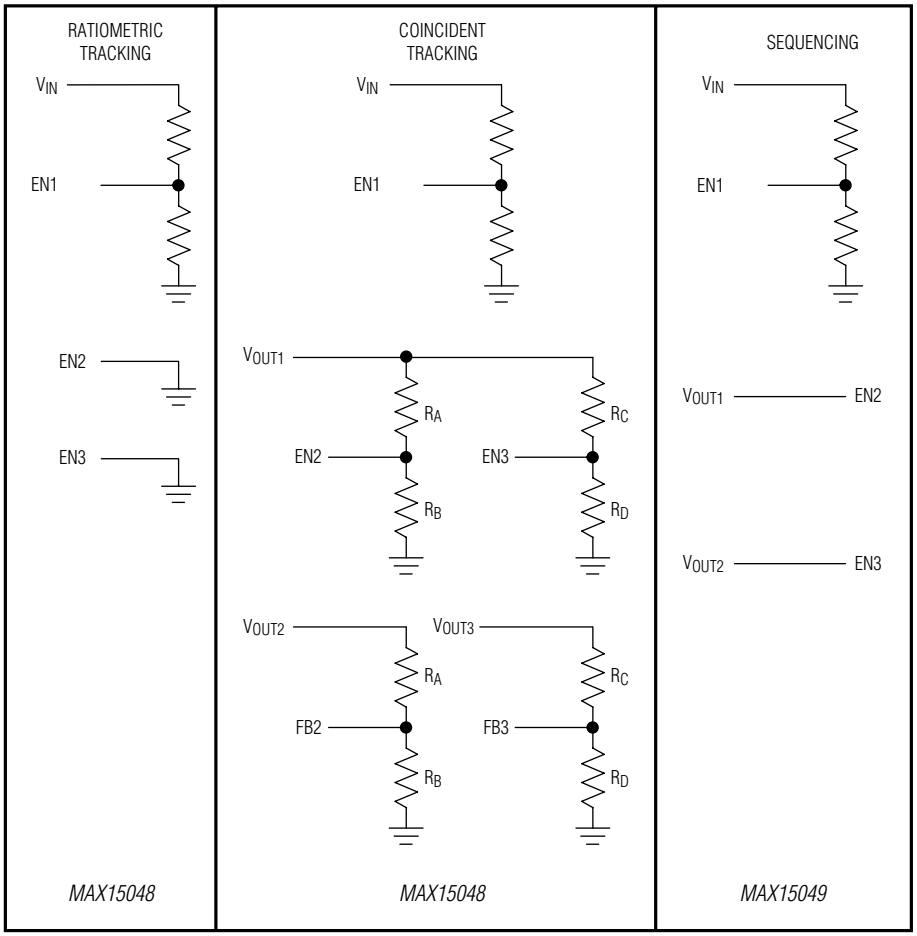


Figure 2. Ratiometric Tracking, Coincident Tracking (MAX15048), and Sequencing (MAX15049) Configurations

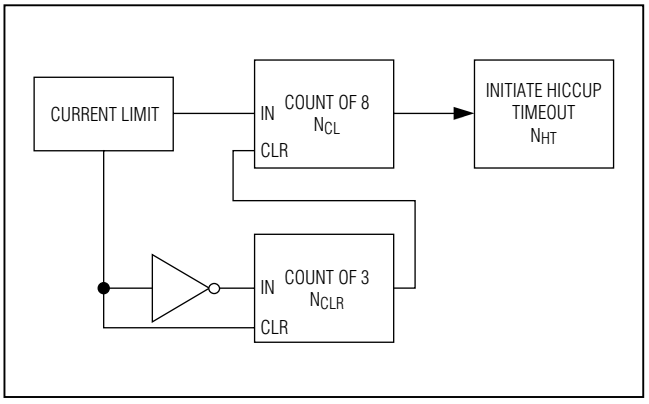


Figure 3. Hiccup-Mode Block Diagram

just before the beginning of a new PWM cycle, the controller skips that cycle. During severe overload or short-circuit conditions, the switching frequency of the device appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

If the current-limit threshold is exceeded for more than eight cumulative clock cycles (N_{CL}), the device shuts down (both DH_ and DL_ are pulled low) for 4096 clock cycles (hiccup timeout) and then restarts with a soft-start sequence. If three consecutive cycles pass without a current-limit event, the count of N_{CL} is cleared (see Figure 3). Hiccup mode protects the circuit against a continuous output short circuit.

Thermal-Overload Protection

The MAX15048/MAX15049 feature an integrated thermal-overload protection with temperature hysteresis. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal-fault condition. When the die temperature exceeds +160°C (typ), an internal thermal sensor shuts down the device, turning off the power MOSFETs and allowing the die to cool. After the die temperature falls by +20°C (typ), the part restarts with a soft-start sequence.

Design Procedure

Setting the Switching Frequency

Connect a 15.625kΩ to 93.75kΩ resistor from RT to SGND to program the switching frequency from 200kHz to 1.2MHz. Calculate the switching frequency using the following equation:

$$f_{SW}\ (kHz) = 12.8 \times R_{RT}\ (k\Omega)$$

Higher switching frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Effective Input Voltage Range

Although the MAX15048/MAX15049 converters can operate from input supplies ranging from 4.7V to 23V, the input voltage range can be effectively limited by the duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum on-time ($t_{ON(MIN)}$):

$$V_{IN(MAX)} \le \frac{V_{OUT_}}{t_{ON(MIN)} \times f_{SW}}$$

where $t_{ON(MIN)}$ is 75ns.

The minimum input voltage is limited by the maximum duty cycle and is calculated using the following equation:

$$V_{IN(MIN)} = \frac{V_{OUT_}}{1-(t_{OFF(MIN)} \times f_{SW})}$$

where $t_{OFF(MIN)}$ typically is equal to 300ns.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15048/MAX15049: inductance value (L), inductor saturation current (I_{SAT}), and inductor series resistance (DCR). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value. A lower inductance value minimizes size and cost and improves large-signal and transient response. However, efficiency is reduced due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. A higher inductance increases efficiency by reducing the ripple current; however, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good rule of thumb is to choose ΔI_{P-P} equal to 30% of the full load current. Calculate the inductance using the following equation:

$$L = \frac{V_{OUT_}(V_{IN} - V_{OUT_})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and $V_{OUT_}$ are typical values so that efficiency is optimum for typical conditions. The switching frequency

(f_{SW}) is programmable between 200kHz and 1.2MHz (see the *Setting the Switching Frequency* section). The peak-to-peak inductor current (ΔI_{P-P}), which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output-Capacitor Selection* section to verify that the worst-case output current ripple is acceptable. The inductor saturation current (I_{SAT}) is also important to avoid runaway current during continuous output short-circuit conditions. Select an inductor with an I_{SAT} specification higher than the maximum peak current. Inductor parasitic resistance (DCR) causes copper losses and affects efficiency. Select a low-loss inductor having the lowest possible DCR that fits in the allocated dimensions.

Input-Capacitor Selection

The discontinuous input current of the buck converter causes large input-ripple currents, and therefore, the input capacitor must be carefully chosen to withstand the input-ripple current and keep the input-voltage ripple within design requirements. The 120° ripple phase operation increases the frequency of the input capacitor ripple current to thrice the individual converter switching frequency. When using ripple phasing, the worst-case input-capacitor ripple current is when only one converter with the highest output current is on.

The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}, which peaks at the end of the on cycle. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \times \left(\frac{V_{OUT_}}{V_{IN}}\right)}{\left(\Delta V_Q + f_{SW}\right)}$$

where:

$$\Delta I_{P-P} = \frac{\left(V_{IN} - V_{OUT_}\right) \times V_{OUT_}}{V_{IN} \times f_{SW} \times L}$$

$I_{LOAD(MAX)}$ is the maximum output current, ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

For the condition with only one converter on, calculate the input-ripple current using the following equation:

$$I_{CIN(RMS)} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT_} \times \left(V_{IN} - V_{OUT_}\right)}}{V_{IN}}$$

The MAX15048/MAX15049 include UVLO hysteresis to avoid possible unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. At lower input voltage, additional input capacitance helps avoid possible undershoot below the UVLO threshold during transient loading.

Output-Capacitor Selection

The allowed output-voltage ripple and the maximum deviation of the output voltage during load steps determine the required output capacitance and its ESR. The steady-state output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the ESR of the output capacitor). The equations for calculating the output capacitance and its ESR are:

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

ΔV_{ESR} and ΔV_Q are not directly additive since they are out of phase from each other. If using ceramic capacitors, which generally have low ESR, ΔV_Q dominates. If using electrolytic capacitors, ΔV_{ESR} dominates.

The allowable deviation of the output voltage during fast-load transients also affects the output capacitance, its ESR, and its ESL. The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the gain bandwidth of the converter (see the *Compensation Design Guidelines* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL, and the capacitor discharge causes a voltage droop during the load-step (I_{STEP}). Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for better load-transient and voltage-ripple performance. Nonleaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output-voltage deviation below the tolerable limits of the electronics being powered.

Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

$$t_{RESPONSE} = \frac{1}{3 \times f_{CO}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, $t_{RESPONSE}$ is the response time of the controller, and f_{CO} is the closed-loop crossover frequency of system (see the *Compensation Design Guidelines* section).

Setting the Current Limit

The MAX15048/MAX15049 use a valley current-sense method for current limiting. The valley current-limit threshold (V_{LIM}) is internally set at 69mV (typ).

The voltage drop across the low-side MOSFET due to its on-resistance is used to sense the inductor current. The voltage drop (V_{VALLEY}) across the low-side MOSFET at the valley point and at I_{LOAD} is:

$$V_{VALLEY} = R_{DS(ON)} \times (I_{LOAD(MAX)} - \frac{\Delta I_{P-P}}{2})$$

$R_{DS(ON)}$ is the on-resistance of the low-side MOSFET, I_{LOAD} is the rated load current, and ΔI_{P-P} is the peak-to-peak inductor current.

The $R_{DS(ON)}$ of the MOSFET varies with temperature. Calculate the $R_{DS(ON)}$ of the MOSFET at its operating junction temperature at full load using its data sheet. To compensate for this temperature variation, the current-limit circuitry has a temperature coefficient of 3333ppm/°C. This allows the valley current-limit threshold (V_{LIM}) to track and partially compensate for the increase in the $R_{DS(ON)}$ of the synchronous MOSFET with increasing temperature.

Power-MOSFET Selection

When choosing the n-channel MOSFETs, consider the total gate charge, $R_{DS(ON)}$, power dissipation, the maximum drain-to-source voltage, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs that are optimized for high-frequency switching applications. The average gate-drive current from the MAX15048/MAX15049s' output is proportional to the frequency and gate charge required to drive the MOSFET. The power dissipated in the MAX15048/MAX15049 is proportional to the input voltage and the average drive current (see the *Power Dissipation* section).

Compensation Design Guidelines

The MAX15048/MAX15049 use a fixed-frequency, voltage-mode control scheme that regulates the output voltage by differentially comparing the "sampled" output voltage against a fixed reference. The subsequent "error" voltage—that appears at the error-amplifier output (COMP_)—is compared against an internal ramp voltage to generate the required duty cycle of the pulse-width modulator. A 2nd-order lowpass LC filter removes the switching harmonics and passes the DC component of the pulse-width-modulated signal to the output. The LC filter, which has an attenuation slope of -40dB/decade, introduces 180° out-of-phase shift at frequencies above the LC resonant frequency. This phase shift, in addition to the inherent 180° of phase shift of the regulator's self-governing (negative) feedback system, poses the potential for positive feedback. The error amplifier and its associated circuitry are designed to compensate for this instability in order to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, associated circuitry, and LC filter), an output feedback divider, and an error amplifier. The power modulator has a DC gain set by V_{IN}/V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}), and its ESR. A second, higher frequency zero also exists, which is a function of the output capacitor's ESR and ESL, though only taken into account when using very high-quality filter components and/or frequencies of operation.

Below are equations that define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$f_{ZERO,\ ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{ZERO,\ ESL} = \frac{ESR}{2\pi \times ESL}$$

The switching frequency is programmable between 200kHz and 1.2MHz using an external resistor at RT. Typically, the crossover frequency (f_{CO}), which is the frequency when the system's closed-loop gain is equal to unity, crosses the 0dB axis, and should be set at or below 1/10 the switching frequency (f_{SW}/10) for stable, closed-loop response.

The MAX15048/MAX15049 provide an internal transconductance amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output-filtering components, especially the output capacitor. For cost-sensitive applications, use aluminum electrolytic capacitors; for space-sensitive applications, use low ESR tantalum or multilayer ceramic chip (MLCC) capacitors at the output. The higher switching frequencies of the MAX15048/MAX15049 allow the use of MLCC as the primary filter capacitor(s).

First, select the passive and active power components that meet the application's output ripple, component size, and component cost requirements. Second, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined below.

Closed-Loop Response and Compensation of Voltage-Mode Regulators

The power modulator's LC lowpass filter exhibits a variety of responses, depending on the value of L and C (and their parasitics).

One such response is shown in Figure 4a. In this example, the power modulator's uncompensated crossover is approximately 1/6 the desired crossover frequency, f_{CO}. Note also, the uncompensated rolloff through 0dB plane follows the double-pole, -40dB/decade slope and approaches 180° of phase shift, indicative of a potentially unstable system. Together with the inherent 180° of phase delay in the negative feedback system, this can lead to near 360°, or "positive" feedback—an unstable system.

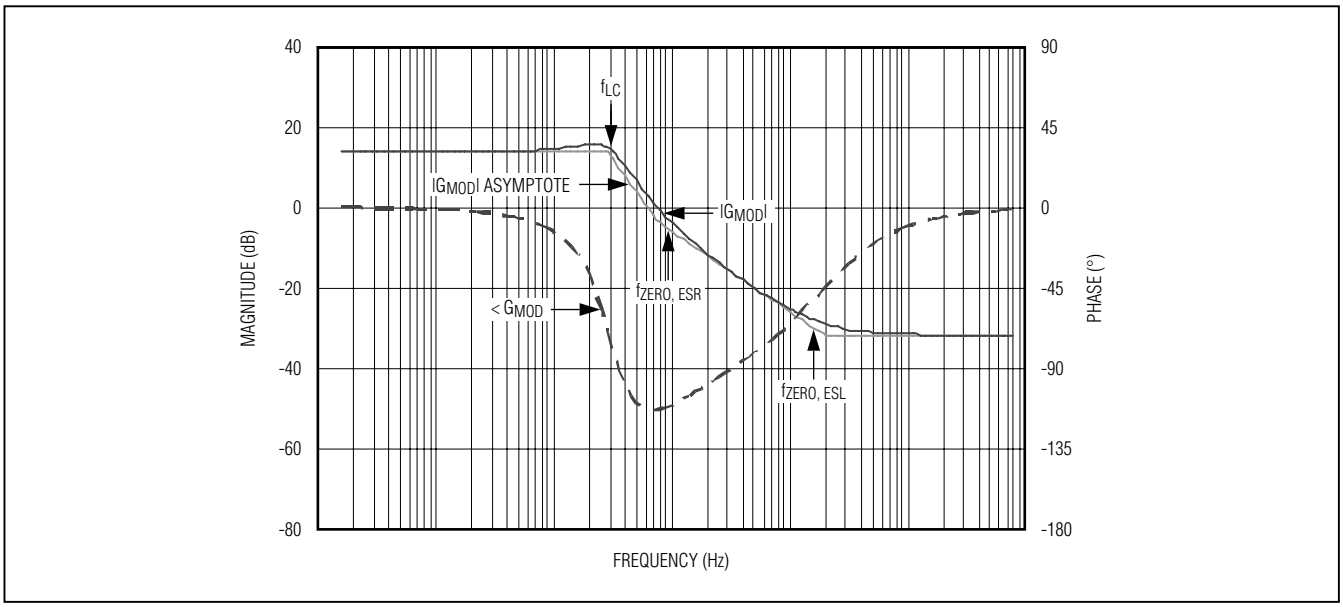


Figure 4a. Power Modulator Gain and Phase Response (Large, Bulk C_{OUT})

The desired (compensated) rolloff follows a -20dB/decade slope (and commensurate 90° of phase shift), and, in this example, occurs at approximately six times the uncompensated crossover frequency, f_{CO}. In this example, a Type II compensator provides stable closed-loop operation, leveraging the +20dB/decade slope of the capacitor's ESR zero (see Figure 4b).

The Type II compensator's midfrequency gain (approximately 18dB shown here) is designed to compensate for the power modulator's attenuation at the desired crossover frequency, f_{CO} ($G_{E/A}$ + G_{MOD} = 0dB at f_{CO}). In this example, the power modulator's inherent -20dB/decade rolloff above the ESR zero ($f_{ZERO, ESR}$) is leveraged to extend the active regulation gain bandwidth of the voltage regulator. As shown in Figure 4b, the net result is a six-time increase in the regulator's gain bandwidth while providing greater than 75° of phase margin (the difference between $G_{E/A}$ and G_{MOD} respective phases at crossover, f_{CO}).

Other filter schemes pose their own problems. For instance, when choosing high-quality filter capacitor(s) (e.g., MLCCs) and inductor, with minimal parasitics, the inherent ESR zero can occur at a much higher frequency, as shown in Figure 4c.

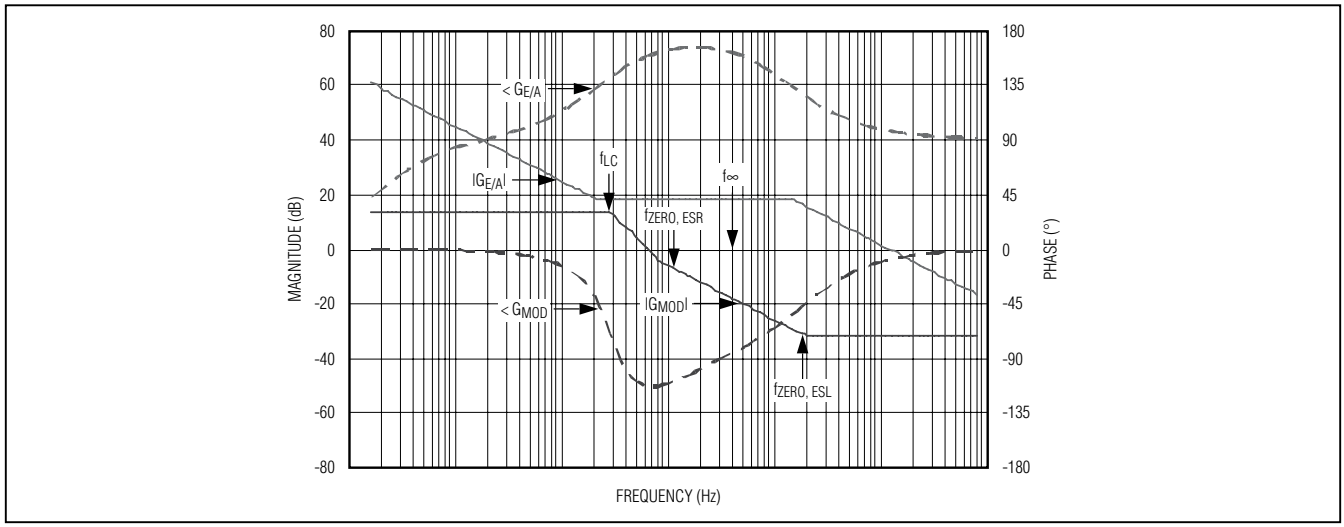


Figure 4b. Power Modulator (Large, Bulk C_{OUT}) and Type II Compensator Responses

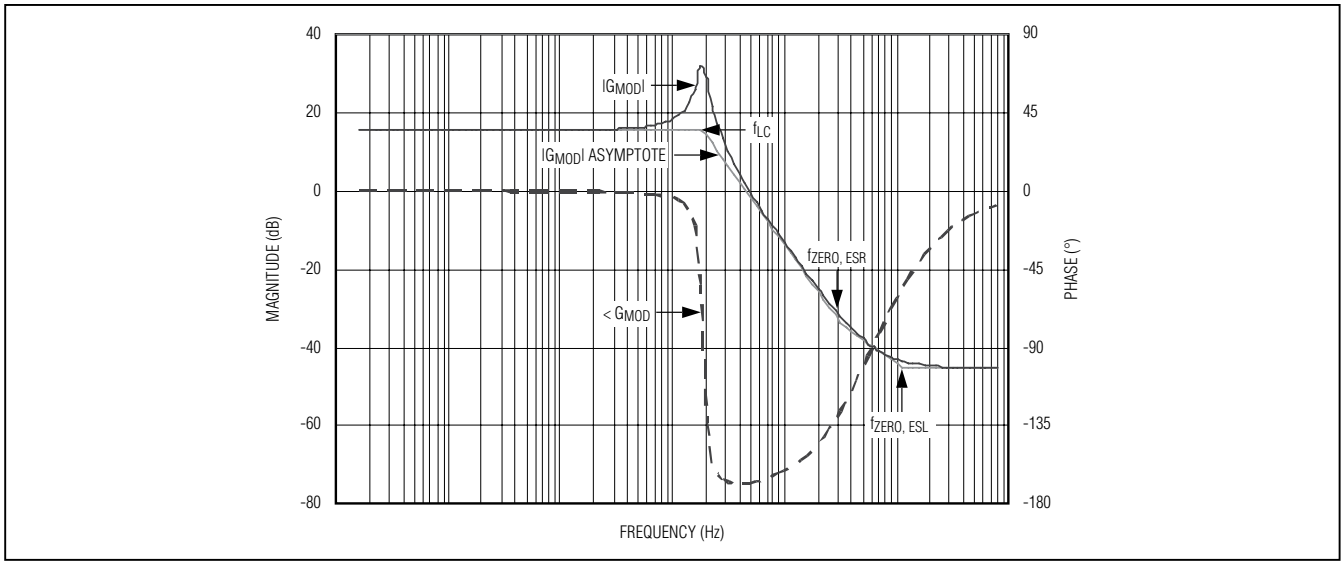


Figure 4c. Power Modulator Gain and Phase Response (High-Quality C_{OUT})

As with the previous example, the actual gain and phase response is overlaid on the power modulator's asymptotic gain response. It is readily observed that the more dramatic gain and phase transition at or near the power modulator's resonant frequency, f_{LC}, vs. the gentler response of the previous example. This is due to the component's lower parasitics leading to the higher frequency of the inherent ESR zero of the output capacitor. In this example, the desired crossover frequency occurs **below** the ESR zero frequency.

In this example, a compensator with an inherent midfrequency double-zero response is required to mitigate the effects of the filter's double-pole. Such is available with the Type III topology.

As demonstrated in Figure 4d, the Type III's midfrequency double-zero gain (exhibiting a +20dB/decade slope, noting the compensator's pole at the origin) is designed to compensate for the power modulator's double-pole -40dB/decade attenuation at the desired crossover frequency, f_{CO} (again, $G_{E/A} + G_{MOD} = 0dB$ at f_{CO}).

In the above example, the power modulator's inherent (midfrequency) -40dB/decade rolloff is mitigated by the midfrequency double-zero's +20dB/decade gain to extend the active regulation gain bandwidth of the voltage regulator. As shown in Figure 4d, the net result is an approximate doubling in the regulator's gain bandwidth while providing greater than 60° of phase margin (the difference between $G_{E/A}$ and G_{MOD} respective phases at crossover, f_{CO}).

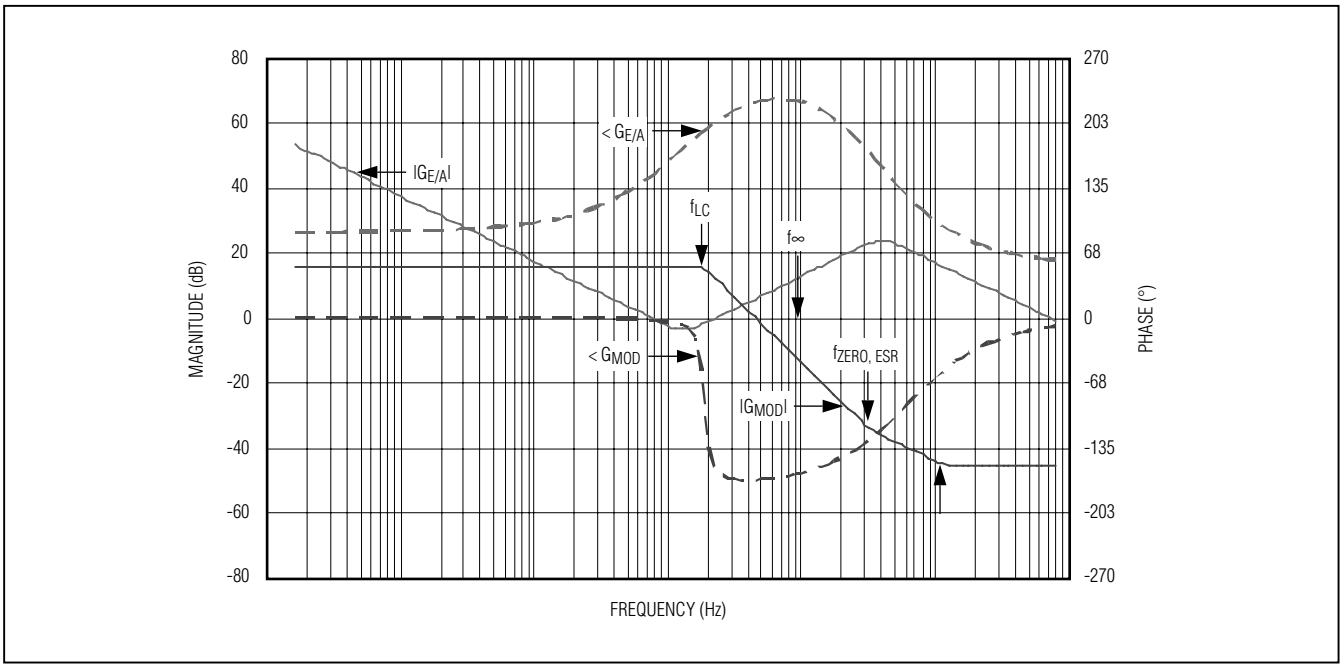


Figure 4d. Power Modulator (High-Quality C_{OUT}) and Type III Compensator Responses

Design procedures for both Type II and Type III compensators are shown below.

Type II: Compensation when $f_{CO} > f_{ZERO, ESR}$

When the $f_{ZERO, ESR}$ is lower than f_{CO} and close to f_{LC}, a Type II compensation network provides the necessary closed-loop response. The Type II compensation network provides a midband compensating zero and high-frequency pole (see Figures 5a and 5b).

R_FC_F provides the midband zero $f_{MID, ZERO}$, and R_FC_{CF} provides the high-frequency pole. Use the following procedure to calculate the compensation network components:

1) Calculate the $f_{ZERO, ESR}$ and LC double pole, f_{LC}:

$$f_{ZERO, ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

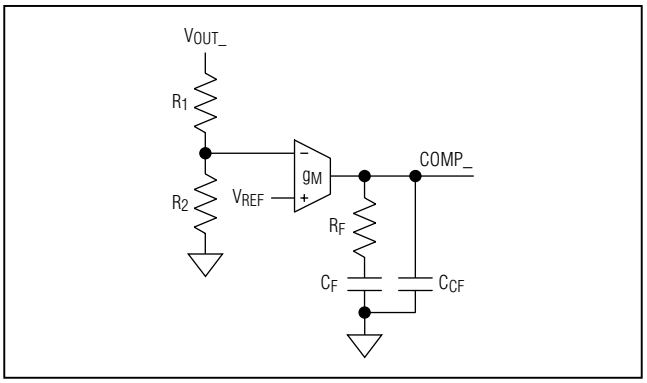


Figure 5a. Type II Compensation Network

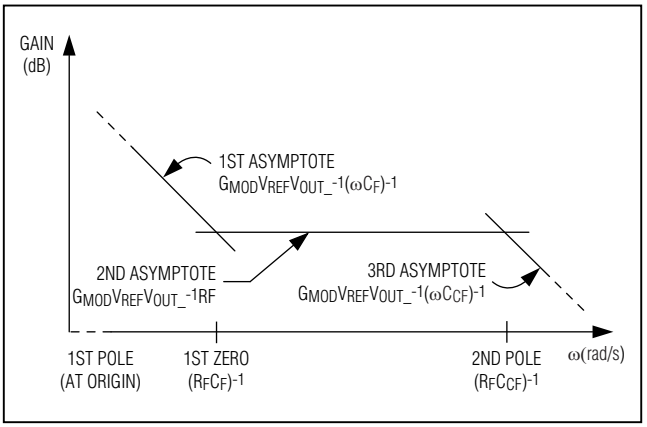


Figure 5b. Type II Compensation Network Response

2) Select the unity-gain crossover frequency as:

$$f_{CO} \le \frac{f_{SW}}{10}$$

3) Determine R_F from the following:

$$R_F = \frac{V_{RAMP} \ (2\pi \times f_{CO} \times L) \ V_{OUT_}}{V_{FB_} \times V_{IN} \times g_{MOD} \times ESR}$$

Note: R_F is derived by setting the total loop gain at crossover frequency to unity, e.g., $G_{E/A}(f_{CO}) \times G_{MOD}(f_{CO}) = 1V/V$. The transconductance error-amplifier gain is $G_{E/A}(f_{CO}) = g_{MOD} \times R_F$, while the modulator gain is:

$$G_{MOD}(f_{CO}) = \frac{V_{IN}}{V_{RAMP}} \times \frac{ESR}{2\pi \times f_{CO} \times L} \times \frac{V_{FB_}}{V_{OUT_}}$$

The total loop gain can be expressed logarithmically as follows:

$$20 \times \log_{10}[g_M R_F] + 20 \times \log_{10}\left[\frac{ESR \times V_{IN} \times V_{FB_}}{(2 \times \pi \times f_{CO} \times L) \times V_{OUT_} \times V_{RAMP}}\right] = 0dB$$

where V_{RAMP} is the peak-to-peak ramp amplitude equal to 1.2V:

4) Place a zero at or below the LC double pole, f_{LC}:

$$C_F = \frac{1}{2\pi \times R_F \times f_{LC}}$$

5) Place a high-frequency pole at or below $f_P = 0.5 \times f_{SW}$:

$$C_{CF} = \frac{1}{\pi \times R_F \times f_{SW}}$$

6) Choose an appropriately sized R_1 (connected from OUT_ to FB_, start with a 10kΩ). Once R_1 is selected, calculate R_2 using the following equation:

$$R_2 = R_1 \times \frac{V_{FB_}}{V_{OUT_} - V_{FB_}}$$

where $V_{FB_} = 0.6V$.

Type III: Compensation when $f_{CO} < f_{ZERO, ESR}$

As previously indicated, the position of the output capacitor's inherent ESR zero is critical in designing an appropriate compensation network. When low-ESR ceramic output capacitors are used, the ESR zero frequency ($f_{ZERO, ESR}$) is usually much higher than unity crossover frequency (f_{CO}). In this case, a Type III compensation network is recommended (see Figure 6a).

As shown in Figure 6b, Type III compensation network introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole at the origin, two zeros, and higher frequency poles. The locations of the zeros and poles should be such that the phase margin peaks at f_{CO}.

Set the ratios of f_{CO}-to-f_Z and f_P-to-f_{CO} equal to five:

$$\left(\frac{f_{CO}}{f_Z} = \frac{f_P}{f_{CO}} = 5\right)$$

to get approximately 60° of phase margin at f_{CO}. Whichever technique is used, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

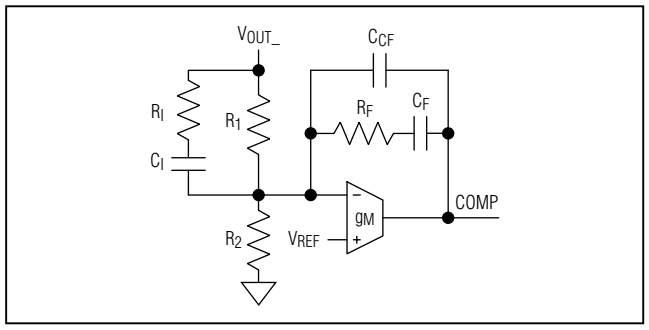


Figure 6a. Type III Compensation Network

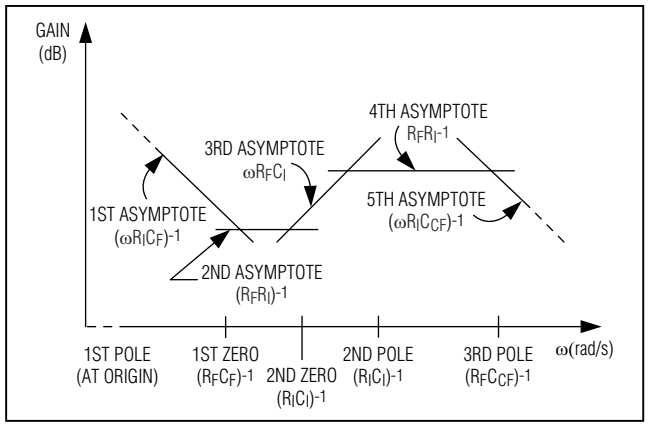


Figure 6b. Type III Compensation Network Response

Use the following procedure to calculate the compensation network components:

1) Select a crossover frequency, f_{CO}:

$$f_{CO} \le \frac{f_{SW}}{10}$$

2) Calculate the LC double-pole frequency, f_{LC} :

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

3) Select $R_F \ge 10k\Omega$.

4) Place a zero:

$$f_{Z1} = \frac{1}{2\pi \times R_F \times C_F} \text{ at } 0.75 \times f_{LC}$$

where:

$$C_F = \frac{1}{2\pi \times R_F \times 0.75 \times f_{LC}}$$

5) Calculate C_I for a target unity-gain crossover frequency, f_C:

$$C_I = \frac{2\pi \times f_{CO} \times L \times C_{OUT} \times V_{RAMP}}{V_{IN} \times R_F}$$

Note: C_I is derived by setting the total loop gain at crossover frequency to unity, e.g. $G_{E/A}(f_{CO}) \times G_{MOD}(f_{CO}) = 1V/V$. The total loop gain can be expressed logarithmically as follows:

$$20 \times \log_{10}\left[2 \times \pi \times f_{CO} \times R_F \times C_I\right] +$$

$$20 \times \log_{10}\left[\frac{G_{MOD(DC)}}{(2 \times \pi \times f_{CO})^2 \times L \times C_{OUT}}\right] = 0dB$$

6) Place a second zero, f_{Z2}, at or below f_{LC}, thereby determining R_1:

$$R_1 = \frac{1}{2\pi \times f_{Z2} \times C_I}$$

7) Place a pole ($f_{P1} = \frac{1}{2\pi \times R_I \times C_I}$) at or below $f_{ZERO, ESR}$:

$$R_I = \frac{1}{2\pi \times f_{ZERO, ESR} \times C_I}$$

8) Place a second pole ($f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}}$) at or below one-half the switching frequency:

$$C_{CF} = \frac{1}{\pi \times f_{SW} \times R_F}$$

9) Calculate R_2 using the following equation:

$$R_2 = R_1 \times \frac{V_{FB_}}{V_{OUT_} - V_{FB_}}$$

where $V_{FB_}$ = 0.6V.

Typical Operating Circuits

Figure 7 shows the MAX15048 coincident tracker. Figure 8 is the MAX15048 ratiometric tracker and Figure 9 is the MAX15049 sequencer. Figure 10 shows the evaluation kit schematic configured for the MAX15049 (sequencer).

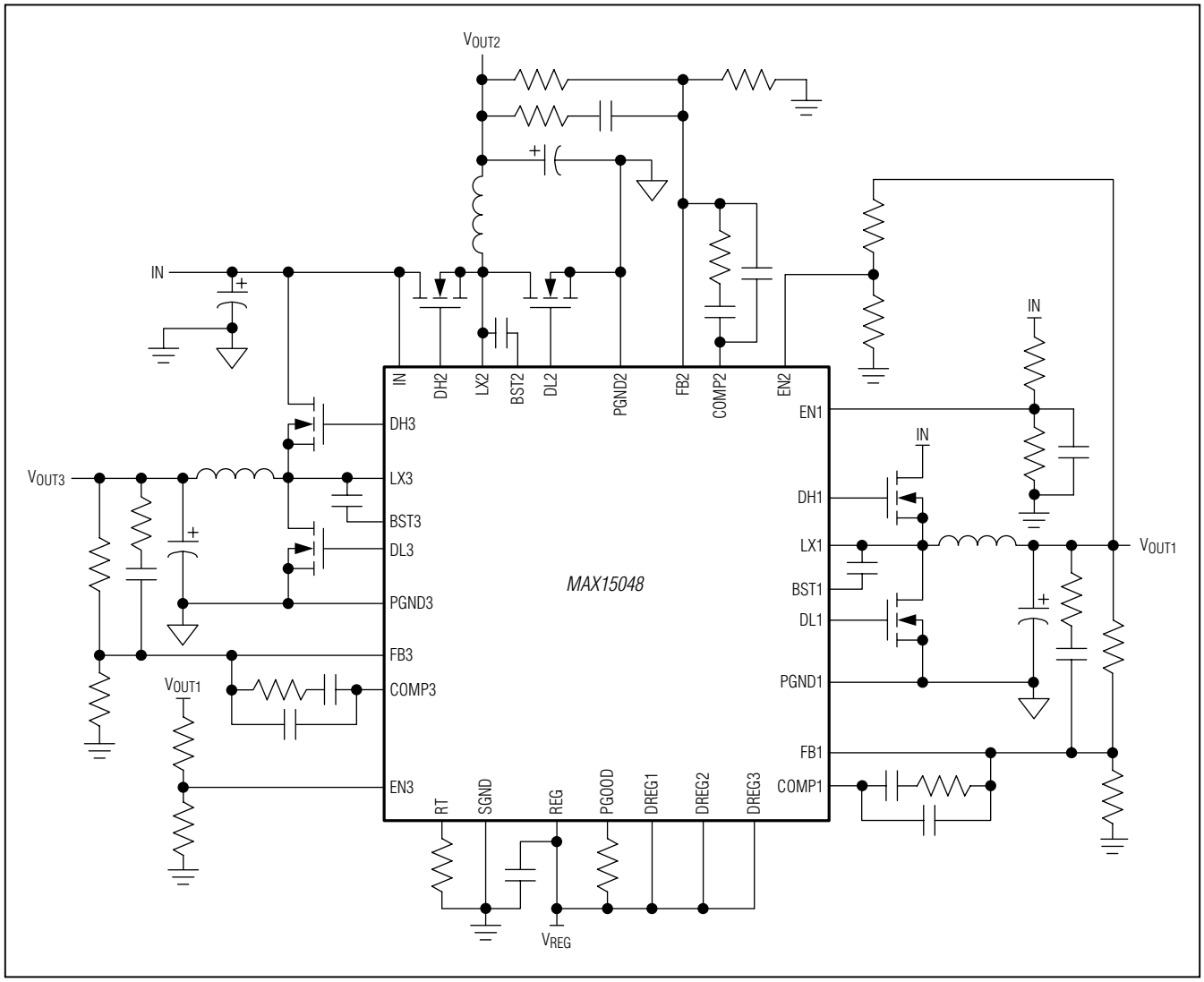


Figure 7. MAX15048 Coincident Tracker Typical Operating Circuit

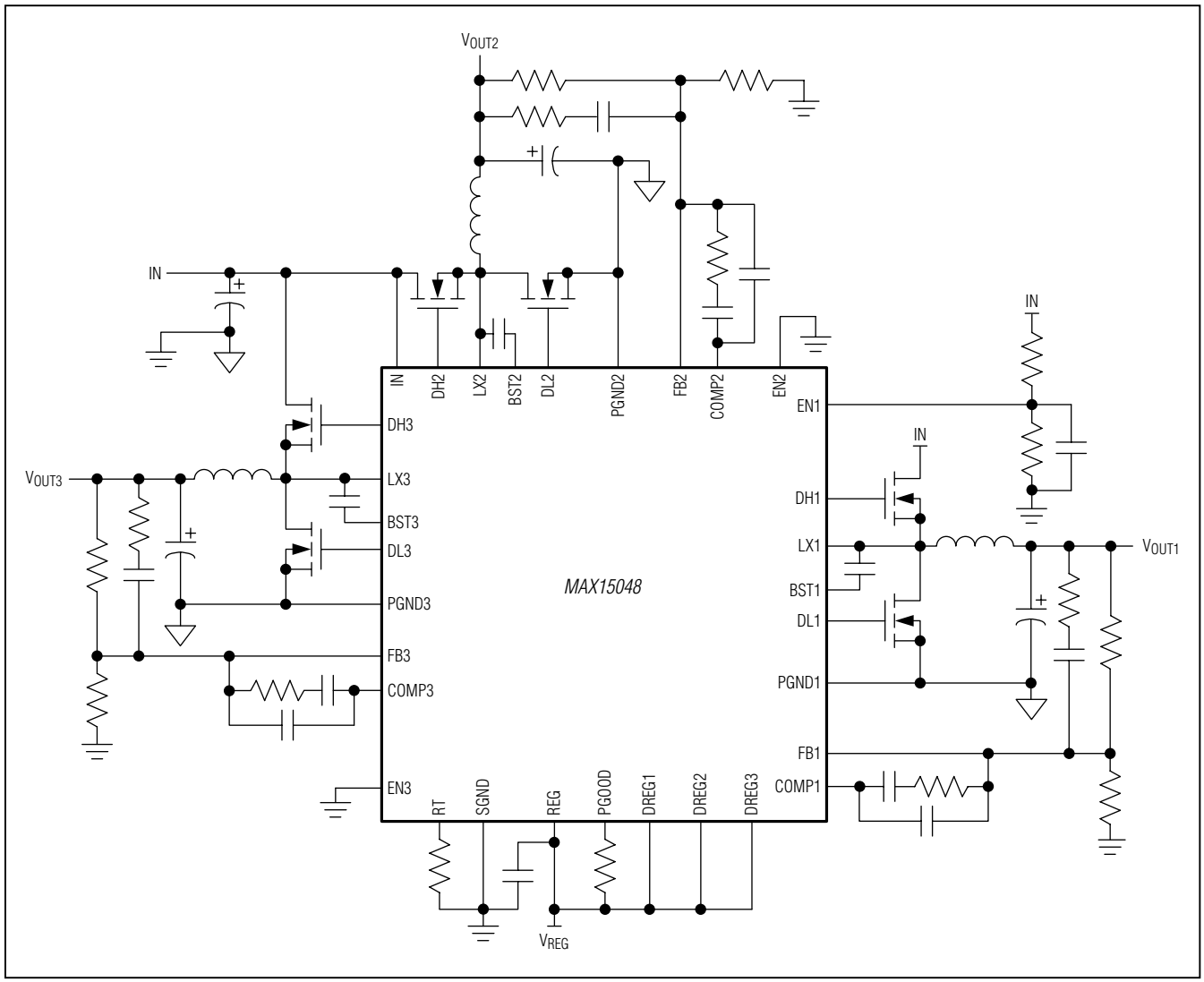


Figure 8. MAX15048 Ratiometric Tracker Typical Operating Circuit

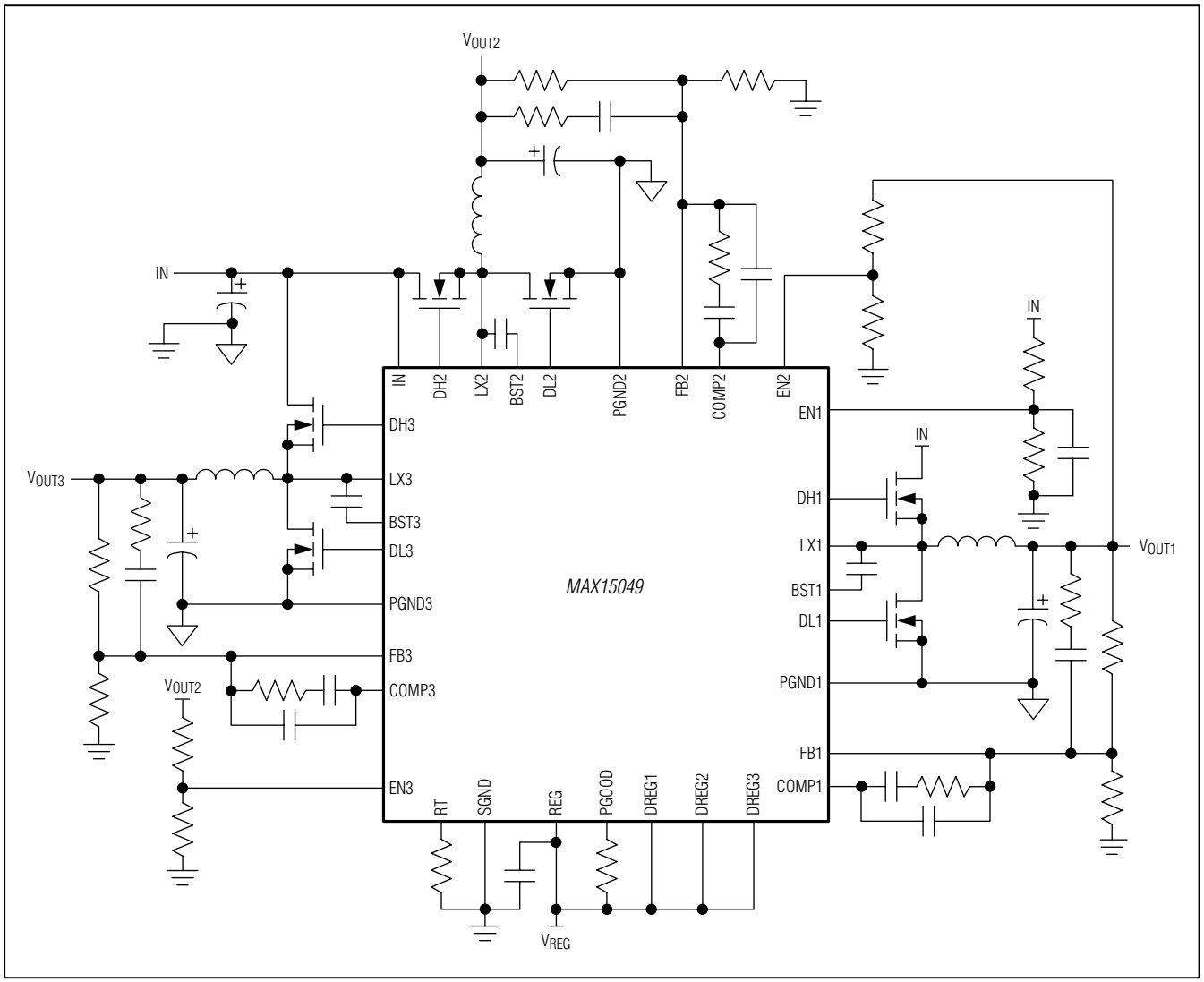


Figure 9. MAX15049 Sequencer Typical Operating Circuit

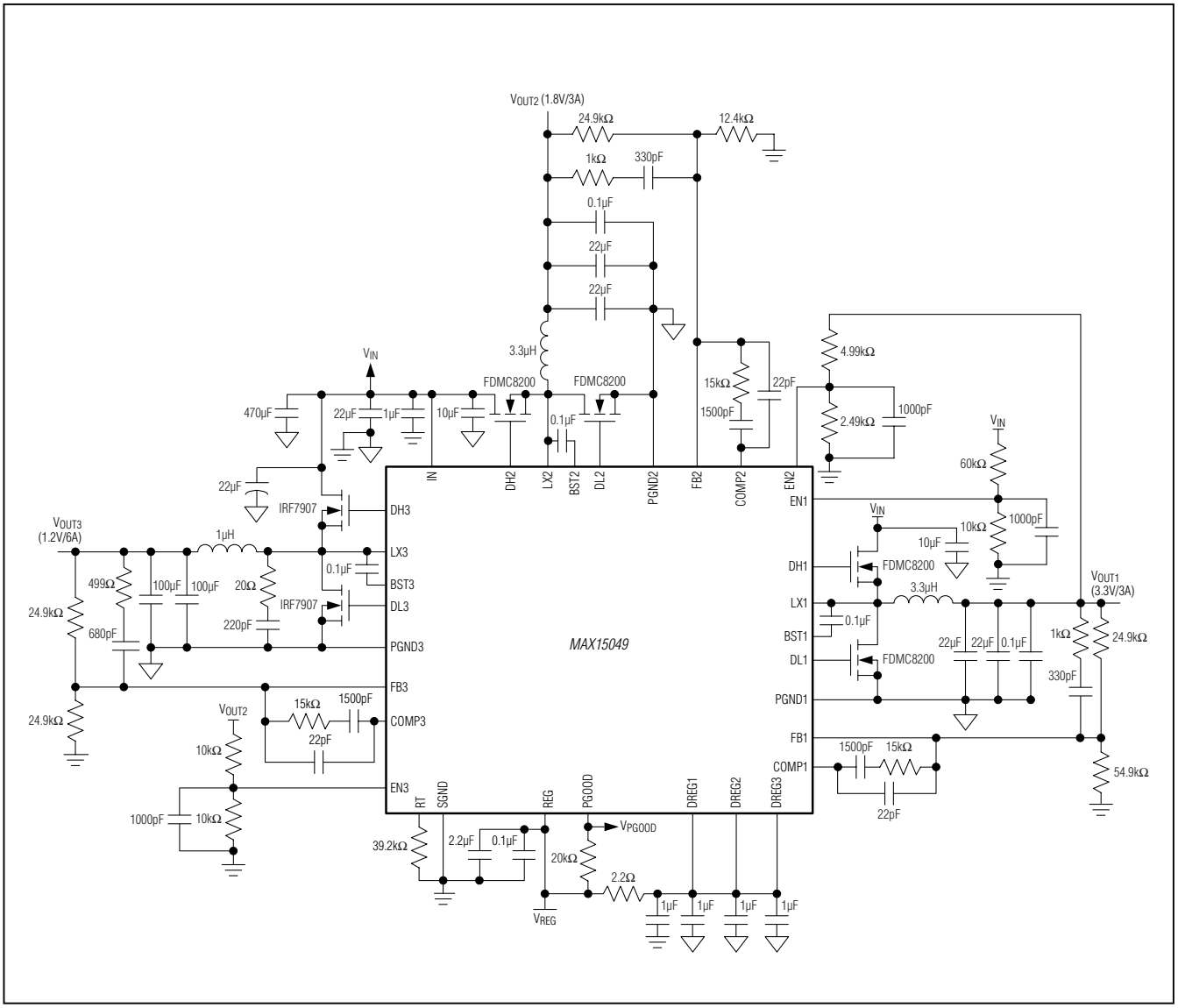


Figure 10. Evaluation Kit Schematic Configured for the MAX15049 (Sequencer)

PWM Controller Applications Information

Power Dissipation

The 32-pin TQFN thermally enhanced package can dissipate up to 2758.6mW. Calculate power dissipation in the MAX15048/MAX15049 as a product of the input voltage and the total REG output current (I_{REG}). I_{REG} includes quiescent current (I_Q) and the total gate-drive current (I_{DREG}):

$$P_D = V_{IN} \times I_{REG}$$

$$I_{REG} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2} + Q_{G3} + Q_{G4} + Q_{G5} + Q_{G6})]$$

where Q_{G1} to Q_{G6} comprise the total gate charge of the low-side and high-side external MOSFETs, f_{SW} is the switching frequency of the converter, and I_Q is the quiescent current of the device at the switching frequency.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A):

$$P_{DMAX} = 34.5 \times (150 - T_A)mW$$

PCB Layout Guidelines

Use the following guidelines to lay out the switching voltage regulator:

1) Place the IN, REG, and DREG_ bypass capacitors close to the MAX15048/MAX15049.
2) Minimize the area and length of the high-current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep the current loop formed by the lower switching MOSFET, inductor, and output capacitor short.
4) Keep SGND and PGND_ isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
5) Avoid long traces between the DREG_ bypass capacitor, low-side driver outputs of the MAX15048/MAX15049, MOSFET gate, and PGND_. Minimize the loop formed by the DREG_ bypass capacitor, bootstrap capacitor, high-side driver output of the MAX15048/MAX15049, and upper MOSFET gates.
6) Place the bank of the output capacitors close to the load.
7) Distribute the power components evenly across the board for proper heat dissipation.
8) Provide sufficient copper area at and around the switching MOSFETs and inductor to aid in thermal dissipation.
9) Connect the MAX15048/MAX15049 exposed pad to a large copper plane to maximize its power dissipation capability. Connect the exposed pad to SGND. Do not connect the exposed pad to the SGND pin directly underneath the IC.
10) Use 2oz copper to keep the trace inductance and resistance to a minimum. Thin copper PCBs can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255+4	21-0140

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