GS12281

12G UHD-SDI Re-timing Cable Driver

Key Features

- Dual non-inverted 75Ω cable interface with on-chip termination
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 11.88Gb/s
- In addition to standard SMPTE rates, the device also supports re-timing of DVB-ASI at 270Mb/s, and MADI at 125Mb/s.
- 3D Input Signal Eye Monitor
- PRBS generator and checker
- Cable driver mode features:
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Automatic/manual output slew rate control
  - Manual or automatic re-timer bypass
  - Manual or automatic Mute or disable on LOS
- Trace equalizer features:
  - Integrated 100Ω, differential input termination
  - Automatic power down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace equalization to compensate for up to 20" FR4 at 11.88Gb/s
  - Automatic input offset compensation
- CDR features:
  - Manual or automatic rate modes
  - Wide Loop bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, 2.97Gb/s, 5.94Gb/s, and 11.88Gb/s. This includes the f/1.001 rates.

Additional Features

- Single 1.8V power supply for analog and digital core
- 2.5V or 3.3V for cable driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- Small 6mm x 4mm 40-pin QFN
- Pin compatible with the GS12181, GS12182, GS12081, and GS3281
- Pb-free/Halogen-free/RoHS and WEEE compliant package

Applications

Next Generation 12G UHD-SDI infrastructures designed to support UHDTV1, UHDTV2, 4K D-Cinema and 3D HFR and HDR production image formats. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

Description

The GS12281 is a low-power, multi-rate, re-timing cable driver supporting rates up to 12G UHD-SDI. It is designed to receive 100Ω differential input signals, automatically recover the embedded clock from the digital video signal and re-time the incoming data, and transmit the re-timed signal over 75Ω coaxial cables. The 100Ω trace input supports up to 17dB of insertion loss.

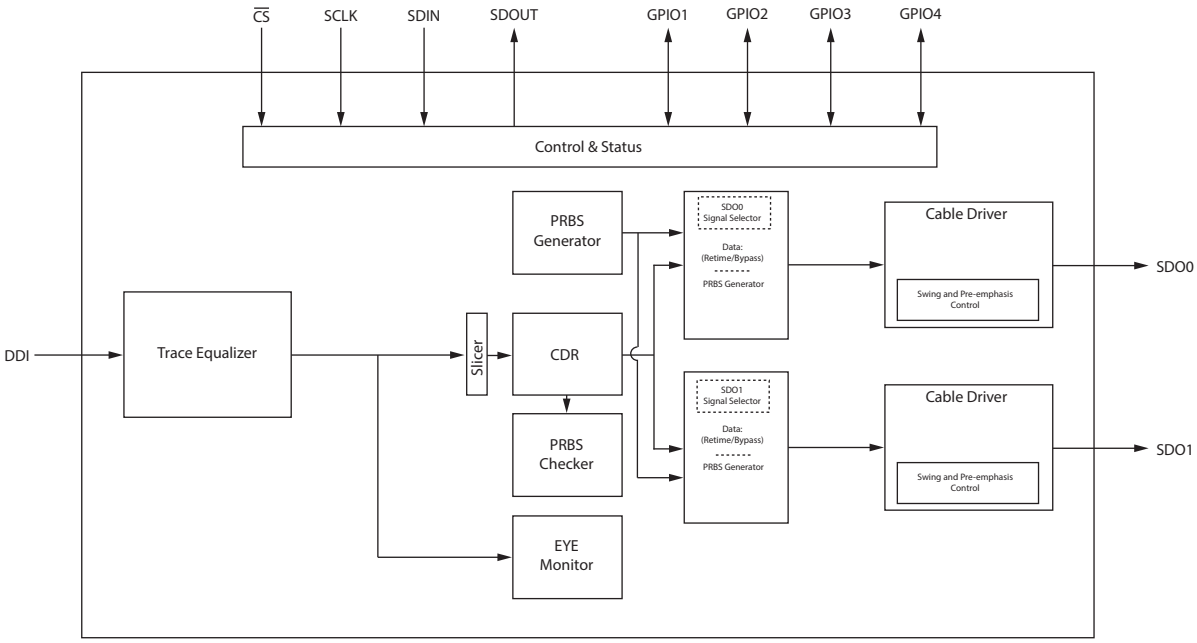
The integrated eye monitor provides non-disruptive mission mode analysis of the post equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed up prototyping and enable field analysis.

Built in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyze long term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors. The two cable drivers have highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses. Additionally, automatic and user selectable output slew rate control is provided for each cable driver output.

The GS12281 is pin compatible with the GS12181 single input, and the GS12182 dual input 12G UHD-SDI Multi-rate Re-timing Cable Drivers, the GS12081 12G UHD-SDI Multi-rate Cable Driver, as well as the GS3281 3G SDI Multi-rate Re-timing Cable Driver.

Note: For the GS12281 to be pin compatible with the GS12182, careful design considerations are required. Contact for your local Semtech FAE for details.



GS12281 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
4	037848	—	August 2017	Added Section 4.7.3, added pin compatibility to list of key features, updated Section 6.1, updated Table 2-2 and Table 2-3.
3	037303	—	June 2017	Updated Table 2-2, Section 4.5, Table 5-3, Figure 6-1, Section 4.9.13 and added Section 4.9.12.
2	036700	—	May 2017	Rewrite of Section 4.4, Section 4.5, Section 4.6, Section 4.7.4 Updated Table 2-2, Table 2-3, Table 5-3 and Table 5-4
1	034008	—	November 2016	Updated Table 1-1, Table 2-1, Figure 4-8, Table 4-12, Figure 6-1 as per Errata (PDS-061434)
0	033175	—	October 2016	New Document.

Contents

1. Pin Out

1.1 GS12281 Pin Assignment

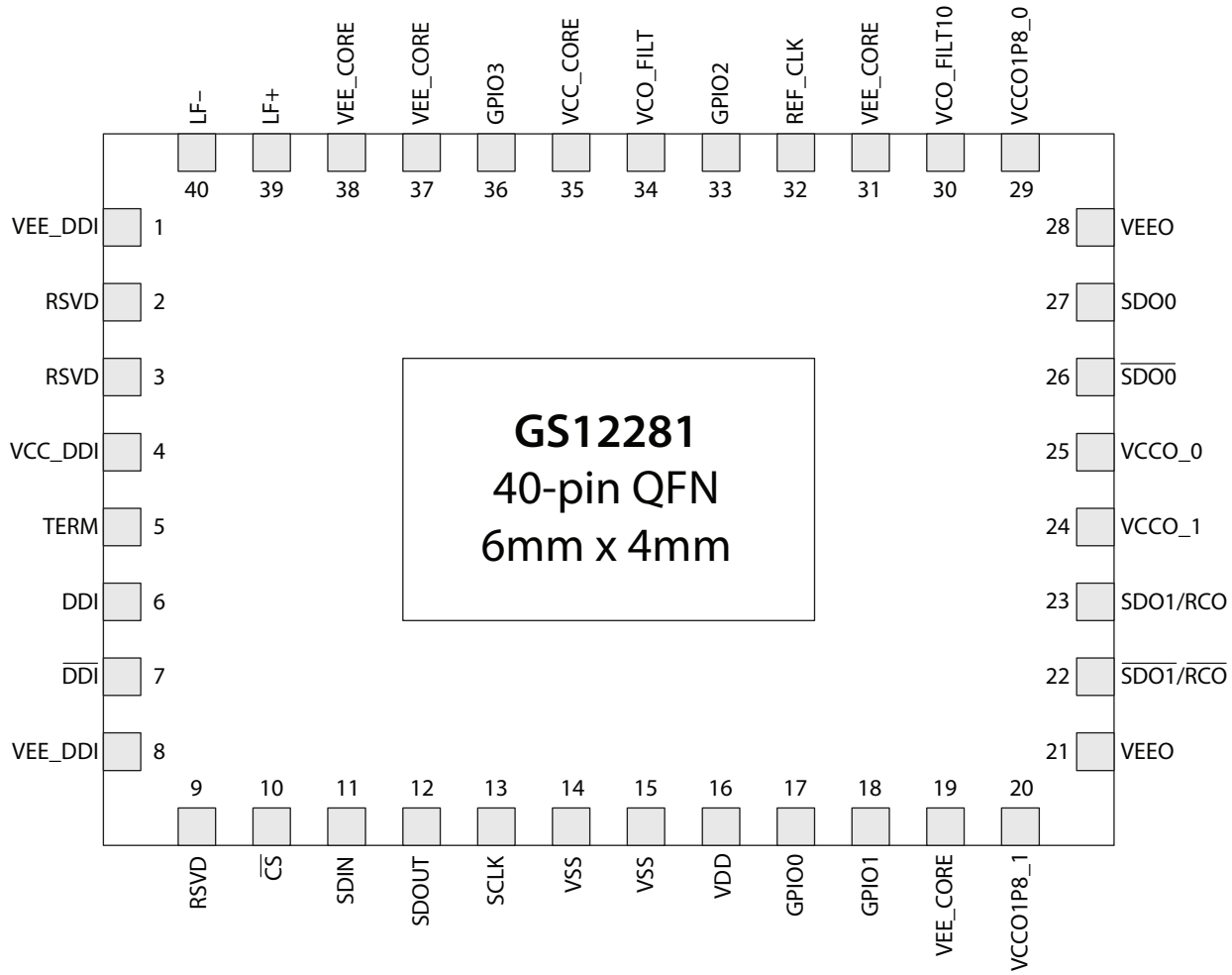


Figure 1-1: GS12281 Pin Assignment

1.2 GS12281 Pin Descriptions

Table 1-1: GS12281 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the Trace Equalizer. Connect to ground.
2, 3, 9	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS12241.
4	VCC_DDI	Power	Most positive power supply connection for the Trace Equalizer. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
5	TERM	—	Input Common Mode termination. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
10	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.9.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.9.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.9.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS12281 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = High indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22,23	$\overline{\text{SDO1}}$/$\overline{\text{RCO}}$, SDO1/RCO	Output	Differential CML output with two internal 75Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resister. See Section 6.1 Typical Application Circuit for values.
24	VCCO_1	Power	Most positive power supply connection for the SDO1/ $\overline{\text{SDO1}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
25	VCCO_0	Power	Most positive power supply connection for the SDO/$\overline{\text{SDO0}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
26, 27	$\overline{\text{SDO0}}$, SDO0	Output	Differential CML output with two internal 75Ω pull-ups. The data signal or PRBS generator can be selected for this output. The PRBS generator can be configured to generate a PRBS7 or a clock pattern. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
29	VCCO1P8_0	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
30	VCO_FILT10	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
32	REF_CLK	Digital Input	Optional 27MHz reference input. 1.8V CMOS input with 100kΩ pull-down. Connect to ground if not used.

Table 1-1: GS12281 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set high to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set high to disable SDO1/$\overline{\text{SDO1}}$ Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through capacitor. See Section 6.1 Typical Application Circuit for values.
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through capacitor. See Section 6.1 Typical Application Circuit for values.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not commended to connect device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage—Core (VCC_DDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage—Output Driver (VCCO_0, VCCO_1)	-0.5V to +3.65V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (DDI, $\overline{DDI}$)	-0.3 to (VCC_DDI +0.3)V
Input Voltage Range (GPIO2, GPIO3 REF_CLK)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_DDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		2.38	2.5	2.63	V	—
			3.14	3.3	3.47	V	—
Power - Mission Mode (SDO0/$\overline{SDO0}$ enabled SDO1/$\overline{SDO1}$ disabled)	P_D	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$,	—	375	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$ with max pre-emphasis	—	390	—	mW	—
Power - Mission Mode (SDO0/$\overline{SDO0}$ disabled SDO1/$\overline{SDO1}$ disabled)	P_D		—	280	—	mW	1
Power - Sleep Mode	P_D	Sleep	—	40	54	mW	—
Supply Current - Cable Driver	I_{CCO_0}, I_{CCO_1}	VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$	—	23	34	mA	1,4
		VCCO_0 = 2.5V, Output Swing = 800mV$_{pp}$, with max pre-emphasis	—	29	38	mA	4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$	—	24	33	mA	1,4
		VCCO_0 = 3.3V, Output Swing = 800mV$_{pp}$, with max pre-emphasis	—	30	37	mA	4
	I_{CCO1P8_0}, I_{CCO1P8_1}	Output Swing = 800mV$_{pp}$	—	20	28	mA	4
Supply Current – Analog Core	I_{CC_CORE}	CDR Locked to Rate	—	120	146	mA	—
		CDR Unlocked During Rate Search	—	143	—	mA	—
		PRBS Generator Enabled	—	71	—	mA	5,6
		PRBS Checker Enabled	—	58	—	mA	5
		Eye Monitor Enabled	—	70	—	mA	5
Supply Current - Trace Equalizer	I_{CC_DDI}		—	21	32	mA	—
Supply Current - Digital Logic	I_{DD}		—	15	18	mA	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
DDI Input Common Mode Voltage	V_{CMIN}		0.94	—	2.525	V	2
SDO Output Common Mode Voltage	V_{CMOUT}		—	$V_{CMOUT} = V_{CCO} - \Delta V_{SDO}/2$	—		—
DDI Input Termination		Differential	—	100	—	Ω	—
SDO Output Termination		Between SDO and GND	—	75	—	Ω	3
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.
2. 0.94V is when trace EQ is DC coupled to upstream driver running from 1.2V supply, and 2.525V is when trace EQ is DC coupled to upstream driver running from 2.5V supply.
3. Applies to both SDO0 and SDO.
4. The specifications provided are per symbol, not a combined value.
5. Current listed is an increase to ICC_CORE when stated condition is true.
6. Selected clock source = VCO free running.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDI}	—	0.001	—	11.88	Gb/s	—
Serial Output Voltage Swing	V_{SDO}	—	720	800	880	mV_{pp}	3
Differential Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	—
Input Trace Equalization	—	12G	—	20	—	Inches	14dB, 8
		6G	—	30	—	Inches	12dB, 8
		3G	—	60	—	Inches	13dB, 8
		HD	—	60	—	Inches	6dB, 8
		SD	—	60	—	Inches	3dB, 8
		MADI	—	60	—	Inches	3dB, 8
Intrinsic Input Jitter Tolerance Square Wave Modulation	IIJT	12G	0.7	0.85	—	UI	—
		MADI/SD/HD/3G/6G	0.8	0.95	—	UI	—
PLL Lock Time – Asynchronous	t_{ALOCK}	Referenceless with MADI OUT (Cable Driver Mode)	—	—	16.7	ms	5
		Referenceless with MADI IN (Cable Driver Mode)	—	—	32	ms	5
PLL Lock Time – Synchronous	t_{SLOCK}	SD	—	—	10	µs	5
		HD/3G/6G/12G	—	—	5	µs	5
SDO/$\overline{SDO}$ Rise/Fall Time	$t_{riseSDO}$, $t_{fallSDO}$	SD	400	—	1000	ps	6
		HD/3G	—	—	70	ps	6
		6G/12G	—	—	40	ps	6
SDO/$\overline{SDO}$ Mismatch in Rise/Fall Time	—	SD	—	—	100	ps	6
		HD/3G	—	—	20	ps	6
		6G/12G	—	—	10	ps	6
SDO/$\overline{SDO}$ Eye Cross Shift	—	SD	—	—	5	%	6
		HD/3G	—	—	8	%	6
		6G/12G	—	—	9	%	6
SDO/$\overline{SDO}$ Overshoot	—	—	—	—	10	%	6
Output Return Loss	—	5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
		2.97GHz to 5.94GHz	—	—	-8	dB	1
		5.94GHz to 11.88GHz	—	—	-5	dB	1

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Output Jitter (SDO/$\overline{SDO}$)	$t_{OJ(125Mb/s)}$	BW = default, Pattern = PRBS	—	0.015	0.08	UI_{pp}	2, 6, 9
	$t_{OJ(270Mb/s)}$		—	0.03	0.08	UI_{pp}	2, 6, 9
	$t_{OJ(1.485Gb/s)}$		—	0.03	0.08	UI_{pp}	2, 6, 9
	$t_{OJ(2.97Gb/s)}$		—	0.04	0.08	UI_{pp}	2, 6, 9
	$t_{OJ(5.94Gb/s)}$		—	0.05	0.1	UI_{pp}	2, 6, 9
	$t_{OJ(11.88Gb/s)}$		—	0.08	0.16	UI_{pp}	2, 6, 9
	$t_{OJ(Bypass)}$		—	0.13	0.2	UI_{pp}	2, 6, 7

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	10	—	kHz	4
		Setting 0.125x	—	20	—	kHz	4
		Setting 0.25x	—	38	—	kHz	4
		Setting 0.5x (Default)	—	76	—	kHz	4
		Setting 1.0x	—	150	—	kHz	4
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	20	—	kHz	4
		Setting 0.125x	—	40	—	kHz	4
		Setting 0.25x	—	80	—	kHz	4
		Setting 0.5x	—	160	—	kHz	4
		Setting 1.0x (Default)	—	316	—	kHz	4
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	110	—	kHz	4
		Setting 0.125x	—	220	—	kHz	4
		Setting 0.25x	—	440	—	kHz	4
		Setting 0.5x (Default)	—	876	—	kHz	4
		Setting 1.0x	—	1750	—	kHz	4
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	220	—	kHz	4
		Setting 0.125x	—	440	—	kHz	4
		Setting 0.25x	—	880	—	kHz	4
		Setting 0.5x (Default)	—	1.76	—	MHz	4
		Setting 1.0x	—	3.5	—	MHz	4
	$BW_{LOOP(5.94Gb/s)}$	Setting 0.0625x	—	440	—	kHz	4
		Setting 0.125x	—	880	—	kHz	4
		Setting 0.25x	—	1.76	—	MHz	4
		Setting 0.5x (Default)	—	3.5	—	MHz	4
		Setting 1.0x	—	7	—	MHz	4
	$BW_{LOOP(11.88Gb/s)}$	Setting 0.0625x	—	880	—	kHz	4
		Setting 0.125x	—	1.76	—	MHz	4
		Setting 0.25x	—	3.5	—	MHz	4
		Setting 0.5x (Default)	—	7	—	MHz	4
		Setting 1.0x	—	14	—	MHz	4

Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default driver swing Setting.
4. Please see PLL_LOOP_ BANDWIDTH_ 0 for the full range of loop bandwidth settings.
5. Please see Section 4.3.3.1for the further definition on Synchronous and Asynchronous Lock Time.
6. This specification applies to SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$.
7. For 12G and minimum trace loss.
8. Trace insertion loss was measured with FR4 material using 7 mil stripline traces using a PRBS23 signal.
9. Measured under minimal trace loss conditions.

Note: For GSPI Timing see Table 4-10: GSPI Timing Parameters.

3. Input/Output Circuits

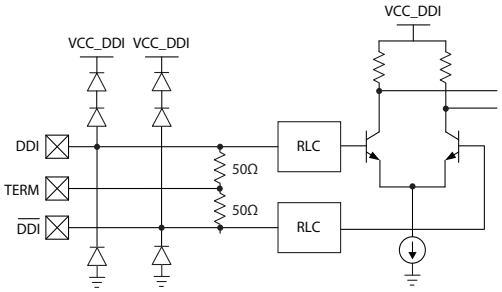


Figure 3-1: DDI, $\overline{DDI}$

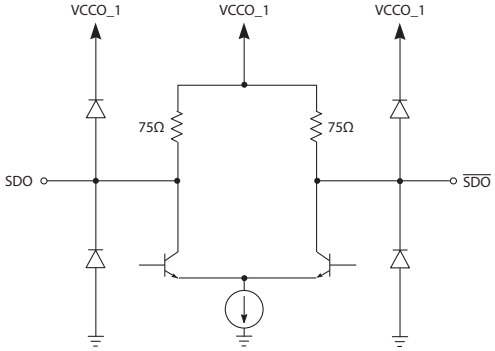


Figure 3-2: SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$

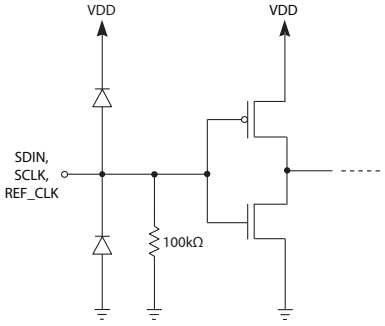


Figure 3-3: SDIN, SCLK, REF_CLK

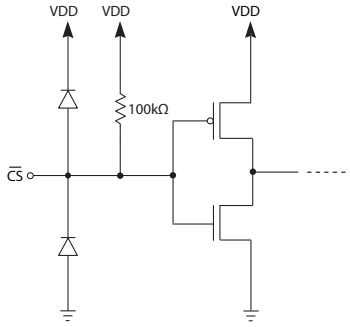


Figure 3-4: $\overline{CS}$

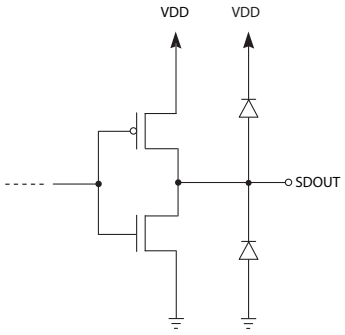


Figure 3-5: SDOUT

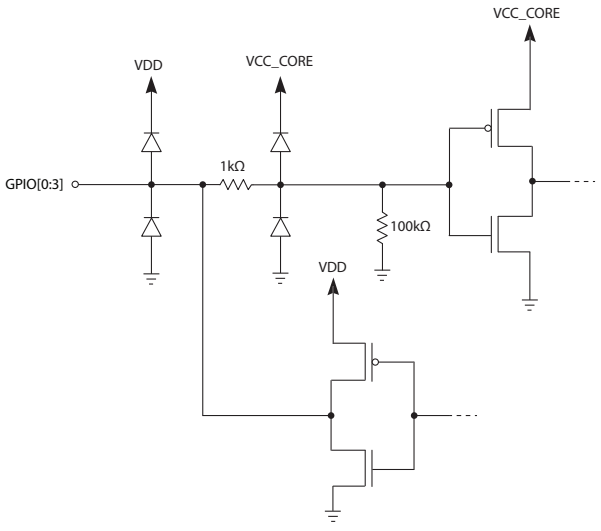


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS12281 is a dual output SMPTE compliant re-timing cable driver with integrated 75Ω internal terminations. It includes a 100Ω differential trace equalizer to receive the outgoing signal from the system. The Trace Equalizer has offset correction and boost control, which can compensate for 17dB of insertion loss at 5.94GHz. The device includes a CDR which will lock to and retime valid SMPTE signals to produce extremely low output jitter, even at extended trace lengths. The CDR has extensive LBW control to enable jitter transfer optimization. To facilitate system testing, the device also includes 3D eye monitor, PRBS7 checker and generator. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The pre-emphasis control is two dimensional, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.1.1 Sleep Mode

To enable low power operation, the GS12281 has manual and automatic sleep mode control.

The default mode is automatic sleep mode on LOS (Loss of signal). The device can also be manually put into sleep mode. When the device is in sleep mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The cable driver can be configured to be disabled or muted during sleep.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (auto sleep). While in auto sleep mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b manual sleep control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default GPIO pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.6 describes the PRBS generator function. If the device's PRBS generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.2.

4.2 Trace Equalizer

The GS12281 features a differential input buffer with 100Ω differential input termination, which includes a trace equalizer that can be configured to compensate for up to 20" of 7-mil stripline of FR4 at 11.88Gb/s and up to 60" at 3Gb/s.

The differential input signal can be either DC-coupled or AC-coupled and is capable of operation with any binary coded signal that between 1Mb/s and 11.88Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC coupled using industry standard 100Ω differential termination circuitry.

The trace equalizer includes an automatic input offset compensation circuit. This reduces offset-induced data jitter in the link created due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the trace equalizer.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.2.1 Input Trace Equalization

The trace equalizer can compensate for up to 17dB of insertion loss at 5.94GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (2_h). Please refer to Figure 4-1 for recommended boost setting.

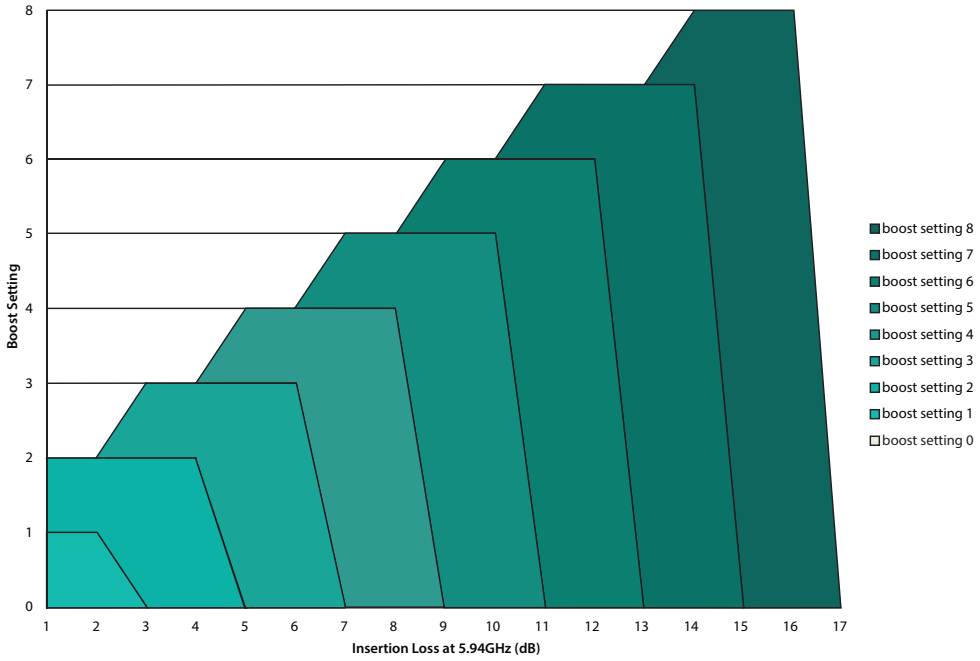


Figure 4-1: GS12281 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7-mil stripline in FR4 material at high frequencies.

Note: Although not a requirement, launch swing of 800mV$_{ppd}$ is recommended for trace lengths longer than 5".

4.2.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the trace equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the trace equalizer is highly configurable and allows the system designer to optimize the sensitivity and hysteresis of the Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting **CFG_TREQ0_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are is 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register (0x49). See Section 4.7.5 for more details.

Given a differential input trace with 17dB of insertion loss at 5.94GHz and **CFG_TREQ0_CD_BOOST** = 0_b, Figure 4-2 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 11.88Gb/s.

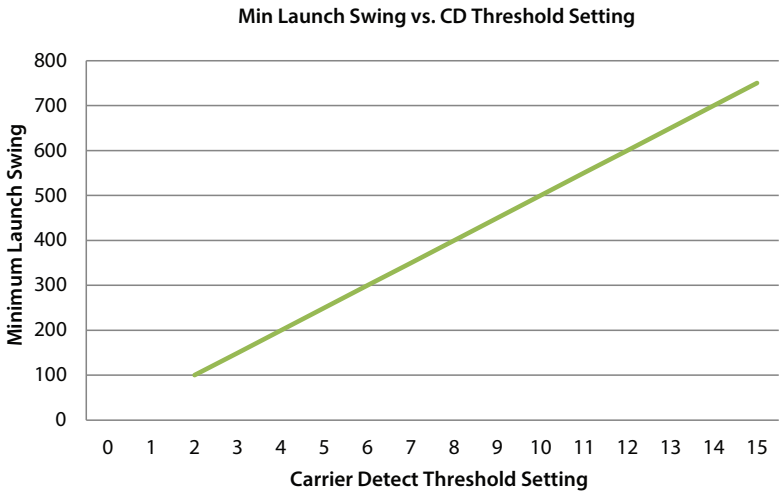


Figure 4-2: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-1: Trace Equalizer Configuration and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
1F, TREQ0_CD_ HYSTERESIS	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.
	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
1E, TREQ0_ INPUT_BOOST	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.
	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary carrier detection status.

4.3 Serial Digital Re-timer (CDR)

The GS12281 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the trace equalizer stage and produce a lower jitter signal at the cable driver outputs. The CDR will attempt to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates. The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection.

Note: The parameters referred to within Section 4.3.1 to Section 4.3.3.1 are linked to their respective registers in Table 4-3. For a complete list of registers and functions, please see Section 5.

4.3.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL LBW. Although the default LBW settings for the GS12281 CDR are ideal for most SDI signals, the GS12281 allows the user to adjust the LBW for each MADI and SMPTE compliant rate.

Registers 0x0A through 0x0C contain the following parameters which allow the user to configure rate dependent LBW: **CFG_PLL_LBW_12G**, **CFG_PLL_LBW_6G**, **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The LBW settings are defined in terms of ratios of the nominal LBW. For each rate, where '1.0x' is the nominal LBW, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and LBW setting. Lowering the LBW will lower the jitter amplitude above the LBW frequency. Although lower output jitter is desirable, the lower LBW may reduce the device's IJT to very high jitter that may be present outside the LBW.

4.3.2 Automatic and Manual Rate Detection

With the default rate detect setting, the CDR will automatically attempt to lock to any of following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates. However, the CDR can be configured to only lock to a single rate, by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x06. In addition to **CFG_MANUAL_RATE**, with automatic rate detection enabled (**CFG_AUTO_RATE_DETECT_ENA** = 1), specific rates can be excluded from the rate detect list through the **CFG_RATE_ENA_<r>** rate disable mask parameter in 0x06, where r is the rate to be disabled. For details on specific settings, please see the RATE_ DETECT_ MODE register.

The **STAT_LOCK** parameter in register 0x86 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on any *GPIO* pin, however it is the default mode for *GPIO1*, pin 18. The **STAT_DETECTED_RATE** parameter in register 0x87 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 6_d will indicate that the device is locked to one of the six available rates between MADI at 125Mb/s and UHD-SDI at 11.88Gb/s.

Table 4-2: Detected Data Rates

STAT_DETECTED_RATE [2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	6G (5.94Gb/s)
6	12G (11.88Gb/s)

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the signal can automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control enabled) signals are available at the appropriate output. See the Section 4.7 for more details.

4.3.3 Lock Time

4.3.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes. The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD-SDI signal. HD, 3G, 6G, or 12G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

Table 4-3: CDR Control and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
06, RATE_ DETECT_ MODE	CFG_AUTO_RATE_DETECT_ENA	Enables or disables the automatic rate detection mode of the CDR.
	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when CFG_AUTO_RATE_DETECT_ENA is 0_b.
	CFG_RATE_ENA_12G	12G auto rate detection enable
	CFG_RATE_ENA_3G	3G auto rate detection enable
	CFG_RATE_ENA_6G	6G auto rate detection enable
	CFG_RATE_ENA_HD	HD auto rate detection enable
	CFG_RATE_ENA_SD	SD auto rate detection enable
	CFG_RATE_ENA_MADI	MADI auto rate detection enable
08, REF_CLK_ MODE	CFG_REF_CLK_MODE_MANUAL	Enables or disables external reference clock mode.
0A, PLL_LOOP_ BANDWIDTH_ 0	CFG_PLL_LBW_12G	Configures the Loop Bandwidth for 12G signals.
	CFG_PLL_LBW_6G	Configures the Loop Bandwidth for 6G signals.
0B, PLL_LOOP_ BANDWIDTH_ 1	CFG_PLL_LBW_3G	Configures the Loop Bandwidth for 3G signals.
	CFG_PLL_LBW_HD	Configures the Loop Bandwidth for HD signals.
0C, PLL_LOOP_ BANDWIDTH_ 2	CFG_PLL_LBW_SD	Configures the Loop Bandwidth for SD signals.
	CFG_PLL_LBW_MADI	Configures the LBW for MADI signals.
11, GPIO1_CFG	CFG_GPIO1_FUNCTION	Sets the function of GPIO1.
	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
85, STICKY_ COUNTS_1	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
86, CURRENT_ STATUS_0	STAT_LOCK	The status of the PLL. Locked, or unlocked.
87, CURRENT_ STATUS_1	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.4 PRBS Checker

The GS12281 includes an integrated PRBS checker, which can error check a PRBS7 signal out of the trace equalizer input blocks.

There are two modes of operation for the PRBS checker:

- Timed Mode: Used for precise measurements of up to ~3.334s.
  - In timed mode, the host sets the measurement time and executes the checker operation. The device ends the PRBS error check measurement when the timer expires, and the host reads back the measurement status and error count.
- Continuous Mode: Can be used for longer measurements but with less precision in the time interval.
  - In continuous mode, the host controls the starts and stops of the PRBS error checking operation then reads back the measurement status and error count.

Note: When working with the PRBS Checker, please note the following.

- The parameters referred to in Section 4.4.1 to Section 4.4.2 are briefly described and linked to their respective registers in Table 4-4. For a complete list of registers and functions, please see Section 5.
- The PRBS generator and checker can be active at the same time, however, the generator can not be looped back on itself for error checking.

4.4.1 Timed PRBS Check Measurement Procedure

For applications where measurement times are ~3.34s or less, the timed PRBS check mode is the most suitable. Alternatively, to achieve precise timing for lower BER signals, the timed PRBS check measurement can be repeated by the host and the total measurement time and error count is determined by summing the individual measurements.

In timed mode, the host sets the total measurement time by setting the **CFG_PRBS_CHECK_PREDIVIDER** and the **CFG_PRBS_CHECK_MEAS_TIME** parameters to the required values to achieve the total measurement time required by the application.

To perform a timed PRBS measurement, please complete the following steps:

1. Set the appropriate settings within **CFG_PRBS_CHECK_PREDIVIDER** and **CFG_PRBS_CHECK_MEAS_TIME** to achieve the total measurement time required by the application. The TMT (total measurement time) is determined by the following equation:

   TMT = CFG_PRBS_CHECK_PREDIVIDER * (CFG_PRBS_CHECK_MEAS_TIME *256+1) * (1/40MHz)

   Note: Using the default **CFG_PRBS_CHECK_PREDIVIDER** setting of 0 (pre-divider = 4) and **CFG_PRBS_CHECK_MEAS_TIME** setting of 3 (MEAS_TIME = 3), the TMT (total measurement time) is ~77µs per measurement.
2. Follow the steps outlined in Figure 4-3: Timed PRBS Check Flow.

4.4.2 Continuous PRBS Check Measurement Procedure

As previously mentioned, the maximum measurement time for a timed PRBS error measurement is ~3.35 seconds. For links with very low error rates, this time is insufficient to capture an adequate number of errors. For these situations, the continuous PRBS check measurement is more appropriate.

In continuous PRBS measurement mode, the measurement can run as long as required (assuming the device remains locked) to ensure the BER test level is met.

To perform a continuous PRBS measurement, please follow the steps outlined in the flowchart found within Figure 4-4: Continuous PRBS Check Flow.

Table 4-4: PRBS Checker Parameter Description

Register Address$_h$ and Name	Parameter Name	Description
50, PRBS_ CHK_CFG	CFG_PRBS_CHECK_PREDIVIDER	Selects pre-divider for PRBS check measurement timer.
	CFG_PRBS_CHECK_MEAS_TIME	Selects PRBS check measurement interval for timed measurements.
51, PRBS_CHK_ CTRL	CTRL_PRBS_CHECK_TIMED_CONT_B	Selects between timed and continuous type PRBS measurement.
	TRL_PRBS_CHECK_START	Used to start and stop PRBS measurements.
89, PRBS_ CHK_ ERR_CNT	STAT_PRBS_CHK_ERR_CNT	PRBS error count storage location.
8A, PRBS_ CHK_STATUS	STAT_PRBS_CHECK_STATUS	Status indication of PRBS checker.
	STAT_PRBS_CHECK_LAST_ABORT	Indication bit for PRBS successful completion or abort.

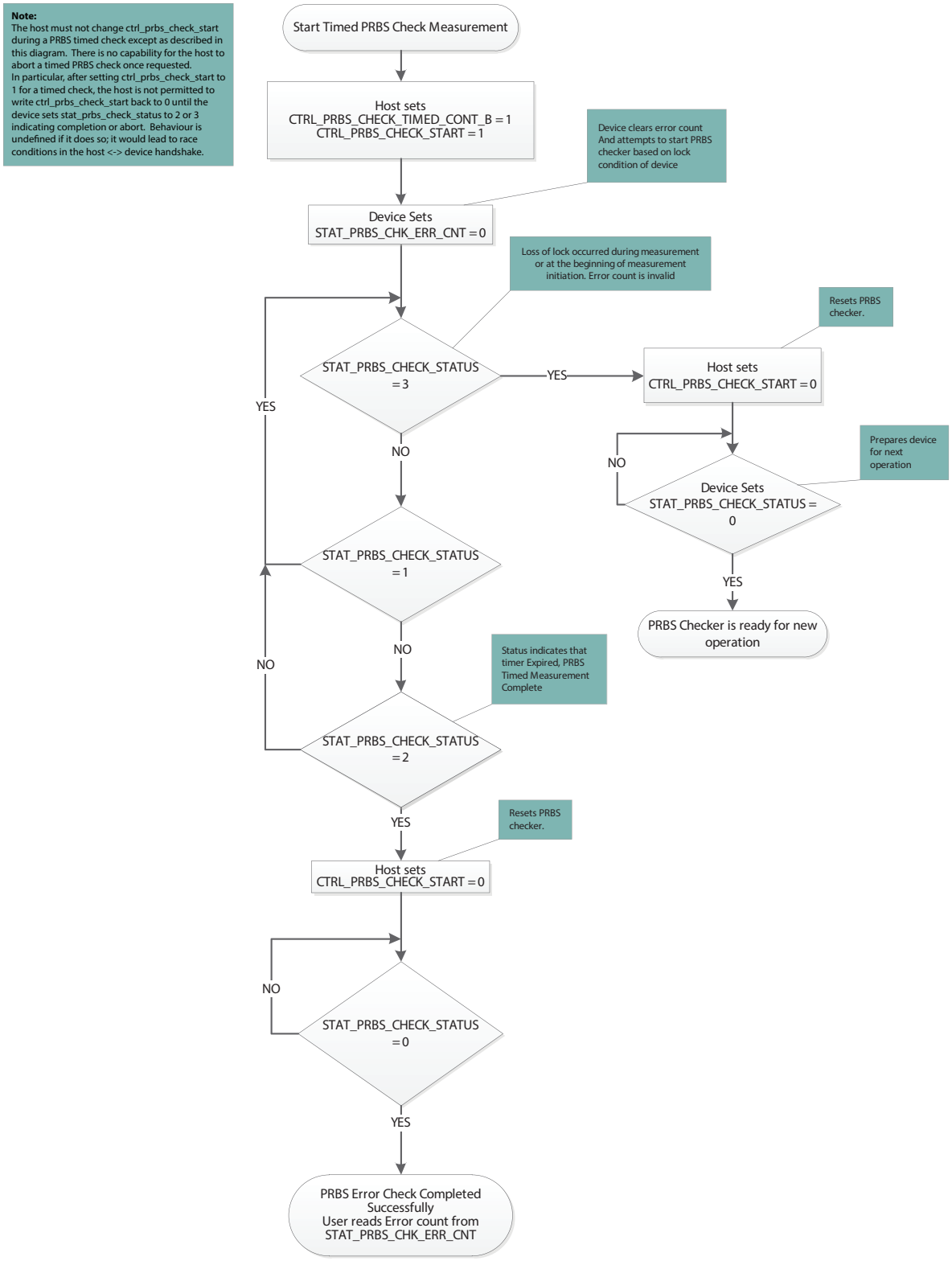


Figure 4-3: Timed PRBS Check Flow

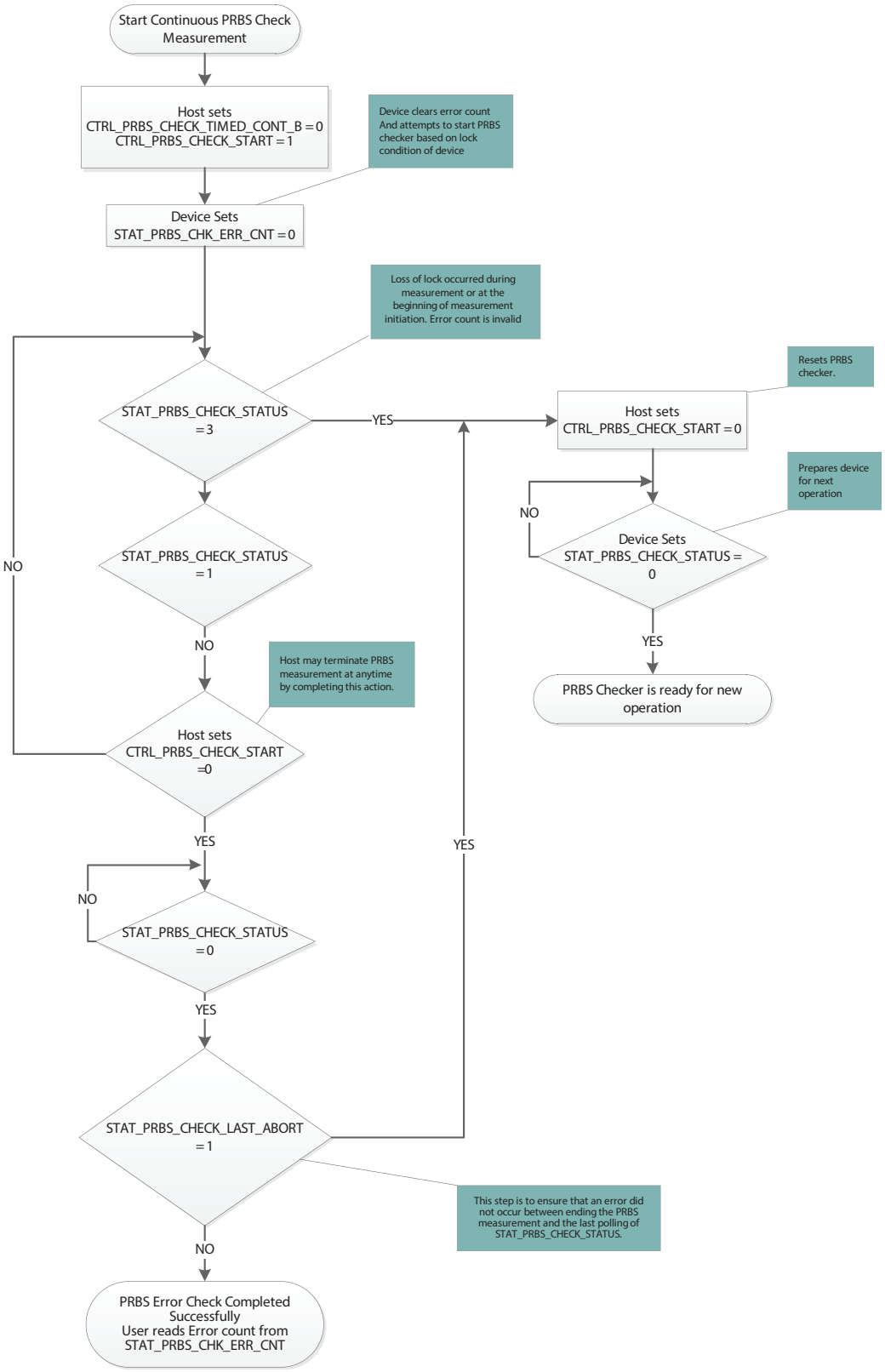


Figure 4-4: Continuous PRBS Check Flow

4.5 EYE Monitor

The GS12281 includes an integrated eye monitor, which can scan the equalized signal from the trace equalizer input block. The eye monitor is capable of performing a full 128h x 256v matrix-scan or simply a 4 coordinate shape-scan of the equalized signal (See Figure 4-5).

Note: If the eye monitor will be used during normal operation of the device (cable driver mission mode), the user must ensure that the Device Power-up Sequence in Section 4.9.12 is completed to prevent temporary signal disturbance when enabling the eye monitor.

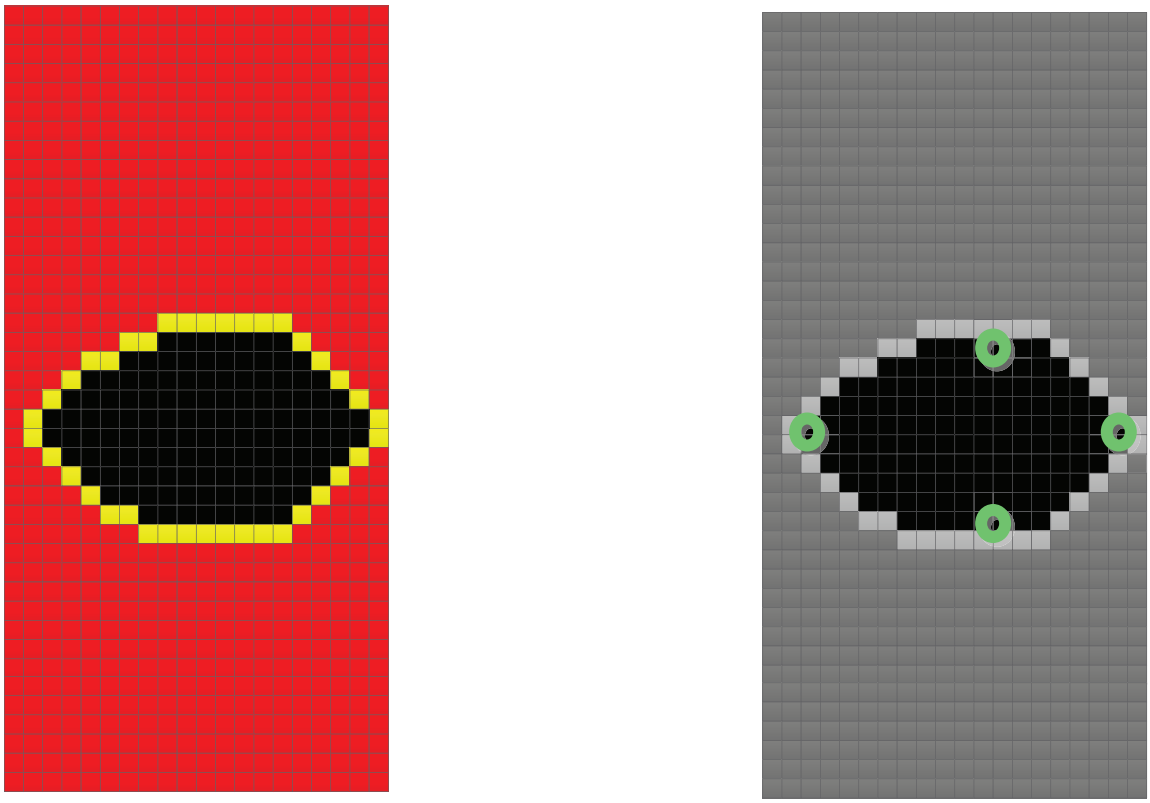


Figure 4-5: Full Matrix Scan (left) and 4-Point Shape Scan (right)

The eye monitor is highly configurable, and the host can configure the offset, resolution, sample time, and error threshold parameters to control the depth and execution time of the scan. The EYE monitor scans the signal from the trace equalizer block. Similar to the PRBS Checker, the eye monitor is controlled through a 4-way handshake mechanism. The following sections outline the scan parameters and procedure to configure the eye scan area, error threshold, and run a shape or full scan.

4.5.1 Shape Scan and Measurement Time

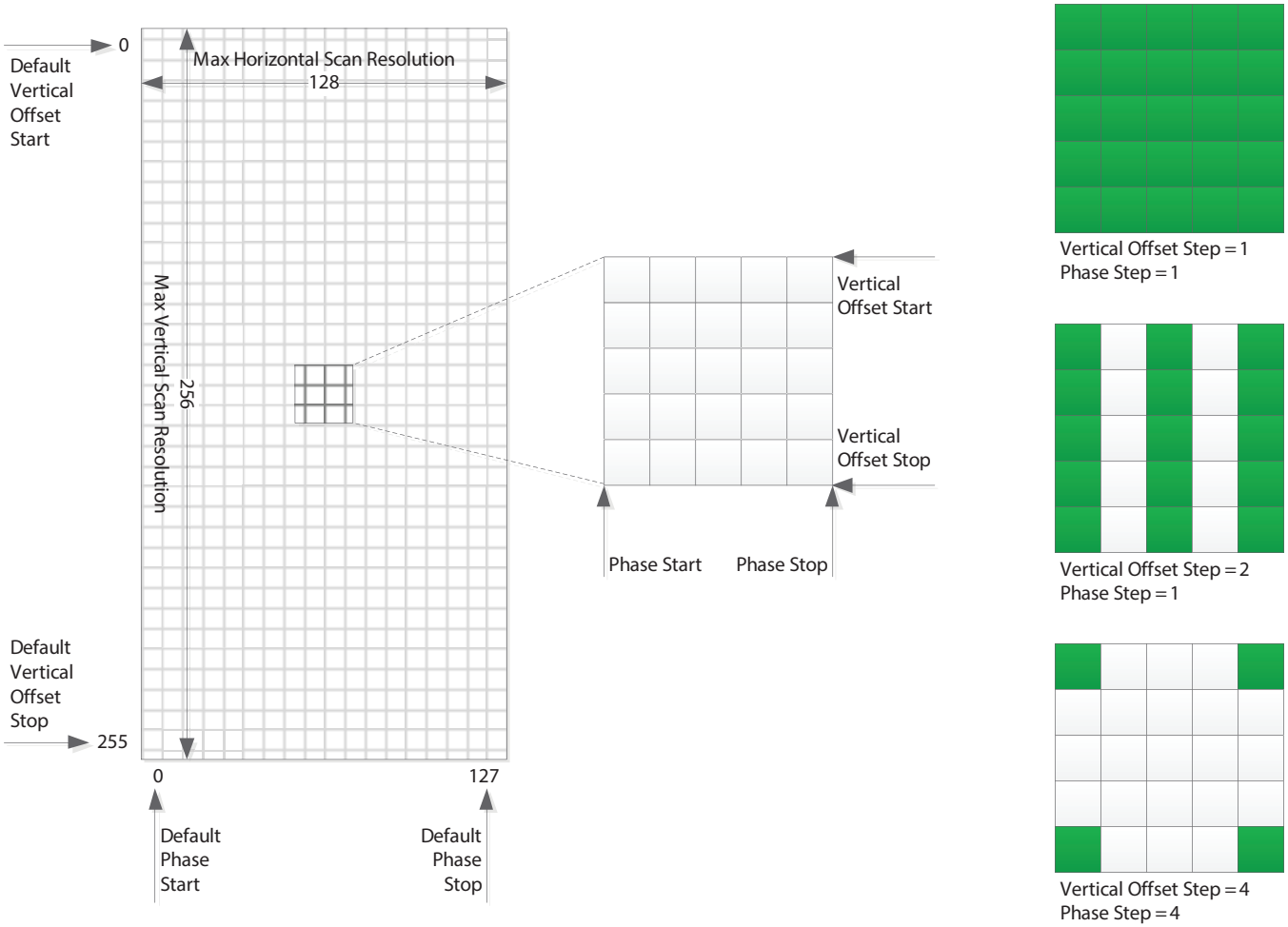


Figure 4-6: Eye Scan Matrix Parameters

Figure 4-6 shows a visual representation of the scan matrix and indicates the spatial parameters that determine the scan area and resolution. Running a scan using the default offset and step parameters, results in 32768 (128x255) samples. The number of samples and thus, the total scan time can be reduced to meet the needs of the application. The scan area can be reduced by reducing the span determined by the vertical and phase start and stop offsets, or the resolution can be reduced by increasing the step size between adjacent samples. On the right in Figure 4-6, there are three step settings used as examples, however there are a total of nine combinations possible. See Table 4-5 for the register addresses and parameter names of the spatial eye scan parameters.

For example, by increasing the vertical and phase step size to 4, the resolution is reduced to $(1/4)^2$, thus reducing the number of samples down to 2048 (32768x1/16).

The vertical and horizontal scan information is useful when adjusting pre-emphasis and equalization of a link. However, once this is accomplished, it may be sufficient to use the eye scanner to only monitor jitter by setting the offsets to simply slice the eye at the centre offset position, thus obtaining a simple 128 sample horizontal scan. A horizontal eye can be configured to run in just over a millisecond.

In addition to the spatial parameters, the sample time, and thus the bit error rate resolution for the eye scan can be adjusted; longer scans can detect finer bit error rates. However, this proportionally increases the total scan time. The sample time in microseconds is determined by a 32-bit time-out value split across two 16 bit registers. See Table 4-6 for the register addresses and parameter names of the time-out eye scan parameters.

For example, using the default spatial and temporal measurement scan parameters, the scan time is approximately 6.6 seconds (32768 x 2 x100µs). However, by changing the vertical and horizontal step size to 4, the scan time can be reduced to 400ms (2048x2x100µs).

The error count information can be used as is to determine the minimum inner contour based on the measurement time. However, the basic data can be post processed to determine things like error rate, and error threshold.

The following equations provide guidance for user post-processing:

Equation 4-1

$$\mathbf{error\ rate} = \frac{\mathbf{sample\ error\ count}}{\mathbf{sample\ time}}$$

Contour maps can be created by defining error rate thresholds, and grouping sampled points that fall between thresholds.

For example:

Equation 4-2

$$\frac{\mathbf{sample\ time}}{\mathbf{error\ rate\ threshold}\ 1} < \mathbf{sample\ error\ threshold} < \frac{\mathbf{sample\ time}}{\mathbf{error\ rate\ threshold}\ 2}$$

Some sampling scopes provide eye maps with BER contours; similar limited BER contour approximations can be obtained from the eye scan by using BER threshold groups.

For example:

Equation 4-3

$$\frac{\mathbf{sample\ time\ x\ data\ rate}}{\mathbf{error\ rate\ threshold}\ 1} < \mathbf{sample\ error\ threshold} < \frac{\mathbf{sample\ time\ x\ data\ rate}}{\mathbf{error\ rate\ threshold}\ 2}$$

Table 4-5: Spatial Scan Configuration Parameters

Register Address$_h$ and Name	Parameter Name	Description
5A, EYE_MON_ SCAN_CTRL_0	CTRL_EYE_PHASE_START	Horizontal phase start index
	CTRL_EYE_PHASE_STOP	Horizontal phase stop index
5B, EYE_MON_ SCAN_CTRL_1	CTRL_EYE_PHASE_STEP	Horizontal phase step size
	CTRL_EYE_VERT_OFFSET_START	Vertical offset start index
5C, EYE_MON_ SCAN_CTRL_2	CTRL_EYE_VERT_OFFSET_STOP	Vertical offset stop index
	CTRL_EYE_VERT_OFFSET_STEP	Vertical offset step size

The next section describes the implementation of the matrix-scan and shape-scan.

4.5.2 Matrix-Scan and Shape-Scan Operation

The previous section described the parameters used to adjust the spatial and temporal eye scan settings. Each sample of the eye scan can record up to 65536 errors. A full eye scan would require 64KB (256 x 128 x 2 Bytes) of memory to store the data of a full scan. The eye monitor was implemented to use device resources more efficiently by segmenting a full scan into several partial scan segments. Each partial scans segment can contain up to 512B of scan data.

In the case of a full matrix-scan, there are 128 partial scan segments and each partial scan segment contains two complete scan lines (2 x 128 x 2B = 512B). In the case of a partial matrix-scan, each scan segment contains multiple partial scan lines including partial lines (see Figure 4-7).

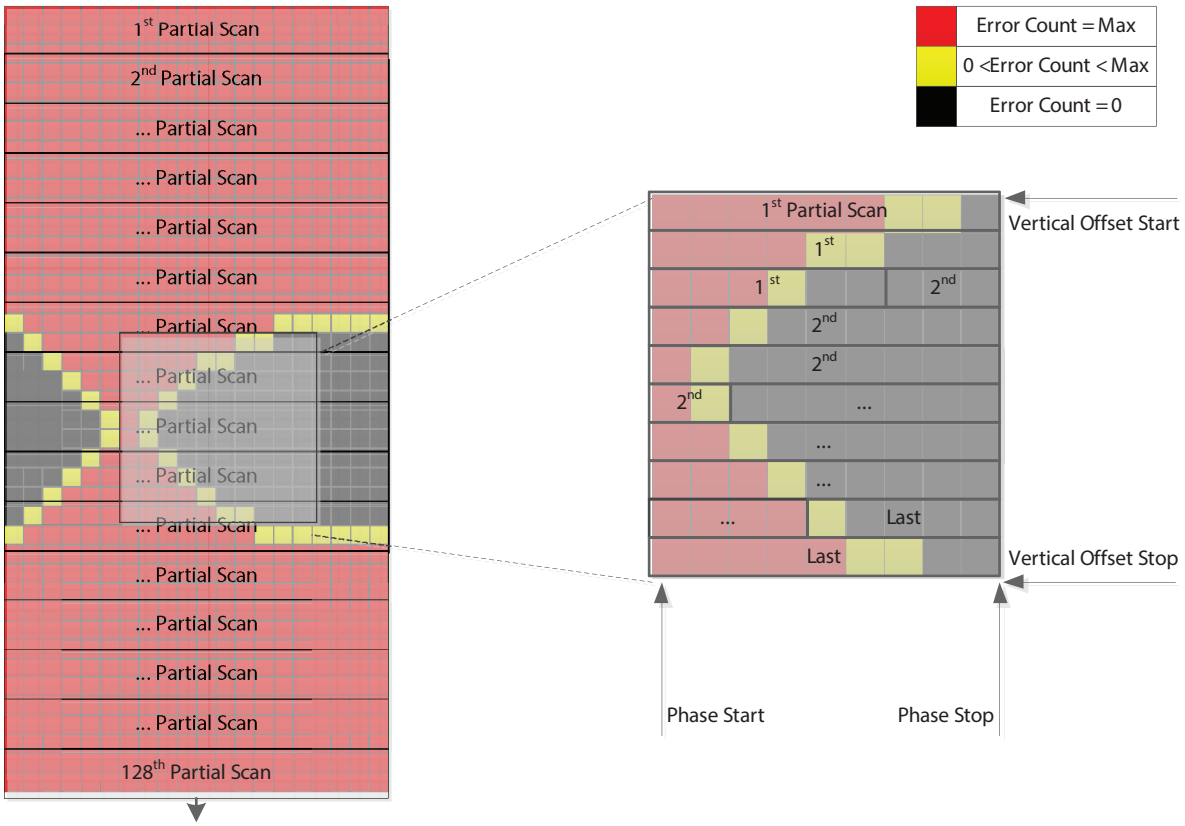


Figure 4-7: Full Matrix Scan (left) and Partial Matrix Scan (right)

Figure 4-7 illustrates an example of an eye scan, where the sampled eye data is not centred within the scan matrix. The eye scan data has an arbitrary centre phase relative to the centre of the matrix which is determined when the eye monitor is powered up. While the eye monitor remains powered, subsequent scans will maintain the same relative phase allowing for consecutive scans to be compared for changes.

Although the scan data is not centred, a simple algorithm can be applied to the data to shift the eye data and extract the relevant information.

In addition to the matrix-scan, the eye monitor includes a built-in function called a shape-scan. The shape-scan returns four coordinates corresponding to the horizontal and vertical extremes of the inner eye (See Figure 4-8).

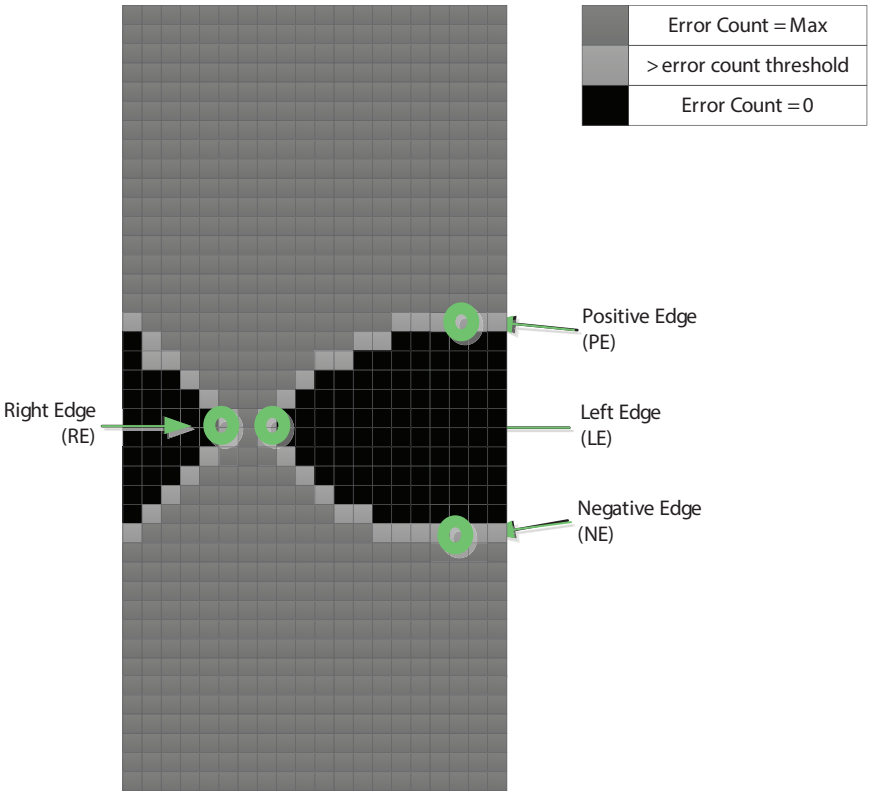


Figure 4-8: 4-Point Scan Coordinates Relative to the Eye

The four points obtained from the shape-scan can be used to quickly and easily calculate the eye height and width of the signal eye. The shape-scan alone will most likely meet the signal analysis requirements of most applications. Alternatively, the coordinates obtained from the shape-scan can be used to optimize the bounds of a partial matrix-scan. The four points returned from the shape-scan are determined by the error rate threshold set by the error threshold parameter and the time-out parameters previously discussed.

Table 4-6: Time-out Eye Scan Parameters

Register Address$_h$ and Name	Parameter Name	Description
56, EYE_MON_ INT_CFG_2	CFG_EYE_BER_THRESHOLD	Number of sample errors to determine fail
54, EYE_MON_ INT_CFG_0	CFG_EYE_MON_TIMEOUT_MS	MSB of measurement time in microseconds
55, EYE_MON_ INT_CFG_1	CFG_EYE_MON_TIMEOUT_LS	LSB of measurement time in microseconds

This section provides a step-by-step procedure to run a matrix and shape-scan. The shape-scan procedure is described first.

Shape-Scan Procedure:

1. Ensure the offset and step parameters described in Table 4-5 are set to their default values.
2. Configure the 4-point error rate threshold by setting each of the parameters listed in Table 4-6.
3. Configure the eye monitor to run a shape-scan by setting **CTRL_EYE_SHAPE_SCAN_B** to 1.

Start the scan and poll the scanner status register until the scan is complete. Please refer to the flow diagram in Figure 4-9.

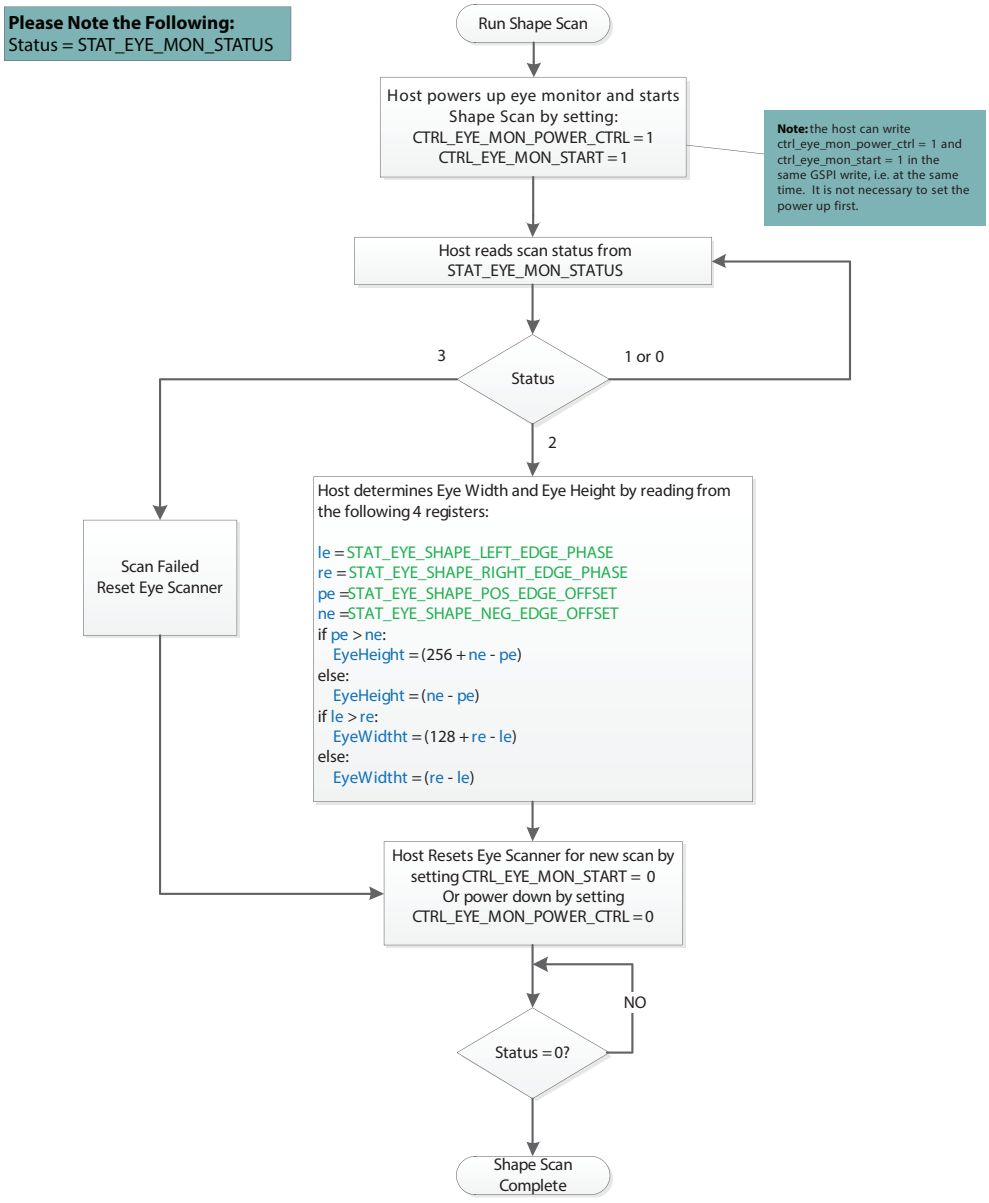


Figure 4-9: Shape-Scan Flow Diagram

Matrix-Scan Procedure:

1. Set the bounds of the matrix-scan with the offset and step parameters described in Table 4-5. The default value results in a full matrix-scan. Alternatively, the shape-scan can be executed and the coordinates returned can be used to minimize the scan time and data size of the scan.
2. Configure the 4-point error rate threshold by setting each of the parameters listed in Table 4-6.
3. Configure the eye monitor to run a matrix-scan by setting **CTRL_EYE_SHAPE_SCAN_B** to 0.
4. Start the scan and poll the scanner status register until the scan is complete. Please refer to the flow diagram in Figure 4-10.

Read Eye Scan Buffer Procedure:

1. Host reads image size from **STAT_EYE_IMAGE_SIZE**.
   Note: The matrix-scan is composed of multiple partial scan segments. The size (in Bytes) of the last partial scan segment is stored in **STAT_EYE_IMAGE_SIZE**.
2. Host reads scan buffer data from register 0x6CC1 to (0x6CC1 + (size read from **STAT_EYE_IMAGE_SIZE**)/2).
   - Address 0x6CC1 is the first header word corresponding to the last vertical offset position in the matrix that was read.
   - Address 0x6CC2 is the second header word corresponding to the image size. This value is a copy of the image size that was read from **STAT_EYE_IMAGE_SIZE**.
   - Address 0x6CC3 to (0x6CC1 + (size read from **STAT_EYE_IMAGE_SIZE**)/2) is the eye scan data.
     - The image data is 2 bytes per sample point.
     - Making reference to the Matrix shown in Figure 4-6, the eye scan data starting at 0x6CC3 is stored in order from left to right, top to bottom, from the last stored vertical/horizontal position in the matrix.

The number of samples contained in the scan buffer is equal to (size read from **STAT_EYE_IMAGE_SIZE** - 4)/2.

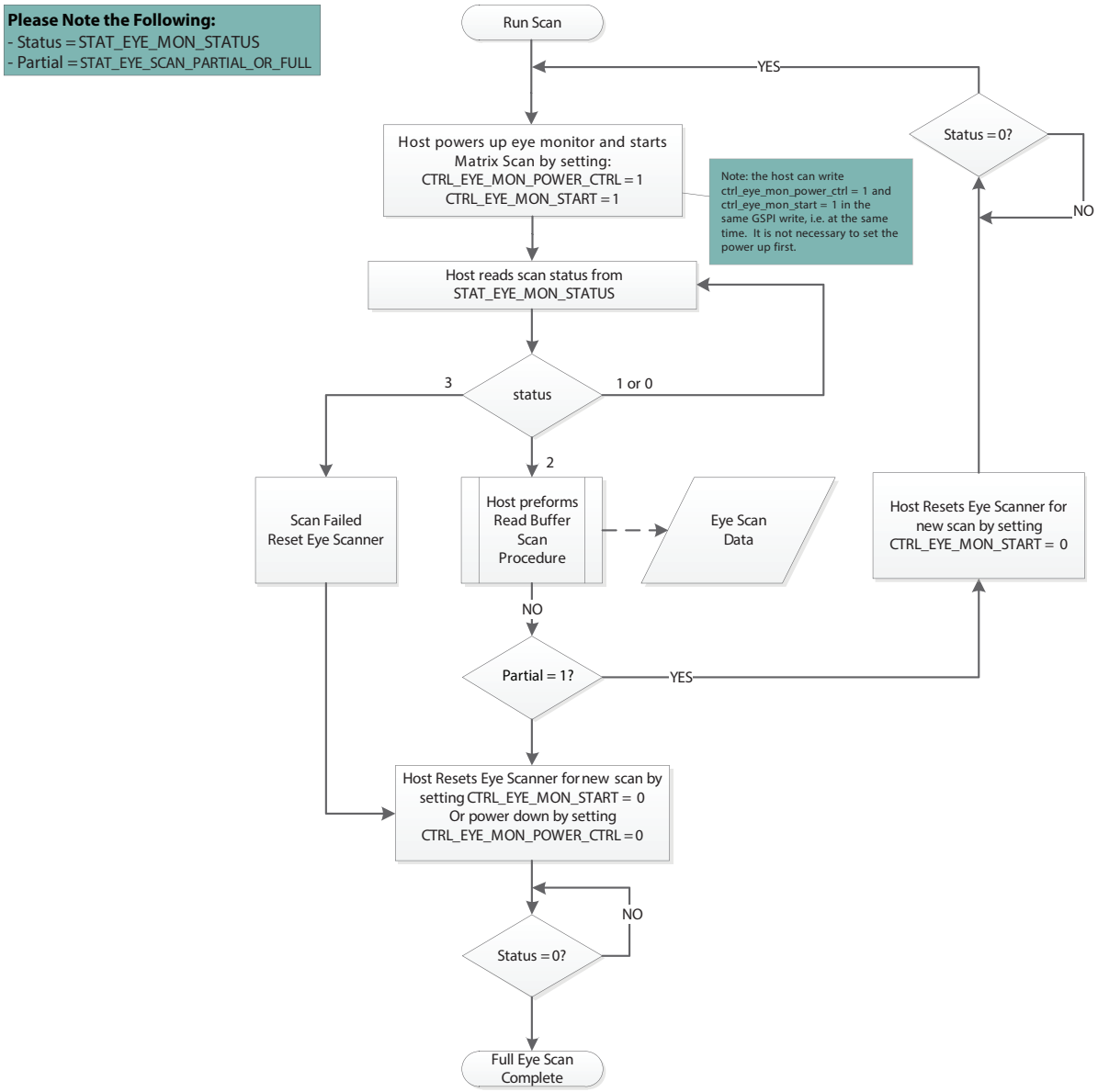


Figure 4-10: Matrix-Scan Flow Diagram

4.6 PRBS Generator

The GS12281 includes an integrated PRBS generator which can produce a differential PRBS7 or a divided clock signal on either output for system testing.

Note: When working with the PRBS Generator, please note the following.

- The PRBS generator and checker can be active at the same time, however, the generator can not be looped back on itself for error checking.
- If the application requires adjustments to the default output swing, please see Section 4.7.4.
- The parameters referred to within this section are linked to their respective registers in Table 4-7. For a complete list of registers and functions, please see Section 5.

To configure the PRBS generator for use, please see the following steps:

1. Select the PRBS generator as the source on the appropriate output:
   - To switch *SDO0/$\overline{SDO0}$* from data mode to PRBS generator mode, set **CTRL_OUTPUT0_SIGNAL_SEL** = 1
   - To switch *SDO1/$\overline{SDO1}$* from data mode to PRBS generator mode, set **CTRL_OUTPUT1_SIGNAL_SEL** = 1
2. The default device settings are configured to power-down the device on loss of input signal. If the PRBS generator is to be used without a valid input signal, then the following automatic setting parameters must be disabled. This must be done to ensure device is powered up and the outputs are active for the PRBS generator.

   The following settings are required for PRBS generator on either output:

   - **CTRL_AUTO_SLEEP** = 0
   - **CTRL_MANUAL_SLEEP** = 0

   The following settings are required when SDO1/$\overline{SDO1}$ is selected as PRBS output:

   - **CTRL_OUTPUT1_AUTO_MUTE** = 0
   - **CTRL_OUTPUT1_MANUAL_MUTE** = 0
   - **CTRL_OUTPUT1_AUTO_DISABLE** = 0
   - **CTRL_OUTPUT1_MANUAL_DISABLE** = 0
   - **CTRL_OUTPUT1_AUTO_SLEW** = 0

   The following settings are required when SDO0/$\overline{SDO0}$ is selected as PRBS output:

   - **CTRL_OUTPUT0_AUTO_MUTE** = 0
   - **CTRL_OUTPUT0_MANUAL_MUTE** = 0
   - **CTRL_OUTPUT0_AUTO_DISABLE** = 0
   - **CTRL_OUTPUT0_MANUAL_DISABLE** = 0
   - **CTRL_OUTPUT0_AUTO_SLEW** = 0

- Manually set the appropriate slew rate in **CTRL_OUTPUT<n>_MANUAL_SLEW** for the rate to be selected in **CTRL_PRBS_GEN_DATA_RATE**
  - 0 for SD and MADI
  - 1 for HD and 3G
  - 2 for 6G and 12G

  Note: The <n> in the control parameter names refers to the output number. Where output 0 is the cable driver output *SDO1/$\overline{SDO1}$* and output 1 is the cable driver output *SDO1/$\overline{SDO1}$*.

3. Set the values within the following parameters which meet the needs of the application:
   - **CTRL_PRBS_GEN_SIGNAL_SELECT**
   - **CTRL_PRBS_GEN_CLK_SRC**
   - **CTRL_PRBS_GEN_DATA_RATE**
     - **Note:** If **CTRL_PRBS_GEN_CLK_SRC** was set to CDR recovered clock a valid signal that the CDR has locked to must be present for proper operation, and the PRBS generator will match this data rate regardless of what rate **CTRL_PRBS_GEN_DATA_RATE** is set to.
   - **CTRL_PRBS_GEN_CLK_DIVIDER**
   - **CTRL_PRBS_GEN_INVERT**
4. Start the generator by setting **CTRL_PRBS_GEN_ENABLE** = 1.

To stop the generator at any time, set CTRL_PRBS_GEN_ENABLE = 0. If the use of the PRBS generator is complete, revert any settings made in steps 1 and 2 to return to normal operation.

Table 4-7: PRBS Generator Parameter Descriptions

Register Address$_h$ and Name	Parameter Name	Description
3, CONTROL_ SLEEP	CTRL_AUTO_SLEEP	Set the device to auto or manual sleep.
	CTRL_MANUAL_SLEEP	Manually set the sleep setting of the device when auto sleep mode is turned off.
48, OUTPUT_ SIG_SELECT	CTRL_OUTPUT1_SIGNAL_SEL	Selects between data or PRBS generator as the driver source for SDO1/$\overline{SDO1}$.
	CTRL_OUTPUT0_SIGNAL_SEL	Selects between data or PRBS generator as the driver source for SDO0/$\overline{SDO0}$.
49, CONTROL_ OUTPUT_ MUTE	CTRL_OUTPUT1_AUTO_MUTE	Select automatic or manual mute control for SDO1/$\overline{SDO1}$.
	CTRL_OUTPUT1_MANUAL_MUTE	Manually set the mute control for SDO1/$\overline{SDO1}$ when auto mute mode is turned off.
	CTRL_OUTPUT0_AUTO_MUTE	Select automatic or manual mute control for SDO0/$\overline{SDO0}$.
	CTRL_OUTPUT0_MANUAL_MUTE	Manually set the mute control of the SDO0/$\overline{SDO0}$ when auto mute mode is turned off.

Table 4-7: PRBS Generator Parameter Descriptions (Continued)

Register Address$_h$ and Name	Parameter Name	Description
4A, CONTROL_ OUTPUT_ DISABLE	CTRL_OUTPUT1_AUTO_DISABLE	Selects automatic or manual disable control for SDO1/$\overline{\text{SDO1}}$.
	CTRL_OUTPUT1_MANUAL_DISABLE	Manually set the disable control of the SDO1/$\overline{\text{SDO1}}$ when auto disable mode is turned off.
	CTRL_OUTPUT0_AUTO_DISABLE	Selects automatic or manual disable control for SDO0/$\overline{\text{SDO0}}$.
	CTRL_OUTPUT0_MANUAL_DISABLE	Manually set the disable control of the SDO0/$\overline{\text{SDO0}}$ when auto disable mode is turned off.
4B, CONTROL_ OUTPUT_ SLEW	CTRL_OUTPUT0_AUTO_SLEW	Selects auto or manual slew rate selection for SDO0/$\overline{\text{SDO0}}$.
	CTRL_OUTPUT0_MANUAL_SLEW	Manually set the slew rate for SDO0/$\overline{\text{SDO0}}$ when auto slew mode is turned off.
	CTRL_OUTPUT1_AUTO_SLEW	Selects auto or manual slew rate selection for SDO1/$\overline{\text{SDO1}}$.
	CTRL_OUTPUT1_MANUAL_SLEW	Manually set the slew rate for SDO1/$\overline{\text{SDO1}}$ when auto slew mode is turned off.
52, PRBS_GEN_ CTRL	CTRL_PRBS_GEN_SIGNAL_SELECT	Selects between setting the output of the PRBS generator to being a clock or a PRBS test signal.
	CTRL_PRBS_GEN_CLK_SRC	Selects the clock source used by the PRBS generator.
	CTRL_PRBS_GEN_CLK_DIVIDER	If a clock is selected as the PRBS output signal, this parameter sets the divide ratio of the clock.
	CTRL_PRBS_GEN_INVERT	Allows the polarity of the PRBS signal to be inverted.
	CTRL_PRBS_GEN_DATA_RATE	If a PRBS test signal is selected as the output signal, this parameter sets the data rate of the PRBS7 signal.
	CTRL_PRBS_GEN_ENABLE	Used to enable or disable the PRBS generator.

4.7 Output Drivers

The GS12281 features two independently configurable output drivers (see Figure 3-3), with data (re-timed or bypassed) available on both outputs. The two drivers provide highly configurable amplitude and pre-emphasis control. The signal on the outputs can be inverted to help with signal polarity when layout requires trace inversion. The PRBS generator is available on both outputs. The LOS (Loss of Signal) status from the equalizer stage can be used to automatically mute or disable the outputs on their assertion. The Loss of Lock status from the CDR block can be used to mute the outputs. The cable drivers can be configured to mute or disable during sleep. The sleep control modes takes precedence over the manual or automatic LOS and Loss of Lock output control modes.

Note: The <n> in the control parameter names refers to the output number. Output 0 is the cable driver output SDO0/$\overline{\text{SDO0}}$ and output 1 is the cable driver output SDO1/$\overline{\text{SDO1}}$.

4.7.1 Bypassed Re-timer Signal Output Control

With the default power-up settings, the GS12281 outputs will automatically switch to the bypassed signal (non-re-timed) whenever the PLL is unlocked. Alternatively, manual re-timer bypass may be configured by setting the **CTRL_OUTPUT<n>_RETIMER_AUTO_BYPASS** and **CTRL_OUTPUT<n>_RETIMER_MANUAL_BYPASS** parameters in register 0x4C to 0_b and 1_b respectively via the host interface, in which case the PLL will remain bypassed for all rates.

The re-timer bypass function, manual or automatic, does not affect the input equalization function of the device.

If both outputs are manually disabled, then the device will power down the CDR block and features of the re-timer such as rate detect and lock detect will no longer be accessible in this mode.

4.7.2 Output Driver Polarity Inversion

While in data mode, the signal polarity may be inverted at the outputs through the **CTRL_OUTPUT<n>_ DATA_ INVERT** parameters in register 0x48. This may be useful to compensate for an inverted upstream signal or to facilitate board signal routing. To invert the polarity of either of the two output drivers, write 1_b to control parameter **CTRL_OUTPUT<n>_DATA_ INVERT**.

4.7.3 Output Driver Data Rate Selection

By default, the GS12281 uses the output driver and slew rate group settings for the data rate to which the CDR is locked.

When the CDR is unlocked it will use the 6G/12G rate group:

- **CFG_OUTPUT<n>_CD_UHD_DRIVER_SWING**
- **CFG_OUTPUT<n>_CD_UHD_PREEMPH_WIDTH**
- **CFG_OUTPUT<n>_CD_UHD_PREEMPH_AMPL**
- **CFG_OUTPUT<n>_CD_UHD_PREEMPH_PWRDWN**

If required, manual selection of the output driver and slew rate group is possible using the following steps:

1. Set **CTRL_OUTPUT<n>_AUTO_SLEW** = 0
2. Set **CTRL_OUTPUT<n>_MANUAL_SLEW** to the desired rate group. The slew rate options are as follows:

   0 = SD/MADI
   1 = HD/3G
   2 = 6G/12G

4.7.4 Amplitude and Pre-Emphasis Control

The two output drivers offer very granular amplitude and pre-emphasis control. For optimal loss compensation, both the pre-emphasis pulse amplitude and the pre-emphasis pulse width can be independently configured on both output drivers. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of interconnect composed of trace, connector and via losses. The swing and pre-emphasis can be independently configured for specific data rates.

Note: The parameters referred to within this section are linked to their respective registers in Table 4-8. For a complete list of registers and functions, please see Section 5.

The output swing can be configured for the following three rate groups:

CFG_OUTPUT<n>_CD_SD_DRIVER_SWING (MADI and SD)
CFG_OUTPUT<n>_CD_HD_DRIVER_SWING (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_DRIVER_SWING (6G and 12G)

The output pre-emphasis can be configured for the following two rate groups:

CFG_OUTPUT<n>_CD_HD_PREEMPH_WIDTH (HD and 3G)
CFG_OUTPUT<n>_CD_HD_PREEMPH_AMPL (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_WIDTH (6G and 12G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_AMPL (6G and 12G)

The output driver swing and pre-emphasis will use the rate specific swing configuration when the CDR is locked to that rate. The default swing setting is 800mVpp single ended into an external 75Ω load. The swing can be adjusted in ~20mV increments. Applications where maximum output swing and pre-emphasis range are desired, it is recommended that the output supplies *VCCO_0* and *VCCO_1* be connected to a 3.3V supply. For most applications with short trace between GS12281 and output BNC, 2.5V power supply can be used.

4.7.4.1 Pre-Emphasis Optimization

The goal of pre-emphasis is to open the eye at the downstream receiver as much as possible. This means minimizing ISI jitter while meeting sufficient inner eye amplitude to meet a receiver's input sensitivity. The cable driver has the additional requirement to meet the SMPTE output specification.

The GS12281 has a high level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. The default cable driver settings should meet SMPTE output specification for most applications with short (1 to 2 inch) trace between the GS12281 and the output BNC. However, the pre-emphasis values may be adjusted to produce a better-looking eye. It is difficult to provide guidance regarding dB, as a 12G eye diagram looks different depending on the video test equipment used. The designer must optimize for their targets.

Table 4-8: Output Swing and Pre-Emphasis Control Parameters

Register Name and Address$_h$	Parameter Name	Description
0x2B/0x29, OUTPUT_ PARAM_CD_ SD_3/ OUTPUT_ PARAM_CD_ SD_1	CFG_OUTPUT<n>_CD_ SD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For SD and MADI rates on SDO0. <n> = 1: For SD and MADI rates on SDO1.
0x2D/0x2F OUTPUT_ PARAM_ CD_HD_1/ OUTPUT_ PARAM_ CD_HD_3	CFG_OUTPUT<n>_CD_ HD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x2C/0x2E OUTPUT_ PARAM_ CD_HD_0/ OUTPUT_ PARAM_ CD_HD_2	CFG_OUTPUT<n>_CD_HD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x31/0x33 OUTPUT_ PARAM_ CD_UHD_1/ OUTPUT_ PARAM_ CD_UHD_3	CFG_OUTPUT<n>_CD_UHD_ DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
0x30/0x32 OUTPUT_ PARAM_ CD_UHD_0/ OUTPUT_ PARAM_ CD_UHD_2	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.

4.7.5 Output State Control Modes

The GS12281 provides several output state control modes to meet specific application requirements. The cable driver has the following three output modes: operational, muted, disabled, or balanced. During non-sleep, if the control modes are configured such that multiple output modes are enabled, the priorities of the control modes from highest to lowest are the following: balanced, disabled, and then muted.Section 4.7.5.1 through Section 4.7.5.3 describe how to configure the output control modes that are enabled during non-sleep. If the device enters sleep, either manually or automatically, the sleep output control modes take precedence over the non-sleep control modes. The default cable driver configuration is for it to be disabled during sleep; however the cable driver can be configured to mute during sleep by setting the **CFG_SLEEP_OUTPUT<n>_MUTE** parameter in register 0x5 to 1_b.

4.7.5.1 Output Mute Control Mode

Each of the outputs on the GS12281 have independent mute control modes, which can be configured through the host interface.

The following are the four output mute control modes:

1. The outputs automatically mute on LOS (default).
2. The outputs automatically mute on LOS and during rate search.
3. The outputs never mute.
4. The outputs are always muted.

The first mute control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_MUTE** control parameter in register 0x49 is set to 1_b). In this mode, the outputs will automatically mute on the assertion of LOS. In addition to mute on LOS, with auto mute control mode configured, setting the **CTRL_OUTPUT<n>_AUTO_MUTE_DURING_RATE_SEARCH** control parameter in register 0x49 to 1_b, will configure the outputs to also mute when the device loses lock and begins to rate search.

The outputs can be manually configured to never mute by setting both the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters in register 0x49 to 0_b. Alternatively, the outputs can be manually configured to always be muted by setting the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_ MANUAL_MUTE** control parameters to 0_b and 1_b respectively.

4.7.5.2 Output Disable Control Mode

Each of the outputs on the GS12281 also have independent disable control modes, which can be configured through the host interface.

The following are the three output disable control modes:

1. The outputs are never disabled (default).
2. The outputs are automatically disabled on LOS.
3. The outputs are always disabled.

The first disable control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_DISABLE** and **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameters in register 0x49 are both set to 0_b). In this mode, the outputs will never disable. By setting the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter in register 0x49 to 1_b, the outputs will automatically disable on the assertion of LOS.

The output can be manually disabled by leaving the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter set to 0_b and setting the **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameter to 1_b.

The disable control mode takes precedence over the output mute control mode.

4.7.5.3 Output Balanced Control Mode

The GS12281 has a feature designed to facilitate reliable Output Return Loss (ORL) measurement while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while ORL is being measured. BALANCE mode can be enabled through the host interface, by setting control parameter **CTRL_OUTPUT<n>_ BALANCED** in register 4D to 1_b. This control mode takes precedence over both the output mute and output disable control modes.

4.7.6 Output Waveform Specifications

The Duty Cycle Distortion (DCD) of the serial digital differential outputs is less than 12ps. DCD is defined as the difference in the width of an output logic "1" versus that of output logic "0" as measured at the 50% point of the output waveform.

The DCD of the serial digital single ended outputs is less than 30ps.

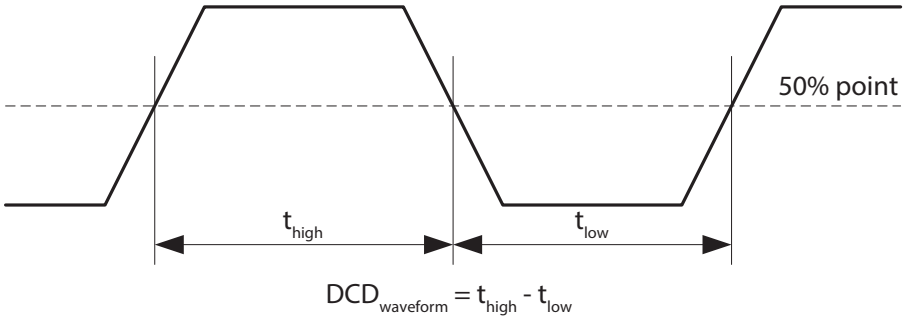


Figure 4-11: Traditional Waveform Definition of DCD

4.8 GPIO Controls

There are four configurable *GPIO* pins which can independently be configured as inputs or outputs. Each GPIO has a default function which can be re-configured through the host interface.

If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a *GPIO* pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. The logic HIGH and LOW levels of the *GPIO[3:0]* pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For a list of available functions and configuration details of *GPIO[3:0]*, please refer to the GPIO Configuration registers in Section 5.

4.9 GSPI Host Interface

The GS12281 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*SDIN* pin), serial data output signal (*SDOUT* pin), an active-LOW chip select ($\overline{CS}$ pin) and a burst clock (*SCLK* pin).

The GS12281 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.9.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-LOW signal provided by the host processor to the GS12281.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS12281.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS12281.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.9.2 SDIN Pin

The *SDIN* pin is the GSPI serial data input pin of the GS12281.

The 32-bit Command and 16-bit Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.9.3 SDOUT Pin

The *SDOUT* pin is the GSPI serial data output of the GS12281.

All data transfers out of the GS12281 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the *SDOUT* pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *SDOUT* pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.9.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the **GSPI_LINK_DISABLE** bit in **CONTROL_REG**. When disabled, any data appearing at the *SDIN* pin will not appear at the *SDOUT* pin and the *SDOUT* pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd\_GSPI\_config}$ (4 SCLK cycles).

Table 4-9: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

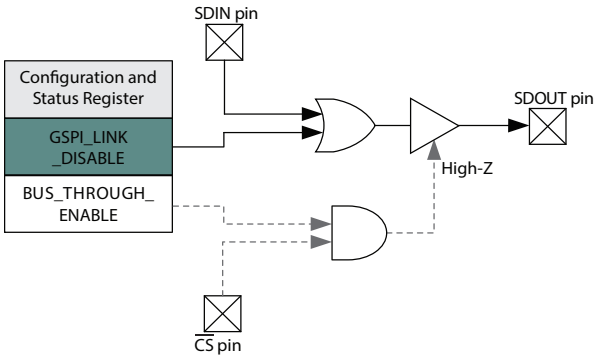


Figure 4-12: GSPI_LINK_DISABLE Operation

4.9.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS12281 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting **GSPI_BUS_THROUGH_ENABLE** bit to 1, the *SDOUT* pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the *SDOUT* pin will be driven and will follow regular read and write operation as described in Section 4.9.3.

Multiple chains of GS12281 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

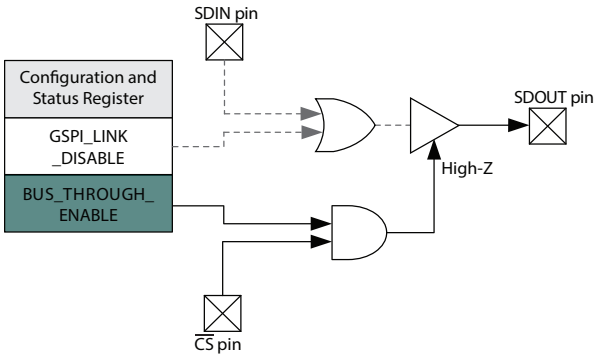


Figure 4-13: GSPI_BUS_THROUGH_ENABLE Operation

4.9.4 SCLK Pin

The *SCLK* pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS12281 *SDIN* pin on the rising edge of SCLK. Serial data is clocked out of the device from the *SDOUT* pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.9.5 Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select ($\overline{CS}$) pin of the GS12281.

The format of the Command Words and Data Word are shown in Figure 4-14.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.9.5.1 R/$\overline{W}$ bit—B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.9.5.2 B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (**AUTOINC** = 0) or Data Words (**AUTOINC** = 1) are written to the register specified by the ADDRESS field of the Command Words (and subsequent addresses when **AUTOINC** = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

4.9.5.3 EMEM—B13 Command Word 1

The EMEM bit must be set to 1 in Command Word 1. When EMEM is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

4.9.5.4 AUTOINC—B12 Command Word 1

When **AUTOINC** is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When **AUTOINC** is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in **CONTROL_REG**.

4.9.5.5 UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed **DEV_UNIT_ADDRESS** in **CONTROL_REG**.

By default at power-up or after a device reset, the **DEV_UNIT_ADDRESS** is set to 00_h.

4.9.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 4-14 and Figure 4-15 below.

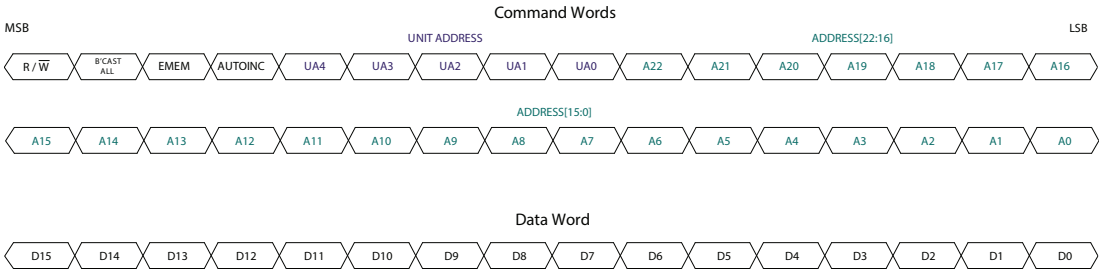


Figure 4-14: Command and Data Word Format

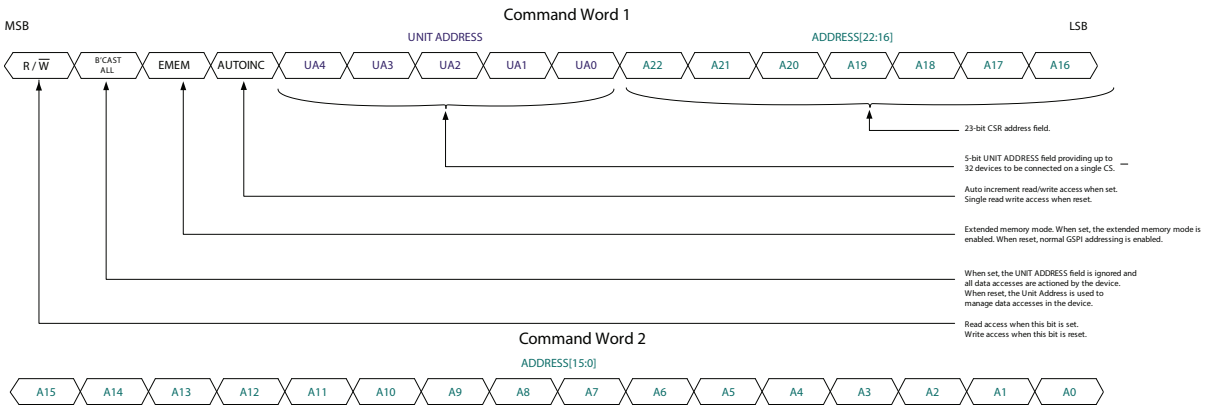


Figure 4-15: Command Word 1 and Command Word 2 Details

4.9.6 GSPI Transaction Timing

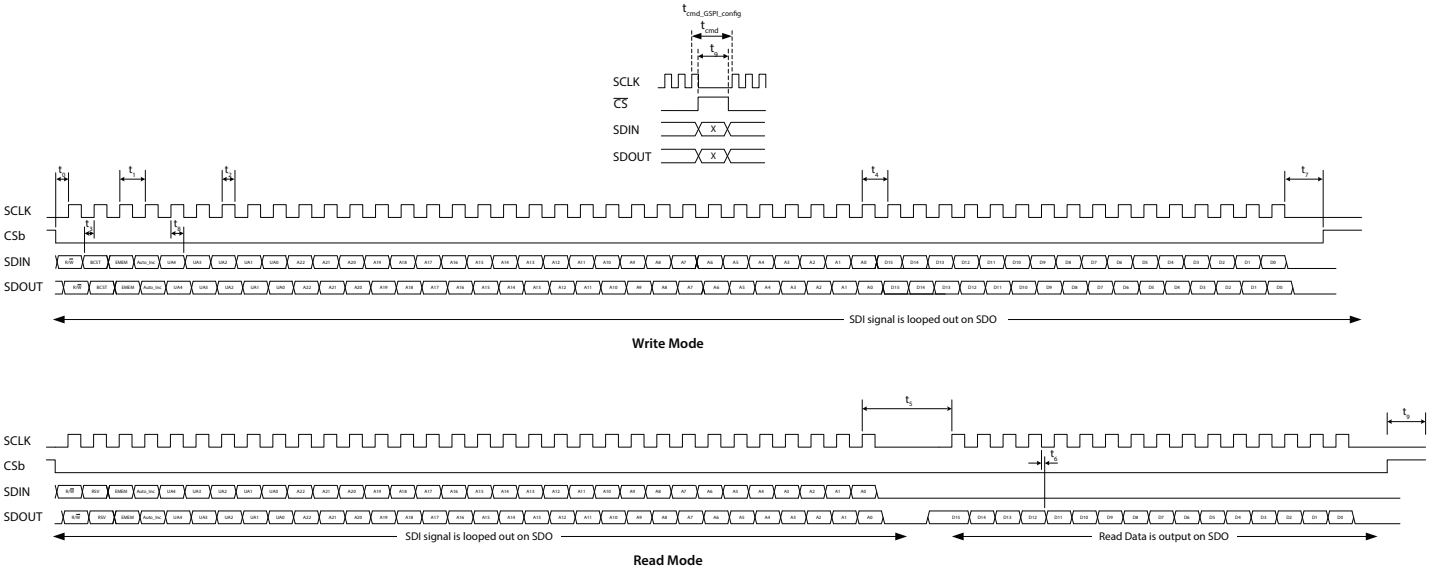


Figure 4-16: GSPI External Interface Timing

Table 4-10: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK Frequency	—	—	—	—	27	MHz
$\overline{CS}$ LOW Before SCLK Rising Edge	t_0	—	1.7	—	—	ns
SCLK Period	t_1	—	37	—	—	ns
SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2.3	—	—	ns
SCLK Idle Time – Write	t_4	1	1/SCLK	—	—	ns
SCLK Idle Time – Read	t_5	—	138	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	115	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd\_GSPI\_conf}$[1]	4	139	—	—	ns
SDOUT After SCLK Falling Edge	t_6	—	1.3	—	6.4	ns
CS HIGH After Final SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1.2	—	—	ns
$\overline{CS}$ HIGH Time	t_9	—	58	—	—	ns
SDIN to SDOUT Combinatorial Delay	—	—	—	—	3.4	ns
Max chips daisy-chained at max SCLK frequency (26 MHz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	8	# of compatible Semtech devices
Max frequency for 32 daisy-chained devices	When host clocks in SDOUT data on falling edge of SCLK		—	—	7.5	MHz

Note:

1. $t_{cmd\_GSPI\_conf}$ inter-command delay must be used whenever modifying **CONTROL_REG** register at address 0x00.

4.9.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-17 to Figure 4-21.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a HIGH-to-LOW transition of the $\overline{CS}$ pin. The read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in **CONTROL_REG**, the inter-command delay time, $t_{cmd\_GSPI\_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 27MHz.

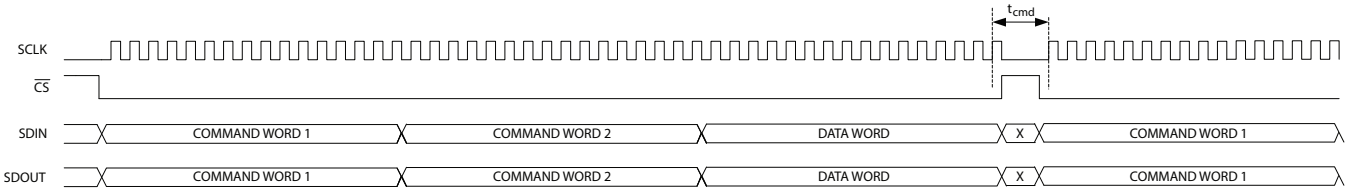


Figure 4-17: GSPI Write Timing—Single Write Access with Loop-Through Operation (default)

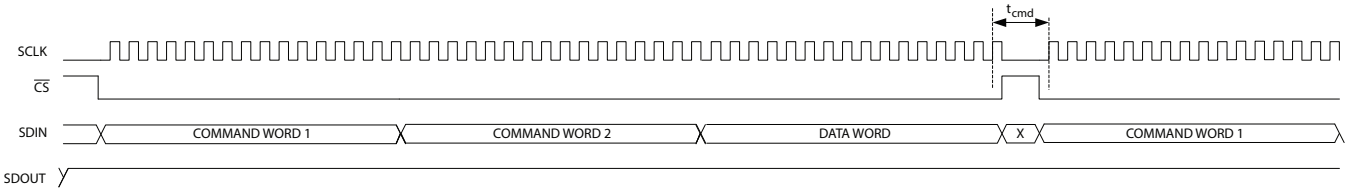


Figure 4-18: GSPI Write Timing—Single Write Access with GSPI Link-Disable Operation

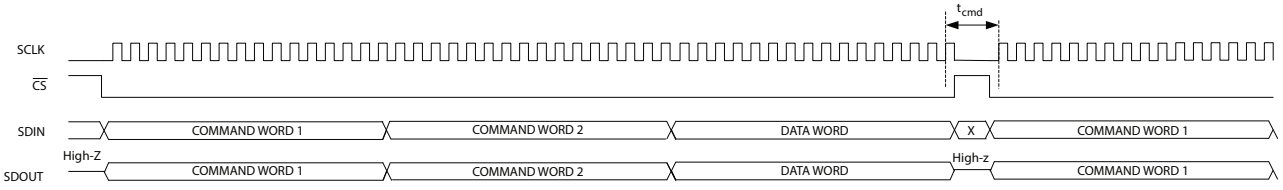


Figure 4-19: GSPI Write Timing—Single Write Access with Bus-Through Operation

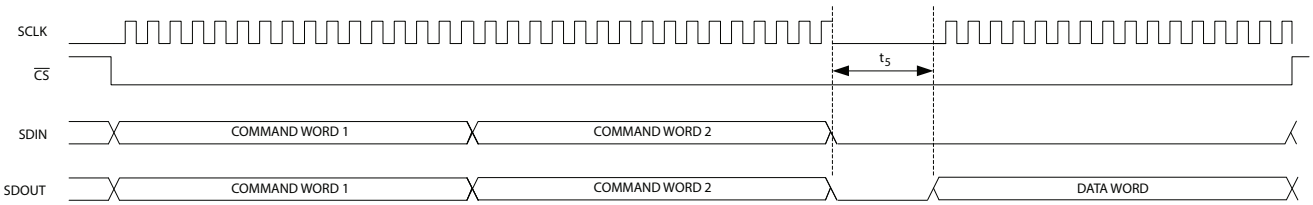


Figure 4-20: GSPI Read Timing—Single Read Access with Loop-Through Operation (default)

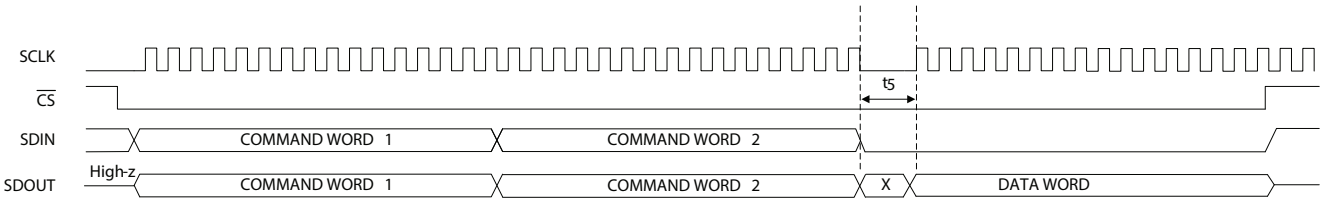


Figure 4-21: GSPI Read Timing—Single Read Access with Bus-Through Operation

4.9.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-22 to Figure 4-26.

Auto-increment mode is enabled by the setting the **AUTOINC** bit of Command Word 1.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of two Command Words and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

Note: Writing to **CONTROL_REG** using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the second Command Word to the start of the data output of the first Data Word as defined by t_5 will be no less than 4 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

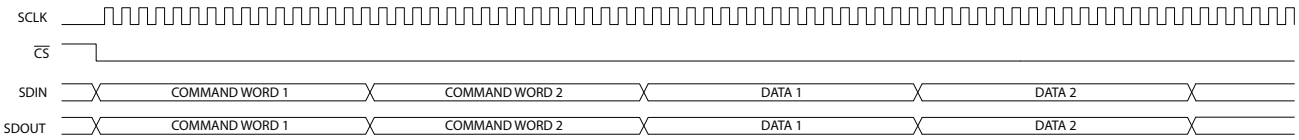


Figure 4-22: GSPI Write Timing—Auto-Increment with Loop-Through Operation (default)

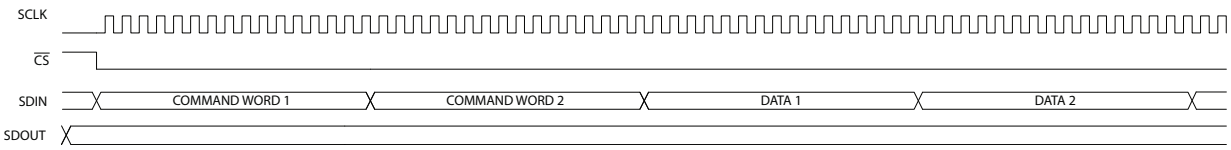


Figure 4-23: GSPI Write Timing—Auto-Increment with GSPI Link Disable Operation

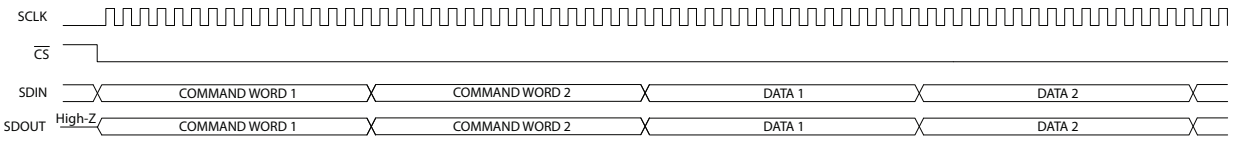


Figure 4-24: GSPI Write Timing—Auto-Increment with Bus-Through Operation

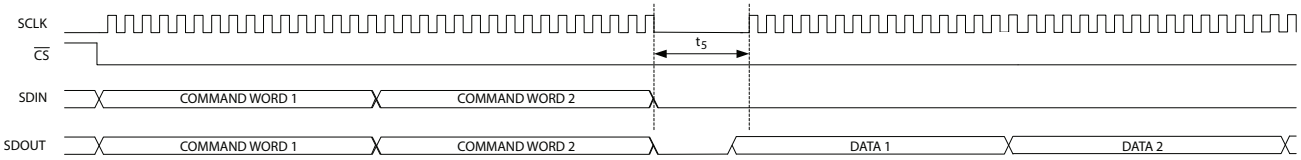


Figure 4-25: GSPI Read Timing—Auto-Increment Read with Loop-Through Operation (default)

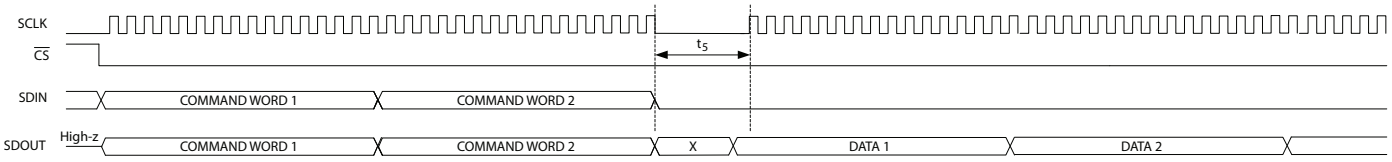


Figure 4-26: GSPI Read Timing—Auto-Increment Read with Bus-through Operation

4.9.9 Setting a Device Unit Address

Multiple (up to 32) GS12281 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the **DEV_UNIT_ADDRESS** of each device is set to 0_h and the SDIN→SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEV_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEV_UNIT_ADDRESS** field set to 0. This disables the direct SDIN→SDOUT non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting **CONTROL_REG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEV_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEV_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEV_UNIT_ADDRESS** value 0.
3. Repeat step 2 using new, unique values for the **DEV_UNIT_ADDRESS** field in **CONTROL_REG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd\_GSPI\_conf}$ delay must be observed after every write that modifies **CONTROL_REG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEV_UNIT_ADDRESS** in **CONTROL_REG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.9.10 Default GSPI Operation

By default at power up or after a device reset, the GS12281 is set for Loop-Through Operation and the internal **DEV_UNIT_ADDRESS** field of the device is set to 0.

Figure 4-27 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS12281.

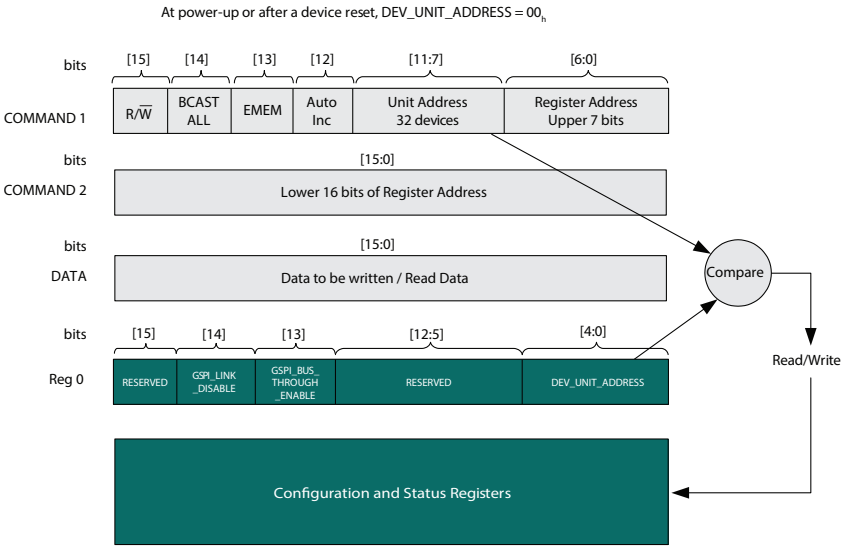


Figure 4-27: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access (R/$\overline{W}$ = 0); set Auto Increment; set the Unit Address field in the Command Word 1 to match the configured **DEV_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEV_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEV_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

4.9.11 Clear Sticky Counts Through Four Way Handshake

There are four sticky counters that keep count of changes in status of primary and secondary carrier detect, rate changes, and lock changes. The counters can be read from the following four parameters in register 0x84 and 0x85: **STAT_CNT_PRI_CD_CHANGES, STAT_CNT_SEC_CD_CHANGES**, **STAT_CNT_RATE_CHANGES**, and **STAT_CNT_PLL_LOCK_CHANGES**. The counters saturate at 255 (0xFF) and must be cleared before additional status changes can be counted. The following four way handshake procedures clears the counters.

1. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 0 (idle), then set **CTRL_CLEAR_COUNTS** = 1 (clear sticky counts).
2. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 2 (cleared), then reset **CTRL_CLEAR_COUNTS** to 0.

The device will now reset **STAT_CLEAR_COUNTS_STATUS** to 0 (idle) and the clearing process can be repeated at any time.

4.9.12 Device Power Up Sequence

The device does not require a specific power supply initialization sequence, and all chip supplies can be powered up simultaneously.

If all power supplies cannot be guaranteed to power up simultaneously, ensure that *VCC_DDI* powers up first. Please note that there is no minimum time requirement between power supply initializations after *VCC_DDI* is energized.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.9.12.1 Power-Up Timing Sequence

The following timing sequence must be observed after power-up when no external configuration loading is required. See Figure 4-28 for the timing requirements of Steps 1 and 2 below.

Step 1 – No GSPI Access Allowed

a) Device supply reaches 90% of target. POR (Power On Reset) is activated.

b) Internal blocks reset, default device configuration boot-up begins.

c) Default device configuration boot-up process.

Step 2 – GSPI Access Allowed

a) Host sets **EYE_MON_INT_CFG_3** (register address 0x57) to 0x8006.

b) If there are multiple devices on the GSPI chain, the host should configure the unit address of each device. See Section 4.9.9 for further information on unit addressing.

c) Host sets custom application specific settings.

d) Normal operation begins.

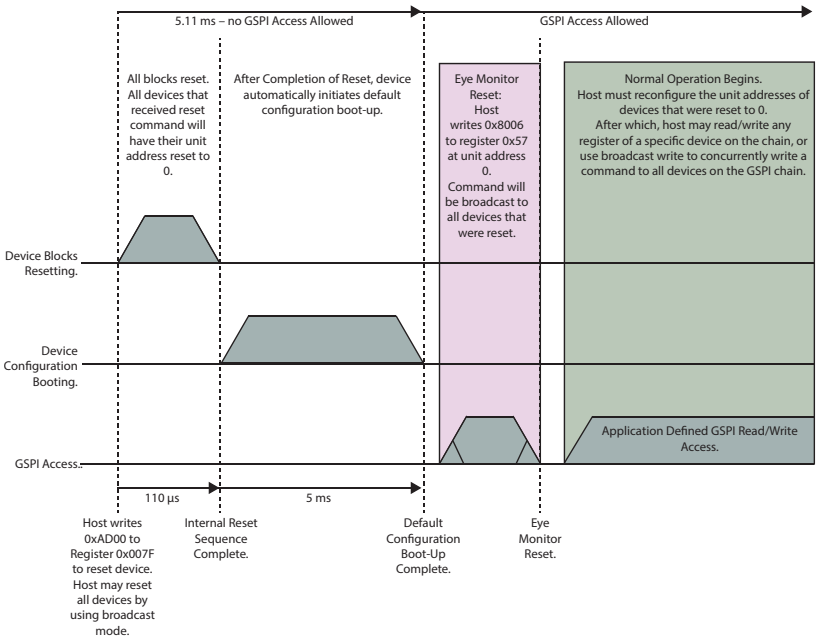


Figure 4-28: Power-Up Sequence.

4.9.13 Host Initiated Device Reset

The GS12281 includes a reset function accessible via the device's host interface, which reverts all internal logic and register values to their default values.

The device can be reset with a single write of $AD00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register, which will assert and de-assert the device reset within the duration of the GSPI write access Data Word.

The device can be placed and held in reset by writing $AA00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register. Subsequent writes of $DD00_h$ to the **RESET_CONTROL** bits will de-assert device reset.

The current state of user-initiated device reset can be read from the **RESET_CONTROL** bits of **CONTROL_RESET** register.

While in reset, host interface access to any other register will not be functional and all logic and configuration registers will be in reset state. While in reset, serial digital differential output behaviour is undefined. The digital logic and registers within the device will exit the reset state 5ms after device reset is de-asserted.

The following timing sequence must be observed to initiate a device reset.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.9.13.1 Host Initiated Device Reset Timing Sequence

The following timing sequence must be observed after a Host Initiated Device Reset when no external configuration loading is required. See Figure 4-29 for the timing requirements of the Steps 1 to 3 below.

Step 1 – GSPI Access Allowed

a) Host writes 0xAD00 to register 0x007F to reset selected devices, or all devices using broadcast.

Step 2– No GSPI Access Allowed

a) Internal blocks reset, default device configuration boot-up begins.

b) Default device configuration boot-up completes.

Step 3 – GSPI Access Allowed

a) Host sets **EYE_MON_INT_CFG_3** (register address 0x57) to 0x8006.

b) If there are multiple devices on the GSPI chain, host must reconfigure unit address of each device that was reset. See Section 4.9.9 for further information on unit addressing.

c) Host sets custom application specific settings.

d) Normal operation begins.

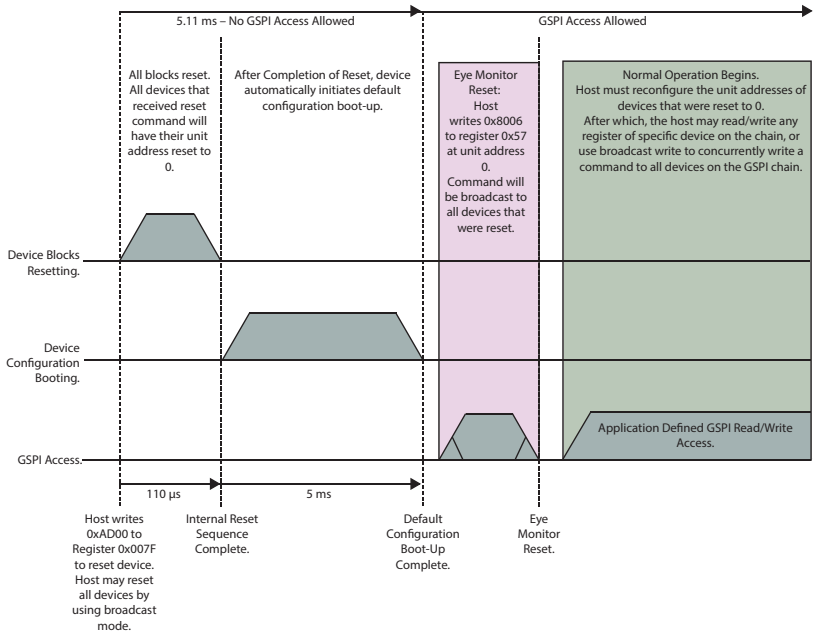


Figure 4-29: Host Initiated Device Reset Timing Sequence.

5. Register Map

The host interface on the GS12281 provides users complete control of key features such as GPIO configuration, PLL loop bandwidth settings, re-time parameters, carrier detection, trace equalization, bypass modes, output swing controls, mute functions, pre-emphasis control and many others.

It also includes a wide selection of Status registers which allow the user to read back several key metrics of information from the GS12281 to add more flexibility to their designs. Section 5.1 to Section 5.3 cover each Control and Status register in detail.

5.1 Control Registers

Table 5-1: Control Registers

GSPI $Address_h$	Register Name	R/W
0	CONTROL_ REG	RW
1	DEVICE_ID	RO
2	RSVD	RW
7F	CONTROL_ RESET	RW
3	CONTROL_ SLEEP	RW
4	MISC_CNTRL	RW
5	MISC_CFG	RW
6	RATE_ DETECT_ MODE	RW
7	RSVD	RW
CDR Configuration		
8	REF_CLK_ MODE	RW
9	FACTORY_ CDR_ PARAMETERS	RW
0A	PLL_LOOP_ BANDWIDTH_ 0	RW
0B	PLL_LOOP_ BANDWIDTH_ 1	RW
0C	PLL_LOOP_ BANDWIDTH_ 2	RW
0D to 0F	RSVD	RW
GPIO Configuration		
10	GPIO0_CFG	RW
11	GPIO1_CFG	RW
12	GPIO2_CFG	RW
13	GPIO3_CFG	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
Equalizer Configuration		
14 to 1D	RSVD	RW
1E	TREQ0_ INPUT_BOOST	RW
1F	TREQ0_CD_ HYSTERESIS	RW
20 to 25	RSVD	RW
Output Configuration		
26 to 27	RSVD	RW
28	OUTPUT_ PARAM_CD_ SD_0	RW
29	OUTPUT_ PARAM_CD_ SD_1	RW
2A	OUTPUT_ PARAM_CD_ SD_2	RW
2B	OUTPUT_ PARAM_CD_ SD_3	RW
2C	OUTPUT_ PARAM_ CD_HD_0	RW
2D	OUTPUT_ PARAM_ CD_HD_1	RW
2E	OUTPUT_ PARAM_ CD_HD_2	RW
2F	OUTPUT_ PARAM_ CD_HD_3	RW
30	OUTPUT_ PARAM_ CD_UHD_0	RW
31	OUTPUT_ PARAM_ CD_UHD_1	RW
32	OUTPUT_ PARAM_ CD_UHD_2	RW
33	OUTPUT_ PARAM_ CD_UHD_3	RW
34 to 47	RSVD	RW
Output Control		
48	OUTPUT_ SIG_SELECT	RW
49	CONTROL_ OUTPUT_ MUTE	RW
4A	CONTROL_ OUTPUT_ DISABLE	RW
4B	CONTROL_ OUTPUT_ SLEW	RW
4C	CONTROL_ RETIMER_ BYPASS	RW
4D	CONTROL_ BALANCED_ MODE	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
4E to 4F	RSVD	RW
Test Functions		
50	PRBS_ CHK_CFG	RW
51	PRBS_CHK_ CTRL	RW
52	PRBS_GEN_ CTRL	RW
53	RSVD	RW
54	EYE_MON_ INT_CFG_0	RW
55	EYE_MON_ INT_CFG_1	RW
56	EYE_MON_ INT_CFG_2	RW
57	EYE_MON_ INT_CFG_3	RW
58 to 59	RSVD	RW
5A	EYE_MON_ SCAN_CTRL_0	RW
5B	EYE_MON_ SCAN_CTRL_1	RW
5C	EYE_MON_ SCAN_CTRL_2	RW
5D	EYE_MON_ SCAN_CTRL_3	RW
Internal Only Configuration		
5E to 7E	RSVD	RW

5.2 Status Registers

Table 5-2: Status Registers

GSPI Address$_h$	Register Name	R/W
80	RSVD	RW
81	VERSION_0	RW
82	VERSION_1	RW
83	VERSION_2	RW
84	STICKY_ COUNTS_0	RW
85	STICKY_ COUNTS_1	RW
86	CURRENT_ STATUS_0	RW
87	CURRENT_ STATUS_1	RW

Table 5-2: Status Registers (Continued)

GSPI Address$_h$	Register Name	R/W
88	RSVD	RW
89	PRBS_ CHK_ ERR_CNT	RW
8A	PRBS_ CHK_STATUS	RW
8B	EYE_MON_ SCAN_ SIZE_OUTPUT	RW
8C	EYE_MON_ SHAPE_ OUTPUT_0	RW
8D	EYE_MON_ SHAPE_ OUTPUT_1	RW
8E	EYE_MON_ SHAPE_ OUTPUT_2	RW
8F	EYE_MON_ SHAPE_ OUTPUT_3	RW
90	EYE_MON_ STATUS	RW
91 to BF	RSVD	RW

5.3 Register Descriptions

Table 5-3: Control Register Descriptions

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Device Configuration And Control						
0	CONTROL_ REG	RSVD	15	R/W	0	Reserved do not modify.
		GSPI_LINK_DISABLE	14	R/W	0	0 = Enable loop-through. SDIN pin is looped through to the SDOUT pin. 1 = Disable loop-through. Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.
		GSPI_BUS_THROUGH_ ENABLE	13	R/W	0	0 = Disable bus-through mode 1 = Enable bus-through mode
		DEV_UNIT_ADDRESS	4:0	R/W	0	Device address programmed by application. See Section 4.9.9 for further information
1	DEVICE_ID	DEVICE_VERSION	15:0	RO	—	This register contains the device's identification, including revision. Contact the local technical sales representative for more details.
2	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7F	CONTROL_ RESET	RESET_CONTROL	15:0	R/W	DD00	Device Reset, Reverts all internal logic and register values to defaults. Write Values: $AA00_h$ = Asserts device reset $DD00_h$ = De-assert device reset $AD00_h$ = Assert/de-assert device reset in a single write Read Values: $AA00_h$ = User-initiated reset is asserted $DD00_h$ = User-initiated reset is de-asserted See Section 4.9.13 for further information
3	CONTROL_ SLEEP	RSVD	15:2	R/W	0	Reserved - do not modify.
		CTRL_MANUAL_SLEEP	1	R/W	0	Sleep manual mode control: 0 = Never Sleep 1 = Always Sleep Controls sleep mode when auto sleep (CTRL_AUTO_SLEEP) is disabled.
		CTRL_AUTO_SLEEP	0	R/W	1	Sleep auto mode control: 0 = Disable auto sleep mode 1 = Enable auto sleep mode If CTRL_AUTO_SLEEP = 0 (manual sleep mode), then CTRL_MANUAL_SLEEP controls sleep. If CTRL_AUTO_SLEEP = 1 (auto sleep mode), sleep is automatically entered on loss of signal.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4	MISC_CNTRL	RSVD	15:1	R/W	0	Reserved - do not modify.
		CTRL_CLEAR_COUNTS	0	R/W	0	Clear sticky counts control register. 0 = no action 1 = clear sticky counts. Part of a four way handshake with STAT_CLEAR_COUNTS_STATUS. See Section 4.9.11 for more details on implementing the four way handshake for this operation.
5	MISC_CFG	RSVD	15:4	R/W	0	Reserved - do not modify.
		CFG_SLEEP_ OUTPUT1_MUTE	3	R/W	0	Controls whether cable driver (SDO1) is muted or disabled (powered down) during sleep: 0 = disable (power down) output during sleep. 1 = mute output during sleep.
		CFG_SLEEP_ OUTPUT0_MUTE	2	R/W	0	Controls whether cable driver (SDO0) is muted or disabled (powered down) during sleep: 0 = disable (power down) output during sleep. 1 = mute output during sleep.
		RSVD	1:0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
CDR Configuration						
6	RATE_ DETECT_ MODE	RSVD	15:14	R/W	3	Reserved - do not modify.
		CFG_RATE_ENA_12G	13	R/W	1	12G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_6G	12	R/W	1	6G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_3G	11	R/W	1	3G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_HD	10	R/W	1	HD auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_SD	9	R/W	1	SD auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_MADI	8	R/W	0	MADI auto rate detection enable: 0 = Disable rate 1 = Enable rate
		RSVD	7:5	R/W	0	Reserved - do not modify.
		CFG_MANUAL_RATE	4:1	R/W	0	Manual rate selection. The CDR will only lock to the selected rate if CFG_AUTO_RATE_DETECT_ENA = 0: 0 = Trace Equalizer bypass mode enable 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = 6G 6 = 12G 7 = Reserved - do not modify.
		CFG_AUTO_RATE_DETE CT_ENA	0	R/W	1	Set or disable auto rate detection mode for the CDR. 0 = Disable auto rate detection 1 = Enable auto rate detection When automatic rate detection is disabled (CFG_AUTO_RATE_DETECT_ENA = 0), the rate is set by CFG_MANUAL_RATE.
7	RSVD	RSVD	15:0	R/W	3	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
8	REF_CLK_ MODE	RSVD	15:2	R/W	0	Reserved - do not modify.
		CFG_REF_CLK_MODE_ MANUAL	1	R/W	1	Manual external reference mode selection: 0 = External reference clock mode 1 = Referenceless mode Controls reference clock mode when CFG_REF_CLK_MODE_AUTO = 0.
		CFG_REF_CLK_MODE_ AUTO	0	R/W	1	Automatic external reference selection mode. 0 = Disable auto mode 1 = Enable auto mode In auto mode, the device automatically switches to reference clock mode when the reference clock is detected. When auto mode is disabled, reference clock mode is controlled by CFG_REF_CLK_MODE_MANUAL. **Note:** Once the device has been switched to external reference mode, either manual or automatically, it can not be manually set back to referenceless mode unless it is followed by a device reset.
9	FACTORY_ CDR_ PARAMETERS	RSVD	15:4	R/W	7	Reserved - do not modify.
		PHASE_MODE	3:2	R/W	0	Set to 3_h when using a PRBS7 signal or similar repetitive short pattern.
		CFG_MIN_LBW	1	R/W	0	To maximize LBW of PLL and consequently IJT of CDR, set this parameter to 0.
		RSVD	0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0A	PLL_LOOP_BANDWIDTH_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_12G	12:8	R/W	8	Configure PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). 11.88Gb/s (12G) loop bandwidth setting: 0x00 = Reserved - do not use 0x01 = 0.0625x 0x02 = 0.125x 0x03 = 0.1875x 0x04 = 0.25x 0x05 = 0.3125x 0x06 = 0.375x 0x07 = 0.4375x 0x08 = 0.5x 0x09 = 0.5625x 0x0A = 0.625x 0x0B = 0.6875x 0x0C = 0.75x 0x0D = 0.8125x 0x0E = 0.875x 0x0F = 0.9375x 0x10 to 0x1B = Reserved - do not use 0x1C = 1.0x (nominal) 0x1D = 1.0625x 0x1E = 1.125x 0x1F = 1.1875x
		RSVD	7:5	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_6G	4:0	R/W	8	Configure 5.94Gb/s (6G) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_12G parameter for available settings.
0B	PLL_LOOP_BANDWIDTH_1	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_3G	12:8	R/W	8	Configure 2.97Gb/s (3G) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_12G parameter for available settings.
		RSVD	7:5	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_HD	4:0	R/W	8	Configure 1.485Gb/s (HD) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_12G parameter for available settings.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0C	PLL_LOOP_BANDWIDTH_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_SD	12:8	R/W	1C	Configure 270Mb/s (SD) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_12G parameter for available settings.
		RSVD	7:5	R/W	0	Reserved - do not modify.
		CFG_PLL_LBW_MADI	4:0	R/W	8	Configure 125Mb/s (MADI) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_12G parameter for available settings.
0D	RSVD	RSVD	15:0	R/W	8	Reserved - do not modify.
0E to 0F	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
GPIO Configuration						
		RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO0_ OUTPUT_ENA	8	R/W	1	GPIO0 buffer mode control. 0 = GPIO pin is configured as an input (tri-stated / high impedance). 1 = GPIO pin is configured as an output.
10	GPIO0_CFG	CFG_GPIO0_FUNCTION	7:0	R/W	80	Function select for GPIO0 pin. GPIO0 output functions: 0x00 = Output driven LOW 0x01 = Output driven HIGH 0x02 = PLL lock status (HIGH — PLL locked) 0x03 to 0x7E = Reserved - do not use. 0x80 = LOS equivalent to inverse of STAT_PRI_CD (Default mode for GPIO0) 0x81 = carrier detect status (STAT_PRI_CD) 0x82 = Sleep mode status (HIGH — Device in sleep mode) 0x83 = HIGH for SD, LOW for all other rates. 0x84 = Rate detected [0] 0x85 = Rate detected [1] 0x86 = Rate detected [2] **Note:** To have full rate range using the GPIO rate detect function, one GPIO pin must be used for each Rate Detect bit[2:0]. Please see Table 4-2: Detected Data Rates for the indication values. 0x87 to 0xFF = Reserved - do not use. GPIO0 input functions: 0x00 to 0x7E = Reserved - do not use. 0x80 = Unused 0x81 = SDO0 disable control (HIGH — disable) 0x82 = SDO1 disable control (HIGH — disable) 0x83 = Reserved - do not modify. 0x84 = Unused 0x85 = Retimer bypass enable (HIGH — Bypass enabled) 0x86 = Sleep control (HIGH — Sleep) 0x87 to 0xFF = Reserved - do not use.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
11	GPIO1_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO1_ OUTPUT_ENA	8	R/W	1	GPIO1 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Output
		CFG_GPIO1_ FUNCTION	7:0	R/W	2	Function select for GPIO1 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x02 = PLL lock status
12	GPIO2_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO2_ OUTPUT_ENA	8	R/W	0	GPIO2 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO2_FUNCTION	7:0	R/W	86	Function select for GPIO2 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x86 = Sleep control
13	GPIO3_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO3_ OUTPUT_ENA	8	R/W	0	GPIO3 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO3_FUNCTION	7:0	R/W	82	Function select for GPIO3 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x82 = SDO1 disable control (HIGH disable)

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Trace Equalizer Configuration						
14 to 1D	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
1E	TREQ0_ INPUT_BOOST	RSVD	15:5	R/W	0	Reserved - do not modify.
		CFG_TREQ0_BOOST	4:1	R/W	2	Trace equalizer boost setting for TEQ (Trace Equalizer): 0 = Bypass equalization stage 1 to 8 = 1 to 17dB of insertion loss at 5.94GHz (see Figure 4-1). Bypass is the minimum boost setting; boost 8 is maximum boost setting.
		CFG_TREQ0_ CD_BOOST	0	R/W	0	Selects boost level applied to DDI input signal for carrier detection function only. 0 = Sets to boost 8 (See Figure 4-1) 1 = Use CFG_TREQ0_BOOST setting
1F	TREQ0_CD_ HYSTERESIS	RSVD	15:8	R/W	0	Reserved - do not modify.
		CFG_TREQ0_CD_ ASSERT_THRESH	7:4	R/W	4	Sets assert threshold for trace equalizer carrier detect 0 to15_d, where 0 is minimum threshold and 15_d is maximum threshold (see Figure 4-2).
		CFG_TREQ0_CD_ DEASSERT_THRESH	3:0	R/W	3	Sets deassert threshold for trace equalizer carrier detect 0 to15_d, where 0 is minimum threshold and 15_d is maximum threshold (see Figure 4-2).
20 to 25	MISC_ OUTPUT_CFG	RSVD	15:0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Output Configuration						
26 to 27	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
28	OUTPUT_ PARAM_CD_ SD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ SD_PREEMPH_WIDTH	12:8	R/W	3	Configure the MADI/SD rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ SD_PREEMPH_ PWRDWN	6	R/W	1	Power down the MADI/SD rate pre-emphasis on cable driver output1 (SDO1). 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_ SD_PREEMPH_AMPL	5:0	R/W	0	Configure the MADI/SD rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
29	OUTPUT_ PARAM_CD_ SD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ SD_DRIVER_SWING	13:8	R/W	17	Configure the MADI/SD rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	A0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2A	OUTPUT_PARAM_CD_SD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_SD_PREEMPH_WIDTH	12:8	R/W	3	Configure the MADI/SD rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_SD_PREEMPH_PWRDWN	6	R/W	1	Power down the MADI/SD rate pre-emphasis on cable driver output0 (SDO0). 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_SD_PREEMPH_AMPL	5:0	R/W	0	Configure the MADI/SD rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2B	OUTPUT_PARAM_CD_SD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_SD_DRIVER_SWING	13:8	R/W	17	Configure the MADI/SD rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	A0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2C	OUTPUT_PARAM_CD_HD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_HD_PREEMPH_WIDTH	12:8	R/W	8	Configure the HD/3G rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_HD_PREEMPH_PWRDWN	6	R/W	0	Power down the HD/3G rate pre-emphasis on cable driver output1 (SDO1) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_HD_PREEMPH_AMPL	5:0	R/W	5	Configure the HD/3G rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2D	OUTPUT_PARAM_CD_HD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_HD_DRIVER_SWING	13:8	R/W	19	Configure the HD/3G rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	80	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2E	OUTPUT_PARAM_CD_HD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_HD_PREEMPH_WIDTH	12:8	R/W	8	Configure the HD/3G rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W		Reserved - do not modify.
		CFG_OUTPUT0_CD_HD_PREEMPH_PWRDWN	6	R/W	0	Power down the HD/3G rate pre-emphasis on cable driver output0 (SDO0) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_HD_PREEMPH_AMPL	5:0	R/W	5	Configure the HD/3G rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2F	OUTPUT_PARAM_CD_HD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_HD_DRIVER_SWING	13:8	R/W	19	Configure the HD/3G rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	80	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
30	OUTPUT_ PARAM_ CD_UHD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_PREEMPH_ WIDTH	12:8	R/W	4	Configure the 6G/12G rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_PREEMPH_ PWRDWN	6	R/W	0	Power down the 6G/12G rate pre-emphasis on cable driver output1 (SDO1) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_ UHD_PREEMPH_AMPL	5:0	R/W	4	Configure the 6G/12G rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
31	OUTPUT_ PARAM_ CD_UHD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_DRIVER_ SWING	13:8	R/W	1B	Configure the 6G/12G rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the differential cable driver amplitude. The default value produces an amplitude of 800mVpp.
		RSVD	7:0	R/W	40	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
32	OUTPUT_ PARAM_ CD_UHD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ UHD_PREEMPH_ WIDTH	12:8	R/W	4	Configure the 6G/12G rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ UHD_PREEMPH_ PWRDWN	6	R/W	0	Power down the 6G/12G rate pre-emphasis on cable driver output0 (SDO0) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_ UHD_PREEMPH_AMPL	5:0	R/W	4	Configure the 6G/12G rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
33	OUTPUT_ PARAM_ CD_UHD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ UHD_DRIVER_SWING	13:8	R/W	1B	Configure the 6G/12G rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	40	Reserved - do not modify.
34 to 3B	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
3C	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
3D	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
3E	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
3F	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
40	RSVD	RSVD	15:0	R/W	340	Reserved - do not modify.
41	RSVD	RSVD	15:0	R/W	850	Reserved - do not modify.
42	RSVD	RSVD	15:0	R/W	340	Reserved - do not modify.
43	RSVD	RSVD	15:0	R/W	850	Reserved - do not modify.
44	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
45	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
46	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
47	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
Output Control						
48	OUTPUT_ SIG_SELECT	RSVD	15:4	R/W	10	Reserved - do not modify.
		CTRL_OUTPUT0_ DATA_INVERT	3	R/W	0	Controls optional signal polarity inversion on cable driver output0 (SDO0) when data is selected (CTRL_OUTPUT0_SIGNAL_SEL = 0).
		CTRL_OUTPUT1_ DATA_INVERT	2	R/W	0	Controls optional signal polarity inversion on cable driver output1 (SDO1) when data is selected (CTRL_OUTPUT1_SIGNAL_SEL = 0).
		CTRL_OUTPUT0_ SIGNAL_SEL	1	R/W	0	Select between Data and PRBS generator on output0 (SDO0). 0 = Data 1 = PRBS generator output (PRBS7 or divided version of PRBS generator clock)
		CTRL_OUTPUT1_ SIGNAL_SEL	0	R/W	0	Select between data or PRBS generator on output1 (SDO1). 0 = Data 1 = PRBS generator output (PRBS7 or divided version of PRBS generator clock)

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
49	CONTROL_OUTPUT_MUTE	RSVD	15:6	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_AUTO_MUTE_DURING_RATE_SEARCH	5	R/W	0	Selects whether auto-mute mutes cable driver output1 (SDO1) during rate search or not (i.e. based on loss of lock) in addition to loss of the selected carrier. This is undesirable if the application passes non-standard rates through the part using CDR bypass.
		CTRL_OUTPUT0_AUTO_MUTE_DURING_RATE_SEARCH	4	R/W	0	Selects whether auto-mute mutes cable driver output0 (SDO0) during rate search or not (i.e. based on loss of lock) in addition to loss of the selected carrier. This is undesirable if the application passes non-standard rates through the part using CDR bypass. When 1 this mutes the output when not locked. Host should set this to 0 if using PRBS generator with CTRL_PRBS_GEN_CLK_SRC = 0, 1 or 2.
		CTRL_OUTPUT1_MANUAL_MUTE	3	R/W	0	Controls mute for cable driver output1 (SDO1) when auto mute (CTRL_OUTPUT1_AUTO_MUTE = 0) is disabled. 0 = Unmute output driver 1 = Mute output driver.
		CTRL_OUTPUT1_AUTO_MUTE	2	R/W	1	Select automatic or manual mute control for cable driver output1 (SDO1) 0 = Disable auto mute mode 1 = Enable auto mute mode If CTRL_OUTPUT1_AUTO_MUTE = 0, then CTRL_OUTPUT1_MANUAL_MUTE controls mute for SDO1.
		CTRL_OUTPUT0_MANUAL_MUTE	1	R/W	0	Controls mute for cable driver output0 (SDO0) when auto mute (CTRL_OUTPUT0_AUTO_MUTE = 0) is disabled. 0 = Unmute output driver 1 = Mute output driver.
		CTRL_OUTPUT0_AUTO_MUTE	0	R/W	1	Select automatic or manual mute control for cable driver output0 (SDO0) 0 = Disable auto mute mode 1 = Enable auto mute mode If CTRL_OUTPUT0_AUTO_MUTE = 0, then CTRL_OUTPUT0_MANUAL_MUTE controls mute for SDO0.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4A	CONTROL_ OUTPUT_ DISABLE	RSVD	15:4	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ MANUAL_DISABLE	3	R/W	0	Controls disable for cable driver output1 (SDO1) when auto disable (CTRL_OUTPUT1_AUTO_DISABLE = 0) is disabled. 0 = Enable output driver 1 = Disable (power down) output driver.
		CTRL_OUTPUT1_ AUTO_DISABLE	2	R/W	0	Select automatic or manual disable control for cable driver output1 (SDO1) 0 = Disable auto disable mode 1 = Enable auto disable mode If CTRL_OUTPUT1_AUTO_DISABLE = 0, then CTRL_OUTPUT1_MANUAL_DISABLE controls mute for SDO1.
		CTRL_OUTPUT0_ MANUAL_DISABLE	1	R/W	0	Controls disable for cable driver output0 (SDO0) when auto disable (CTRL_OUTPUT0_AUTO_DISABLE = 0) is disabled. 0 = Enable output driver 1 = Disable (power down) output driver.
		CTRL_OUTPUT0_ AUTO_DISABLE	0	R/W	0	Select automatic or manual disable control for cable driver output0 (SDO0) 0 = Disable auto disable mode 1 = Enable auto disable mode If CTRL_OUTPUT0_AUTO_DISABLE = 0, then CTRL_OUTPUT0_MANUAL_DISABLE controls mute for SDO0.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4B	CONTROL_OUTPUT_SLEW	RSVD	15:11	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_MANUAL_SLEW	10:9	R/W	2	Selects slew rate for cable driver output1 (SDO1) when auto slew rate is disabled. 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		CTRL_OUTPUT1_AUTO_SLEW	8	R/W	1	Selects between auto or manual slew rate selection for cable driver output1 (SDO1). 0 = Disable auto slew rate selection. 1 = Enable auto slew rate selection. This may be necessary when device is passing an unsupported rate, or when using the PRBS generator when the device is not locked to an input signal.
		RSVD	7:3	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT0_MANUAL_SLEW	2:1	R/W	2	Selects slew rate for cable driver output0 (SDO0) when auto slew rate is disabled. 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		CTRL_OUTPUT0_AUTO_SLEW	0	R/W	1	Selects between auto or manual slew rate selection for cable driver output0 (SDO0). 0 = Disable auto slew rate selection. 1 = Enable auto slew rate selection. This may be necessary when device is passing an unsupported rate, or when using the PRBS generator when the device is not locked to an input signal. **Note:** In auto-mode, the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to 6G/12G Slew (see Table 2-3 for Rise/Fall Times).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4C	CONTROL_ RETIMER_ BYPASS	RSVD	15:4	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ RETIMER_MANUAL_ BYPASS	3	R/W	0	Controls retimer bypass for cable driver output1 (SDO1), when auto mode is disabled (CTRL_OUTPUT1_RETIMER_AUTO_BYPASS = 0). 0 = Disable retimer bypass 1 = Enable retimer bypass
		CTRL_OUTPUT1_ RETIMER_AUTO_ BYPASS	2	R/W	1	Selects between auto and manual control of retimer bypass for cable driver output1 (SDO1) 0 = Disable auto mode 1 = Enable auto mode
		CTRL_OUTPUT0_ RETIMER_MANUAL_ BYPASS	1	R/W	0	Controls retimer bypass for cable driver output0 (SDO0), when auto mode is disabled (CTRL_OUTPUT0_RETIMER_AUTO_BYPASS = 0). 0 = Disable retimer bypass 1 = Enable retimer bypass
		CTRL_OUTPUT0_ RETIMER_AUTO_ BYPASS	0	R/W	1	Selects between auto and manual control of retimer bypass for cable driver output0 (SDO0) 0 = Disable auto mode 1 = Enable auto mode
4D	CONTROL_ BALANCED_ MODE	RSVD	15:2	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ BALANCED	1	R/W	0	Enable or Disable balanced mode on cable driver output1 (SDO1) for powered ORL measurement. 0 = Disable 1 = Enable
		CTRL_OUTPUT0_ BALANCED	0	R/W	0	Enable or Disable balanced mode on cable driver output (SDO0) for powered ORL measurement. 0 = Disable 1 = Enable
4E to 4F	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Diagnostic Control Features						
50	PRBS_ CHK_CFG	RSVD	15	R/W	0	Reserved - do not modify.
		CFG_PRBS_CHECK_ PHASEADJUST	14:13	R/W	0	Adjusts the phase of the clock to the PRBS checker: 0 = 0 1 = 90 2 = 180 3 = 270 **Note:** A setting of 0 is ideal for most applications. Adjustment is not expected.
		CFG_PRBS_CHECK_ INVERT	12	R/W	0	Optionally inverts the retimed data at the input to the PRBS checker: 0 = no inversion 1 = data inverted
		CFG_PRBS_CHECK_ PREDIVIDER	11:8	R/W	0	Selects pre-divider for PRBS check measurement timer: setting = pre-divider value 0 = 4 1 = 8 2 = 16 3 = 32 4 = 64 5 = 128 6 = 256 7 = 512 8 = 1024 9 = 2048
		CFG_PRBS_CHECK_ MEAS_TIME	7:0	R/W	3	Selects PRBS check measurement interval for timed measurements. See Section 4.4.1 for more details.
51	PRBS_CHK_ CTRL	RSVD	15:9	R/W	0	Reserved - do not modify.
		CTRL_PRBS_CHECK_ TIMED_CONT_B	8	R/W	0	Selects between timed and continuous PRBS check mode. 0 = Selects continuous PRBS check mode. 1 = Selects timed PRBS check mode.
		RSVD	7:1	R/W	0	Reserved - do not modify.
		CTRL_PRBS_CHECK_ START	0	R/W	0	Set to 1 by host to start a timed operation. Set to 0 by host after completion or abort of the operation (by the device due to loss of lock) to tell the device that PRBS result has been read by the host. See Section 4.4 for more details on PRBS checker function.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
52	PRBS_GEN_CTRL	RSVD	15:10	R/W	0	Reserved - do not modify.
		CTRL_PRBS_GEN_ENABLE	9	R/W	0	Selects whether the PRBS generator is enabled or not: 0 = PRBS Generator disabled 1 = PRBS Generator enabled **Note:** enabling the PRBS generator does not automatically override other device modes such as auto-sleep, auto-output-mute, auto-output-disable, etc. These continue to function normally. The user/host may need to adjust those settings to ensure the part will output the PRBS signal.
		CTRL_PRBS_GEN_SIGNAL_SELECT	8	R/W	1	Select output signal from PRBS generator as either PRBS7 or divided clock (divided version of the PRBS generator clock source): 0 = clock divider (using ratio set by CTRL_PRBS_GEN_CLK_DIVIDER) 1 = PRBS7
		CTRL_PRBS_GEN_CLK_SRC	7:6	R/W	0	Selects clock source for PRBS generator: 0 = VCO (free running) 1 = Reserved 2 = Clock reference PLL (internal reference clock) 3 = Data reference PLL (CDR recovered clock)

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
52 (Continued)	PRBS_GEN_ CTRL (Continued)	CTRL_PRBS_GEN_ CLK_DIVIDER	5:4	R/W	0	Selects clock divider ratio for when host selects divided clock to output on PRBS generator (CTRL_PRBS_GEN_SIGNAL_SELECT = 0): 0 = divide by 2 1 = divide by 4 2 = divide by 8 3 = divide by 16
		CTRL_PRBS_GEN_ INVERT	3	R/W	0	Controls optional inversion of the generated PRBS pattern: 0 = true sense 1 = inverted
		CTRL_PRBS_GEN_ DATA_RATE	2:0	R/W	6	Select PRBS7 data rate when PRBS clock source not recovered clock (CTRL_PRBS_GEN_CLK_SRC ≠ 3) 0 = Reserved - do not use. 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = 6G 6 = 12G 7 = Reserved - do not use. If CTRL_PRBS_GEN_CLK_SRC = 3, then CTRL_PRBS_GEN_DATA_RATE setting has no effect and the CDR rate is used (based on automatic rate detection or manual rate selection). Additionally, if the device is locked to an input signal, only the same rate can be selected for the PRBS generator.
53	RSVD	RSVD	15:0	—	—	Reserved - do not modify.
54	EYE_MON_ INT_CFG_0	CFG_EYE_MON_ TIMEOUT_MS	15:0	R/W	0	CFG_EYE_MON_TIMEOUT[31:16]. Most significant 16 bits of the measurement time. This is the time spent measuring bit errors at each point in the eye scan, i.e. the time to measure one point in the eye. Units are in microseconds. The Eye Scanner scans each point twice and there is some overhead, so the actual measurement time is twice the number entered.
55	EYE_MON_ INT_CFG_1	CFG_EYE_MON_ TIMEOUT_LS	15:0	R/W	64	CFG_EYE_MONT_TIMEOUT[15:0] Least significant 16 bits of the measurement time. See CFG_EYE_MON_ TIMEOUT_MS

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
56	EYE_MON_ INT_CFG_2	CFG_EYE_BER_ THRESHOLD	15:0	R/W	64	Threshold of bit error counts to define good vs bad points in eye for shape scan. See Section 4.5 for further details.
57	EYE_MON_ INT_CFG_3	CFG_EYE_DEFAULT_ VERT_OFFSET	15:8	R/W	80	The vertical offset slice that will be used for eye shape queries. Offset values: 0 to 255_d. 0 represents the most negative slice since 128_d is the 0V slice level and 255_d is the most positive slice level. Default is 128_d
		RSVD	7:3	R/W	0	Reserved - do not modify.
		CFG_EYE_INIT_RESET	2	R/W	0	Eye monitor initialization bit. Set HIGH during Device Power-Up Sequence. See Section 4.9.12 for details.
		RSVD	1:0	R/W	0	Reserved - do not modify.
58	RSVD	RSVD	15:0	R/W	D280	Reserved - do not modify.
59	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
5A	EYE_MON_ SCAN_CTRL_0	RSVD	15	R/W	0	Reserved - do not modify.
		CTRL_EYE_PHASE_ START	14:8	R/W	0	Starting phase offset. Valid range is 0 to 127_d. Reset value must be used for shape scan.
		RSVD	7	R/W	0	Reserved - do not modify.
		CTRL_EYE_PHASE_ STOP	6:0	R/W	7F	Phase offset limit. Valid range is 0 to 127_d. CTRL_EYE_PHASE_STOP must be greater or equal to CTRL_EYE_PHASE_START. Reset value must be used for shape scan.
5B	EYE_MON_ SCAN_CTRL_1	RSVD	15	R/W	0	Reserved - do not modify.
		CTRL_EYE_PHASE_ STEP	14:8	R/W	1	Unsigned value for phase step size. Valid values are 1,2, and 4. Reset value must be used for shape scan. Behaviour is undefined for other values. In order to use a step size of 2 or 4, CTRL_EYE_PHASE_START and CTRL_EYE_PHASE_STOP must be set to their default values.
		RSVD	7	R/W	0	Reserved - do not modify.
		CTRL_EYE_VERT_ OFFSET_START	6:0	R/W	0	Starting voltage offset. Valid range is 0 to 255_d.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
5C	EYE_MON_ SCAN_CTRL_2	CTRL_EYE_VERT_ OFFSET_STOP	15:8	R/W	FF	Voltage offset limit. Valid range is 0 to 255_d. CTRL_EYE_VERT_OFFSET_STOP must be greater or equal to CTRL_EYE_VERT_OFFSET_START. Reset value must be used for shape scan. In order to use a step size of 2 or 4, CTRL_EYE_VERT_ OFFSET_START and CTRL_EYE_VERT_ OFFSET_STOP must be set to their default values.
		RSVD	7	R/W	0	Reserved - do not modify.
		CTRL_EYE_VERT_ OFFSET_STEP	6:0	R/W	1	Unsigned value for voltage offset step size. Valid values are 1,2, and 4. Behaviour is undefined for other values.
5D	EYE_MON_ SCAN_CTRL_3	RSVD	15:9	R/W	0	Reserved - do not modify.
		CTRL_EYE_SHAPE_ SCAN_B	8	R/W	0	Selects whether the eye monitor should perform an eye scan or eye shape capture: 0 = Selects eye scan (new or continued). 1 = Selects eye shape capture.
		RSVD	7:2	R/W	0	Reserved - do not modify.
		CTRL_EYE_MON_ POWER_CTRL	1	R/W	0	Power control for the eye monitor: 0 = Power down the eye monitor 1 = Power up the eye monitor Host is permitted to change this any time between eye scans (but not between partial eye scans). This must be set to 1 to run an eye scan. Behaviour is undefined if host sets CTRL_EYE_MON_START = 1 without setting this bit to 1.
		CTRL_EYE_MON_START	0	R/W	0	Part of a four way handshake with STAT_EYE_MON_STATUS: 0 = Set by host to tell the device to clear the status bit. 1 = Set by host only in order to begin/continue an eye scan or start an eye shape capture. See Section 4.5 for more details on implementing the four way hand shake for this operation.
5E to 5F	RSVD	RSVD	15:0	R/W		Reserved - do not modify.
Factory Settings						
60 to 7E	RSVD	RSVD	15:0	RO	—	Reserved.

Table 5-4: Status Register Descriptions

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
80	RSVD	RSVD	15:0	RO	—	Reserved.
81	VERSION_0	STAT_CONFIG_VER0	15:0	RO	—	This register contains the first part of the device configuration version. Please contact your local technical sales representative for more details.
82	VERSION_1	STAT_CONFIG_VER1	15:0	RO	—	This register contains the second part of the device configuration version. Please contact your local technical sales representative for more details.
83	VERSION_2	STAT_HW_VERSION	15:0	RO	—	This register contains the devices identification, including revision. Please contact your local technical sales representative for more details.
84	STICKY_ COUNTS_0	STAT_CNT_PRI_CD_ CHANGES	15:8	RO	—	Count of primary carrier detection status changes since last cleared. The count saturates at 255_d (0xFF). See Section 4.9.11 for procedure to clear the counts.
		RSVD	7:0	RO	—	Reserved.
85	STICKY_ COUNTS_1	STAT_CNT_RATE_ CHANGES	15:8	RO	—	Count of PLL rate changes since last cleared. The count saturates at 255_d (0xFF). See Section 4.9.11 for procedure to clear the counts.
		STAT_CNT_PLL_ LOCK_CHANGES	7:0	RO	—	Count of PLL lock status changes since last cleared. The count saturates at 255_d (0xFF). See Section 4.9.11 for procedure to clear the counts.

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
86	CURRENT_STATUS_0	RSVD	15	RO	—	Reserved
		STAT_CLEAR_COUNTS_STATUS	14:13	RO	—	Clear counts status: 0 = Idle 1 = Reserved 2 = Indicates device has cleared the sticky counts 3 = Reserved. Part of a four-way handshake with CTRL_CLEAR_COUNTS. See Section 4.9.11 for more details on implementing the four way handshake for this operation.
		STAT_LOCK	12	RO	—	PLL lock status: 0 = PLL is unlocked 1 = PLL is locked
		STAT_SLEEP	11	RO	—	Sleep status: 0 = Device is not in sleep 1 = Device is currently in sleep
		RSVD	10:8	RO	—	Reserved
		STAT_OUTPUT1_MODE	7:4	RO	—	Cable driver output1 (SDO1) output status: 0 = Mission Cable Driver SD/MADI slew rate 1 = Mission Cable Driver HD/3G slew rate 2 = Mission Cable Driver 6G/12G slew rate 3 = Reserved 4 = Reserved 5 = Balanced 6 = Mute 7 = Disabled
		STAT_OUTPUT0_MODE	3:0	RO	—	cable driver output0 (SDO0) output status: 0 = Mission Cable Driver SD/MADI slew rate 1 = Mission Cable Driver HD/3G slew rate 2 = Mission Cable Driver 6G/12G slew rate 3 = Reserved 4 = Reserved 5 = Balanced 6 = Mute 7 = Disabled

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
87	CURRENT_STATUS_1	STAT_OUTPUT1_DISABLE	15	RO	—	Cable driver output1 (SDO1) disable status: 0 = SDO1 is not disabled 1 = SDO1 is disabled
		STAT_OUTPUT0_DISABLE	14	RO	—	Cable driver output0 (SDO0) disable status: 0 = SDO0 is not disabled 1 = SDO0 is disabled
		STAT_OUTPUT1_MUTE	13	RO	—	Cable driver output1 (SDO1) mute status: 0 = SDO1 is not disabled 1 = SDO1 is disabled
		STAT_OUTPUT0_MUTE	12	RO	—	Cable driver output0 (SDO0) mute status: 0 = SDO0 is not disabled 1 = SDO0 is disabled
		STAT_OUTPUT1_RETIMER_BYPASS	11	RO	—	Cable driver output1 (SDO1) re-timer status: 0 = Retimer path to SDO1 is not bypassed 1 = Retimer path to SDO1 is bypassed
		STAT_OUTPUT0_RETIMER_BYPASS	10	RO	—	Cable driver output1 (SDO0) re-timer status: 0 = Retimer path to SDO0 is not bypassed 1 = Retimer path to SDO0 is bypassed
		RSVD	9	RO	—	Reserved
		STAT_PRI_CD	8	RO	—	Primary carrier detection status. 0 = Primary carrier is not detected 1 = Primary carrier is detected
		RSVD	7	RO	—	Reserved
		STAT_OUTPUT1_SLEW_RATE	6:5	RO	—	The current slew rate of cable driver output1 (SDO1): 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
87 (Continued)	CURRENT_ STATUS_1 (Continued)	STAT_OUTPUT0_ SLEW_RATE	4:3	RO	—	The current slew rate of cable driver output0 (SDO0): 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		STAT_DETECTED_RATE	2:0	RO	—	Rate at which the CDR is locked. 0 = Unlocked 1 = MADI (125Mb/s) 2 = SD (270Mb/s) 3 = HD (1.485Gb/s) 4 = 3G (2.97Gb/s) 5 = 6G (5.94Gb/s) 6 = 12G (11.88Gb/s) 7 = Reserved
88	RSVD	RSVD	15:0	RO	—	Reserved
89	PRBS_ CHK_ ERR_CNT	STAT_PRBS_CHK_ ERR_CNT	15:0	RO	—	PRBS checker error count. Cleared to 0 at the start of a measurement. Updated by the device on completion of a measurement. Value is undefined in case of abort due to loss of CDR lock (STAT_PRBS_CHECK_LAST_ABORT = 1).

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
		RSVD	15:8	RO	—	Reserved
		STAT_PRBS_CHECK_NODATA	9	RO	—	0 = Normal 1 = No data transitions were seen during the previous PRBS check. This bit is set to 1 to indicate that the input data was all 0's during a PRBS check. When that happens, the error count will be zero when in fact there was no valid PRBS pattern.This bit is updated by the device on completion of a measurement. It retains its value until the next PRBS check operation is requested. Value is undefined in case of abort (STAT_PRBS_CHECK_LAST_ABORT = 1). Value does not increment during a measurement until it completes.
8A	PRBS_CHK_STATUS	STAT_PRBS_CHECK_LAST_ABORT	8	RO	—	PRBS abort status. 0 = Normal. 1 = PRBS check was aborted due to loss of lock or sleep. This bit retains its value until the next PRBS operation is requested.
		RSVD	7:2	RO	—	Reserved
		STAT_PRBS_CHECK_STATUS	1:0	RO	—	Status for PRBS checker: 0 = PRBS check idle; ready for new operation. 1 = PRBS check timed or continuous operation in progress. 2 = PRBS check timed operation completed (success) 3 = PRBS check timed or continuous operation aborted (error) Part of a four way handshake with CTRL_PRBS_CHECK_START (Section 4.4). Abort will be reported if loss of lock or sleep occurred during a PRBS check operation or those conditions existed when the operation was requested by the host.
8B	EYE_MON_SCAN_SIZE_OUTPUT	STAT_EYE_IMAGE_SIZE	15:0	RO	—	The size in bytes of the last partial scan segment.

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
8C	EYE_MON_SHAPE_OUTPUT_0	STAT_EYE_SHAPE_LEFT_EDGE_OFFSET	15:8	RO	—	Left Edge Voltage Offset returned from shape scan. Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_LEFT_EDGE_PHASE	7:0	RO	—	Left Edge Phase returned from shape scan. Phase values 0 to 127_d.
8D	EYE_MON_SHAPE_OUTPUT_1	STAT_EYE_SHAPE_POS_EDGE_OFFSET	15:8	RO	—	Positive (top) Edge Voltage Offset returned from shape scan. Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_POS_EDGE_PHASE	7:0	RO	—	Positive (top) Edge Phase returned from shape scan. Phase values 0 to 127d.
8E	EYE_MON_SHAPE_OUTPUT_2	STAT_EYE_SHAPE_RIGHT_EDGE_OFFSET	15:8	RO	—	Right Edge Voltage Offset returned from shape scan. Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_RIGHT_EDGE_PHASE	7:0	RO	—	Right Edge Phase returned from shape scan. Phase values 0 to 127_d.
8F	EYE_MON_SHAPE_OUTPUT_3	STAT_EYE_SHAPE_NEG_EDGE_OFFSET	15:8	RO	—	Negative (bottom) Edge Voltage Offset returned from shape scan. Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_NEG_EDGE_PHASE	7:0	RO	—	Negative (bottom) Edge Phase returned from shape scan. Phase values 0 to 127_d.

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
90	EYE_MON_ STATUS	RSVD	15:9	RO	—	Reserved
		STAT_EYE_SCAN_ PARTIAL_OR_FULL	8	RO	—	Full scan status: 0 = Full scan complete. 1 = Partial scan complete. On completion of an eye monitor eye scan (CRTL_EYE_SHAPE_SCAN_B = 0), indicates whether the eye monitor completed the full scan or a partial scan. Undefined for eye shape scan (CTRL_EYE_SHAPE_SCAN_B = 1).
		RSVD	7:2	RO	—	Reserved
		STAT_EYE_MON_ STATUS	1:0	RO	—	Eye monitor status: 0 = Eye monitor idle; ready for new operation 1 = Eye monitor operation in progress 2 = Eye monitor operation completed (success) 3 = Eye monitor operation aborted (error). Part of a four way handshake with CTRL_EYE_MON_START, see Section 4.5 for procedure. Abort will be reported by device if loss of lock or sleep occurred during an eye monitor operation or those conditions existed when the operation was requested by the host.
91 - BF	RSVD	RSVD	15:0	-	—	Reserved

6. Application Information

6.1 Typical Application Circuit

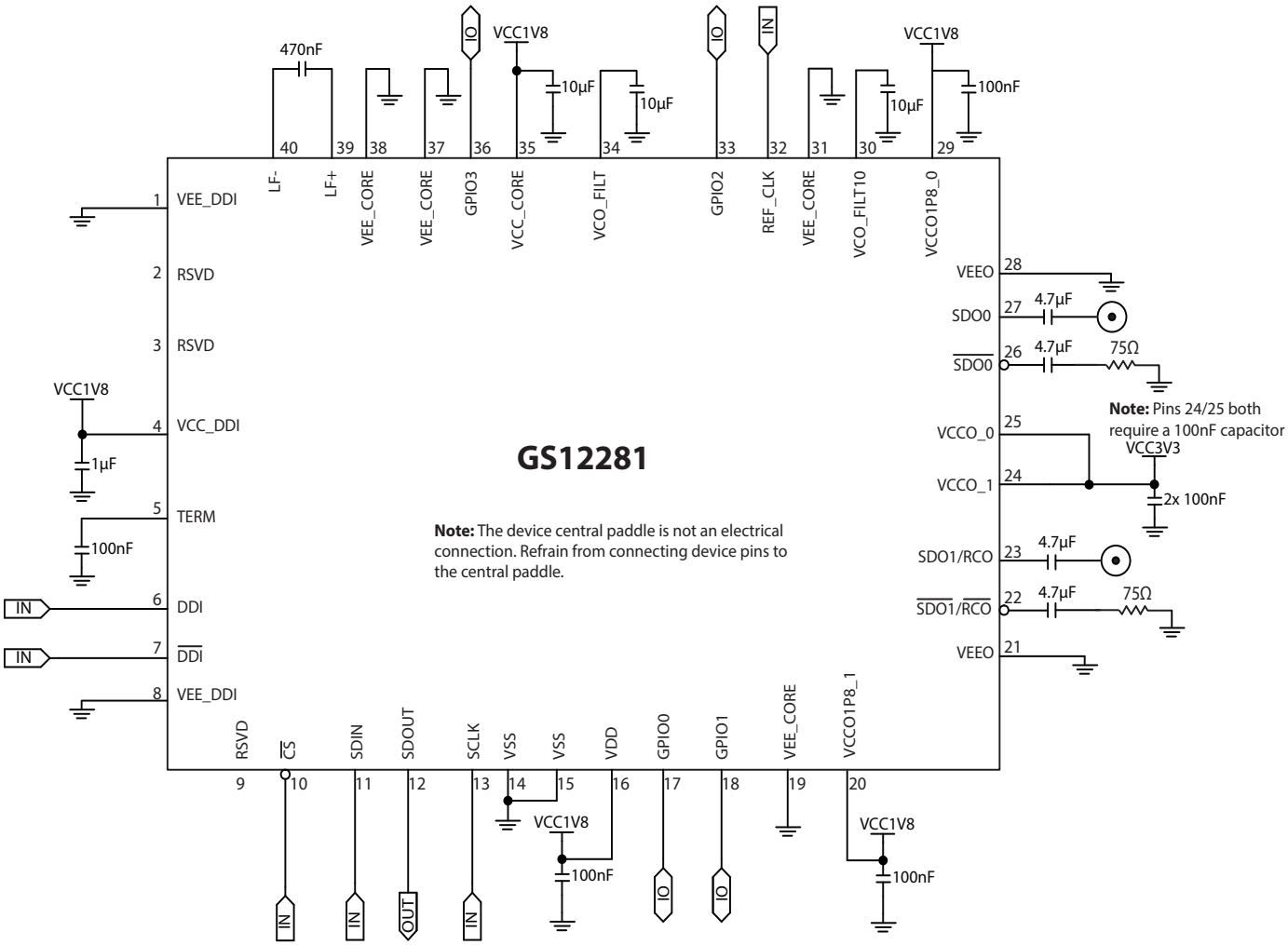


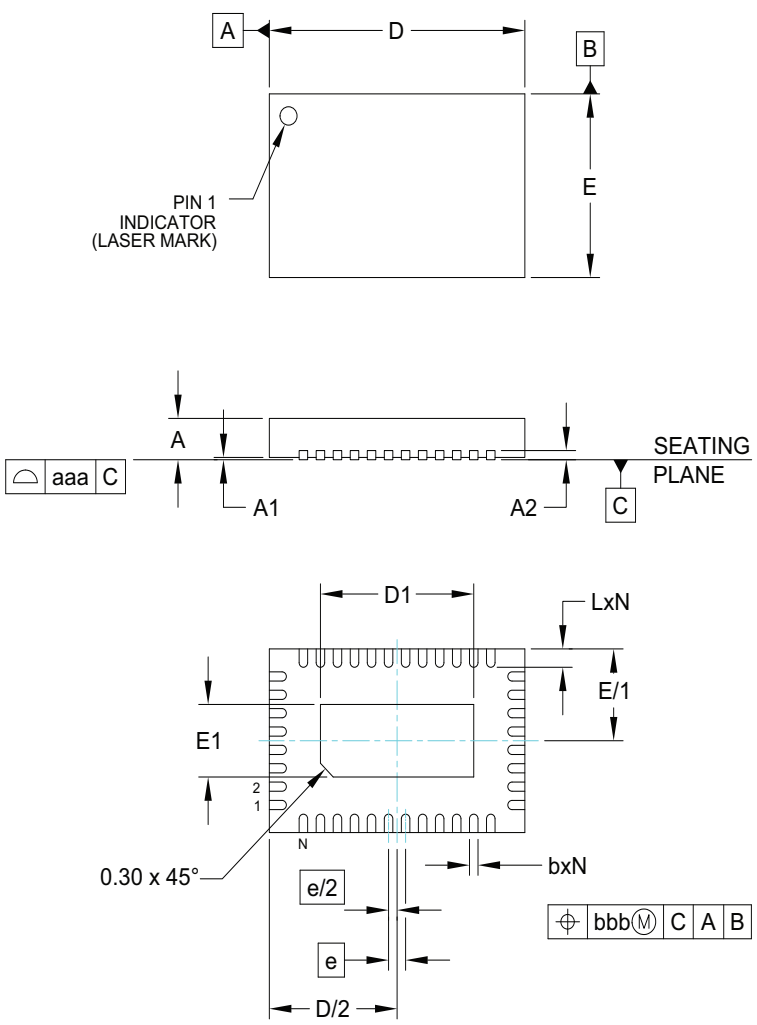
Figure 6-1: Typical Application Circuit

Note 1: 4.7µF AC-coupling capacitors are required on SDO0/$\overline{\text{SDO0}}$ and SDO1/RCO $\overline{\text{SDO1/RCO}}$.

Note 2: It is recommended that separate filtered supplies are used for the following three groups: (VCC_DDI, VCC_CORE), (VCCO1P8_0, VCCO1P8_1, VDD), (VCCO_0, VCCO_1). Multiple devices can share the same filtered supply plane. Contact your local technical representative for layout recommendations to achieve optimal performance.

7. Package & Ordering Information

7.1 Package Dimensions



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.02)	
b	0.15	0.20	0.25
D	5.95	6.00	6.05
D1	3.45	3.60	3.70
E	3.95	4.00	4.05
E1	1.43	1.58	1.68
e	0.40 BSC		
L	0.30	0.40	0.50
N	40		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DIMENSION OF LEAD WIDTH APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.15 to 0.30mm FROM THE TERMINAL TIP.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

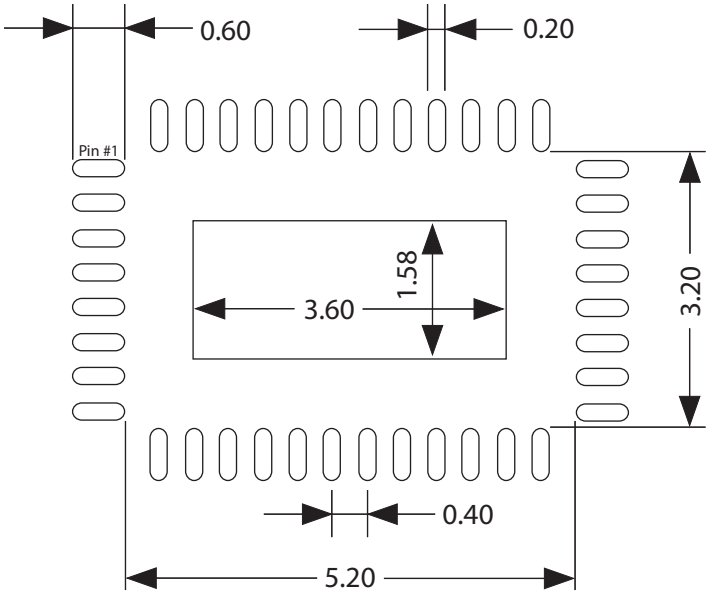


Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 4mm 40-pin QFN
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	40.0°C/W
Junction to Board Thermal Resistance, $\theta_{j\text{-}b}$	32.0°C/W
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	36.0°C/W
Junction-to-Top Characterization Parameter, Psi, Ψ	<1.0°C/W
Pb-free and RoHS compliant	Yes

7.4 Marking Diagram

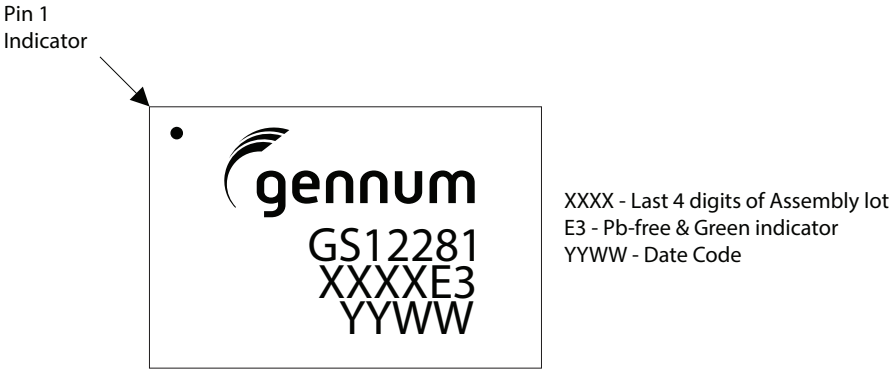


Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

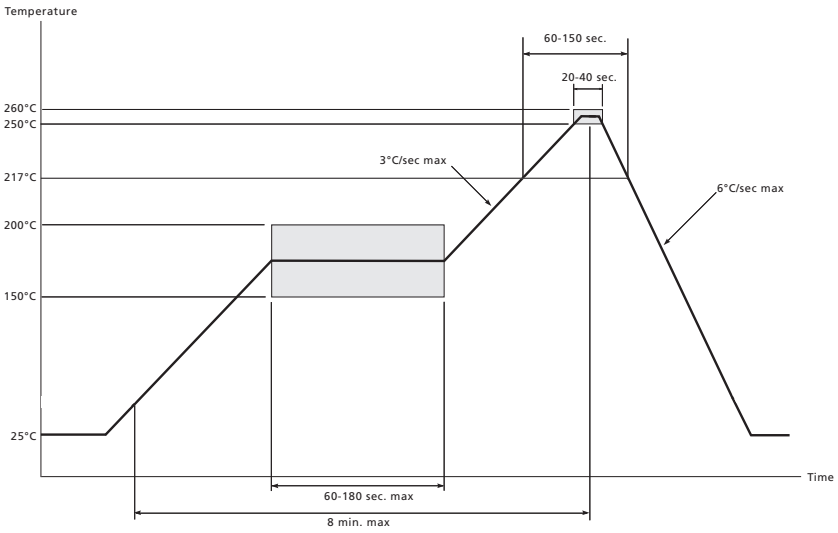


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Minimum Order Quantity	Format
GS12281-INE3	490	Tray
GS12281-INTE3	250	Tape and Reel
GS12281-INTE3Z	2500	Tape and Reel

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9