100-Pin TQFP
Industrial Temp

9Mb Pipelined and Flow Through Synchronous NBT SRAM

333 MHz–150 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization; Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- User-configurable Pipeline and Flow Through mode
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Pin compatible with 2M, 4M, and 18M devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ Pin for automatic power-down
- JEDEC-standard 100-lead TQFP package
- RoHS-compliant 100-lead TQFP package available

Functional Description

The GS880Z18/32/36CT is a 9Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/ single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

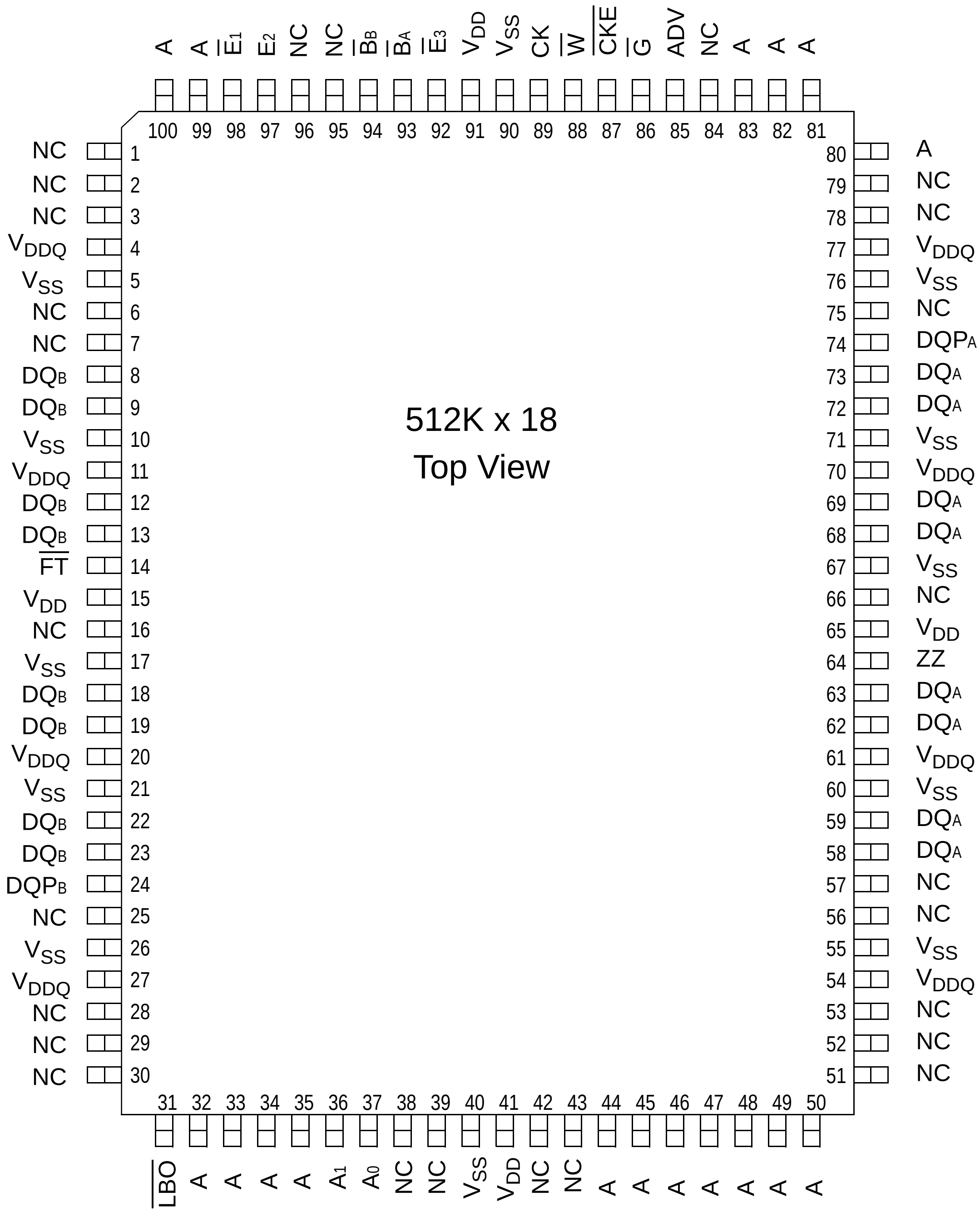
The GS880Z18/32/36CT may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, meaning that in addition to the rising edge triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS880Z18/32/36CT is implemented with GSI's high performance CMOS technology and is available in a JEDEC-standard 100-pin TQFP package.

Parameter Synopsis

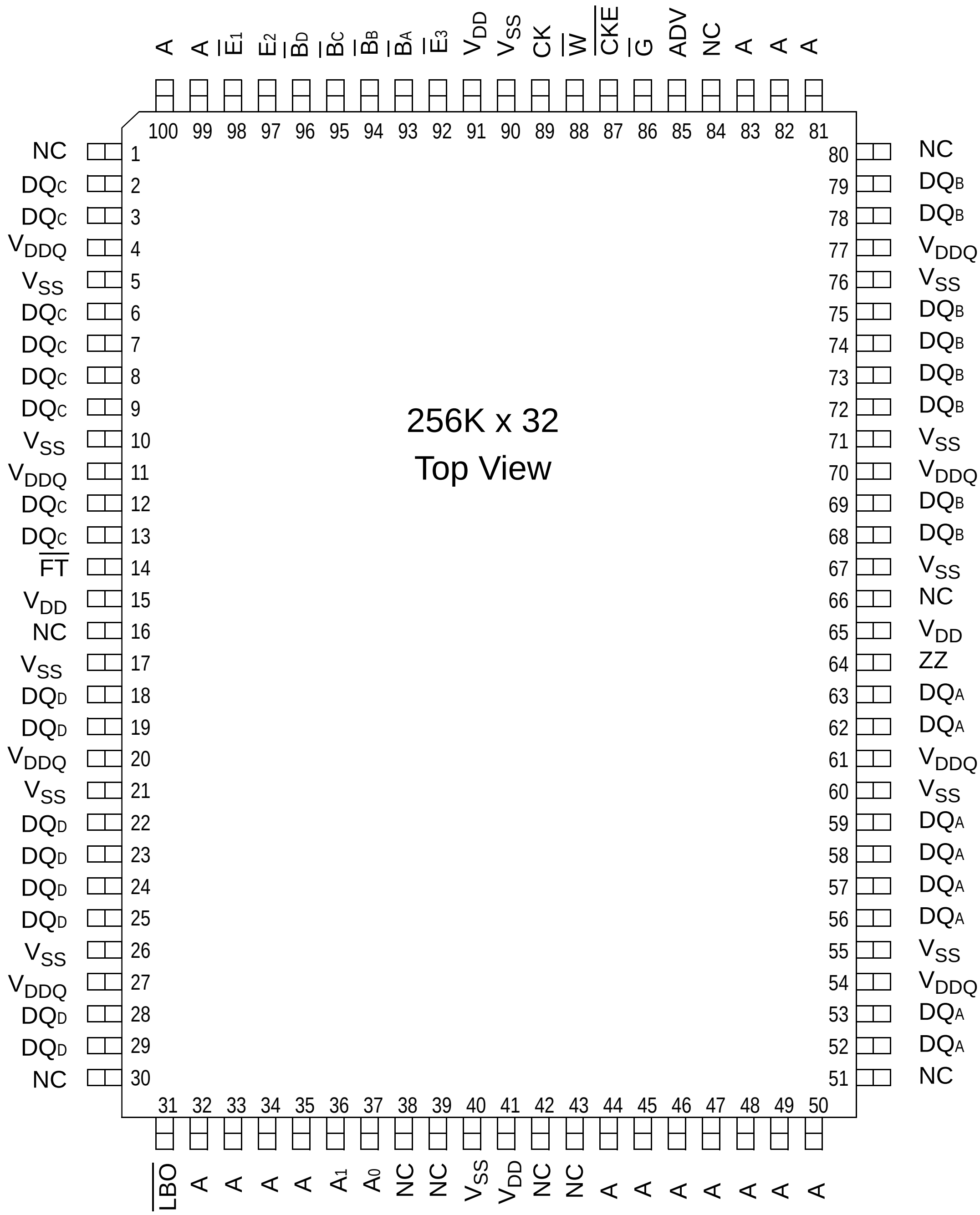
		-333I	-300I	-250I	-200I	-150I	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.5	2.5	3.0	3.8	ns
	tCycle	3.0	3.3	4.0	5.0	6.7	ns
	Curr (x18)	260	245	215	190	160	mA
	Curr (x32/x36)	300	280	245	215	180	mA
Flow Through 2-1-1-1	t_{KQ}	4.5	5.0	5.5	6.5	7.5	ns
	tCycle	4.5	5.0	5.5	6.5	7.5	ns
	Curr (x18)	200	185	180	160	148	mA
	Curr (x32/x36)	225	210	200	180	165	mA

GS880Z18CT 100-Pin TQFP Pinout (Package T)



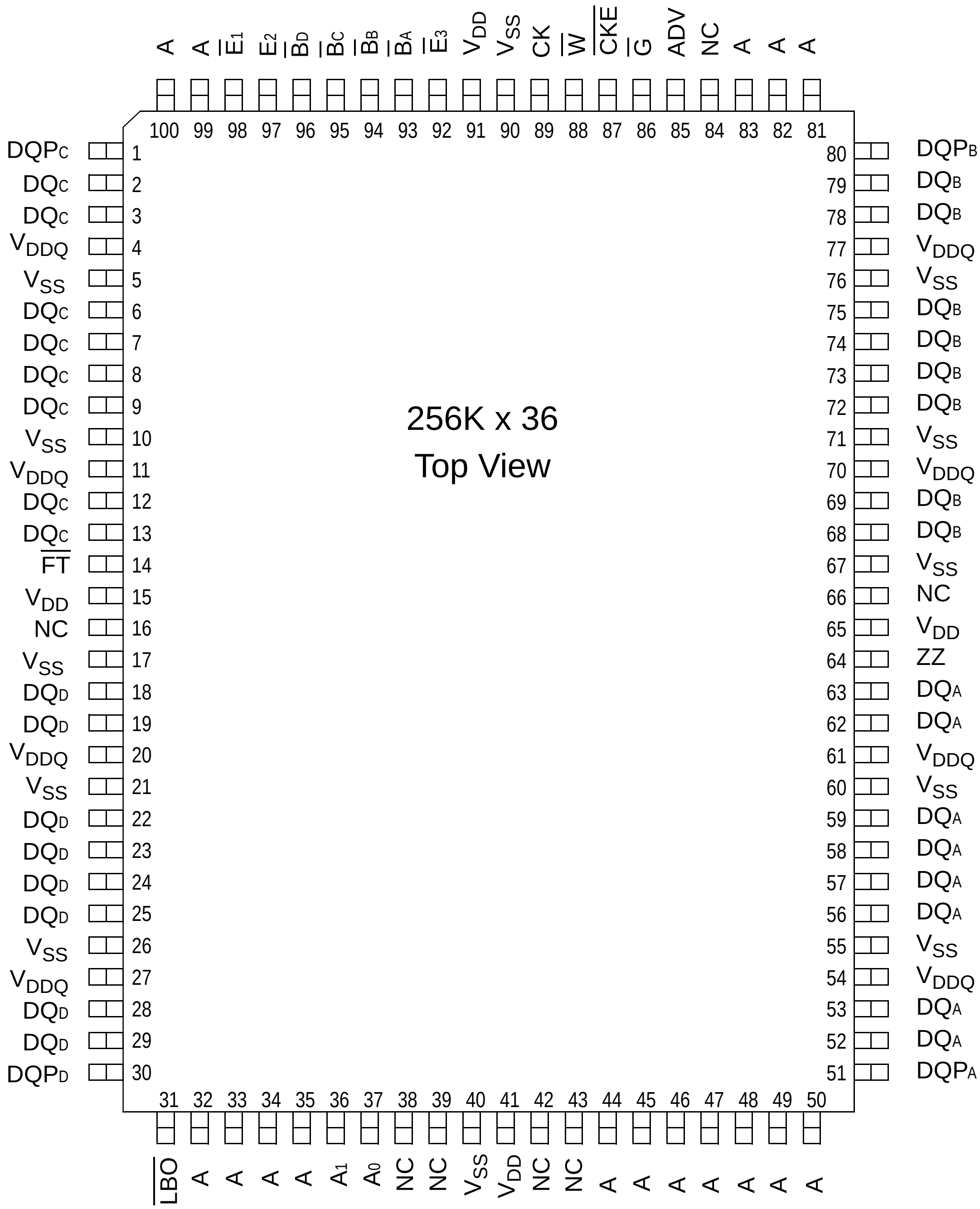
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS880Z32CT 100-Pin TQFP Pinout (Package T)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS880Z36CT 100-Pin TQFP Pinout (Package T)

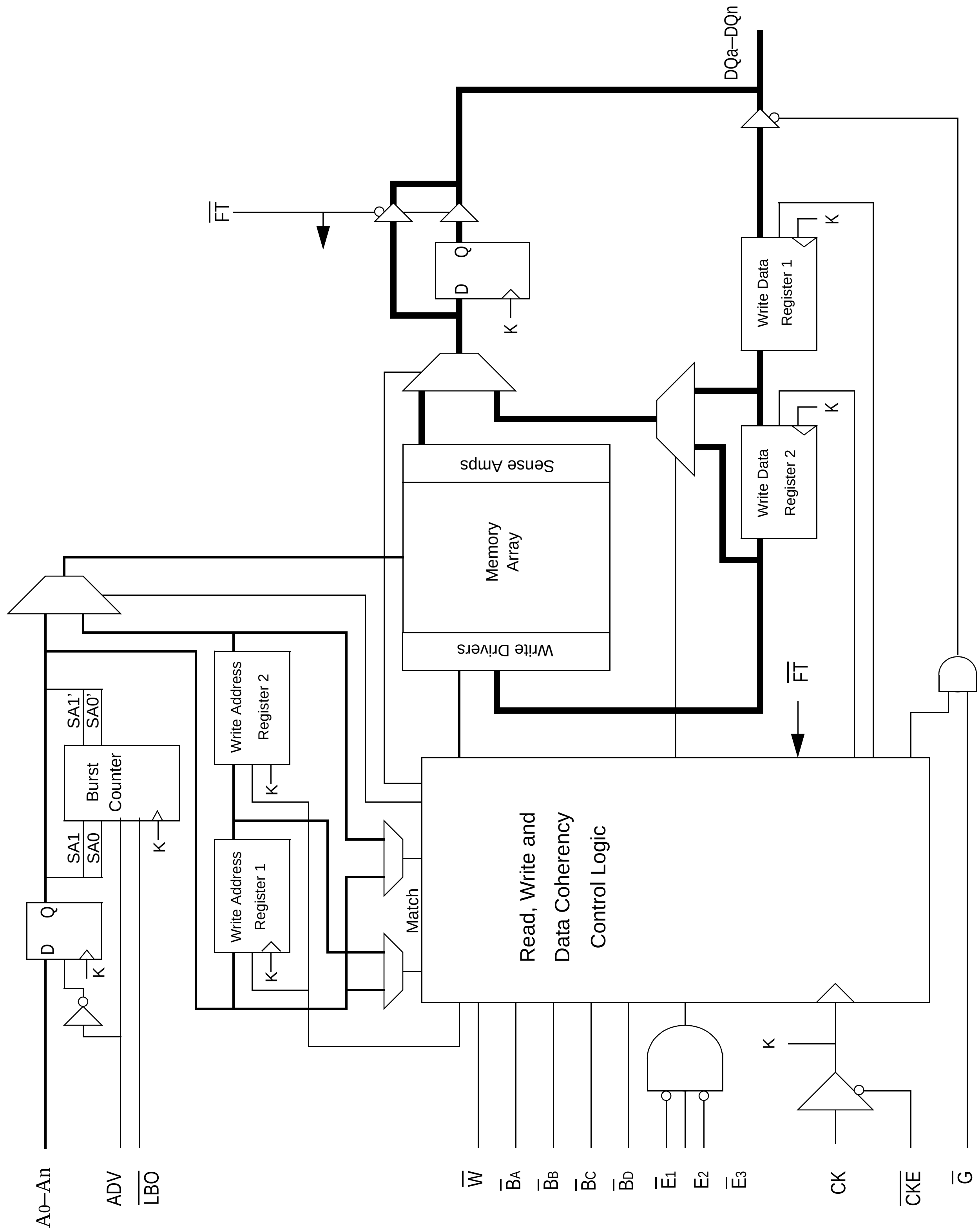


Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

100-Pin TQFP Pin Descriptions

Symbol	Type	Description
A_0, A_1	In	Burst Address Inputs; Preload the burst counter
A	In	Address Inputs
CK	In	Clock Input Signal
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_A; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_B; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_C; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_D; active low
$\overline{W}$	In	Write Enable; active low
$\overline{E}_1$	In	Chip Enable; active low
E_2	In	Chip Enable; Active High. For self decoded depth expansion
$\overline{E}_3$	In	Chip Enable; Active Low. For self decoded depth expansion
$\overline{G}$	In	Output Enable; active low
ADV	In	Advance/$\overline{\text{Load}}$; Burst address counter control pin
$\overline{\text{CKE}}$	In	Clock Input Buffer Enable; active low
NC	—	No Connect
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ_C	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
DQP_A	I/O	9th Data I/O Pin; Byte A
DQP_B	I/O	9th Data I/O Pin; Byte B
DQP_C	I/O	9th Data I/O Pin; Byte C
DQP_D	I/O	9th Data I/O Pin; Byte D
ZZ	In	Power down control; active high
$\overline{\text{FT}}$	In	Pipeline/Flow Through Mode Control; active low
$\overline{\text{LBO}}$	In	Linear Burst Order; active low
V_{DD}	In	Core power supply
V_{SS}	In	Ground
V_{DDQ}	In	Output driver power supply

GS880Z18/32/36C NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{\text{CKE}}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/$\overline{\text{Load}}$ pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2 and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte “a”	L	L	H	H	H
Write Byte “b”	L	H	L	H	H
Write Byte “c”	L	H	H	L	H
Write Byte “d”	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{\text{CKE}}$ is asserted Low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active, and the Write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, & $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

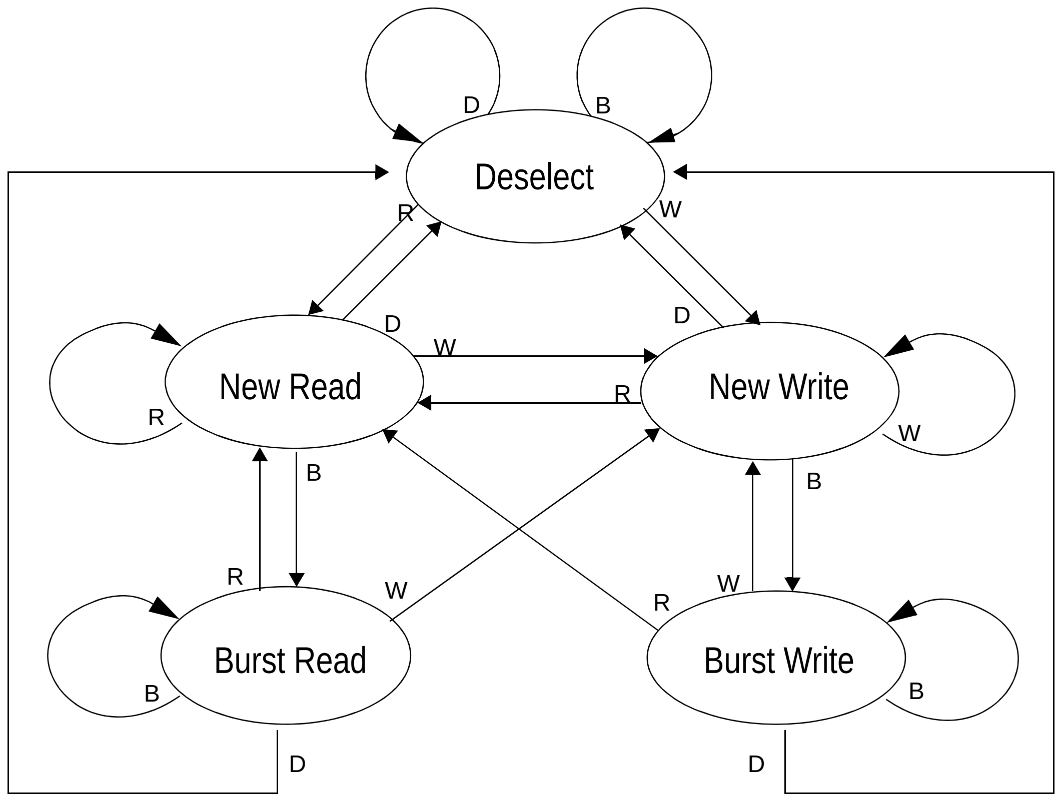
Synchronous Truth Table

Operation	Type	Address	CK	$\overline{\text{CKE}}$	ADV	$\overline{\text{W}}$	$\overline{\text{Bx}}$	$\overline{\text{E}}$1	E2	$\overline{\text{E}}$3	$\overline{\text{G}}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,10
NOP/Read, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	2
Dummy Read, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Abort, Begin Burst	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Write Cycle, Continue Burst	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,3,10
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3,10
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

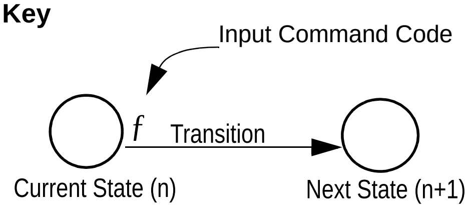
Notes:

1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{\text{W}}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
3. $\overline{\text{G}}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{\text{CKE}}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{\text{CKE}}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{\text{Bx}}$ = High = All Byte Write signals are high; $\overline{\text{Bx}}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{\text{G}}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{\text{CKE}}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

Pipeline and Flow Through Read Write Control State Diagram

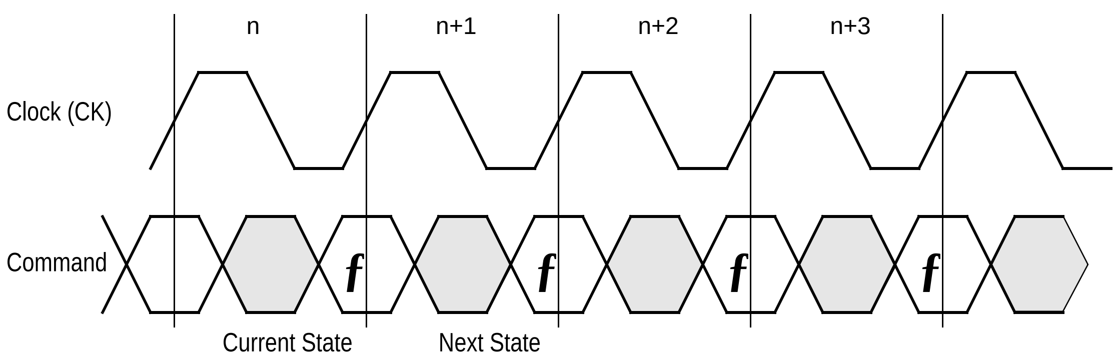


Key



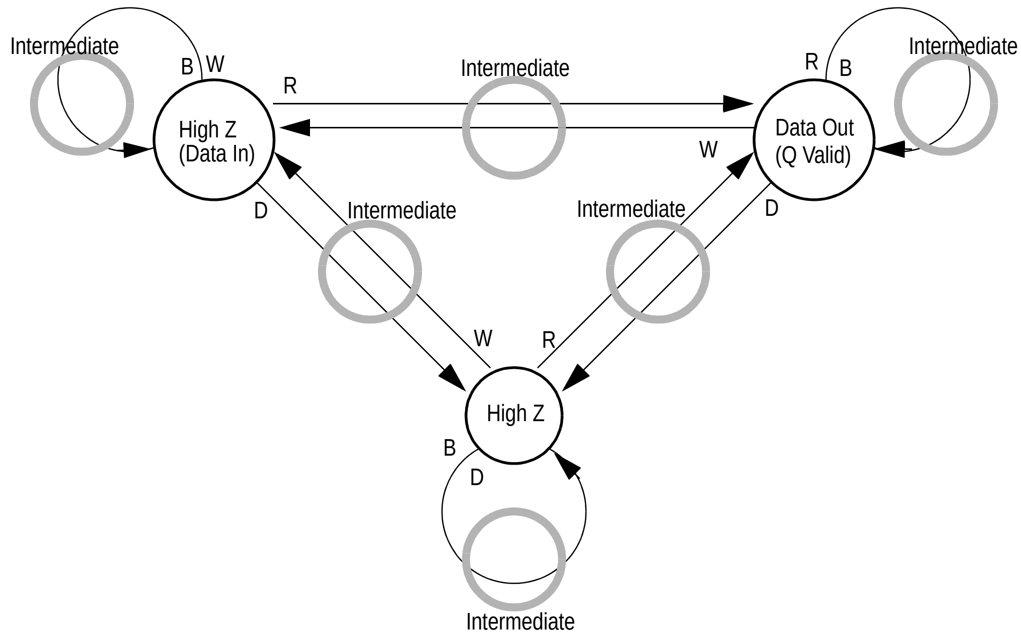
Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B and D represent input command codes, as indicated in the Synchronous Truth Table.



Current State and Next State Definition for Pipeline and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram



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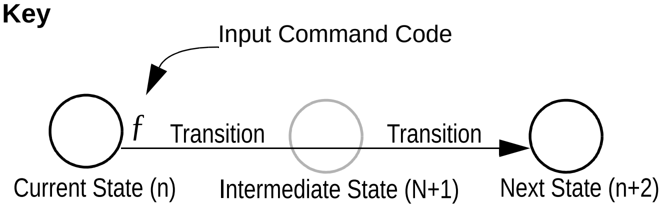
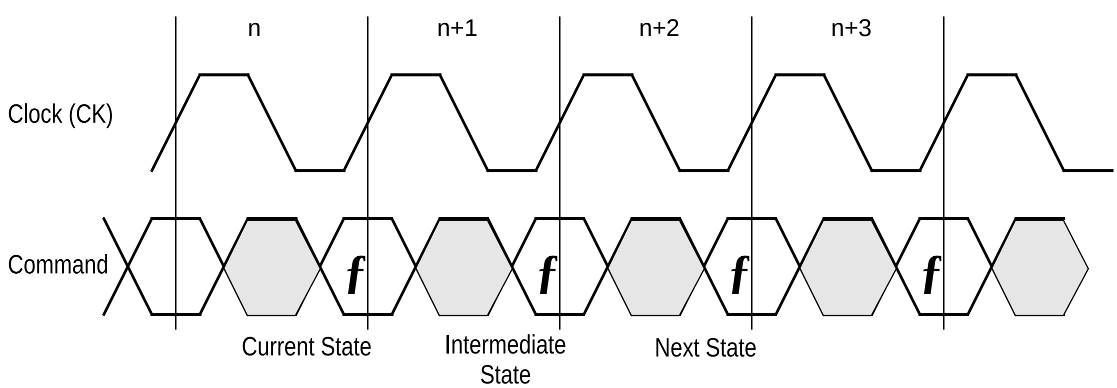


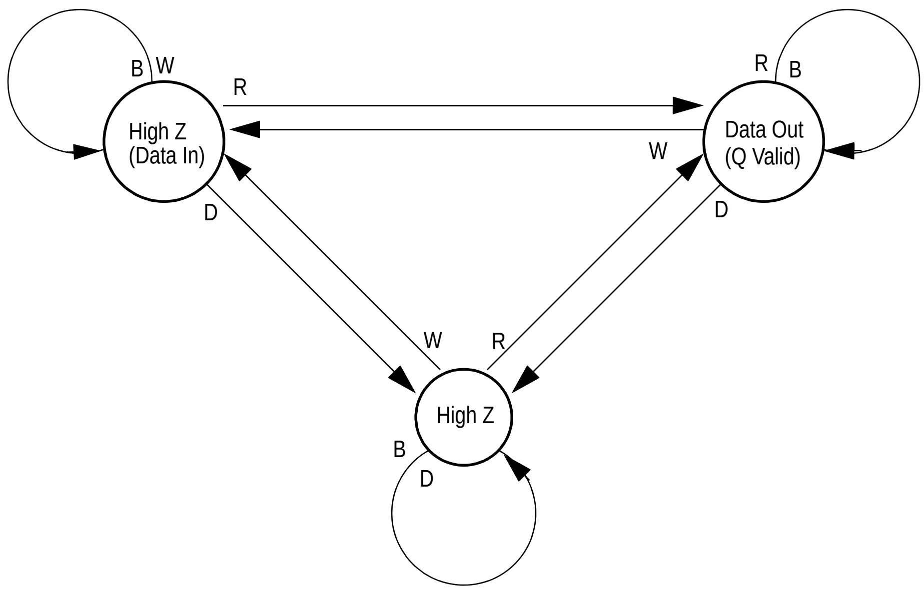
Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

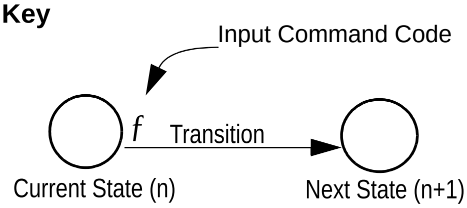


Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram



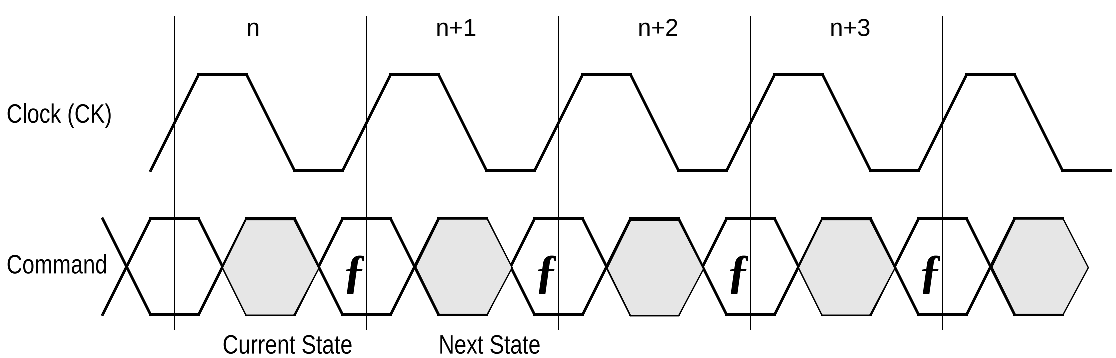
Key



Notes

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.

2. W, R, B and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{\text{LBO}}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

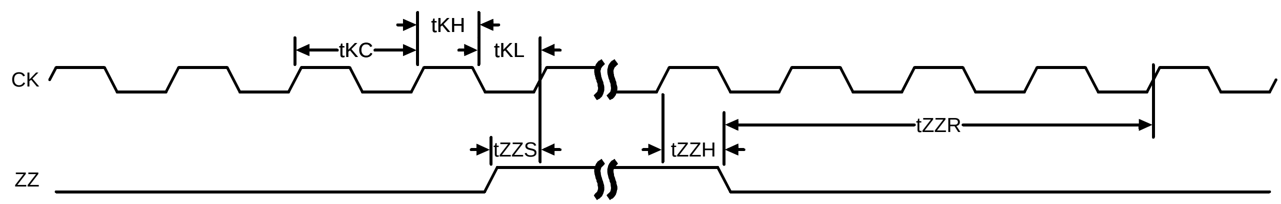
Note:
The burst counter wraps to initial state on the 5th clock.

Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a deselect or read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipeline mode via the $\overline{FT}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	^oC
T_{BIAS}	Temperature Under Bias	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{DD} Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.8	V
V_{DDQ} Input High Voltage	V_{IHQ}	2.0	—	V_{DDQ} + 0.3	V
V_{DDQ} Input Low Voltage	V_{ILQ}	–0.3	—	0.8	V

Note:
V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{DD} Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V
V_{DDQ} Input High Voltage	V_{IHQ}	0.6*V_{DD}	—	V_{DDQ} + 0.3	V
V_{DDQ} Input Low Voltage	V_{ILQ}	–0.3	—	0.3*V_{DD}	V

Note:
V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Temperature (Industrial Range Versions)*	T_A	–40	25	85	°C

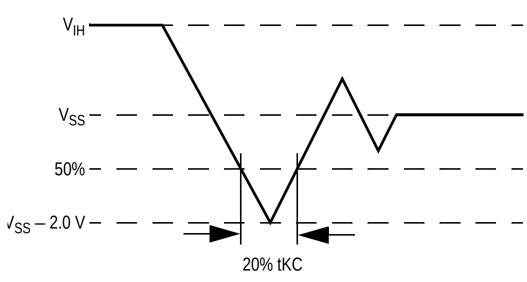
Note:
The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

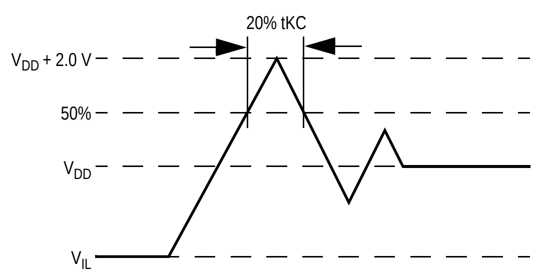
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100 TQFP	4-layer	38.7	33.5	31.9	27.6	10.6

Notes:
1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

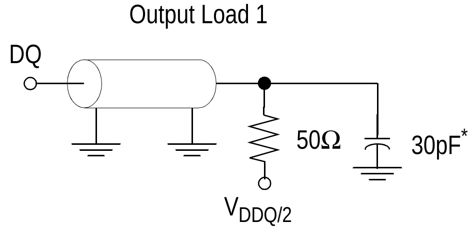
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode		Symbol	-333I	-300I	-250I	-200I	-150I	Unit
					–40 to 85°C	–40 to 85°C	–40 to 85°C	–40 to 85°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/x36)	Pipeline	I_{DD} I_{DDQ}	260 40	245 35	215 30	190 25	160 20	mA
			Flow Through	I_{DD} I_{DDQ}	200 25	185 25	175 25	160 20	150 15	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	240 20	225 20	200 15	175 15	150 10	mA
			Flow Through	I_{DD} I_{DDQ}	185 15	170 15	165 15	150 10	140 8	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	45	45	45	45	45	mA
			Flow Through	I_{SB}	45	45	45	45	45	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	90	85	85	85	80	mA
			Flow Through	I_{DD}	90	85	85	85	80	mA

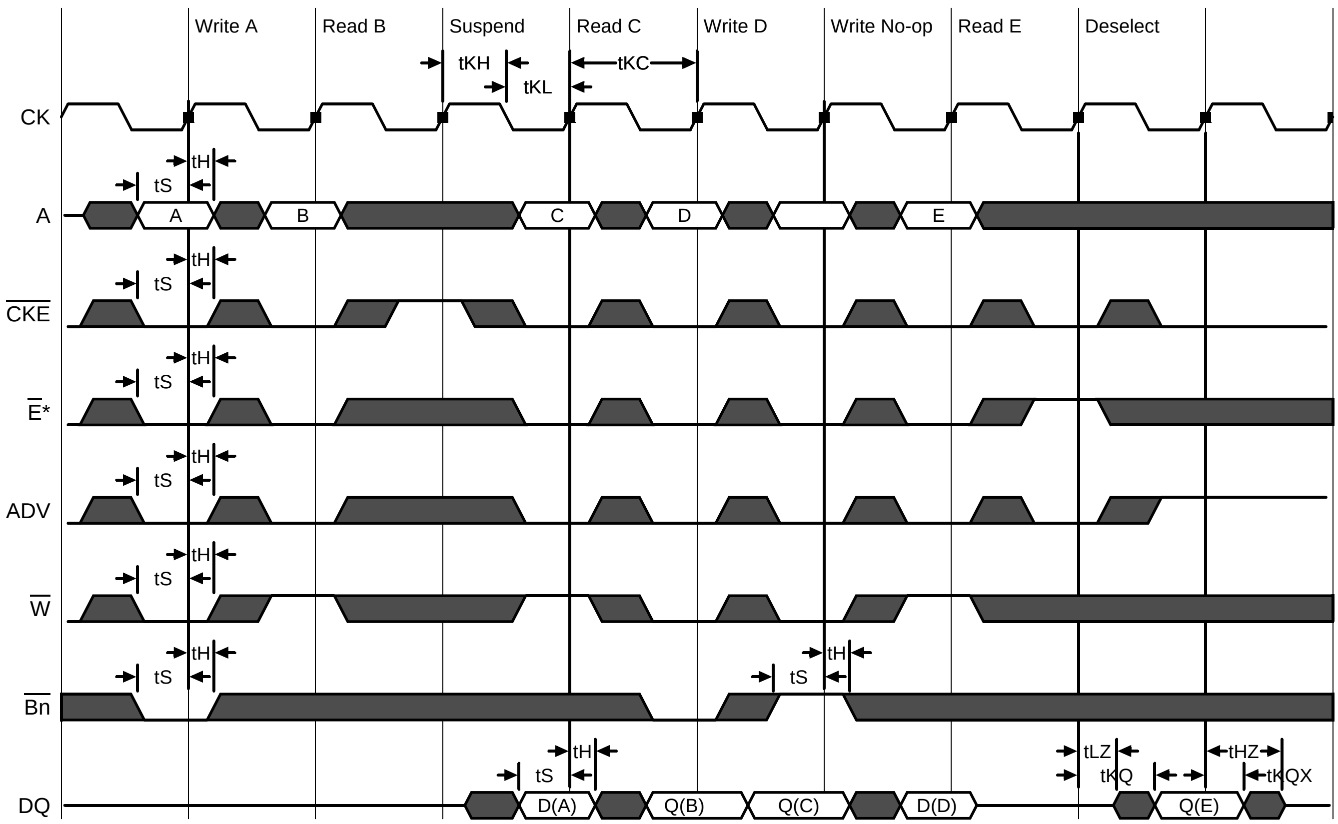
Notes:
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

AC Electrical Characteristics

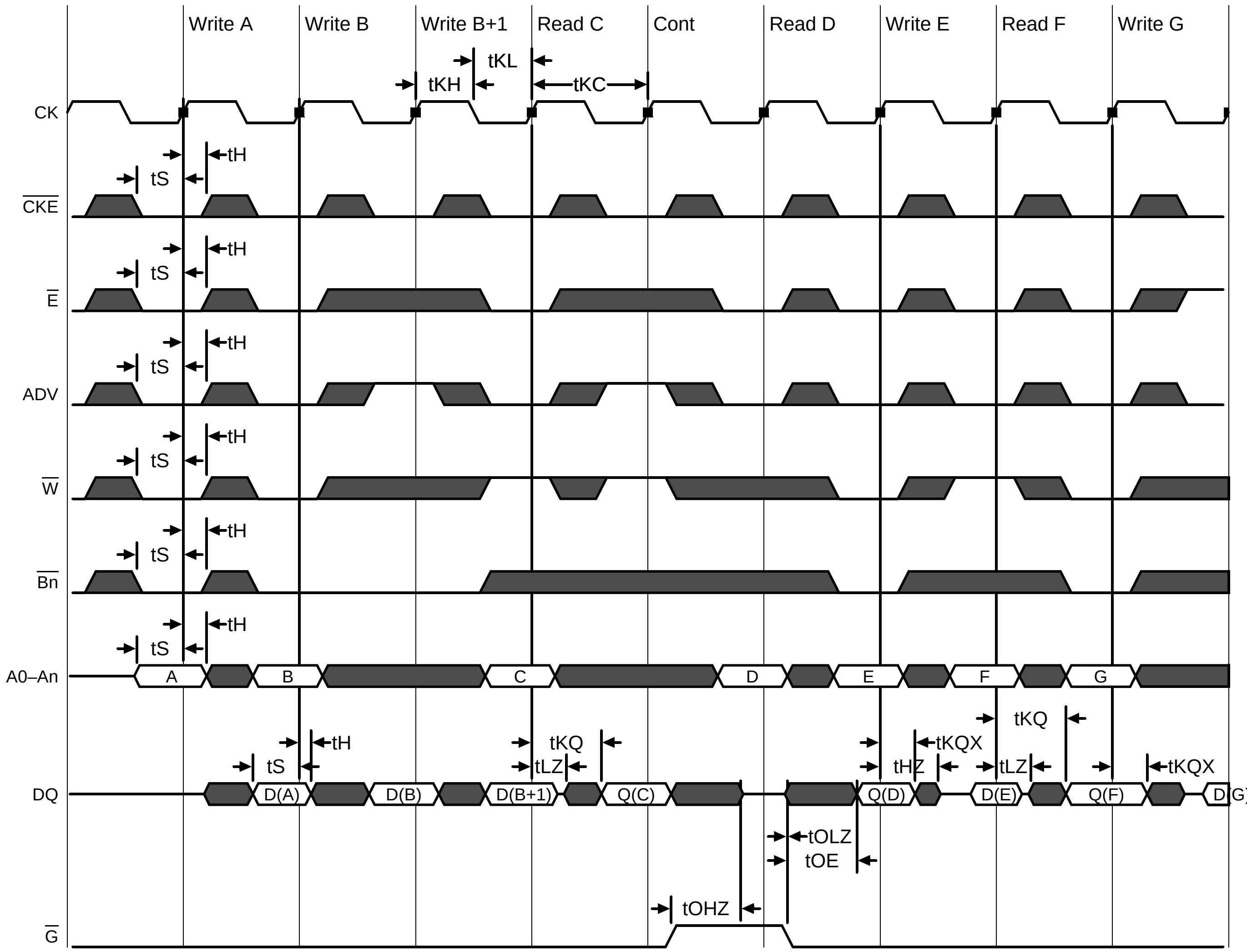
	Parameter	Symbol	-333I		-300I		-250I		-200I		-150I		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	3.0	—	3.3	—	4.0	—	5.0	—	6.7	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.5	—	2.5	—	3.0	—	3.8	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	1.0	—	1.0	—	1.2	—	1.4	—	1.5	—	ns
	Hold time	tH	0.1	—	0.1	—	0.2	—	0.4	—	0.5	—	ns
Flow Through	Clock Cycle Time	tKC	4.5	—	5.0	—	5.5	—	6.5	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	4.5	—	5.0	—	5.5	—	6.5	—	7.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Setup time	tS	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.0	—	1.0	—	1.3	—	1.3	—	1.5	—	ns
	Clock LOW Time	tKL	1.2	—	1.2	—	1.5	—	1.5	—	1.7	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	2.5	1.5	2.5	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	2.5	—	2.5	—	3.0	—	3.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	2.5	—	2.5	—	3.0	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing (NBT)



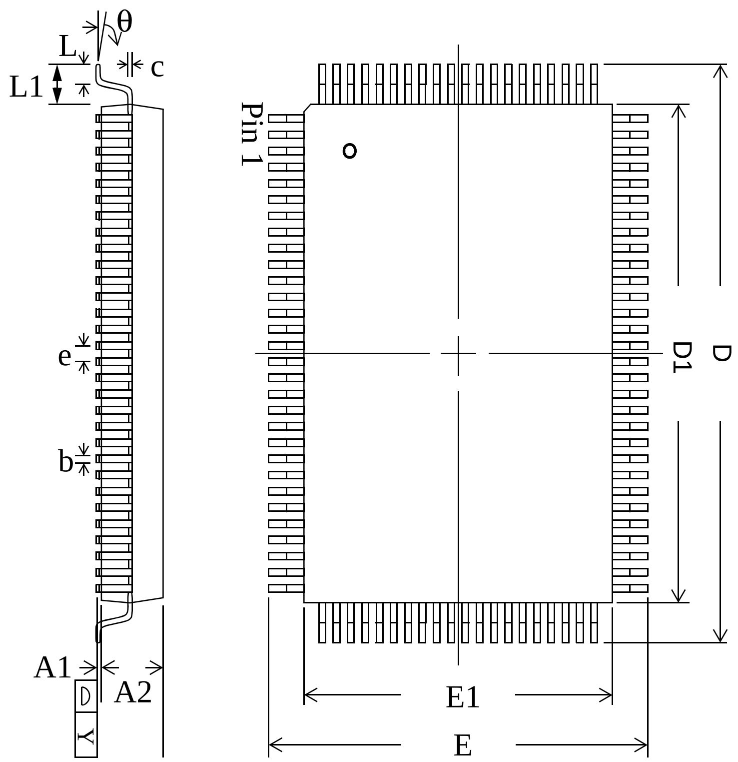
Flow Through Mode Timing (NBT)



*Note: E = High(False) if E1 = 1 or E2 = 0 or E3 = 1

TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Voltage Option	Package	Speed[2] (MHz/ns)	T_A[3]
512K x 18	GS880Z18CT-333I	NBT	3.3 V or 2.5 V	TQFP	333/4.5	I
512K x 18	GS880Z18CT-300I	NBT	3.3 V or 2.5 V	TQFP	300/5	I
512K x 18	GS880Z18CT-250I	NBT	3.3 V or 2.5 V	TQFP	250/5.5	I
512K x 18	GS880Z18CT-200I	NBT	3.3 V or 2.5 V	TQFP	200/6.5	I
512K x 18	GS880Z18CT-150I	NBT	3.3 V or 2.5 V	TQFP	150/7.5	I
256K x 32	GS880Z32CT-333I	NBT	3.3 V or 2.5 V	TQFP	333/4.5	I
256K x 32	GS880Z32CT-300I	NBT	3.3 V or 2.5 V	TQFP	300/5	I
256K x 32	GS880Z32CT-250I	NBT	3.3 V or 2.5 V	TQFP	250/5.5	I
256K x 32	GS880Z32CT-200I	NBT	3.3 V or 2.5 V	TQFP	200/6.5	I
256K x 32	GS880Z32CT-150I	NBT	3.3 V or 2.5 V	TQFP	150/7.5	I
256K x 36	GS880Z36CT-333I	NBT	3.3 V or 2.5 V	TQFP	333/4.5	I
256K x 36	GS880Z36CT-300I	NBT	3.3 V or 2.5 V	TQFP	300/5	I
256K x 36	GS880Z36CT-250I	NBT	3.3 V or 2.5 V	TQFP	250/5.5	I
256K x 36	GS880Z36CT-200I	NBT	3.3 V or 2.5 V	TQFP	200/6.5	I
256K x 36	GS880Z36CT-150I	NBT	3.3 V or 2.5 V	TQFP	150/7.5	I
512K x 18	GS880Z18CGT-333I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	333/4.5	I
512K x 18	GS880Z18CGT-300I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	300/5	I
512K x 18	GS880Z18CGT-250I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	250/5.5	I
512K x 18	GS880Z18CGT-200I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	200/6.5	I
512K x 18	GS880Z18CGT-150I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	150/7.5	I
256K x 32	GS880Z32CGT-333I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	333/4.5	I
256K x 32	GS880Z32CGT-300I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	300/5	I
256K x 32	GS880Z32CGT-250I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	250/5.5	I
256K x 32	GS880Z32CGT-200I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	200/6.5	I
256K x 32	GS880Z36CGT-150I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	150/7.5	I
256K x 36	GS880Z36CGT-333I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	333/4.5	I
256K x 36	GS880Z36CGT-300I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	300/5	I
256K x 36	GS880Z36CGT-250I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	250/5.5	I
256K x 36	GS880Z36CGT-200I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	200/6.5	I
256K x 36	GS880Z36CGT-150I	NBT	3.3 V or 2.5 V	RoHS-compliant TQFP	150/7.5	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS880Z18CT-150IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

9Mb Sync SRAM Data Sheet Revision History

File Name	Types of Changes Format or Content	Revision
880Z18C_r1		• Creation of new datasheet
880Z18C_r1_01	Content	• Update to MP datasheet
880Z18C_r1_02	Content	• Updated Absolute Maximum Ratings • Deleted conditional text
880Z18C_r1_03	Content	• Updated Absolute Maximum Ratings • Added thermal information • Updated Ordering Information
880Z18C_r1_04	Content	• Updated Absolute Maximum Ratings • Removed all Comm Temp references

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