

**ZXMP6A16DN8**

**DUAL P-CHANNEL 60V ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON) Max}$	Package	$I_D$ $T_A = +25^\circ C$ (Notes 4 & 6)
-60V	85mΩ @ $V_{GS} = -10V$	SO-8	-3.9A
	125mΩ @ $V_{GS} = -4.5V$		-3.2A

**Features**

- Low On-Resistance
- Fast Switching Speed
- Low Threshold
- Low Gate Drive
- Low Profile SOIC Package
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Description**

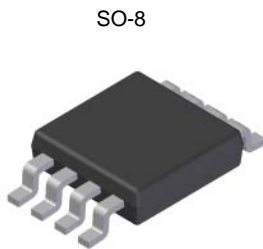
This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

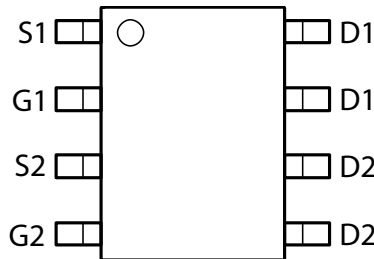
- DC-DC Converters
- Power Management Functions
- Disconnect Switches
- Motor Control

**Mechanical Data**

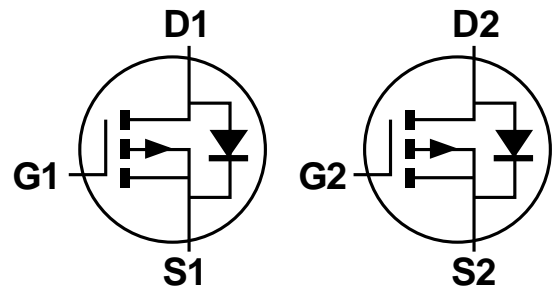
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish; Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)



Top View



Top View



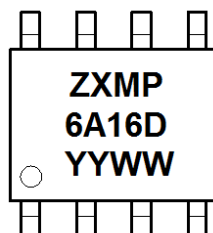
Equivalent Circuit

**Ordering Information**

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMP6A16DN8TA	ZXMP6A16D	7	12	500

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

**Marking Information**



ZXMP6A16D = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Year (ex: 11 = 2011)  
WW = Week (01 - 53)

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

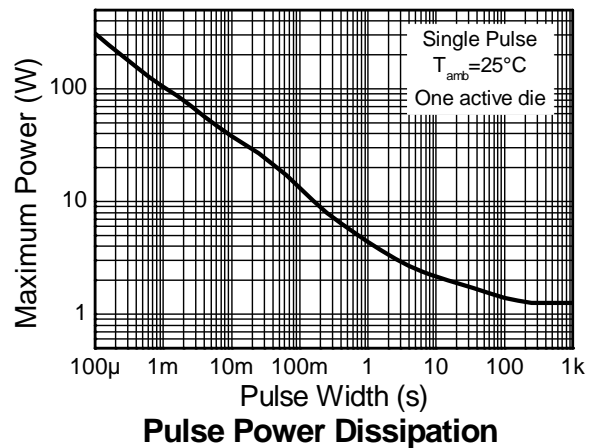
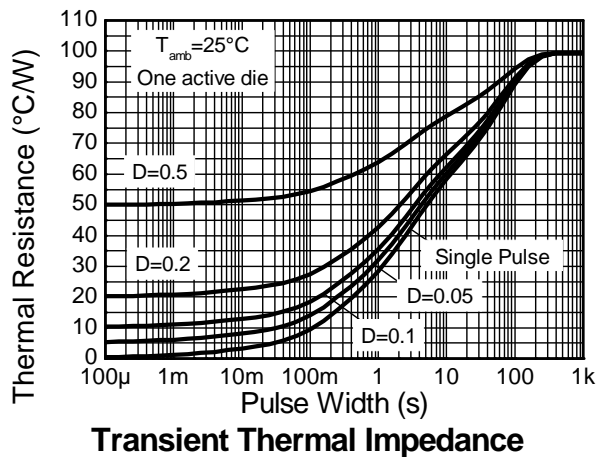
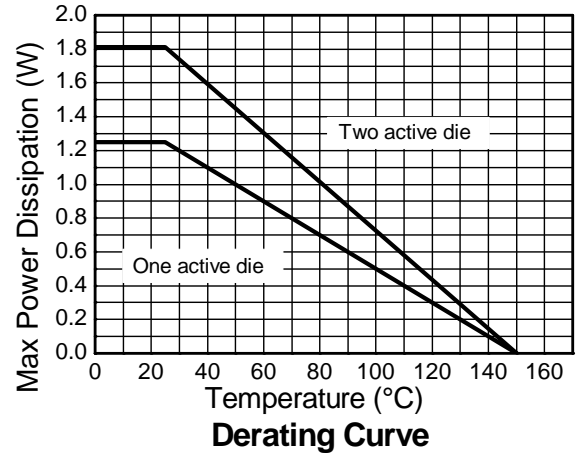
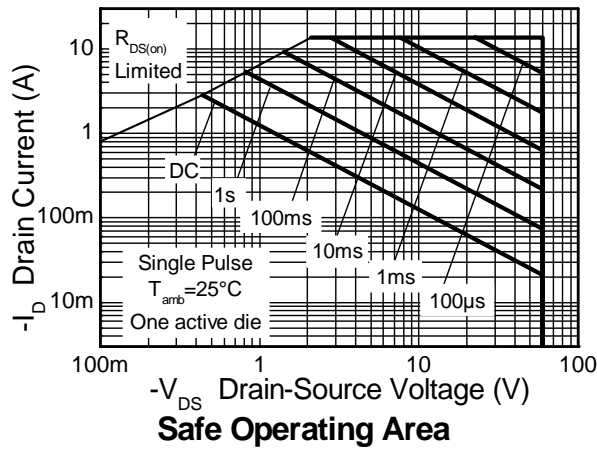
Characteristic		Symbol	Value	Unit
Drain-Source voltage		$V_{DSS}$	-60	V
Gate-Source voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain current	$V_{GS} = 10\text{V}$	(Notes 6 & 8)	-3.9	A
		$T_A = +70^\circ\text{C}$ (Notes 6 & 8)	-3.1	
		(Notes 5 & 8)	-2.9	
Pulsed Drain current		$I_{DM}$	-18.3	A
Continuous Source current (Body diode)		$I_S$	-3.2	A
Pulsed Source current (Body diode)		$I_{SM}$	-18.3	A

**Thermal Characteristics**

Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Notes 5 & 8)	$P_D$	1.25	W mW/ $^\circ\text{C}$
	(Notes 5 & 9)		10.0	
	(Notes 6 & 8)		1.81 14.5	
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	2.15 17	$^\circ\text{C/W}$
	(Notes 5 & 9)		100	
	(Notes 6 & 8)		70 60	
Thermal Resistance, Junction to Lead	(Notes 8 & 10)	$R_{\theta JL}$	48.85	
Operating and storage temperature range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

- Notes:
- AEC-Q101  $V_{GS}$  maximum is  $\pm 16\text{V}$ .
  - For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  - Same as note (5), except the device is measured at  $t \leq 10$  sec.
  - Same as note (5), except the device is pulsed with  $D = 0.02$  and pulse width 300 $\mu\text{s}$ .
  - For a dual device with one active die.
  - For a device with two active die running at equal power.
  - Thermal resistance from junction to solder-point.

**Thermal Characteristics**



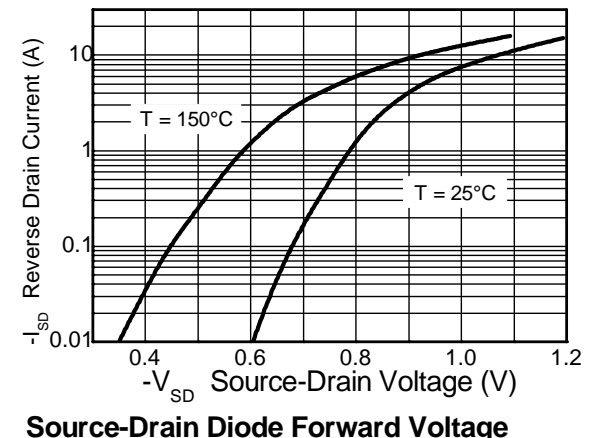
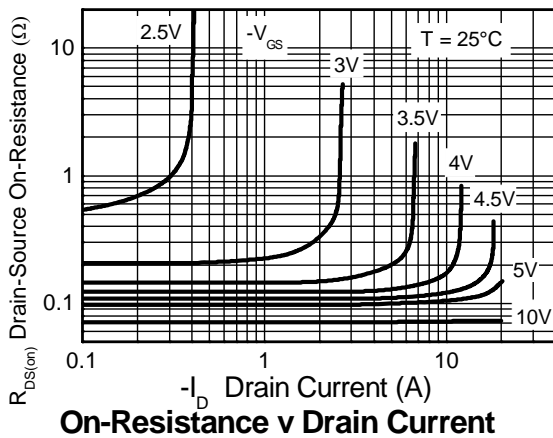
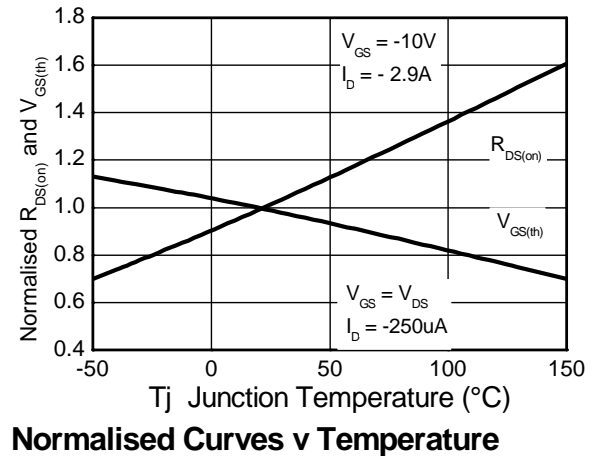
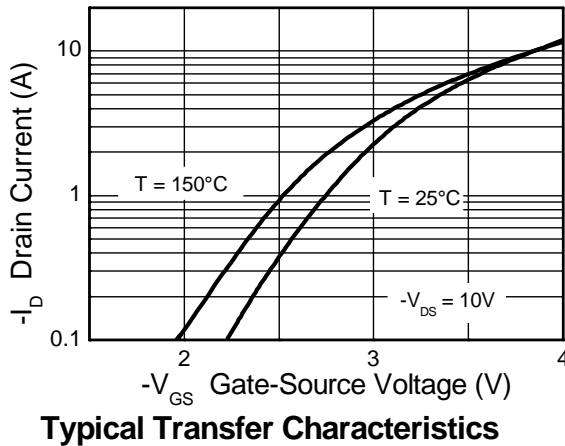
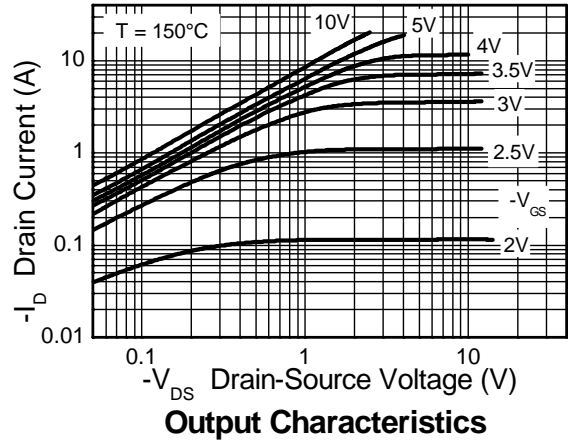
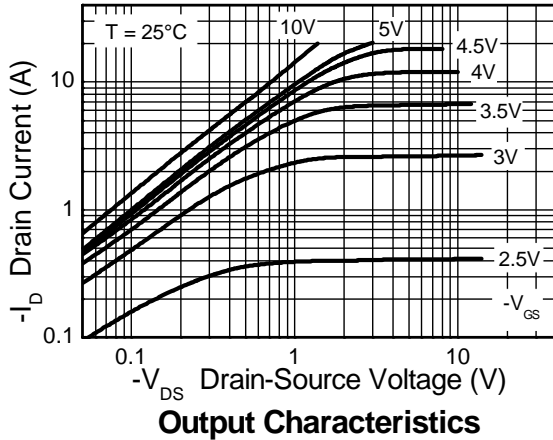
**ZXMP6A16DN8**

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

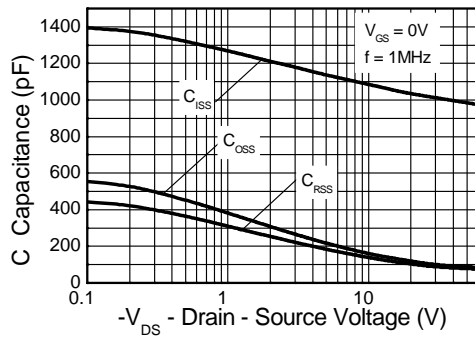
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
<b>OFF CHARACTERISTICS</b>							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-60	—	—	V	I <sub>D</sub> = -250μA, V <sub>GS</sub> = 0V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1.0	μA	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	
<b>ON CHARACTERISTICS</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	—	—	V	I <sub>D</sub> = -250μA, V <sub>DS</sub> = V <sub>GS</sub>	
Static Drain-Source On-Resistance (Note 11)	R <sub>DS(on)</sub>	—	—	85	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -2.9A	
			—	125		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.4A	
Forward Transconductance (Notes 11 & 12)	g <sub>fs</sub>	—	7.2	—	S	V <sub>DS</sub> = -15V, I <sub>D</sub> = -2.9A	
Diode Forward Voltage (Note 11)	V <sub>SD</sub>	—	-0.85	-0.95	V	I <sub>S</sub> = -3.4A, V <sub>GS</sub> = 0V, T <sub>J</sub> = +25°C	
Reverse recovery time (Note 12)	t <sub>rr</sub>	—	29.2	—	ns	I <sub>S</sub> = -2A, di/dt = 100A/μs,	
Reverse recovery charge (Note 12)	Q <sub>rr</sub>	—	39.6	—	nC	T <sub>J</sub> = +25°C	
<b>DYNAMIC CHARACTERISTICS (Note 12)</b>							
Input Capacitance	C <sub>iss</sub>	—	1021	—	pF	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1MHz	
Output Capacitance	C <sub>oss</sub>	—	83.1	—	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	56.4	—	pF		
Total Gate Charge (Note 13)	Q <sub>g</sub>	—	12.1	—	nC	V <sub>GS</sub> = -5V	V <sub>DS</sub> = -30V, I <sub>D</sub> = -2.9A
Total Gate Charge (Note 13)	Q <sub>g</sub>	—	24.2	—	nC	V <sub>GS</sub> = -10V	
Gate-Source Charge (Note 13)	Q <sub>gs</sub>	—	2.5	—	nC		
Gate-Drain Charge (Note 13)	Q <sub>gd</sub>	—	3.7	—	nC		
Turn-On Delay Time (Note 13)	t <sub>D(on)</sub>	—	3.5	—	ns	V <sub>DD</sub> = -30V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A, R <sub>G</sub> ≅ 6.0Ω	
Turn-On Rise Time (Note 13)	t <sub>r</sub>	—	4.1	—	ns		
Turn-Off Delay Time (Note 13)	t <sub>D(off)</sub>	—	35	—	ns		
Turn-Off Fall Time (Note 13)	t <sub>f</sub>	—	10	—	ns		

- Notes:
11. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
  12. For design aid only, not subject to production testing.
  13. Switching characteristics are independent of operating junction temperatures.

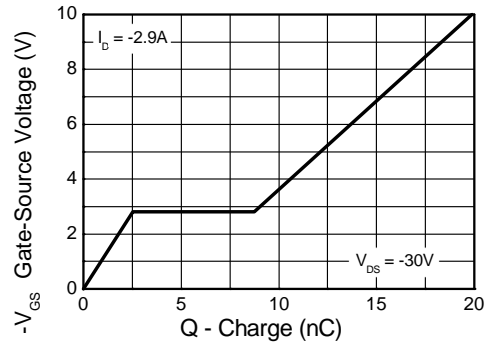
**Typical Characteristics**



**Typical Characteristics (cont.)**

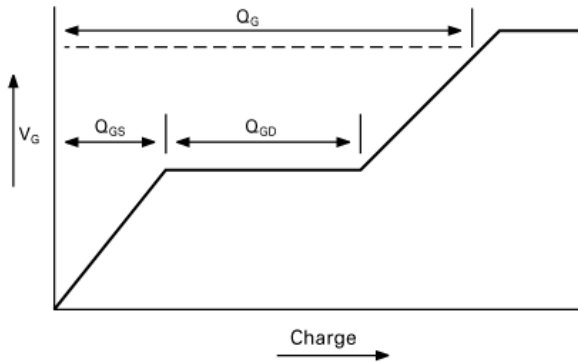


**Capacitance v Drain-Source Voltage**

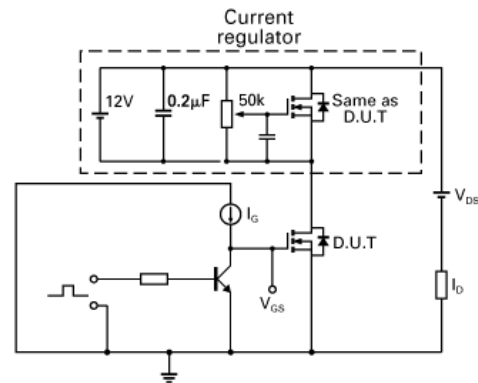


**Gate-Source Voltage v Gate Charge**

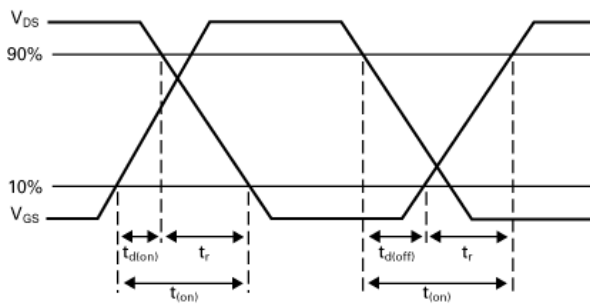
**Test Circuits**



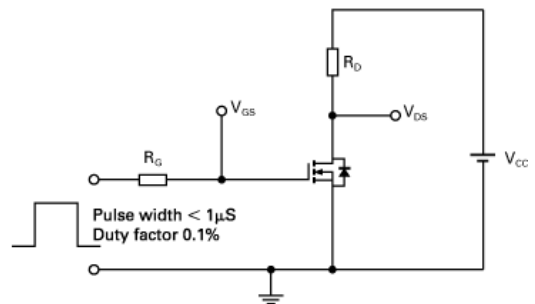
**Basic gate charge waveform**



**Gate charge test circuit**

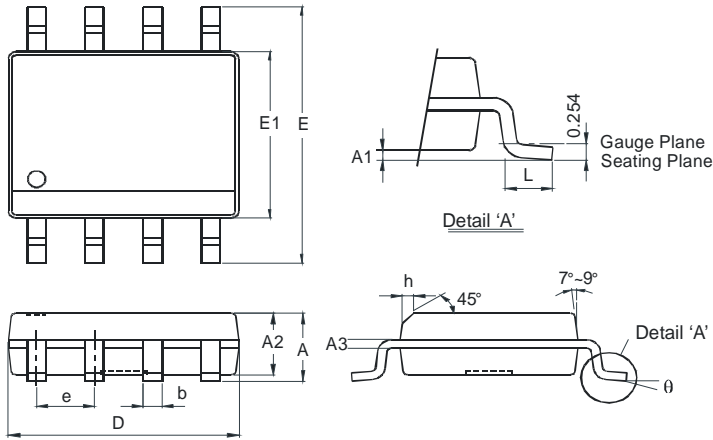


**Switching time waveforms**



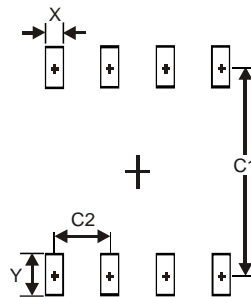
**Switching time test circuit**

**Package Outline Dimensions**



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

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