74AHCT245A

Octal bus transceiver; 3-state

Rev. 2 — 26 October 2016

Product data sheet

General description 1.

The 74AHCT245A is an 8-bit transceiver with 3-state outputs. The device features an output enable (OE) and send/receive (DIR) for direction control. A HIGH on OE causes the outputs to assume a high-impedance OFF-state.

The 74AHCT245A is designed to operate over a V_{CC} range from 4.5 V to 5.5 V. The inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. **Features and benefits**

- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{pd} of 3.0 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 5 V, T_{amb} = 25 °C
- Typical $V_{OH(v)} > 2.3 \text{ V at } V_{CC} = 5 \text{ V}, T_{amb} = 25 ^{\circ}\text{C}$
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 2 kV
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

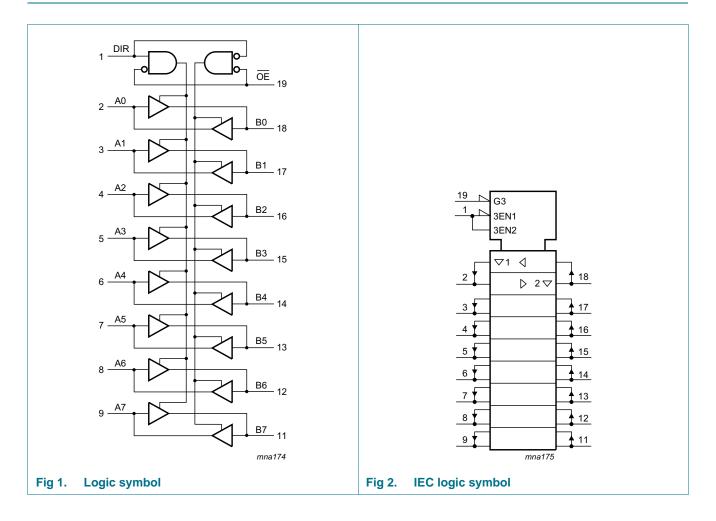


3. Ordering information

Table 1. Ordering information

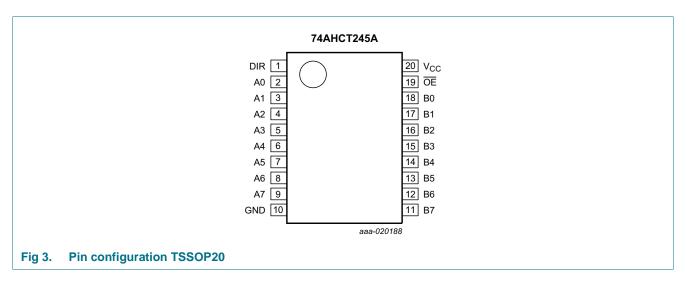
Type number	Package	Package									
	Temperature range	Name	Description	Version							
74AHCT245APW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1							

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
ŌĒ	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Input/output				
OE	DIR	An	Bn			
L	L	A = B	input			
L	Н	input	B = A			
Н	X	Z	Z			

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
V _I	input voltage		[1]	-0.5	+7.0	V
Vo	output voltage	active mode	[2][3]	-0.5	V _{CC} + 0.5	V
		power-down or 3-state mode	[2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V		-20	-	mA
I _{OK}	output clamping current	V _O < 0 V		-20	-	mA
Io	output current	$V_O = 0 \text{ V to } V_{CC}$		-	±25	mA
I _{CC}	supply current			-	75	mA
I _{GND}	ground current			-75	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	<u>[4]</u>	-	500	mW

^[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

^[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

^[3] This value is limited to 7.0 V maximum.

^[4] For TSSOP20 package: above 100 $^{\circ}$ C, the value of P_{tot} derates linearly with 10 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		4.5	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	active mode	0	V _{CC}	V
		power-down or 3-state mode	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C	to +85 °C	-40 °C t	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8 \text{ mA}$	3.94	-	-	3.8	-	3.7	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι _Ο = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8 mA	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL} ; V_O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	μΑ
I _{OFF}	power-off leakage current	V_1 or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	μΑ
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2	-	20	-	20	μΑ
Δl _{CC}	additional supply current	per input pin; $V_I = 3.4 \text{ V}$; $I_O = 0 \text{ A}$; other pins at V_{CC} or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Figure 6.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	An to Bn or Bn to An; see Figure 4	[2]								
		V _{CC} = 4.5 V to 5.5 V									
		C _L = 15 pF		-	3.0	7.7	1	8.5	1	10	ns
		C _L = 50 pF		-	4.8	8.7	1	9.5	1	11	ns
t _{en}	enable time	OE to An or OE to Bn; see Figure 5									
		V _{CC} = 4.5 V to 5.5 V									
		C _L = 15 pF		-	4.5	13.8	1	15	1	17	ns
		C _L = 50 pF		-	6.3	14.8	1	16	1	17.5	ns
t _{dis}	disable time	OE to An or OE to Bn; see Figure 5	[2]								
		V _{CC} = 4.5 V to 5.5 V									
		C _L = 15 pF		-	3.4	10.2	1	11.1	1	12.2	ns
		C _L = 50 pF		-	5.7	15.4	1	16.5	1	18	ns
t _{sk(o)}	output skew time	V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF		-	-	1	-	1	-	1	ns
C _I	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 5 \text{ V}$		-	2	6	-	6	-	6	pF
C _{I/O}	input/output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 5 \text{ V}$		-	5.5	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; $C_L = 0$ pF; $f = 10$ MHz; $V_I = GND$ to V_{CC}	[3]	-	9	-	-	-	-	-	pF

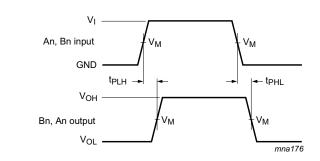
- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 - t_{en} is the same as t_{PZL} and $t_{\text{PZH}}.$
 - $t_{\mbox{\scriptsize dis}}$ is the same as $t_{\mbox{\scriptsize PLZ}}$ and $t_{\mbox{\scriptsize PHZ}}.$
- [3] $\,$ $\,$ $\,$ $\,$ $\,$ $\,$ $\,$ $\,$ C_{PD} is used to determine the dynamic power dissipation P_D (μ W).
 - $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum{(C_L \times V_{CC}{}^2 \times f_o)}$ where:
 - f_i = input frequency in MHz;
 - f_o = output frequency in MHz;
 - C_L = output load capacitance in pF;
 - V_{CC} = supply voltage in Volts.

Table 8. Noise characteristics

GND = 0 V. For test circuit, see Figure 6.

Symbol	Parameter	Conditions	Т	Unit		
			Min	Тур	Max	
$V_{CC} = 5 V$; C _L = 50 pF					
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.5	1.5	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-1.5	-0.3	-	V
V _{OH(v)}	HIGH-level output voltage (valley)		-	4.5	-	V
V _{IH(AC)}	AC HIGH-level input voltage	dynamic	2	-	-	V
V _{IL(AC)}	AC LOW-level input voltage	dynamic	-	-	8.0	V

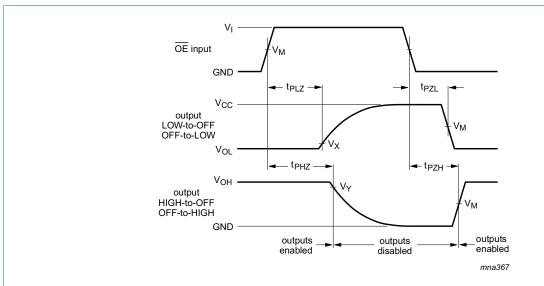
11. Waveforms



Measurement points are given in Table 9.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 4. Propagation delay input (An, Bn) to output (Bn, An)



Measurement points are given in Table 9.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Enable and disable times

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Table 9. Measurement points

Input	Output		
V _M	V _M	V _X	V _Y
1.5 V	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} – 0.3 V

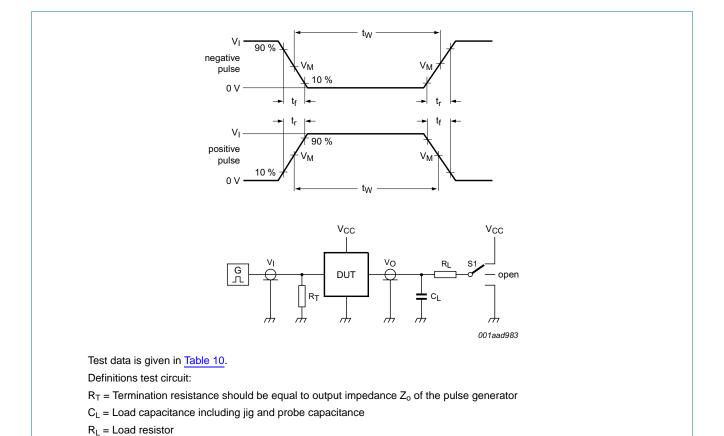


Table 10. Test data

Fig 6.

S1 = Test selection switch

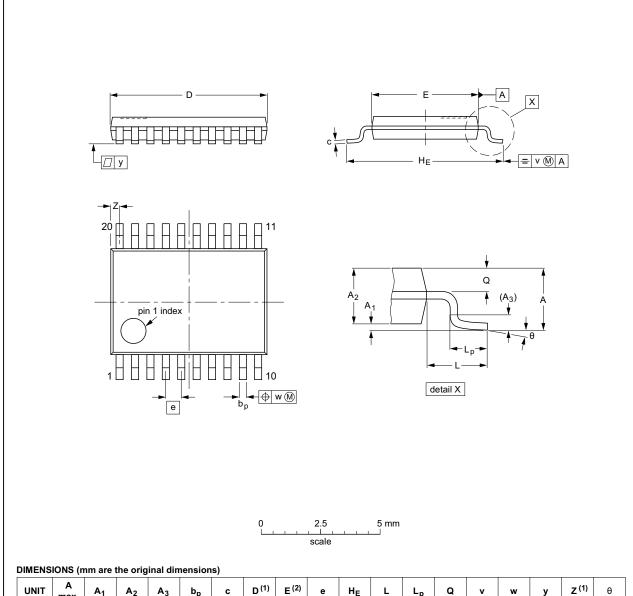
Test circuit for measuring switching times

Input Load				S1 position				
VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}		
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}		

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	C	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	>	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT360-1		MO-153				99-12-27 03-02-19
	VERSION	VERSION IEC	VERSION IEC JEDEC	VERSION IEC JEDEC JEITA	VERSION IEC JEDEC JEITA	VERSION IEC JEDEC JEITA PROJECTION

Fig 7. Package outline SOT360-1 (TSSOP20)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCT245A v.2	20161026	Product data sheet	-	74AHCT245A v.1
Modifications:	Type number 74AHCT245ABQ removed.			
74AHCT245A v.1	20160602	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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