

74AHCT240

Octal buffer/line driver; inverting; 3-state

Rev. 5 — 29 February 2016

Product data sheet

1. General description

The 74AHCT240 is an 8-bit inverting buffer/line driver with 3-state outputs. This device can be used as two 4-bit buffers or one 8-bit buffer. It features two output enables ($\overline{1OE}$ and $\overline{2OE}$), each controlling four of the 3-state outputs. A HIGH on $\overline{nOE}$ causes the outputs to assume a high-impedance OFF-state. Inputs are over voltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- Operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM JESD22-C101D exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHCT240D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT240PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT240BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85\text{ mm}$	SOT764-1

4. Functional diagram

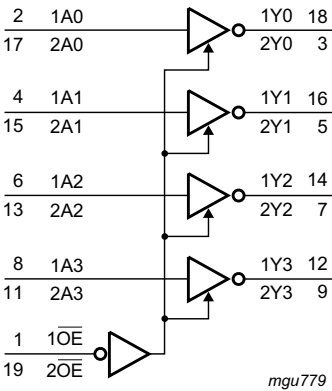


Fig 1. Logic symbol

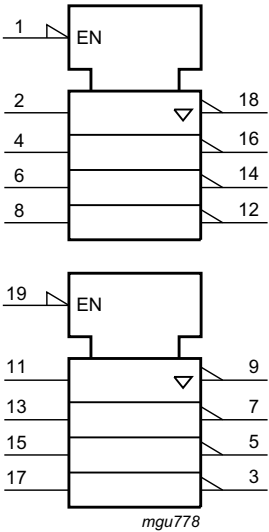


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

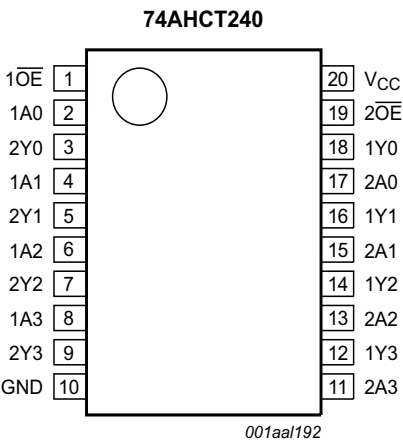
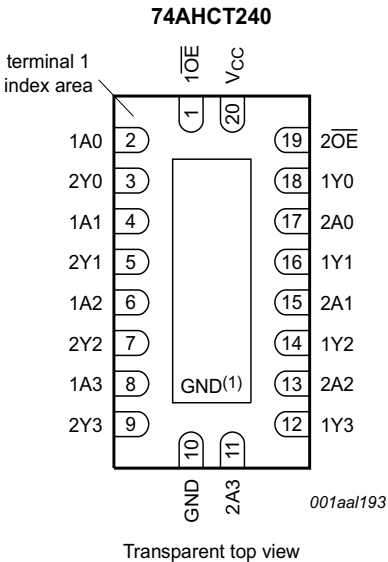


Fig 3. Pin configuration SO20 and TSSOP20



- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$	1	output enable input (active LOW)
$\overline{2OE}$	19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
GND	10	ground (0 V)
V _{CC}	20	power supply

6. Functional description

Table 3. Function table^[1]

Control	Input	Output
$\overline{nOE}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
V _I	input voltage		−0.5	+7.0	V
I _{IK}	input clamping current	V _I < −0.5 V ^[1]	−20	-	mA
I _{OK}	output clamping current	V _O < −0.5 V or V _O > V _{CC} + 0.5 V ^[1]	-	±20	mA
I _O	output current	V _O = −0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		−75	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	T _{amb} = −40 °C to +125 °C ^[2]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 package: above 70 °C the value of P_{tot} derates linearly with 8.0 mW/K.

For TSSOP20 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

For DHVQFN20 package: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 5 V ± 0.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{pd}	propagation delay	nAn to nYn; see Figure 5							
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.0	5.8	1.0	6.8	8.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	4.4	8.4	1.0	9.5	11.9	ns
t _{en}	enable time	nOE to nYn; see Figure 6							
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.4	7.5	1.0	9.0	14.4	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	4.5	9.5	1.0	11.5	14.4	ns
t _{dis}	disable time	nOE to nYn; see Figure 6							
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.9	6.1	1.0	6.7	8.3	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	6.2	8.7	1.0	9.2	11.5	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; C _L = 50 pF; f _i = 1 MHz	-	9	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

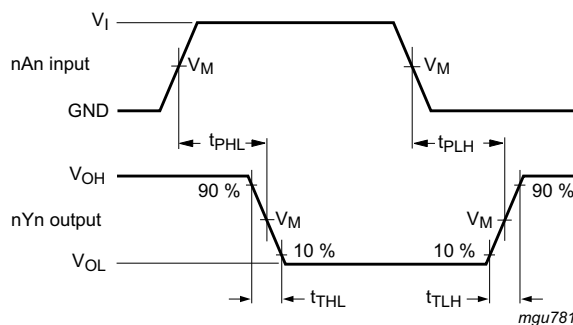
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

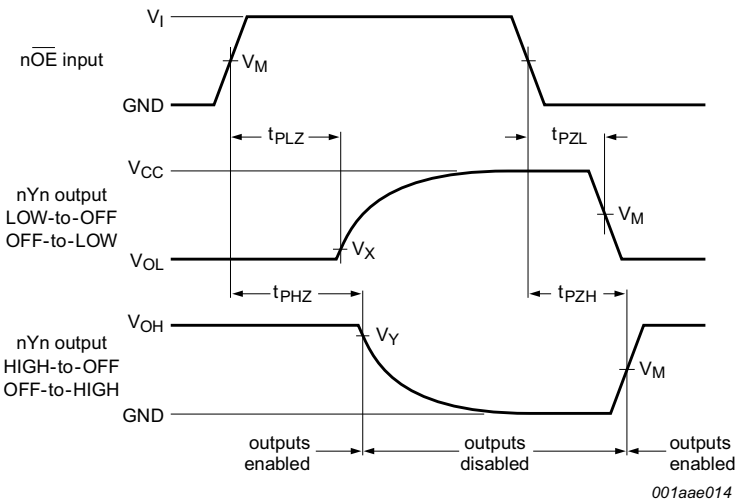
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. Propagation delay input (nAn) to output (nYn)



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

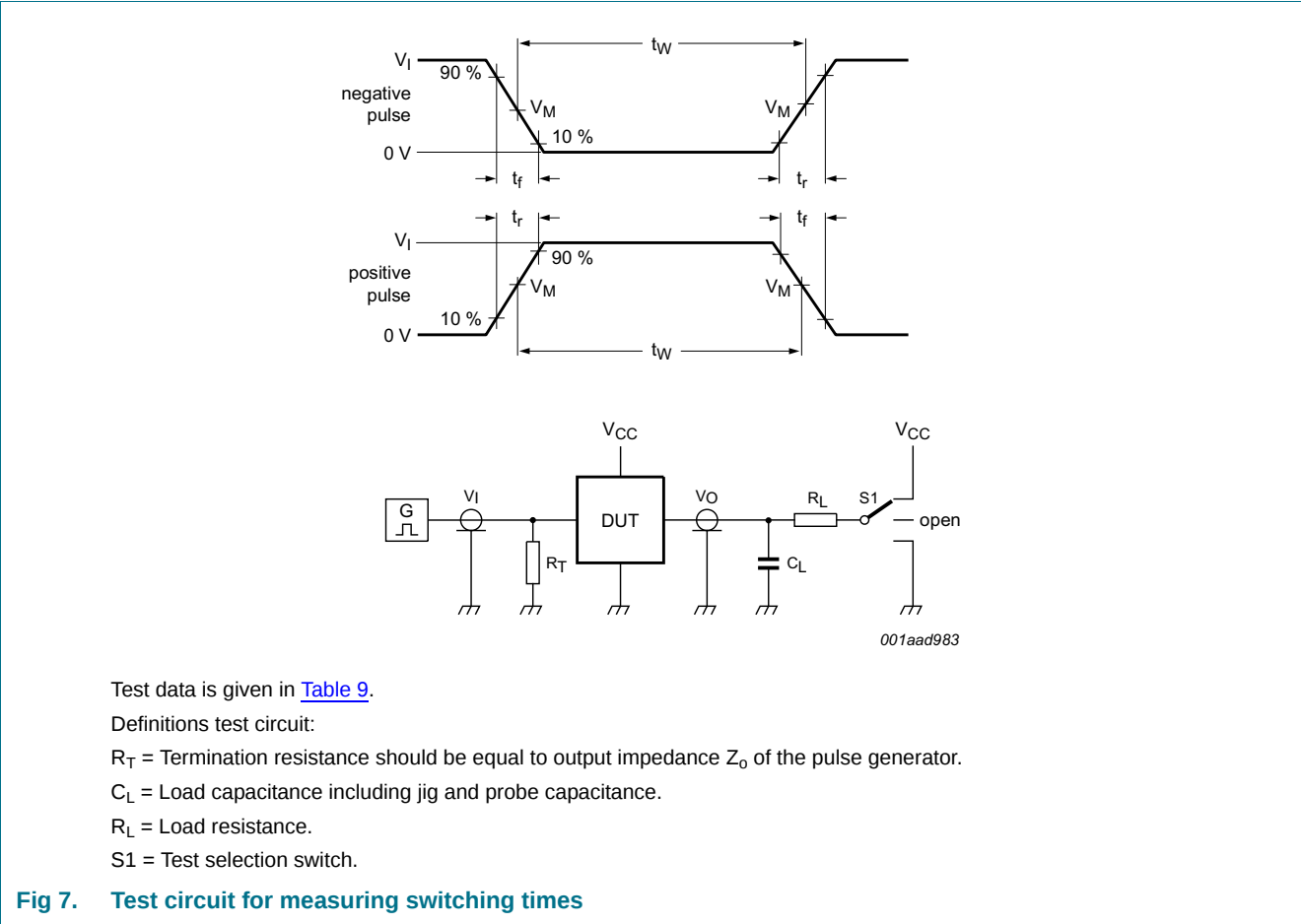


Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

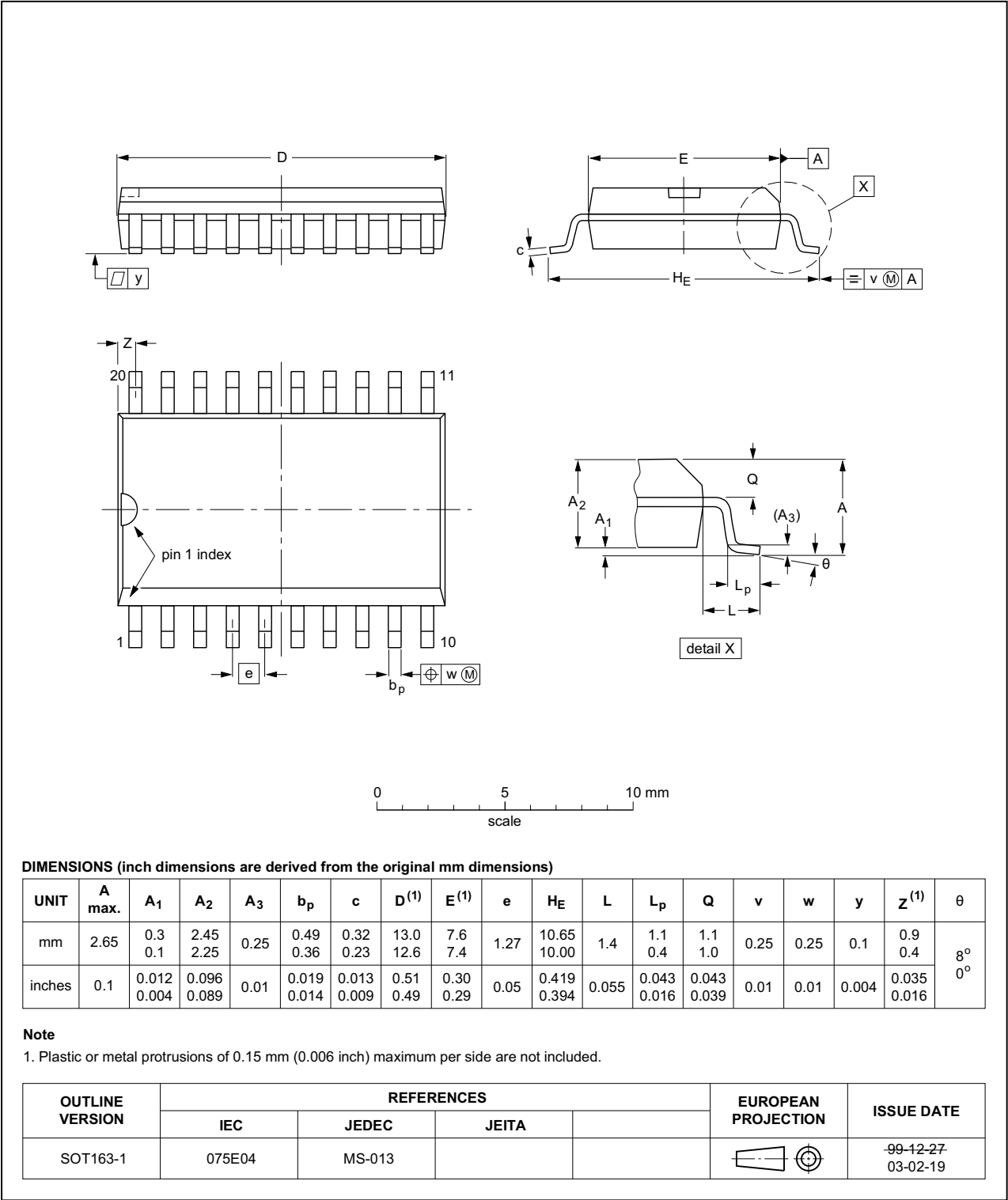


Fig 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

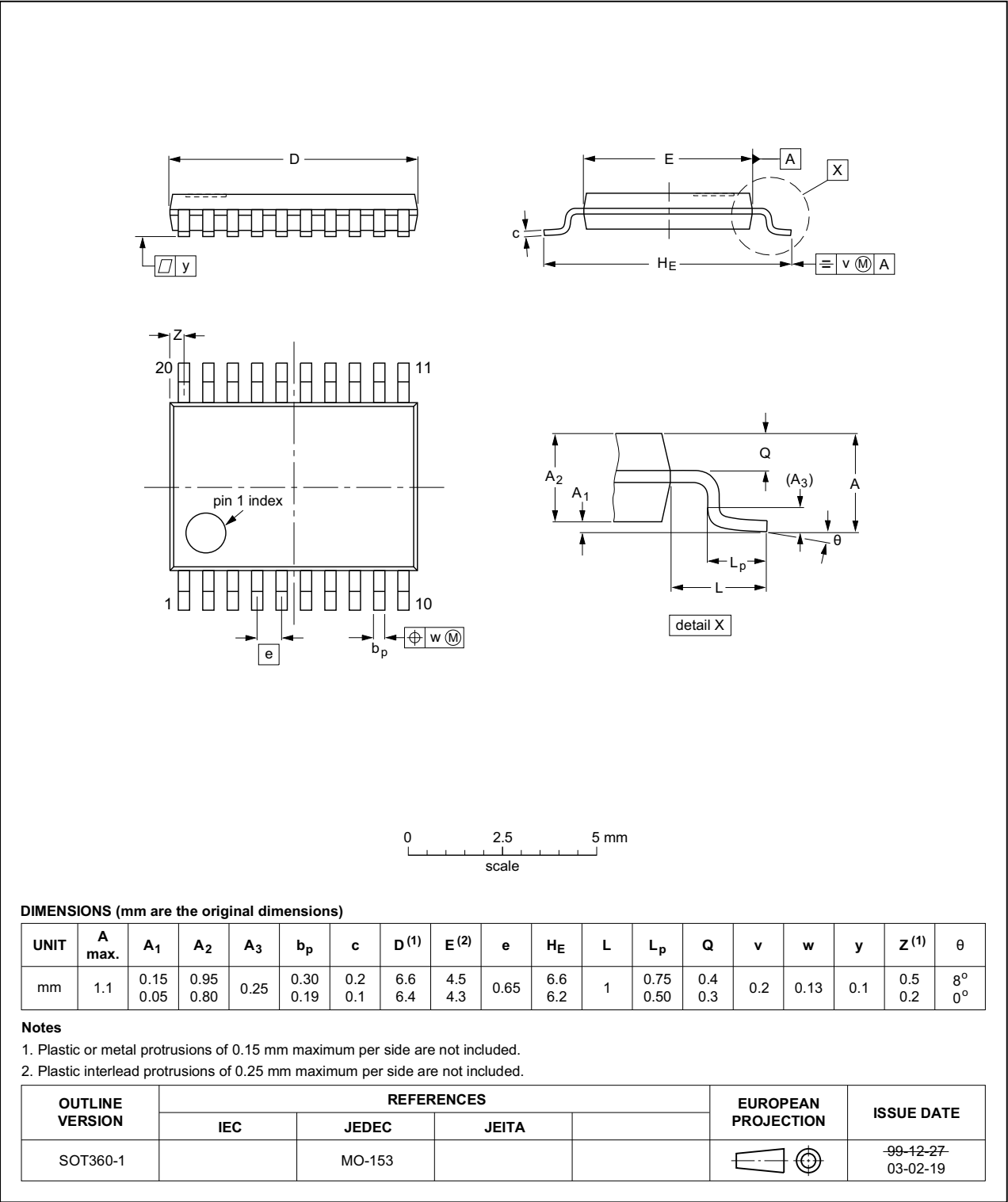


Fig 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

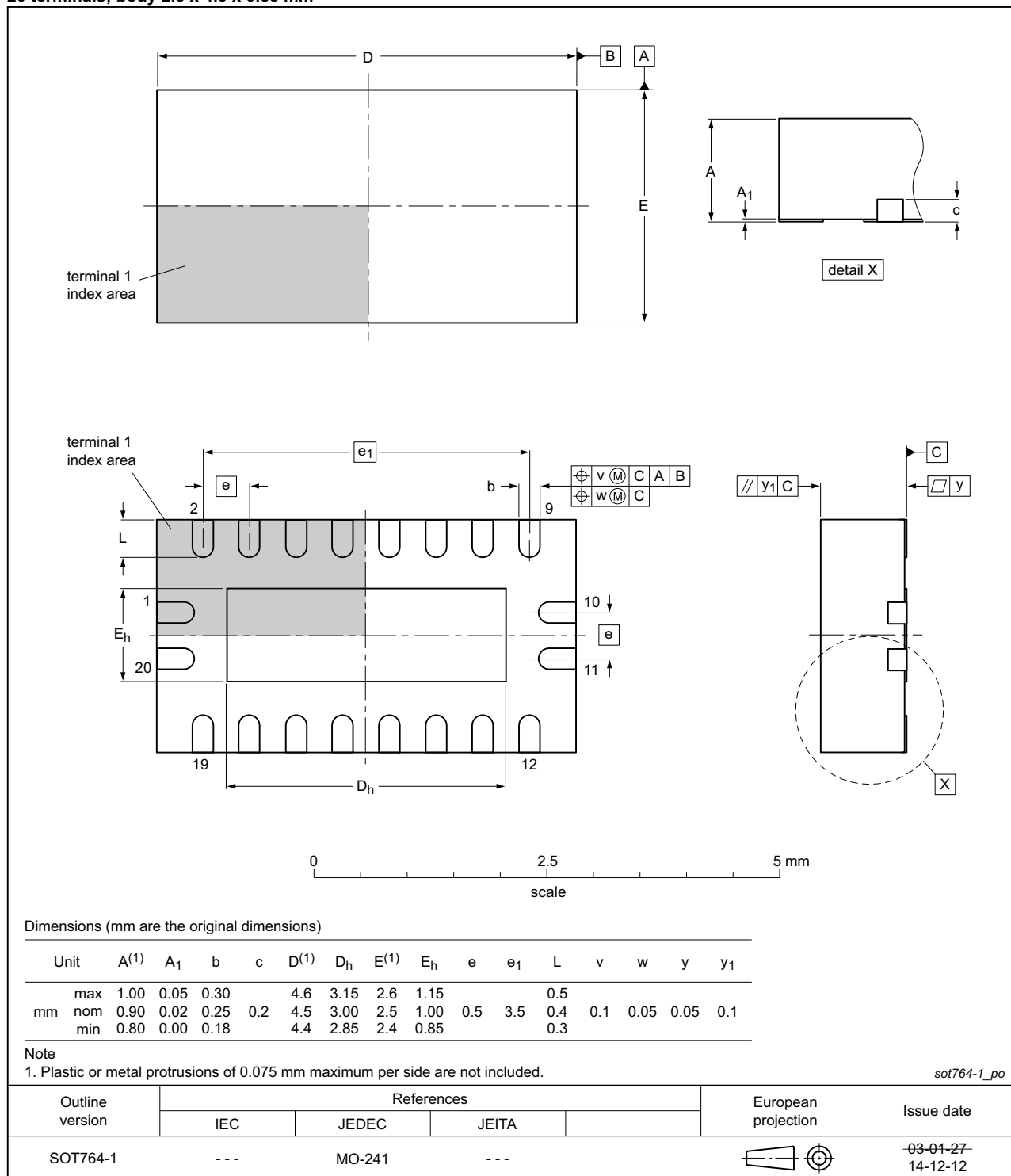


Fig 10. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCT240 v.5	20160229	Product data sheet	-	74AHC_AHCT240 v.4
Modifications:	• Type numbers 74AHC240D, 74AHC240PW and 74AHC240BQ removed.			
74AHC_AHCT240 v.4	20130925	Product data sheet	-	74AHC_AHCT240 v.3
Modifications:	• Figure 5 and 6 have been made visible (errata).			
74AHC_AHCT240 v.3	20111108	Product data sheet	-	74AHC_AHCT240 v.2
Modifications:	• Legal pages updated.			
74AHC_AHCT240 v.2	20101126	Product data sheet	-	74AHC_AHCT240 v.1
74AHC_AHCT240 v.1	20100111	Product data sheet	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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