Si5383/84 Rev D Data Sheet

Network Synchronizer Clocks Supporting 1 PPS to 750 MHz Inputs

The Si5383/84 combines the industry's smallest footprint and lowest power network synchronizer clock with unmatched frequency synthesis flexibility and ultra-low jitter. The Si5383/84 is ideally suited for wireless backhaul, IP radio, small and macro cell wireless communications systems, and data center switches requiring both traditional and packet based network synchronization.

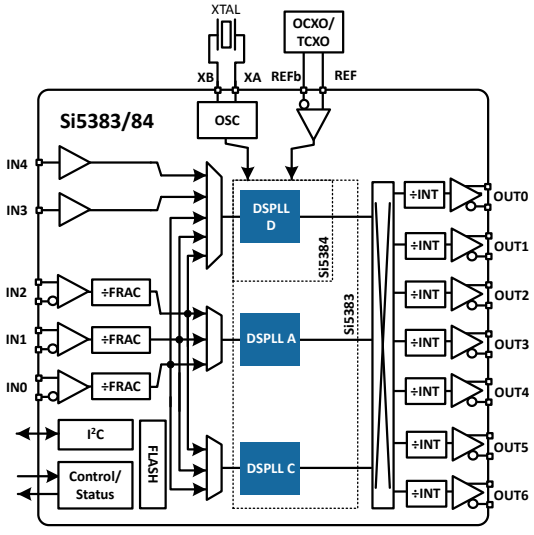
The three independent DSPLLs are individually configurable as a SyncE PLL, IEEE 1588 DCO, or a general-purpose PLL for processor/FPGA clocking. The Si5383/84 can also be used in legacy SETS systems needing Stratum 3/3E compliance. In addition, locking to a 1 PPS input frequency is available on DSPLL D. The DCO mode provides precise timing adjustment to 1 part per trillion (ppt). The unique design of the Si5383/84 allows the device to accept a TCXO/OCXO reference with a wide frequency range, and the reference clock jitter does not degrade the output performance. The Si5383/84 is configurable via a serial interface and programming the Si5383/84 is easy with ClockBuilder Pro software. Factory pre-programmed devices are also available.

KEY FEATURES

- One or three independent DSPLLs in a single monolithic IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Input frequency range:
  - External crystal: 25-54 MHz
  - REF clock: 5-250 MHz
  - Diff clock: 8 kHz - 750 MHz
  - LVCMOS clock: 1 PPS, 8 kHz - 250 MHz
- Output frequency range:
  - Differential: 1 PPS, 100 Hz - 718.5 MHz
  - LVCMOS: 1 PPS, 100 Hz - 250 MHz
- Ultra-low jitter of less than 150 fs

Applications

- Synchronous Ethernet (SyncE) ITU-T G.8262 EEC Options 1 and 2
- Telecom Grand Master Clock (T-GM) as defined by ITU-T G.8273.1
- Telecom Boundary Clock and Slave Clock (T-BC, T-TSC) as defined by ITU-T G. 8273.2
- IEEE 1588 (PTP) slave clock synchronization
- Stratum 3/3E, G.812, G.813, GR-1244, GR-253 network synchronization
- 1 Hz/1 PPS Clock Multiplier



1. Feature List

The Si5383/84 highlighted features are listed below.

- One or three DSPLLs in a single monolithic IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Meets the requirements of:
  - ITU-T G.8273.1 T-GM
  - ITU-T G.8273.2 T-BC, T-TSC
  - Synchronous Ethernet (SyncE) ITU-T G.8262 EEC Options 1 and 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - External crystal: 25 - 54 MHz
  - REF clock: 5 - 250 MHz
  - Diff clock: 8 kHz - 750 MHz
  - LVCMOS clock: 1 PPS, 8 kHz - 250 MHz
- Output frequency range:
  - Differential: 1 PPS, 100 Hz - 718.5 MHz
  - LVCMOS: 1 PPS, 100 Hz - 250 MHz
- Pin or software controllable DCO on each DSPLL with typical resolution to 1 ppt/step
- TCXO/OCXO reference input determines DSPLL free-run/hold-over accuracy and stability
- Excellent jitter performance
- Programmable loop bandwidth per DSPLL:
  - 1 PPS inputs: 1 mHz and 10 mHz
  - All other inputs: 1 mHz to 4 kHz
- Highly configurable output drivers: LVDS, LVPECL, LVCMOS, HCSL, CML
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output supply pins: 3.3 V, 2.5 V, or 1.8 V
- Built-in power supply filtering
- Status monitoring:
  - LOS, LOL: 1 PPS-750 MHz
  - OOF: 8 kHz-750 MHz
- I^2C Serial Interface
- ClockBuilder™ Pro software tool simplifies device configuration
- 5 input, 7 output, 56-pin LGA
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Guide

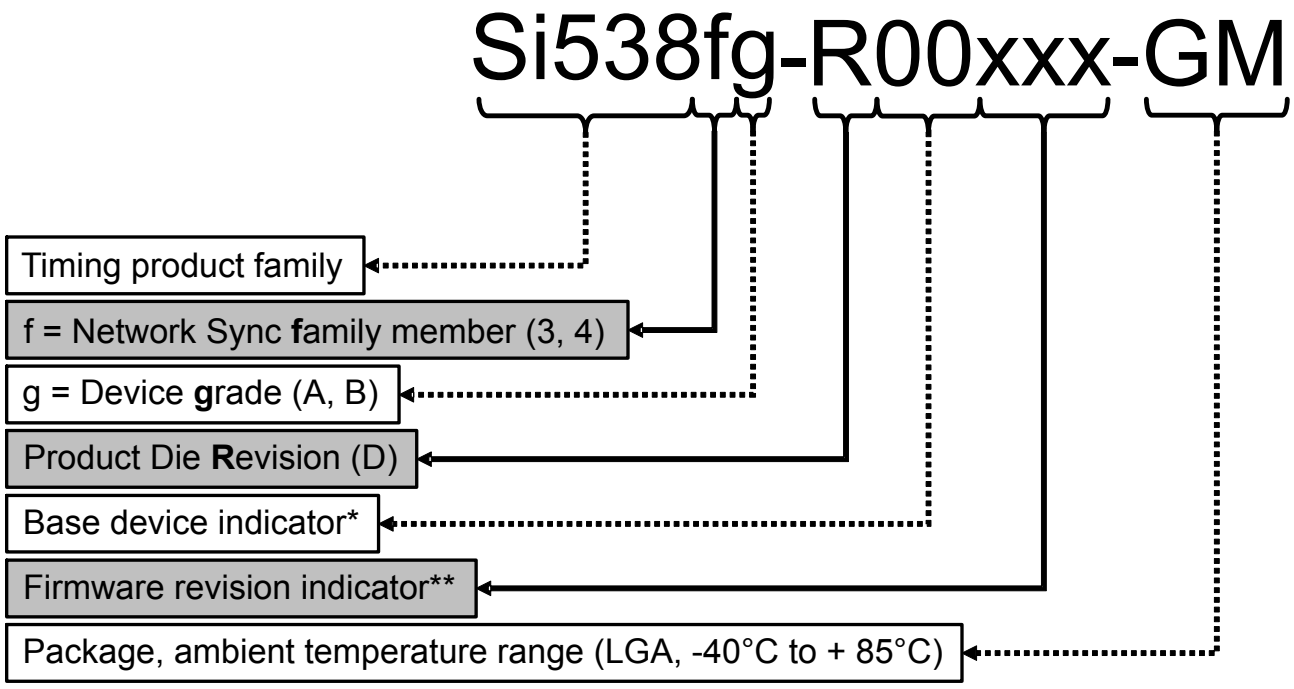
Table 2.1. Ordering Guide

Ordering Part Number (OPN)[1,2]	# of DSPLLs	Maximum Output Frequency	Package	RoHS-6, Pb-Free	Temperature Range
Si5383A-Dxxxxx-GM	3	718.5 MHz	56-Lead 8×8 LGA	Yes	–40 to 85 °C
Si5383B-Dxxxxx-GM		350 MHz			
Si5384A-Dxxxxx-GM	1	718.5 MHz			
Si5384B-Dxxxxx-GM		350 MHz			
Si5383-D-EVB[3]	—	—	Evaluation Board	—	—
SiOCXO1-EVB	—	—	OCXO Evaluation Board	—	—

Notes:

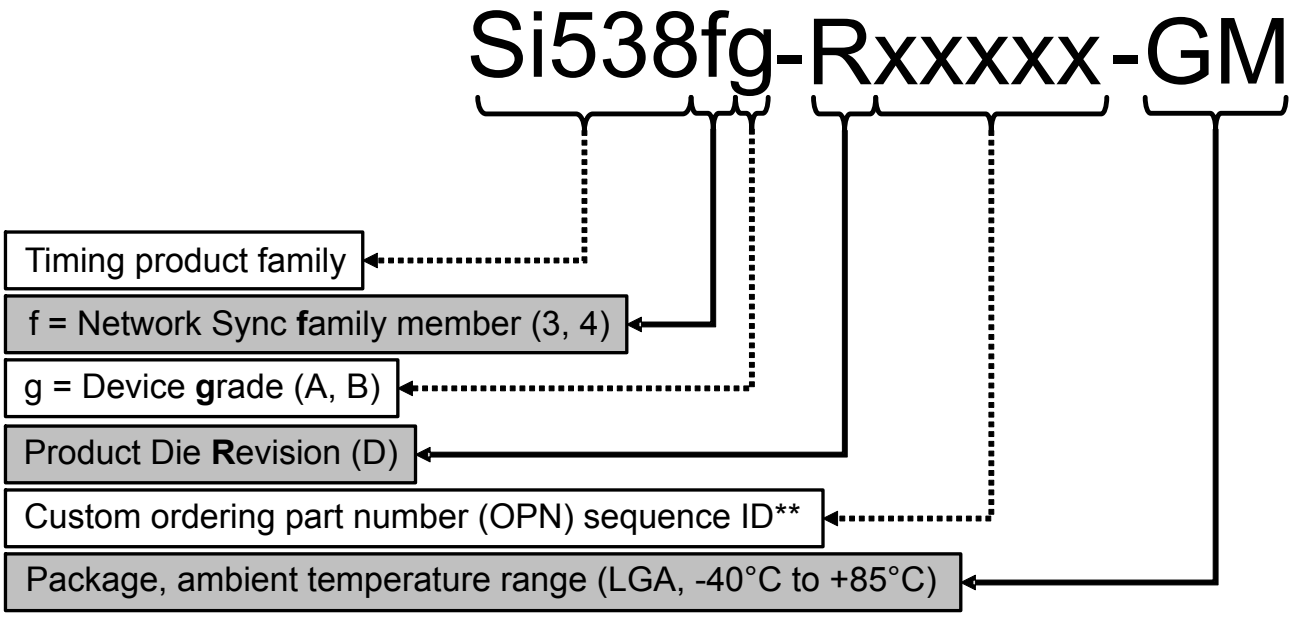
1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See figures below for 5-digit numerical sequence nomenclature.
3. The Si5383-D-EVB ships with an SiOCXO1-EVB board included. Additional SiOCXO1-EVB boards may be ordered separately if needed.

2.1 Ordering Part Number Fields



* Firmware is preprogrammed into base devices, but no configuration settings are present in the device
** 3 digits corresponding to the firmware revision preprogrammed into base devices

Figure 2.1. Ordering Guide Part Number Fields for Base Devices



** 5 digits; assigned by ClockBuilder Pro for custom, factory-preprogrammed OPN devices.
The firmware revision for custom OPN devices is determined by ClockBuilder Pro when a custom part number is created.

Figure 2.2. Ordering Guide Part Number Fields for Custom OPN Devices

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3. Functional Description

The Si5383 offers three DSPLLs and the Si5384 offers one DSPLL that can be independently configured and controlled through the serial interface. In standard input mode, all DSPLLs support high frequency inputs. DSPLL D can be configured to operate in 1 PPS input mode to lock to a 1 Hz input clock. Regardless of the input mode, any of the DSPLLs can be used to generate any valid output frequency.

Each of the DSPLLs have locked, free-run, and holdover modes of operation with an optional DCO mode for IEEE 1588 applications. The device requires an external crystal and an external reference (TCXO or OCXO) to operate. The reference input (REF/REFb) determines the frequency accuracy and stability while in free-run and holdover modes. The external crystal completes the internal oscillator circuit (OSC) which is used by the DSPLL for intrinsic jitter performance. There are three main inputs (IN0 - IN2) for synchronizing the DSPLLs. Input selection can be manual or automatically controlled using an internal state machine. Two additional single-ended inputs are available to DSPLL D. Any of the output clocks (OUT0 to OUT6) can be configured to any of the DSPLLs using a flexible crosspoint connection. Output 5 is the only output that can be configured for a 1 Hz output to support 1 PPS.

3.1 Standards Compliance

Each of the DSPLLs meet the applicable requirements of ITU-T G.8262 (SyncE), G.812, G.813, G.8273.2 (T-BC), in addition to Telcordia GR-1244 and GR-253 as shown in the compliance report for standard input mode. The DCO feature enables IEEE1588 (PTP) implementations in addition to hybrid SyncE + IEEE1588 (T-BC).

3.2 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.3 DSPLL Loop Bandwidth in Standard Input Mode

The DSPLL loop bandwidth determines the amount of input clock jitter and wander attenuation. Register configurable DSPLL loop bandwidth settings of 1 mHz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

Table 3.1. Loop Bandwidth Requirements

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Loop Bandwidth
GR-253 Stratum 3E	G.812 Type III	—	0.001 Hz
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	< 0.1 Hz
—	G.813 Option 1	G.8262 EEC Option 1	1 - 10 Hz

3.3.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. In standard input mode, the fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs for input frequencies $\geq$ 8 kHz..

3.4 DSPLL Loop Bandwidth in 1 PPS Mode

When operating in 1 PPS input mode, the Si5383/84 offers two choices of loop bandwidth for DSPLL D: 1 mHz or 10 mHz.

3.4.1 Smartlock Feature

When operating in 1 PPS input mode, the Si5383/84 offers the Smartlock feature to achieve fast locking to 1 PPS inputs. The Smartlock feature locks to 1 PPS inputs in two phases. During the first phase, large adjustments are made to eliminate the majority of the frequency and phase error. During the second phase, finer adjustments are made until the PLL is locked. Once the PLL is locked, the DSPLLs loop bandwidth will automatically revert to the DSPLL loop bandwidth setting.

3.5 Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 3.1 Modes of Operation on page 8. The following sections describe each of these modes in greater detail.

3.5.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard register reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can either affect all or each DSPLL individually. It is recommended that the device be held in reset during power-up by asserting the RSTb pin. RSTb should be released once all supplies have reached operational levels. The RSTb pin functions as an open-drain output, which drives low during POR. External devices must be configured as open-drain to avoid contention.

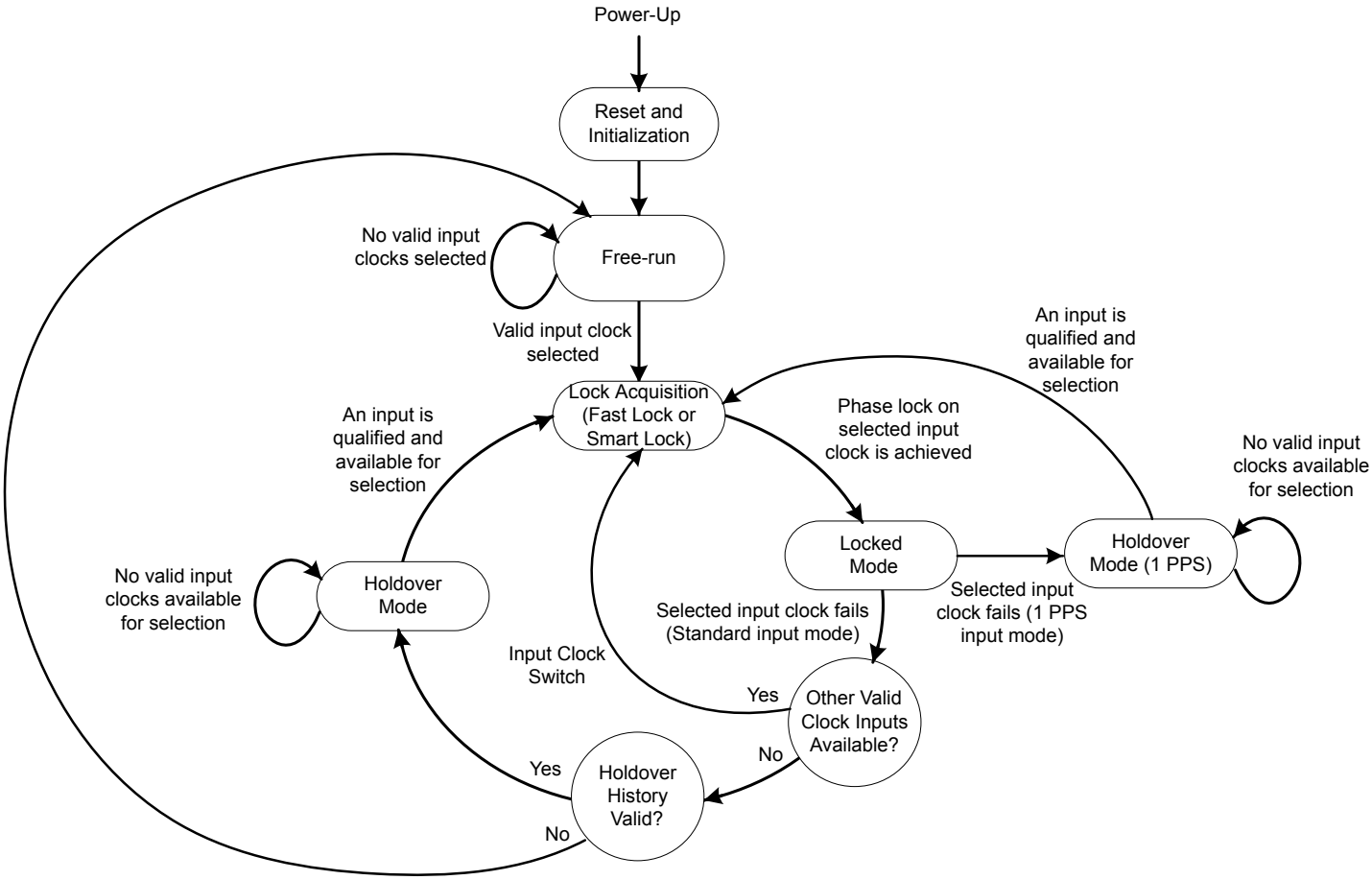


Figure 3.1. Modes of Operation

3.5.2 Free-run Mode

Once power is applied to the Si5383/84 and initialization is complete, all three DSPLLs will automatically enter freerun if no clock input is applied. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the clock source at the reference inputs (REF/REFb). A TCXO or OCXO is recommended for applications that need frequency accuracy and stability to meet the synchronization standards as shown in the following table:

Table 3.2. Free-run Accuracy for North American and European Synchronization Standards

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Free-run Accuracy
GR-253 Stratum 3E	G.812 Type III	—	±4.6 ppm
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	±4.6 ppm
—	G.813 Option 1	G.8262 EEC Option 1	±4.6 ppm

3.5.3 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.If the fast lock feature is enabled for inputs ≥ 8 kHz, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. If the input frequency is configured for 1 PPS, the Smartlock mode is used. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

3.5.4 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own LOLb pin and status bit to indicate when lock is achieved. Refer to Section 3.9.6 LOL Detection for more details on the operation of the loss of lock circuit.

3.5.5 Holdover Mode

Any of the DSPLLs will automatically enter Holdover Mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores several seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

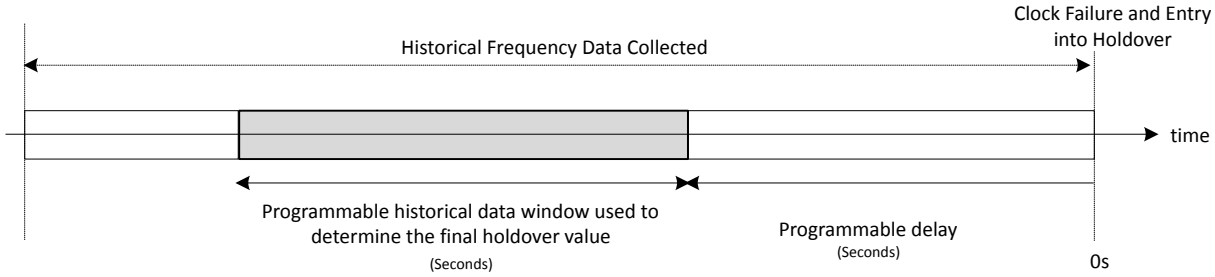


Figure 3.2. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF/REFb pins. When the clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

In standard input mode, the DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching see Section 3.8.6 Ramped Input Switching in Standard Input Mode.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

3.6 Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). However due to slower update rates over the I^2C interface, it is recommended to use pin controls for adjusting the frequency in DCO mode. A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it.

The DCO mode is available when the DSPLL is operating in locked mode. The DCO mode is mainly used with standard input mode in IEEE1588 (PTP) applications where a clock needs to be generated based on recovered timestamps. In this case timestamps are recovered by the PHY/MAC. A processor containing servo software controls the DCO to close the timing loop between the master and slave nodes. The processor has the option of using the FINC/FDEC pin controls to update the DCO frequency or by controlling it through the serial interface.

When operating in 1 PPS input mode, an additional enhanced DCO mode is enabled in the holdover state to facilitate DCO steering. This is useful for applications that require Assisted Partial Timing Support (APTS).

3.6.1 Frequency Increment/Decrement Using Pin Controls (FINC, FDEC)

Controlling the output frequency with pin controls is available in standard input mode. This feature involves asserting the FINC or FDEC pins to step (increment or decrement) the DSPLL's output frequency. Both the step size and DSPLL selection (A, C, D) is made through the serial interface by writing to register bits.

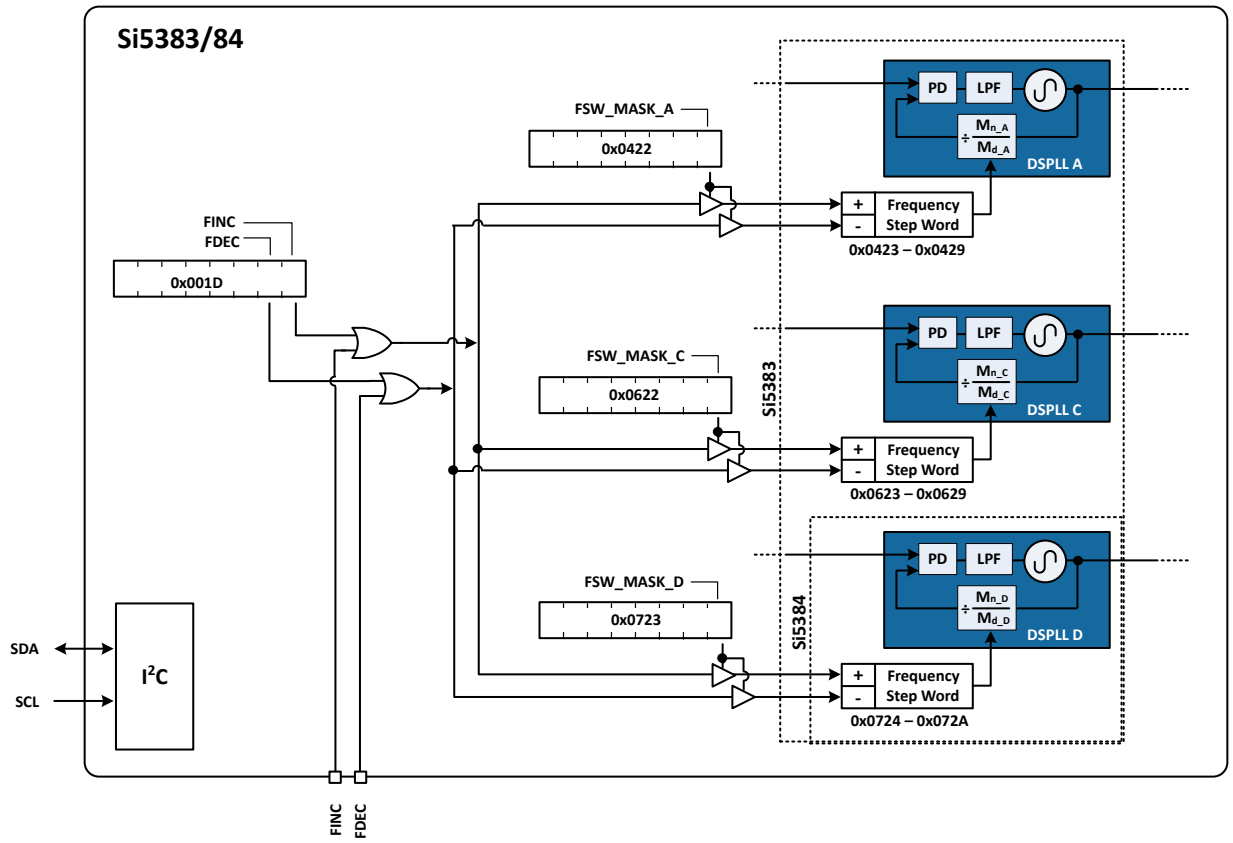


Figure 3.3. Controlling the DCO Mode By Pin Control

3.6.2 Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available. This feature involves asserting the FINC or FDEC bits to activate the frequency change defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affect by the frequency change.

3.7 External Reference (XA/XB, REF/REFb)

The external crystal at the XA/XB pins determines jitter performance of the output clocks, and the external reference clock at the REF/REFb pins determines the frequency accuracy and stability during free-run or holdover modes, and the MTIE/TDEV performance when the DSPLL is locked. Jitter from the external clock on the REF/REFb pins will have little to no effect on the output jitter performance, depending upon the selected bandwidth. This allows using a lower-cost TCXO/OCXO with a higher phase noise floor or an external reference clock distributed over long PCB traces or across a backplane, without impacting output jitter.

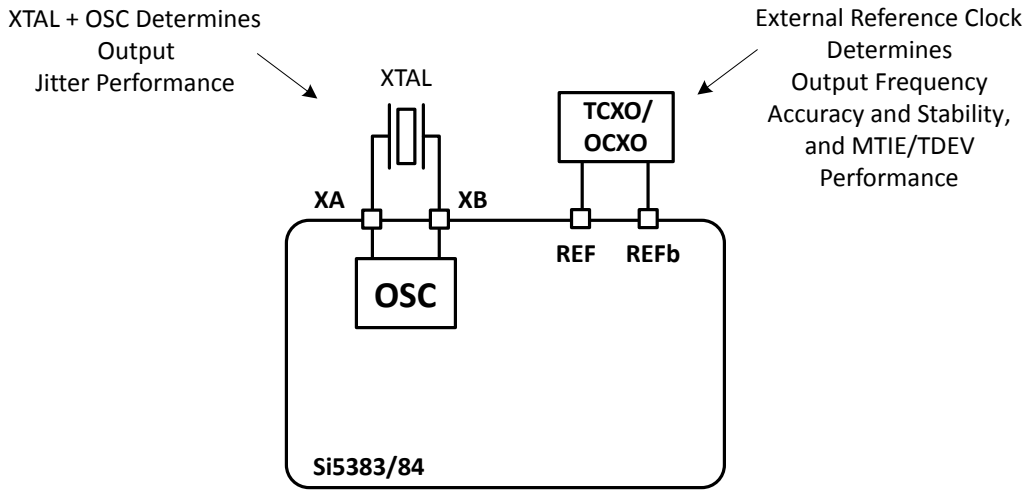
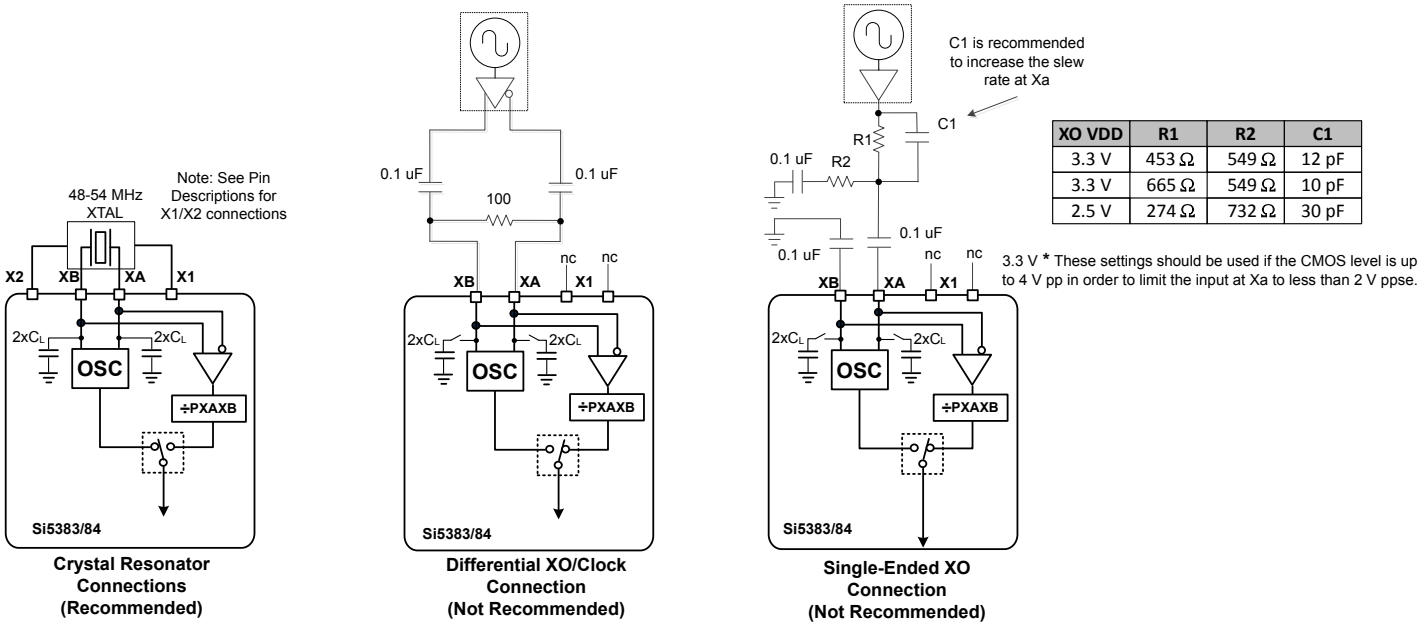


Figure 3.4. External Reference Connections

3.7.1 External Crystal (XA/XB)

The external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLLs. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. Frequency offsets due to CL mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±1000 ppm. The *Si5383/84 Reference Manual* provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Although it is not recommended, the device can also accommodate an external clock at the XA/XB pins instead of a crystal. Selection between the external crystal or clock is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. Refer to Chapter 5. Electrical Specifications for reference clock requirements when using this mode. The *Si5383/84 Reference Manual* provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.



XO VDD	R1	R2	C1
3.3 V	453 Ω	549 Ω	12 pF
3.3 V	665 Ω	549 Ω	10 pF
2.5 V	274 Ω	732 Ω	30 pF

3.3 V * These settings should be used if the CMOS level is up to 4 V pp in order to limit the input at Xa to less than 2 V ppse.

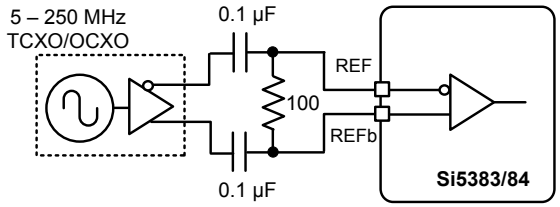
Note: XA and XB must not exceed the maximum input voltage listed in Data Sheet Table Input Clock Specifications

Figure 3.5. Crystal Resonator Connections

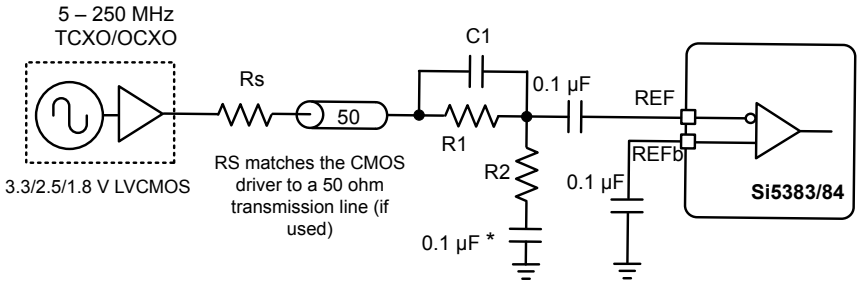
3.7.2 External Reference (REF/REFb)

The external reference at the REF/REFb pins is used to determine output frequency accuracy and stability during free-run and holdover modes. This reference is usually from a TCXO or OCXO and can be connected differentially or single-ended as shown in the figure below:

Standard Differential AC-Coupled Input Buffer



Standard Single-Ended - AC-Coupled Input Buffer



When 3.3 V LVCMOS driver is present, use R2 = 845 ohm and R1 = 267 ohm if needed to keep the signal at INx < 3.6 Vpp_se. Including C1 = 6 pf may improve the output jitter due to faster input slew rate at INx. If attenuation is not needed for Inx<3.6 Vppse, make R1 = 0 ohm and omit C1, R2 and the capacitor below R2. * This cap should have less than ~20 ohms of capacitive reactance at the clock input frequency.

Figure 3.6. External Reference Connections

3.8 Inputs (IN0, IN1, IN2, IN3, IN4)

Inputs IN0, IN1 and IN2 can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows inputs IN0-IN2 to connect to any of the DSPLLs as shown in the figure below. DSPLL D has two additional inputs (IN3-IN4) that are CMOS only inputs. If both IN3 and IN4 are used, they must be the same frequency.

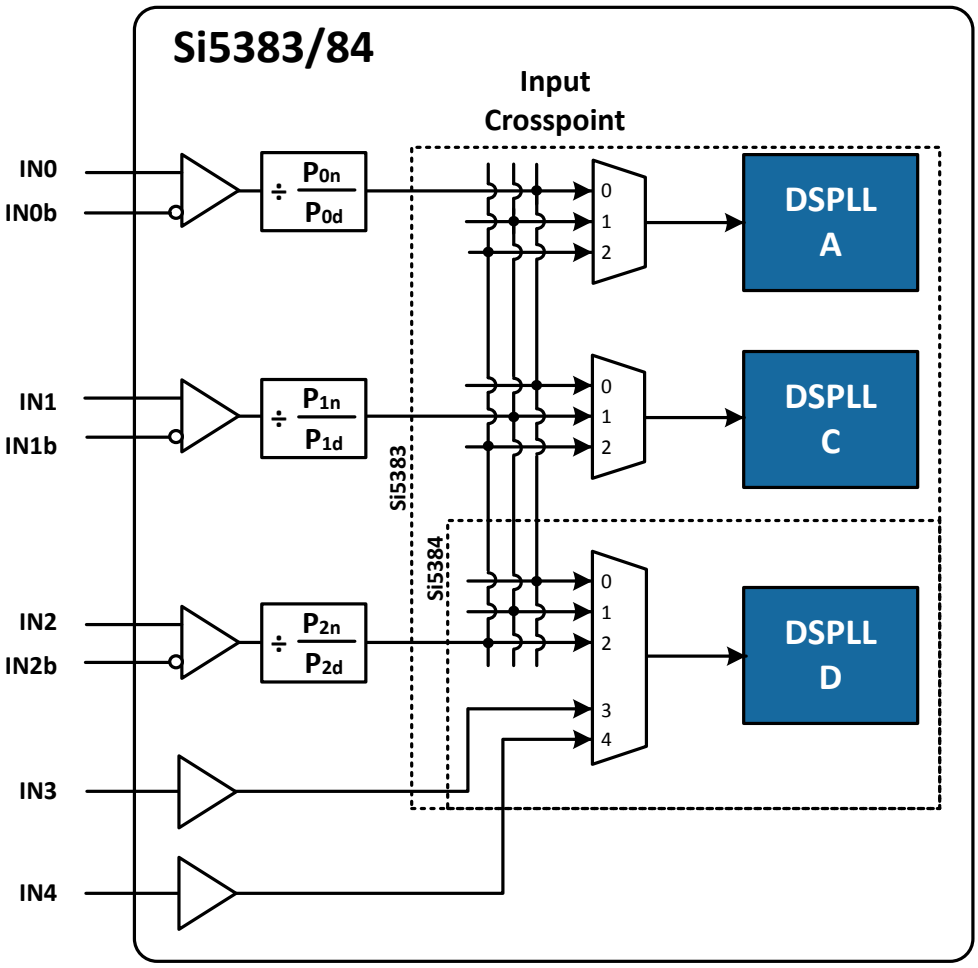


Figure 3.7. Si5383/84 DSPLL Input Selection Crosspoint

3.8.1 Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

3.8.2 Manual Input Selection

In manual mode the input selection is made by writing to a register. IN0-IN2 is available to DSPLL A and C, IN0-IN4 is available to DSPLL D. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

3.8.3 Automatic Input Selection in Standard Input Mode

When configured in this mode, a DSPLL automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS) and inputs IN0-IN2 can be monitored for invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter either holdover or freerun mode if there are no valid inputs available.

3.8.4 Input Configuration and Terminations

Inputs IN0-IN2 can be configured as differential or single-ended LVCMOS. Inputs IN3-IN4 are single-ended only. The recommended input termination schemes are shown in the figure below. Inputs IN0-IN2 can be disabled and left unconnected when not in use. LVCMOS inputs IN3-IN4 should be externally pulled low when not in use.

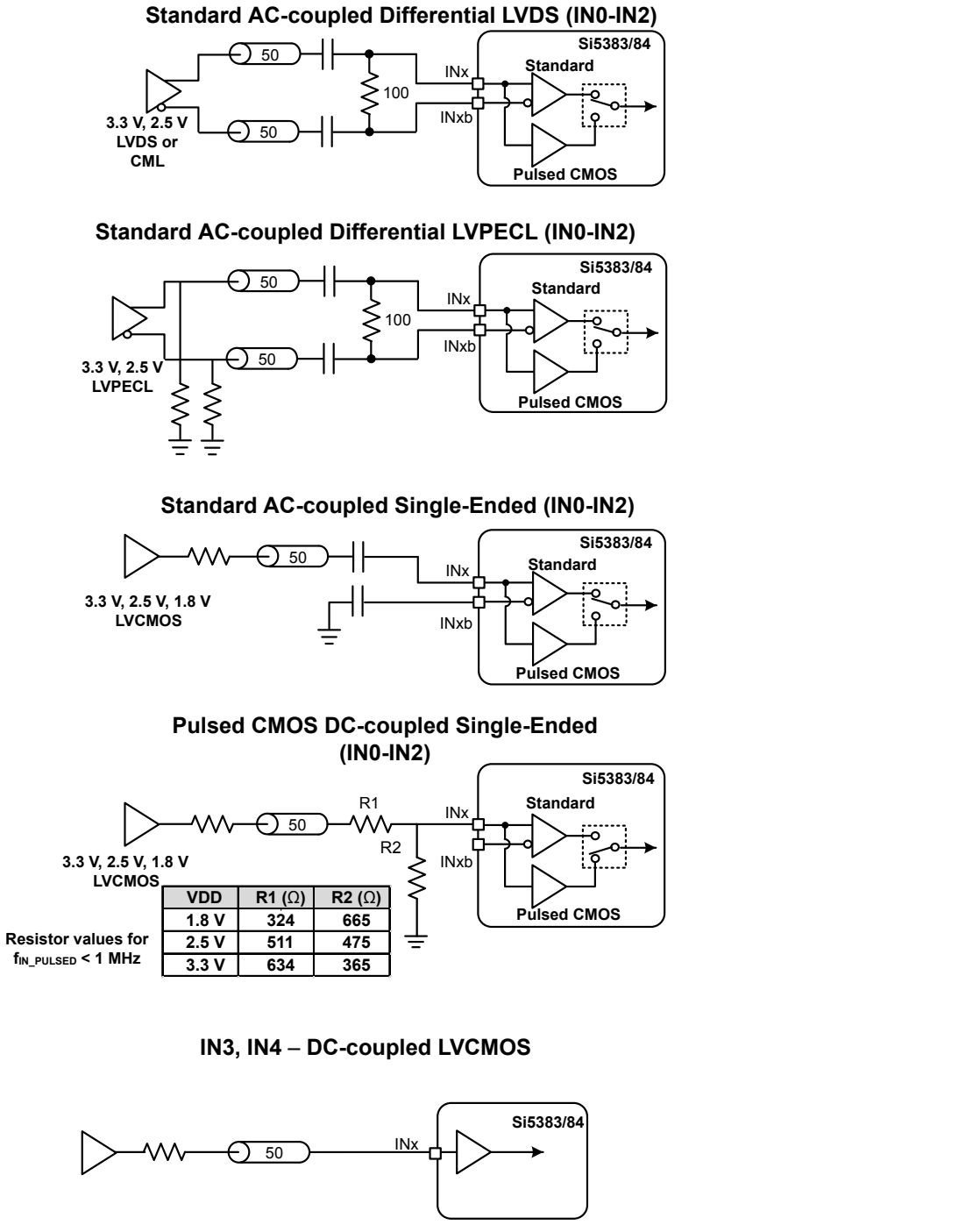


Figure 3.8. Termination of Differential and LVCMOS Input Signals

3.8.5 Hitless Input Switching in Standard Input Mode

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature is not available in 1 PPS input mode. Hitless switching can be enabled on a per DSPLL basis.

3.8.6 Ramped Input Switching in Standard Input Mode

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see Section 3.5.5 Holdover Mode.

3.8.7 Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart for standard input mode, and ±10 ppm apart for 1 PPS input mode. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock or Smartlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition. All clock inputs, including 3 and 4, support glitchless input switching.

3.8.8 Synchronizing to Gapped Input Clocks in Standard Input Mode

Each of the DSPLLs support locking to an input clock that has missing periods in standard input mode. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter, so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the figure below:

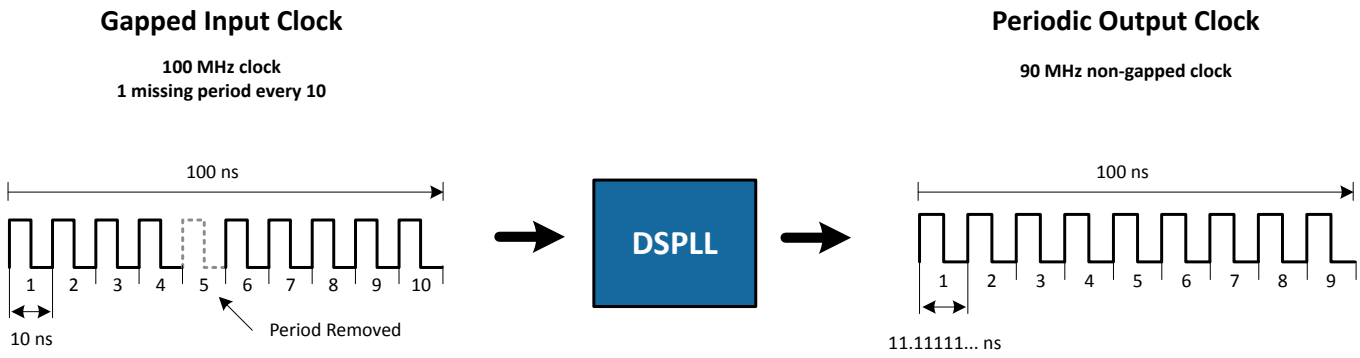


Figure 3.9. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 37 when the switch occurs during a gap in either input clock.

3.9 Fault Monitoring

All input clocks and the reference input (REF/REFb) are monitored for loss of signal (LOS). In addition, inputs IN0-IN2 and REF/REFb are monitored for out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has an LOL indicator, which is asserted when synchronization is lost with their selected input clock.

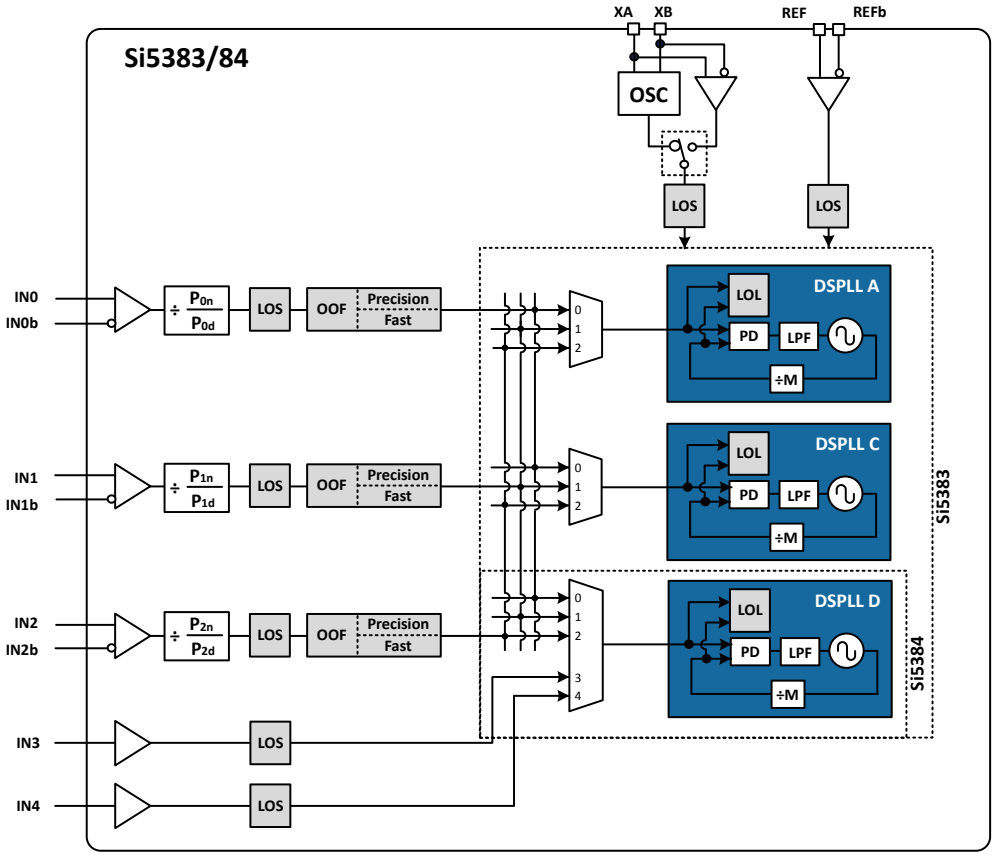


Figure 3.10. Si5383/84 Fault Monitors

3.9.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

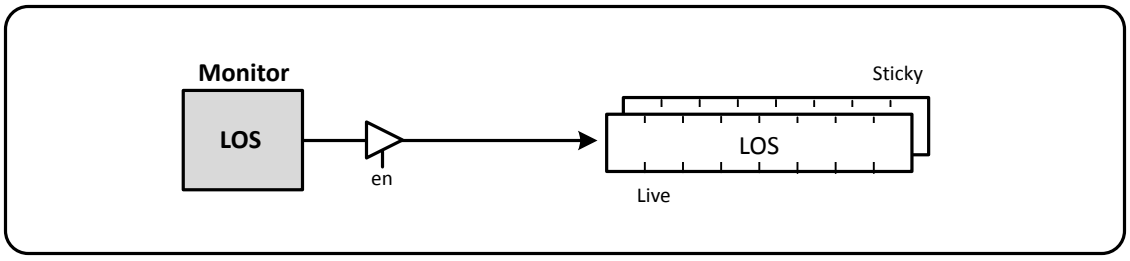


Figure 3.11. LOS Status Indicators

3.9.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.9.3 OOF Detection

In standard input mode, input clocks IN0, IN1, IN2 are monitored for frequency accuracy with respect to an OOF reference, which it considers as its “0_ppm” reference. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

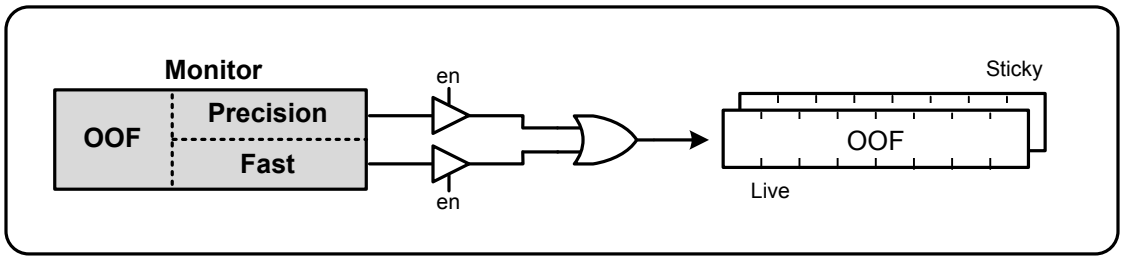


Figure 3.12. OOF Status Indicator

3.9.4 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range, which is register configurable up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 – IN2) as the 0 ppm OOF reference instead of the REF/REFb pins is available. This option is register-configurable. XA/XB can also be used as the 0 ppm reference.

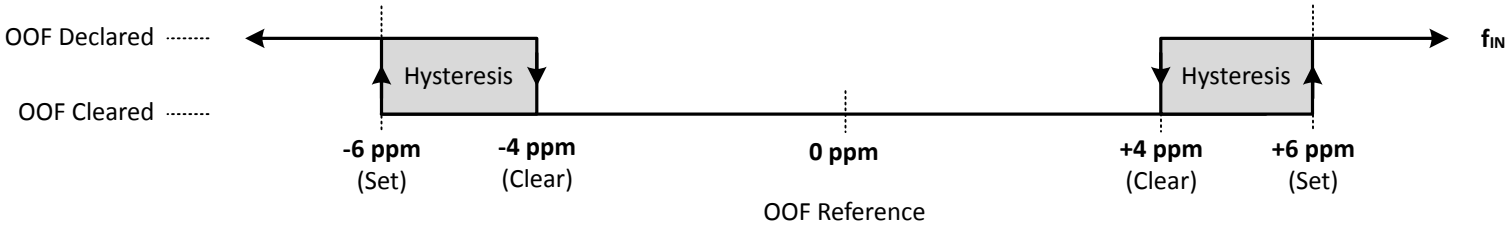


Figure 3.13. Example of Precise OOF Monitor Assertion and De-assertion Triggers

3.9.5 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.9.6 LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts the LOL register bits when a DSPLL has lost synchronization with its selected input clock. Separate LOL register bits are used to indicate LOL for standard input mode versus 1 PPS mode. There is also a dedicated LOL pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Cb, LOL_Db) and also for the reference.

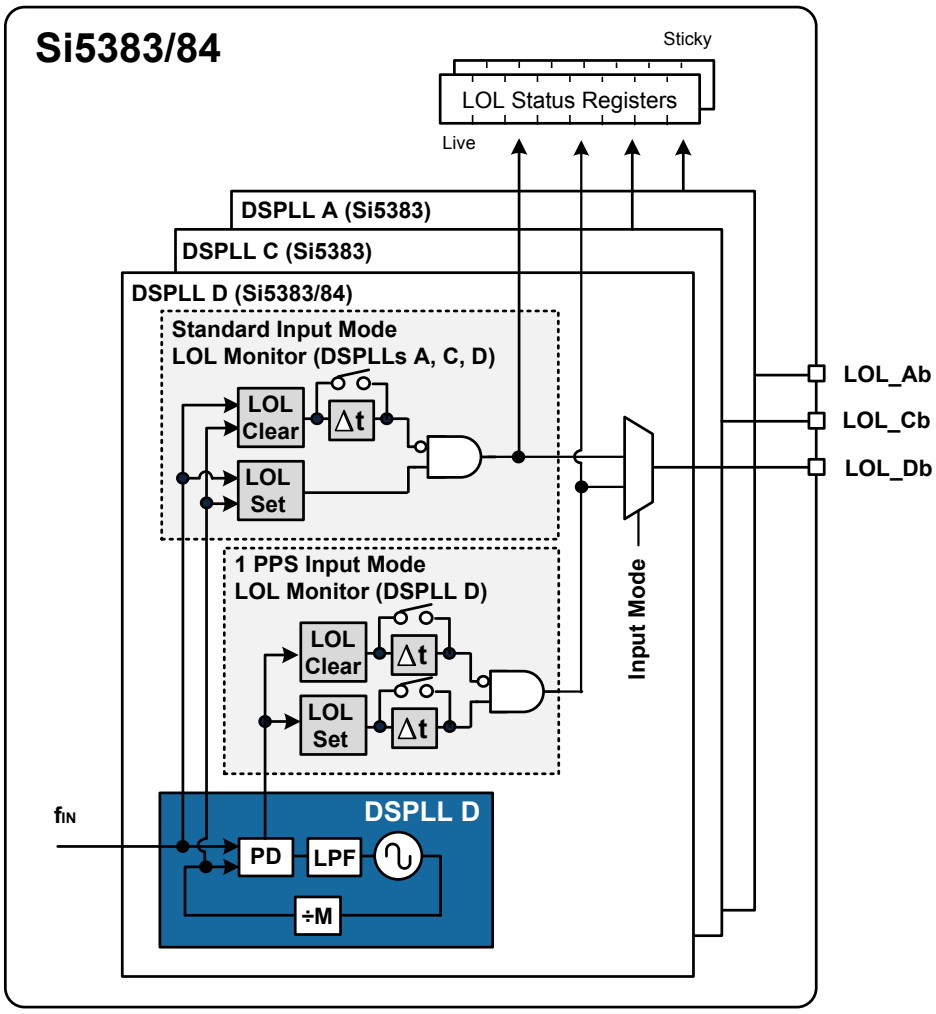


Figure 3.14. Si5383/84 LOL Status Indicators

3.9.6.1 LOL Detection Standard Input Mode

There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

Each of the LOL frequency monitors has adjustable sensitivity, which is register-configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference is shown in the figure below.

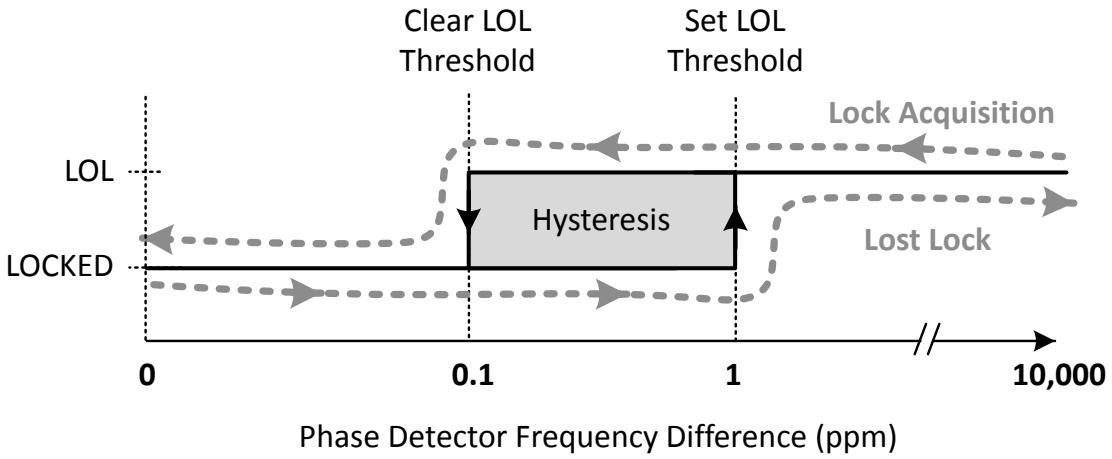


Figure 3.15. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilderPro utility.

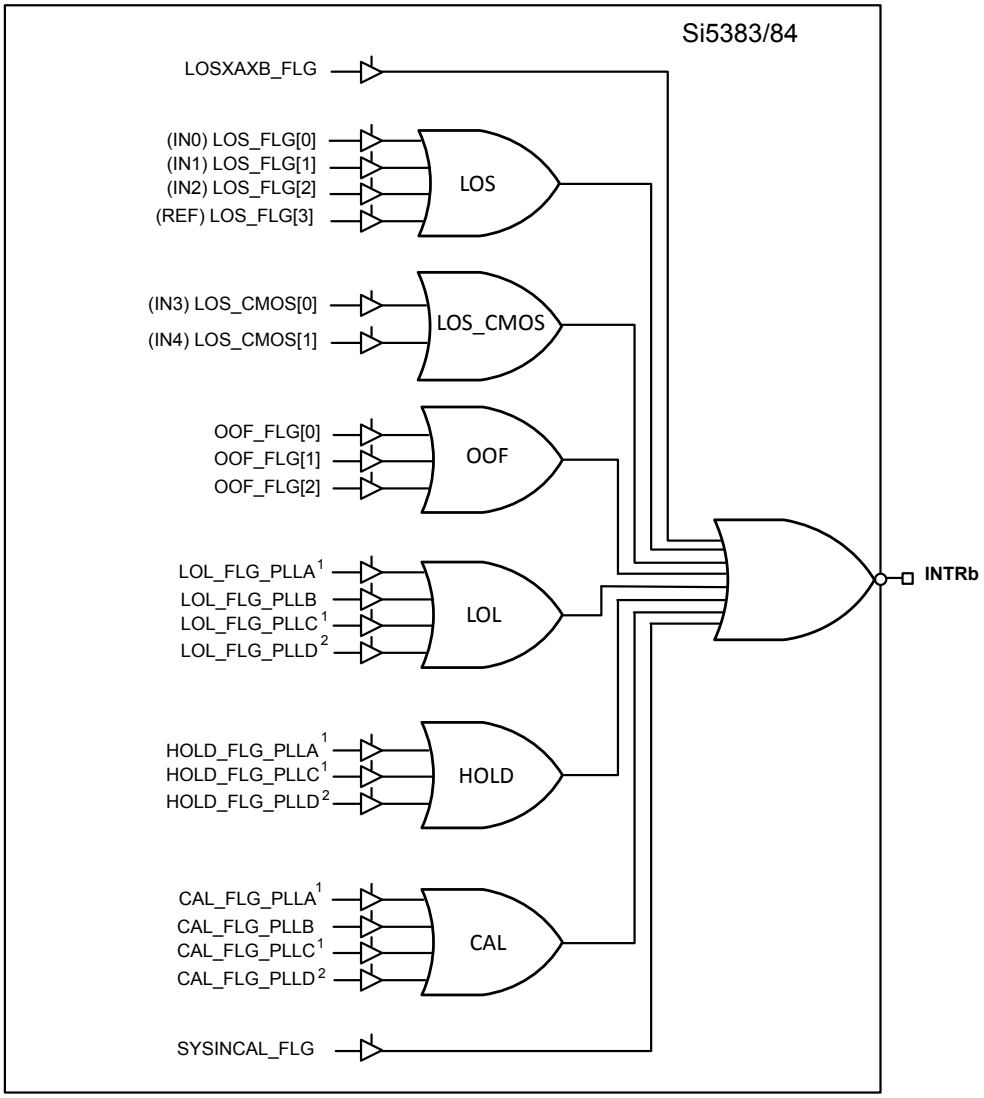
3.9.6.2 LOL Detection in 1 PPS Mode

DSPLL D implements a phase-based LOL detector when operating in PPS mode. Two independent phase error thresholds are included: one for LOL trigger and one for LOL clear. Having two separate phase error thresholds allows for hysteresis to help prevent chattering of the LOL status. An additional level of filtering is provided with trigger and clear counters. These counters represent the number of consecutive clock cycles a threshold must be met before the LOL alarm changes state. These counters prove useful when dealing with transient events, fault conditions, and locking to inputs with noise. For example, the DSPLL may see a large phase error between the time the input signal is lost and the LOS alarm is raised. The user must ensure LOL does not occur during this time to guarantee entry into holdover. This is accomplished by adjusting the LOL trigger counter to a larger value to compensate for this interval.

3.9.7 Interrupt Pin (INTRb)

In standard input mode, an interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

In 1 PPS input mode, the INTRb pin does not provide status indication for DSPLL D. When operating in this mode, loss of lock for DSPLL D can be monitored using the LOL_Db pin.



Notes:
1. Si5383 only
2. Standard input mode only

Figure 3.16. Interrupt Triggers and Masks

3.10 Outputs

The Si5383/84 supports seven differential output drivers. Each driver has a configurable voltage amplitude and common-mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 14 single-ended outputs, or a combination of differential and single-ended outputs. LVCMOS outputs can also be set for in-phase or complementary mode.

3.10.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.

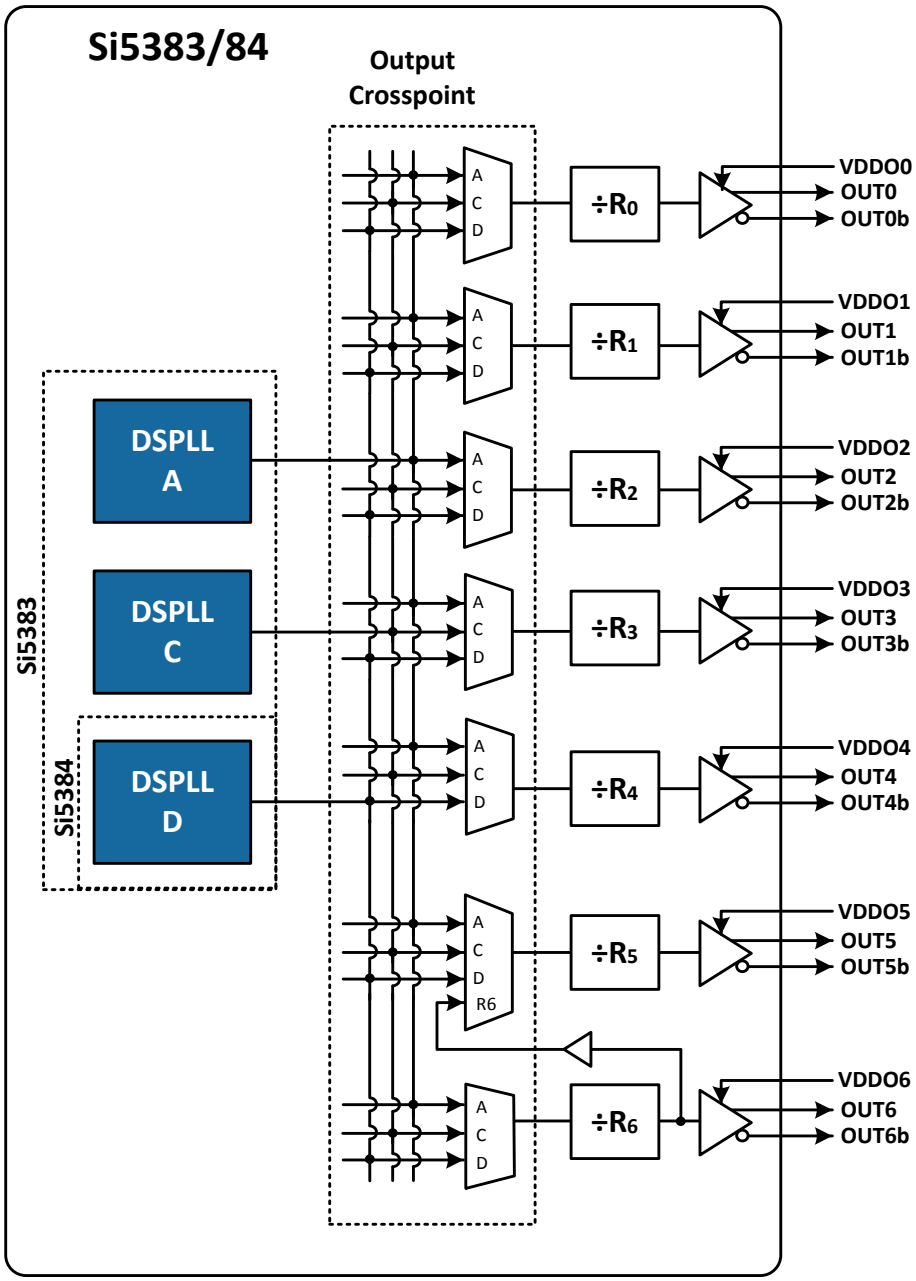


Figure 3.17. DSPLL to Output Driver Crosspoint

3.10.2 Support For 1 Hz Output

Output 5 of the Si5383/84 can be configured to generate a 1 Hz clock by cascading the R6 and R5 dividers. Output 6 cannot be powered down if Output 5 is used for generating a 1Hz clock. Output 6 is still usable in this case but is limited to a maximum frequency of 33.5 MHz. ClockBuilder Pro automatically determines the optimum configuration when generating a 1 Hz output (1 PPS).

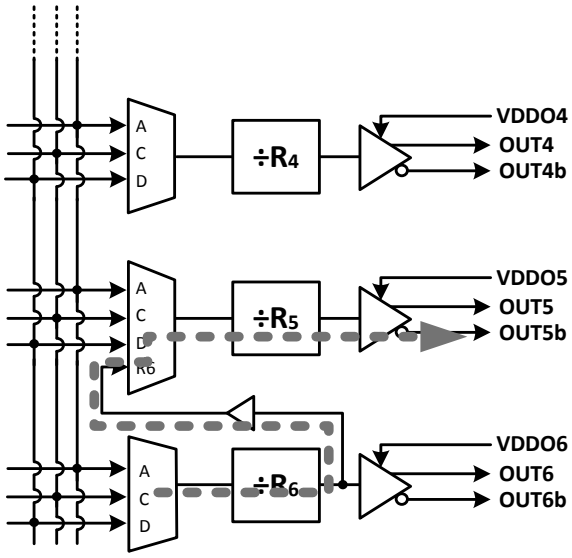
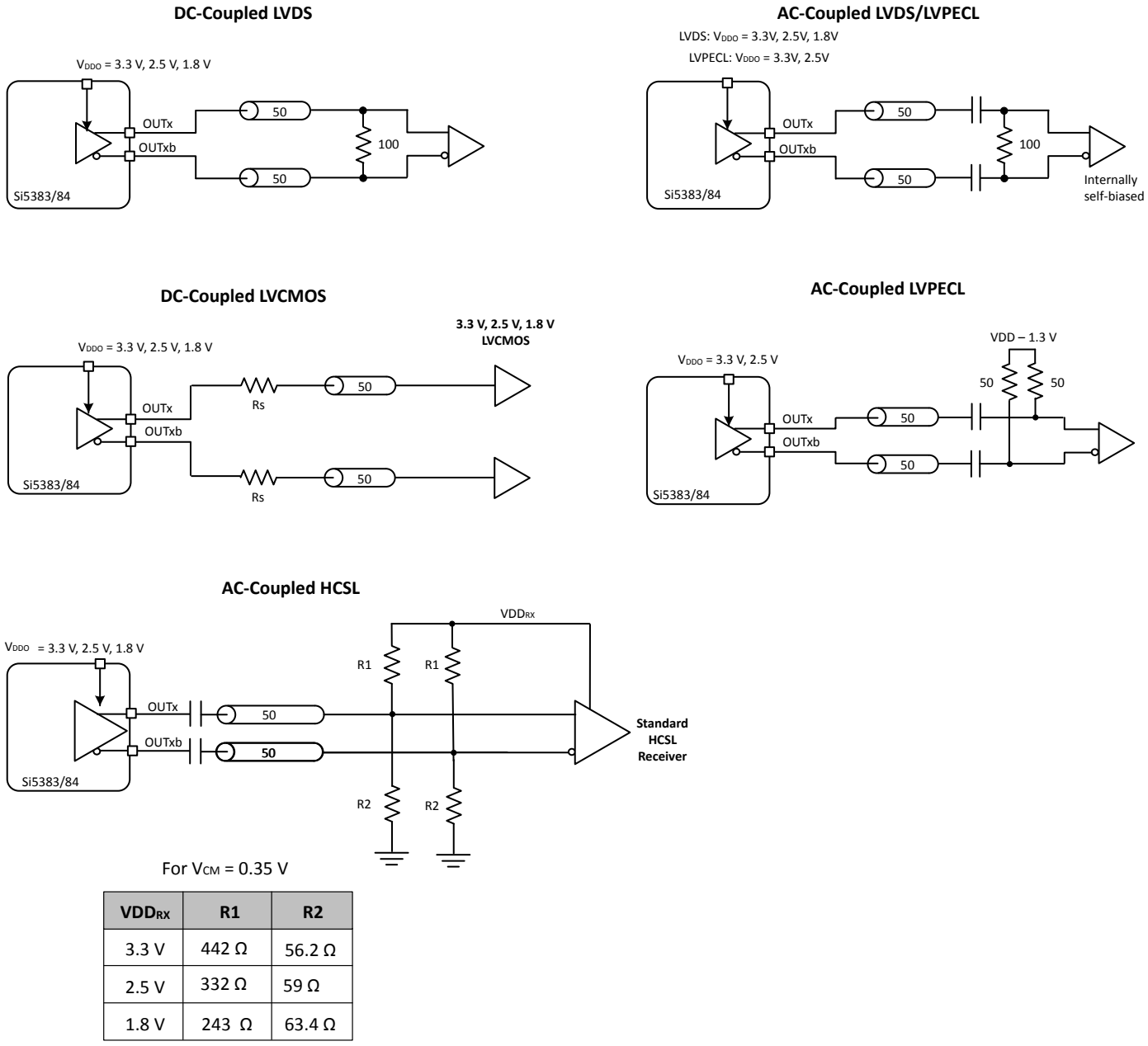


Figure 3.18. Generating a 1 Hz Output using the Si5383/84

3.10.3 Differential Output Terminations

Note: In this document, the terms LVDS and LVPECL refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in the figure below:



For V_{CM} = 0.35 V

VDD_{RX}	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 3.19. Supported Differential Output Terminations

3.10.4 Output Signal Format

The differential output amplitude and common-mode voltage are both programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 14 single-ended outputs or a combination of differential and single-ended outputs.

3.10.5 Programmable Common-Mode Voltage For Differential Outputs

The common-mode voltage (V_{CM}) for the differential modes is programmable and depends on the voltage available at the output's VDDO pin. Setting the common-mode voltage is useful when dc-coupling the output drivers.

3.10.6 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below. Note that selecting a lower source impedance may result in higher output power consumption.

Table 3.3. Typical Output Impedance (Z_S)

VDDO	CMOS_DRIVE_Selection		
	OUTx_CMOS_DRV=1	OUTx_CMOS_DRV=2	OUTx_CMOS_DRV=3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.10.7 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

3.10.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable, which enables either in-phase or complementary clock generation.

3.10.9 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high, all outputs are disabled. When held low, the outputs are enabled. Outputs in the enabled state can be individually disabled through register control.

3.10.10 Output Disable During LOL

By default, a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. In standard input mode, there is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.10.11 Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

3.10.12 Output Driver State When Disabled

The disabled state of an output driver is register configurable as disable low or high.

3.10.13 Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete. By default, ClockBuilder Pro configures outputs for synchronous disable.

3.10.14 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.10.15 Programmable Phase Offset in 1 PPS Mode

When 1 PPS mode is enabled, the Si5383/84 can be programmed to provide a static phase offset on all outputs generated by DSPLL D. This can be used for compensation of PCB trace delays to achieve accurate system phase alignment for 1 PPS.

3.11 Power Management

Unused inputs, output drivers, and DSPLLs can be powered down when unused. Consult the *Si5383/84 Reference Manual* and ClockBuilder Pro configuration utility for details.

3.12 In-Circuit Programming

The Si5383/84 is fully configurable using the I^2C interface. At power-up the device downloads its default register values from internal, flash-based, non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Firmware updates may also be written into NVM.

The NVM is in-circuit programmable with normal operating power supply voltages using the I^2C interface. The NVM update process starts by using ClockBuilder Pro to generate a boot record file. Once the boot record has been generated, it is necessary to place the device into bootloader mode via one of the following methods:

- Pin control: Drive the BLMDb pin low prior to negating the RSTb pin
- Register control: Write a boot reset sequence to the device over I^2C

Once the device has entered bootloader mode, the boot record file can be written to the device over I^2C. Refer to the *Si5383/84 Reference Manual* for a detailed procedure for writing registers to NVM.

3.13 Serial Interface

Configuration and operation of the Si5383/84 is controlled by reading and writing registers using the I^2C interface. Communication requires a 3.3 V I/O voltage. The A0 and A1 pins may be used to set the lower two bits of the I^2C base address if desired. Alternatively, the entire I^2C base address may be configured using ClockBuilder Pro.

3.14 Custom Factory Preprogrammed Parts

Custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will typically ship in two weeks.

3.15 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at www.silabs.com, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the *Si5383/84 Reference Manual*.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common-mode voltages for the clock outputs. After careful review of your project file and requirements, the Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the table below:

Table 3.4. Setting Overrides

Location	Customer Name	Type	Target	Dec Value	Hex Value
0x0435[0]	FORCE_HOLD_PLLA	No NVM	N/A	1	0x1
0x0B48[4:0]	OOF_DIV_CLK_DIS	User	OPN and EVB	31	0x1F

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the figure below:

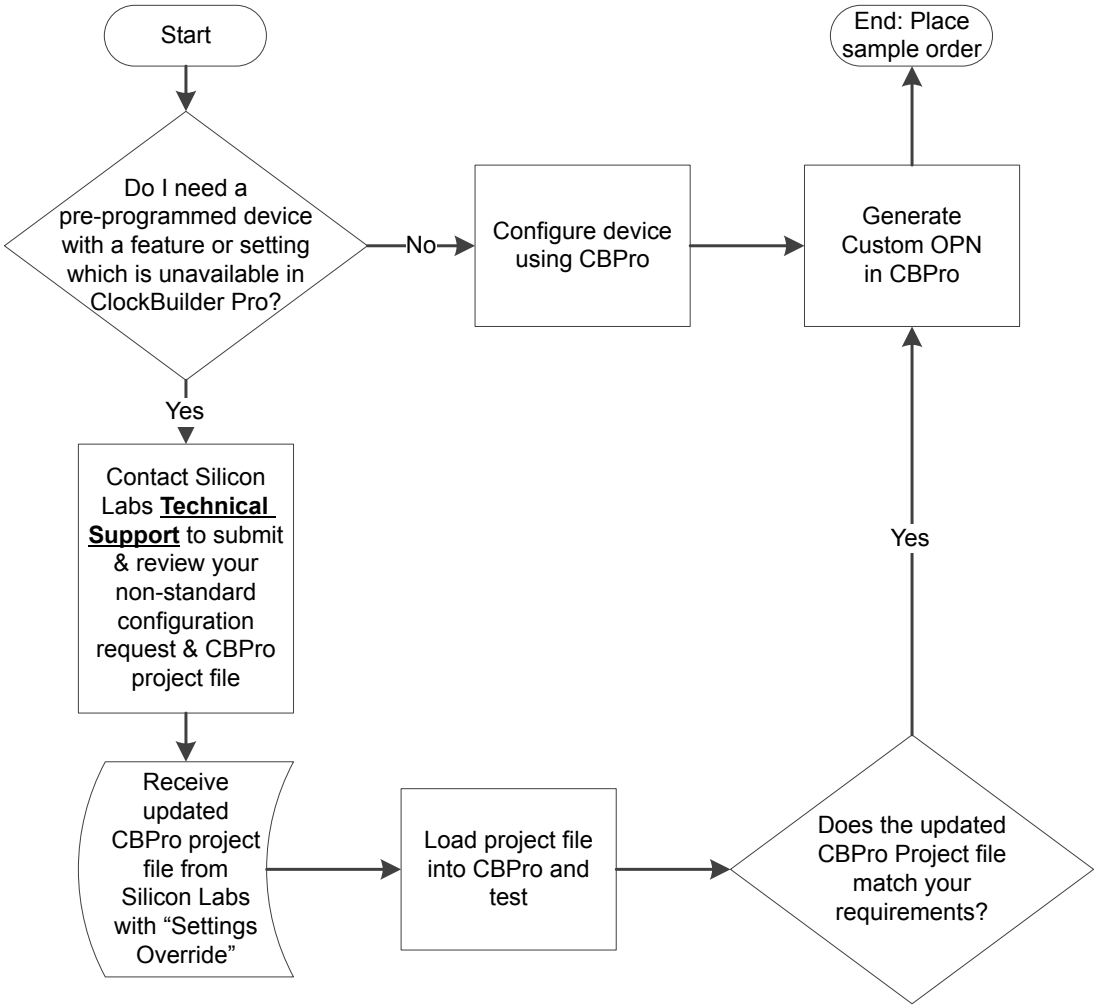


Figure 3.20. Process for Requesting Non-Standard CBPro Features

4. Register Map

Registers in the Si5383/84 require an I^2C command sequence to enable the reading and writing. Once the I^2C command sequences have been sent, it is necessary for the host to poll the status bits to indicate that the read or write command is complete. For read commands, data is available once the status bit indicates the command is complete. Refer to the *Si5383/84 Reference Manual* for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.					

Table 5.2. DC Characteristics

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

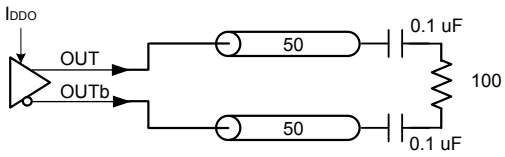
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Si5383, 1 PPS Input Mode[1]	—	245	390	mA
		Si5383, Standard Input Mode[2]	—	240	380	mA
		Si5384, 1 PPS Input Mode[1]	—	165	265	mA
	I_{DDA}	Si5383, 1 PPS Input Mode[1]	—	160	190	mA
		Si5383, Standard Input Mode[2]	—	160	190	mA
		Si5384, 1 PPS Input Mode[1]	—	155	180	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[3] @ 156.25 MHz	—	22	26	mA
		LVDS Output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] Output @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS[4] Output @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS[4] Output @ 156.25 MHz	—	12	16	mA
Total Power Dissipation[5]	P_d	Si5383, 1 PPS Input Mode[1]	—	1265	1620	mW
		Si5383, Standard Input Mode[2]	—	1255	1610	mW
		Si5384, 1 PPS Input Mode[1]	—	1100	1410	mW
Analog Supply Voltage Ramp Time	t_{RMP_VDDA}	Time to V_{DDA} > 2.2 V	10	—	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. Test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. 1 PPS input enabled on DSPLL D. Excludes power in termination resistors.
2. Test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. 1 PPS input not enabled. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV=3, which is the strongest driver setting. Refer to the *Si5383/84 Reference Manual* for more details on register settings.
5. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

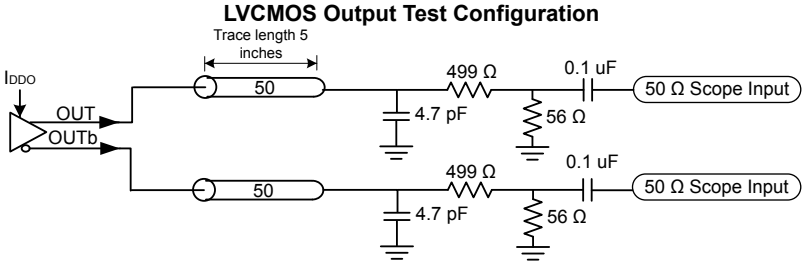


Table 5.3. Input Clock Specifications

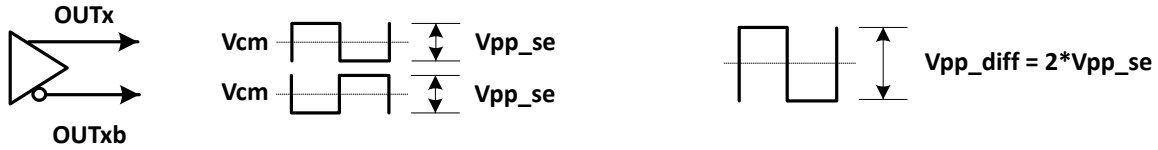
(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Input Buffer with Differential or Single-Ended Configuration - AC-Coupled (IN0, IN1, IN2, REF)						
Input Frequency Range	f_{IN}	Differential	0.008	—	750	MHz
		Single-ended/LVCMOS	0.008	—	250	
		REF	5	—	250	
Voltage Swing [1]	V_{IN}	Differential AC-coupled f_{IN}< 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled 250 MHz < f_{IN}< 750 MHz	225	—	1800	mVpp_se
		Single-Ended AC-coupled f_{IN} < 250 MHz	100	—	3600	mVpp_se
Slew Rate [2,3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		—	2.4	—	pF
Input Resistance	R_{IN}	Differential	—	16	—	kΩ
		Single-ended/LVCMOS	—	8	—	
LVCMOS/Pulsed CMOS - DC-Coupled (IN0, IN1, IN2) [4]						
Input Frequency	f_{IN_CMOS}	LVCMOS Mode	0.008	—	250	MHz
		Pulsed CMOS Mode	0.008	—	1	MHz
		1 PPS Mode	—	1	—	Hz
Input Voltage	V_{IL}		—	—	0.4	V
	V_{IH}		0.8	—	—	V
Slew Rate [2,3]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	LVCMOS CMOS Mode (250 MHz @ 40% Duty Cycle)	1.6	—	—	ns
		Pulsed CMOS (1 MHz @ 5% Duty Cycle)	50	—	—	ns
		1 PPS Mode	10	—	—	us
Duty Cycle	DC	LVCMOS	40	—	60	%
		Pulsed CMOS	5	—	95	%
Input Resistance	R_{IN}		—	8	—	kΩ
LVCMOS - DC Coupled (IN3, IN4)						
Input Frequency	f_{IN_PULSED}	Standard Mode	0.008	—	2.048	MHz
		1 PPS Mode	—	1	—	Hz
Input Voltage	V_{IL}		—	—	$0.3xV_{DDA}$	V
	V_{IH}		$0.7xV_{DDA}$	—	—	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width	PW	Standard Mode, Pulse Input	50	—	—	ns
		1 PPS Mode, Pulse Input	10	—	—	us
Input Resistance	R_{IN}		—	20	—	kΩ
XA/XB (if driven from external oscillator)						
XA/XB Frequency	f_{IN_XAXB}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Frequency range for best output jitter performance.	48	—	54	MHz
Input Voltage Swing	V_{IN_SE}	Single-ended	365	—	2000	mVpp_se
	V_{IN_DIFF}	Differential	365	—	2500	mVpp_diff
Slew rate [2,3]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Note:

1. Voltage swing is specified as single-ended mVpp.



2. Imposed for jitter performance.
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) \times V_{IN_Vpp_se}) / SR$.
4. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.4 and 0.8 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the *Si5383/84 Reference Manual*. Otherwise, for standard LVCMOS input clocks, use the Standard AC-coupled, Single-ended input mode.

Table 5.4. Control Input Pin Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5383/84 Control Input Pins (FINC, FDEC, OEb)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDA}	V
	V_{IH}		0.7 x V_{DDA}	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	FINC, FDEC	100	—	—	ns
Update Rate	F_{UR}	FINC, FDEC	—	—	1	MHz
Si5383/84 Control Input Pin (SCL, SDA, A1, A0, BLMDb, RSTb)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDA}	V
	V_{IH}		0.7 x V_{DDA}	—	—	V
Input Capacitance	C_{IN}		—	7	—	pF
Minimum Reset Pulse Width	PW		15	—	—	µs

Table 5.5. Differential Clock Output Specifications

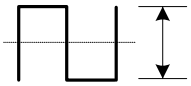
(VDD = 1.8 V ±5%, VDDA = 3.3V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}	Standard input mode		0.0001	—	718.5	MHz
		DSPLL D in 1 PPS mode		0.0001	—	685	MHz
	f_{OUT1Hz}	1 PPS signal only available on Output 5		—	1	—	Hz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 718.5 MHz		45	—	55	%
Output-Output Skew	T_{SK}	Outputs on same DSPLL (measured at 712.5 MHz)		—	—	65	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	50	ps
Output Voltage Amplitude [1]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	430	510	mVpp_se
		V_{DDO} = 3.3 V, or 2.5 V	LVPECL	640	750	900	
Common-Mode Voltage [1]	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.20	1.30	V
			LVPECL	1.90	2.00	2.10	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.10	1.20	1.30	
		V_{DDO} = 1.8 V	sub-LVDS	0.80	0.90	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F			—	100	150	ps
Differential Output Impedance	Z_O			—	100	—	Ω
Power Supply Noise Rejection [2]	PSRR	10 kHz sinusoidal noise		—	–99	—	dBc
		100 kHz sinusoidal noise		—	–96	—	
		500 kHz sinusoidal noise		—	–94	—	
		1 MHz sinusoidal noise		—	–93	—	
Output-output Crosstalk [3]	XTALK	Measured spur from adjacent output [3]		—	–86	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. Output amplitude and common-mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the *Si5383/84 Family Reference Manual* for more suggested output settings. Not all combinations of voltage amplitude and common-mode voltages settings are possible.



2. Measured for 156.25 MHz carrier frequency. 100mVpp of sinewave noise added to VDDO = 3.3V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems, for guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

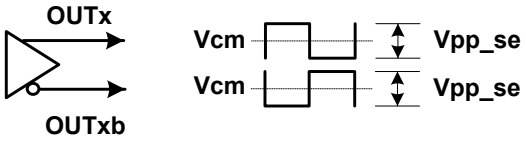


Table 5.6. LVCMOS Clock Output Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3V ±5%, VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, TA = –40 to 85 °C)

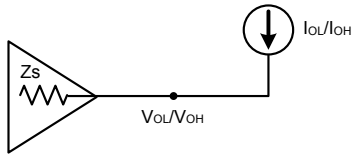
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
	f_{OUT1Hz}	Only Available on Output 5		—	1	—	Hz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		45	—	55	
Output-to-Output Skew	T_{SK}	When outputs are on same DSPLLs with the same R dividers		—	30	140	ps
Output Voltage High [1,2,3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = -10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = -12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = -17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = -6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = -8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = -11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = -4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = -5 mA		—	—	

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Low [1,2]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times [3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	400	600	ps
		VDDO = 2.5 V		—	450	600	ps
		VDDO = 1.8 V		—	550	750	ps

Note:

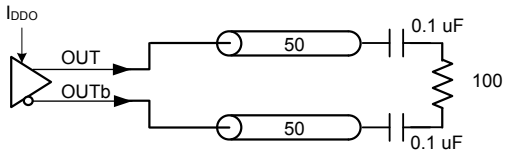
1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the *Si5383/84 Reference Manual* for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.

DC Test Configuration



3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

Differential Output Test Configuration



LVCMOS Output Test Configuration

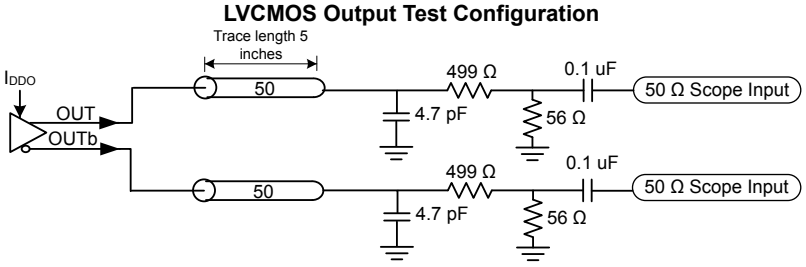


Table 5.7. Output Status Pin Specifications

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5383/84 Status Output Pins (INTRb, LOL_Ab, LOL_Cb, LOL_Db, and LOL_REF)						
Output Voltage	V_{OH}	I_{OH} = -2 mA	V_{DDA} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDA} x 0.15	V
Si5383/84 Status Output Pins (SDA, SCL and RSTb)[1, 2]						
Output Voltage	V_{OL}	I_{OL} = 6.5 mA	—	—	0.6	V

Note:

1. V_{OH} specifications do not apply apply to open-drain outputs.
2. SCL driven low during clock stretching. RSTb driven low during power up and when VDDA falls below minimum operating threshold.

Table 5.8. Performance Characteristics

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range [2]	f_{BW}		0.001	—	4000	Hz
Initial Start-Up Time[1]	t_{START}	1 PPS Input Mode, after Power-Up or Hardware Reset	—	3.1	4.25	s
		Standard Input Mode, after Power-Up or Hardware Reset	—	0.04	0.17	s
PLL Lock Time	t_{ACQ}	Standard Mode, with Fastlock enabled [3]	—	280	300	ms
		1 PPS Mode[8] Phase error < 10 ns	—	25	—	s
		1 PPS Mode [9] Fully Locked	—	2	—	min
		f_{IN} = 19.44 MHz; Ramped Exit from Holdover enabled (recommended)[10]	—	1900	—	ms
Serial Interface Ready Time [4]	t_{RDY}	After Power-Up or Hardware Reset	—	—	75	ms
Flash Memory Endurance (Write/Erase Cycles)	N_{WE}		20 k	100 k	—	Cycles
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz	—	—	0.1	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2, Standard Input Mode Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch [7]	t_{SWITCH}	Standard input mode, single manual or automatic switch between two input clocks at same frequency.	—	—	1.2	ns
Pull-in Range [6]	ωP	Standard mode	—	500	—	ppm
	ωP_{1PPS}	1 PPS mode	-10	—	+10	ppm
1 PPS Input-to-Output Phase Delay	t_{DELAY_1PPS}	1 PPS mode. Assumes noise-free 1 PPS and reference inputs. Measured between a 1 PPS input and 1 PPS output from DSPLL D after fully settling.	-10	—	10	ns
RMS Phase Jitter [5]	J_{GEN}	12 kHz to 20 MHz	—	0.130	—	ps RMS

Notes:

1. Time from hardware reset or when VDD reaches 90% of nominal value to when the device generates free-running clocks.
2. Actual loop bandwidth might be lower; please refer to CBPro for actual value on your frequency plan.
3. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with fastlock bandwidth set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
4. Time from hardware reset or when VDD reaches 90% of nominal value to when the serial interface is ready to respond to commands.
5. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL. (Does not include jitter from input reference).
6. With respect to 0 ppm assuming REF input is ±5 ppm.
7. For input frequency configurations which have F_{PFD} > 1 MHz. Consult your CBPro design report for the F_{PFD} frequency of your configuration.
8. Time from first rising edge on 1 pps input until the phase offset between the input and output 1 pps signals is <10 ns (assumes 0 ns static phase offset between input and output 1 pps signals).
9. Time from first rising edge on 1 pps input until LOL alarm clears. Assumes noise-free 1 pps and reference inputs, and 1 mHz or 10 mHz loop bandwidth. Lock declared when the settling error is below 75/FVCO.
10. Lock time is also affected by frequency ramping when exiting from holdover, and can extend for several seconds depending on multiple settings. Please consult the Reference Manual for more details.

Table 5.9. I²C Timing Specifications (SCL,SDA)

(VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		-	100	—	400	kHz
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs

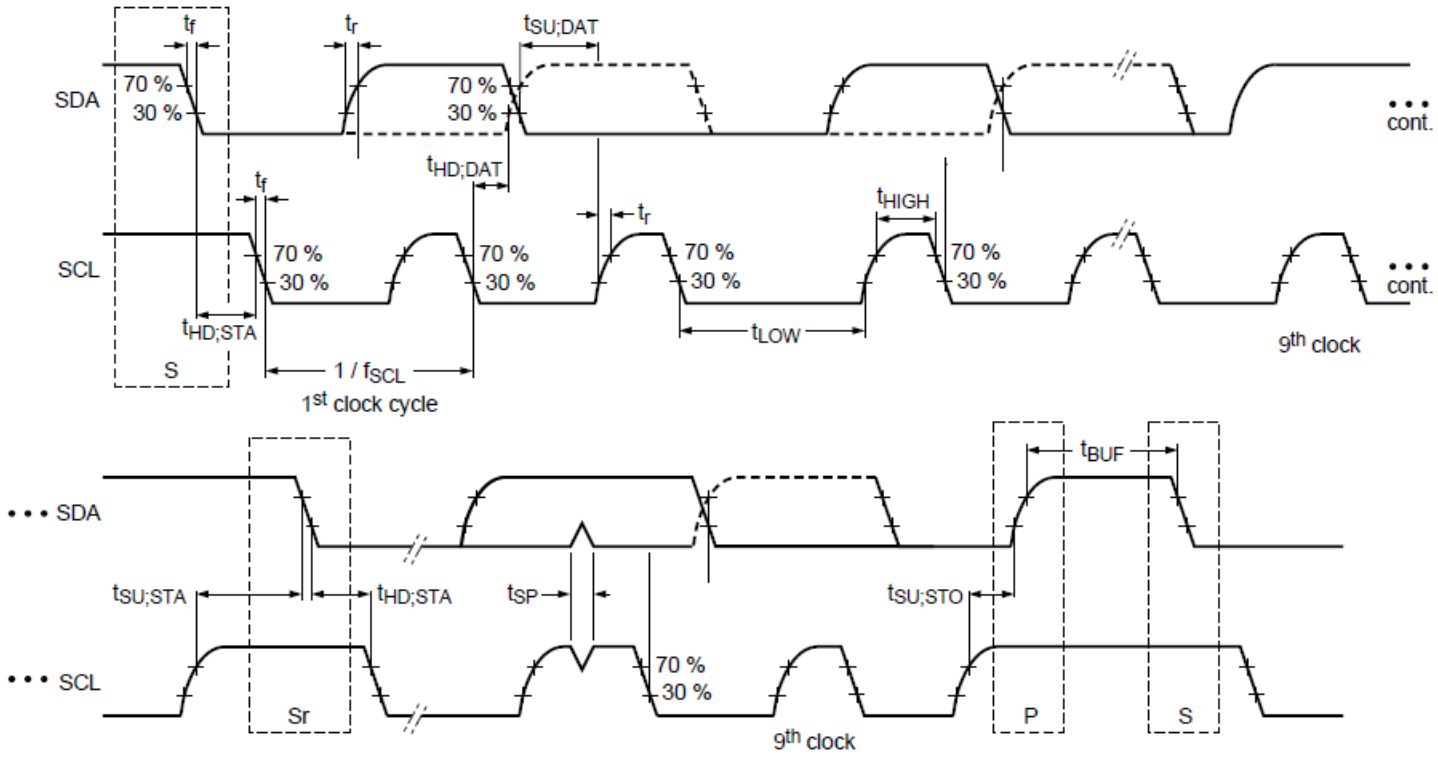


Figure 5.3. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. Crystal Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	f_{XTAL}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance Shunt Capacitance	$r_{ESR\ CO}$	Refer to the *Si5383/84 Reference Manual* to determine ESR and shunt capacitance.				

Note:

1. Refer to the *Si534x/8x Jitter Attenuating Clock, Recommended Crystal, TCXO and OCXO Reference Manual* for recommended 48 to 54 MHz crystals. The Si5383 and Si5384 are designed to work with crystals that meet these specifications.

Table 5.11. Thermal Characteristics

Parameter	Symbol	Test Condition [1]	Value	Unit
Si5383-56LGA and Si5384-56LGA				
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	24.0	°C/W
Thermal Resistance Junction to Case	Θ_{JC}		9.5	
Thermal Resistance Junction to Board	Θ_{JB}		7.7	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.5	

Note:

1. Based on PCB Dimension: 4" × 4.5", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.

Table 5.12. Absolute Maximum Ratings [1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
DC Supply Voltage	V_{DD}		–0.3 to 3.8	V
	V_{DDA}		–0.3 to 3.8	V
	V_{DDO}		–0.3 to 3.8	V
Input Voltage Range	V_{I1}	IN0 - IN2, REF	–1.0 to V_{DDA} + 0.3	V
	V_{I2}	IN3, IN4, OEb, FINC, FDEC	–0.5 to V_{DDA} + 0.3	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
	V_{I4}	RSTb, SDA, SCL, A1, A0, BLMDb	–0.3 to V_{DDA} + 0.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Max Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile) [3]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile) [4]	T_P		20-40	s

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 56-LGA package is RoHS-6 compliant.
3. For detailed MSL and packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

6. Typical Application Diagrams

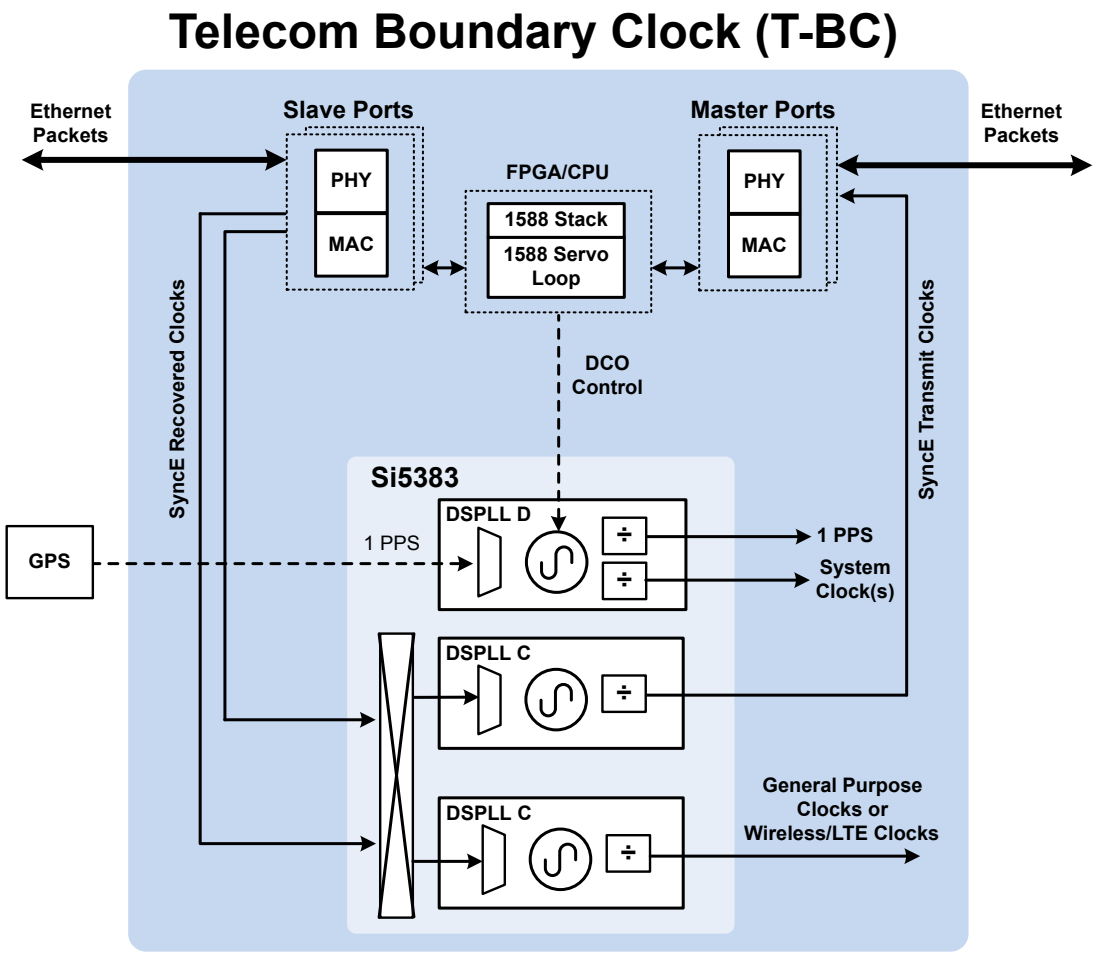


Figure 6.1. Using the Si5383/84 as a Telecom Boundary Clock

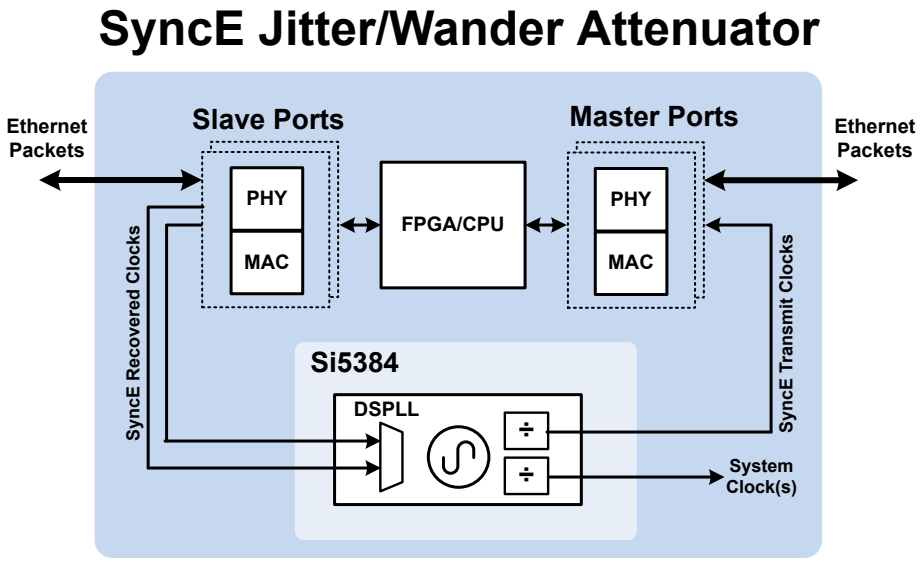


Figure 6.2. Si5384 as a SyncE Jitter/Wander Attenuator

IEEE 1588 DCO

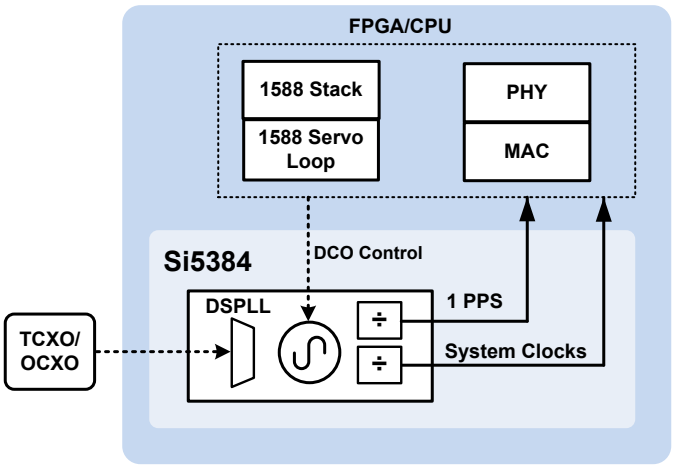


Figure 6.3. Si5384 as an IEEE 1588 DCO

GPS 1 PPS Clock Multiplier

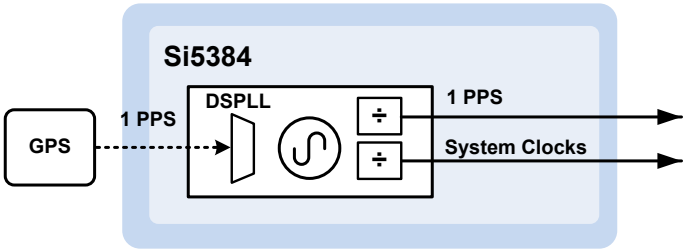


Figure 6.4. Si5384 as a 1 Hz/1 PPS Clock Multiplier

7. Detailed Block Diagram

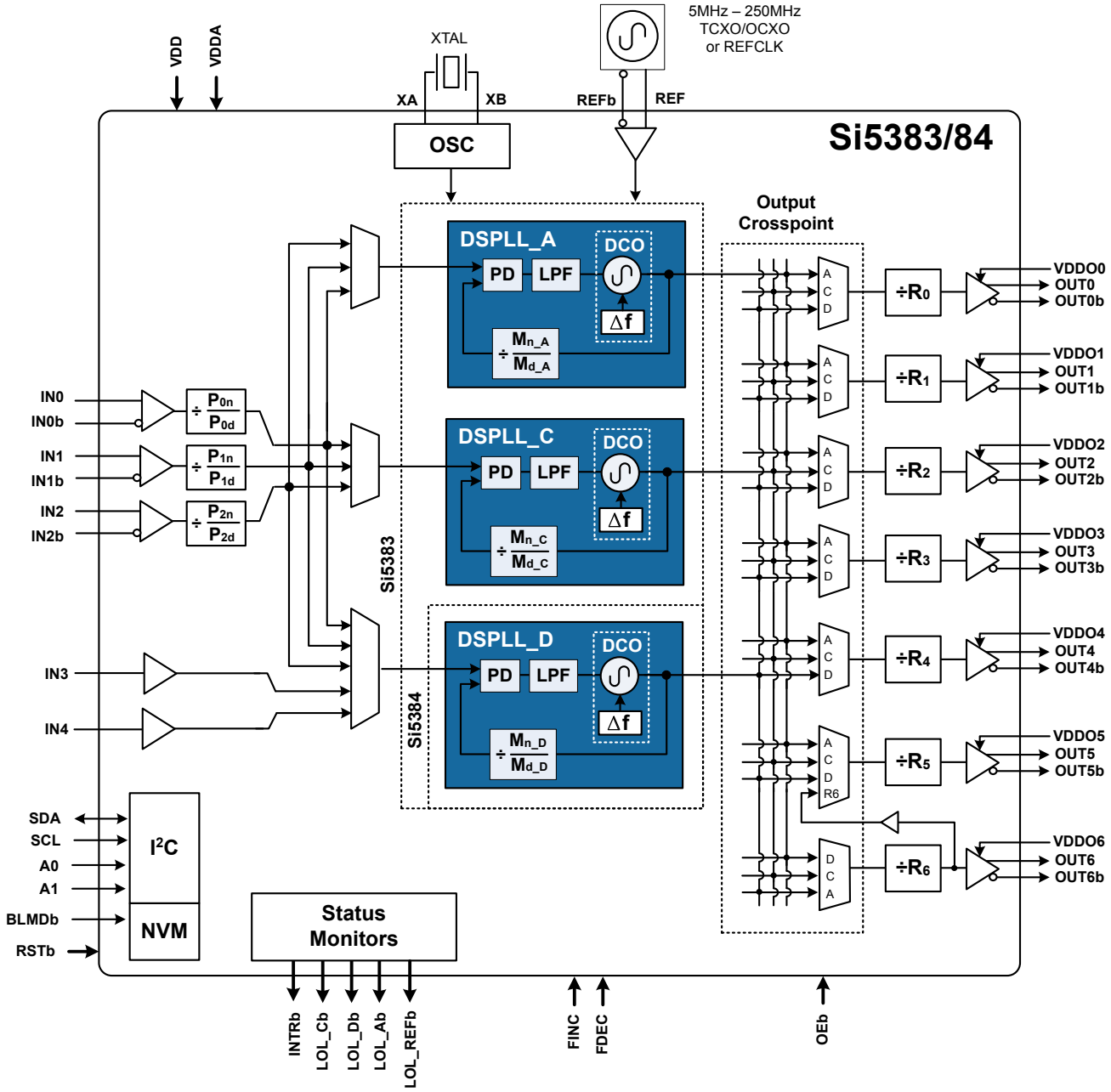


Figure 7.1. Si5383/84 Detailed Block Diagram

8. Typical Operating Characteristics (Jitter and Phase Noise)

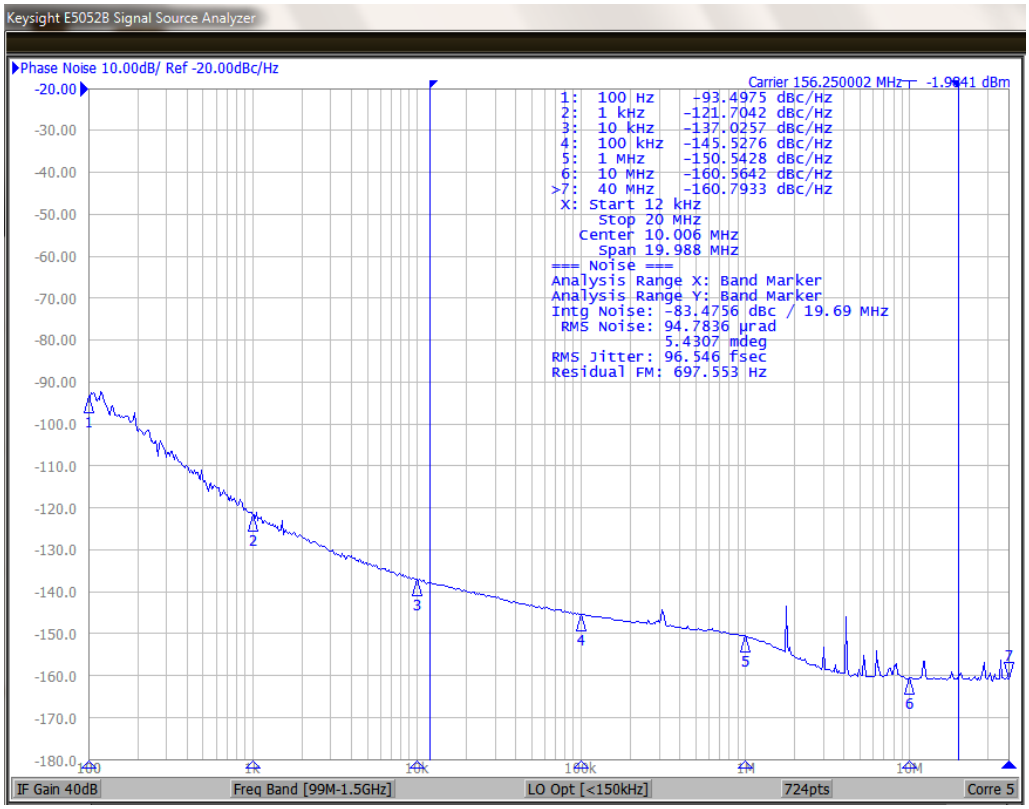


Figure 8.1. F_{IN} = 19.44 MHz; F_{OUT} = 156.25 MHz, 3.3 V LVPECL with Rakon 12.8 MHz Reference, 48 MHz Crystal

9. Pin Descriptions

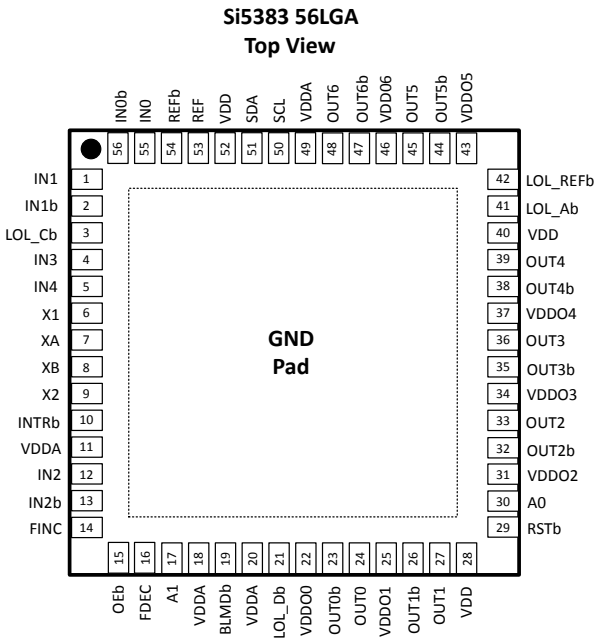


Figure 9.1. Si5383 Pins

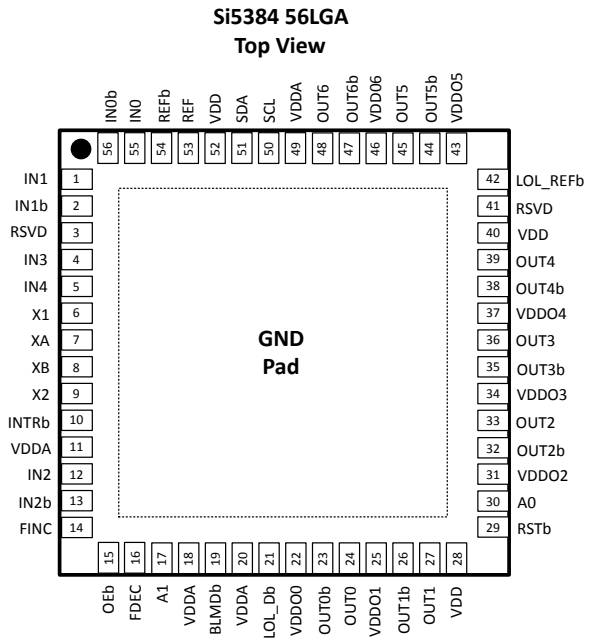


Figure 9.2. Si5384 Pins

Table 9.1. Si5383/84 Pin Descriptions [1]

Pin Name[1]	Pin Number	Pin Type [2]	Function
Inputs			
XA	7	I	**Crystal Input**. Input pin for external crystal (XTAL).
XB	8	I	
X1	6	I	**XTAL Shield**. Connect these pins directly to the XTAL ground pins. The XTAL ground pins should be separated from the PCB ground plane. Refer to the *Si5383/84 Reference Manual* for layout guidelines.
X2	9	I	
IN0	55	I	**Clock Inputs**. IN0-IN2 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to Input Configuration and Terminations input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock. IN3 and IN4 only support single ended LVCMOS signals.These pins are high-impedance and must be terminated externally. IN0-IN2 can be disabled by register configuration and the pins left unconnected if unused. IN3 and IN4 must be externally pulled low when unused.
IN0b	56	I	
IN1	1	I	
IN1b	2	I	
IN2	12	I	
IN2b	13	I	
IN3	4	I	
IN4	5	I	
REF	53	I	**Reference Input**. This input accepts a reference clock from a stable source (eg. TCXO or OCXO) that is used to determine free-run frequency accuracy and stability during free-run or holdover of the DSPLL or DCO. These inputs can accept differential or single-ended connections. Refer to the *Si5383/84 Reference Manual* for recommended TCXOs and OCXOs.
REFb	54	I	

Pin Name[1]	Pin Number	Pin Type [2]	Function
Outputs			
OUT0	24	O	**Output Clocks**. These output clocks support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable using register control.Termination recommendations are provided in Differential Output Terminations. Unused outputs should be left unconnected.
OUT0b	23	O	
OUT1	27	O	
OUT1b	26	O	
OUT2[3]	33	O	
OUT2b[3]	32	O	
OUT3	36	O	
OUT3b	35	O	
OUT4	39	O	
OUT4b	38	O	
OUT5	45	O	
OUT5b	44	O	
OUT6	48	O	
OUT6b	47	O	
Serial Interface			
SDA	51	I/O	**Serial Data Interface**. This is the bidirectional data pin (SDA) for the I^2C interface. This pin must be pulled high to V_{DDA} using an external resistor of at least 1 kΩ.
SCL	50	I/O	**Serial Clock Input Interface**. This is the bidirectional I^2C clock pin. Clock stretching (i.e., driving SCL low to insert wait-states) will be utilized when operating at rates greater than 100 kHz. This pin must be pulled up to V_{DDA} using an external resistor of at least 1 kΩ.
A1	17	I/O	**I^2C Address Select 1**. This pin functions as the optional A1 I^2C address input pin. Attach a 4.7 kΩ pull-up resistor to V_{DDA}, or a 4.7 kΩ pull-down resistor to ground to select the I^2C slave address. This pin can be left floating if unused.
A0	30	I/O	**I^2C Address Select 0**. This pin functions as the optional A0 I^2C address input pin. Attach a 4.7 kΩ pull-up resistor to V_{DDA}, or a 4.7 kΩ pull-down resistor to ground to select the I^2C slave address. This pin can be left floating if unused.
Control/Status			
INTRb	10	O	**Interrupt**. This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	29	I/O	**Device Reset**. This pin functions as an active-low reset input/output. As an input, the pin is used to generate a device reset when held low for more than 15 us. This resets all internal logic to a known state and forces device registers to their default values. Clock outputs are disabled during reset. As an open-drain output, the pin will be driven low during POR. External devices must be configured as open-drain to avoid contention.
OEb	15	I	**Output Enable**. This output enable pin has a programmable register mask which allows it to control any of the output clocks. By default the OEb pin enables all output clocks. This pin must be externally pulled low when not in use.

Pin Name[1]	Pin Number	Pin Type [2]	Function
LOL_Ab (Si5383 only)	41	O	**Loss of Lock_A/C/D/REF**. These output pins indicate when DSPLL A, C, D and the REF input is out-of-lock (low) or locked (high). They can be left unconnected when not in use.
LOL_Cb (Si5383 only)	3	O	
LOL_Db	21	O	
LOL_REF	42	O	
FDEC	16	I	**Frequency Decrement Pin**. This pin is used to step-down the output frequency of a selected DSPLL. The frequency change step size is register configurable. This pin must be externally pulled low when not in use.
FINC	14	I	**Frequency Increment Pin** . This pin is used to step-up the output frequency of a selected DSPLL. The frequency change step size is register configurable. This pin must be externally pulled low when not in use.
BLMDb	19	I	**Bootloader Enable**. This pin should be driven low on reset negation to enable bootloader mode. Under normal operation, this pin should be pulled up to V_{DDA} with a 4.7K resistor.
RSVD (Si5384 only)	41	—	**Reserved**. Leave disconnected.
	3	—	
Power			
VDD	28	P	**Core Supply Voltage**. The device core operates from a 1.8 V supply. See the *Si5383/84 Reference Manual* for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	40		
	52		
VDDA	11	P	**Core Supply Voltage 3.3 V**. This core supply pin requires a 3.3 V power source. See the *Si5383/84 Reference Manual* for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	18		
	49		
	20		
VDDO0	22	P	**Output Clock Supply Voltage 0-6**. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins.
VDDO1	25	P	
VDDO2	31	P	
VDDO3	34	P	
VDDO4	37	P	
VDDO5	43	P	
VDDO6	46	P	
GND PAD	—	P	**Ground Pad**. This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plane as short as possible.

Note:

1. Refer to the *Si5383/84 Reference Manual* for more information on register setting names.
2. I = Input, O = Output, P = Power.
3. If this output is not used, it should be brought out to a test point to facilitate system debug.

10. Package Outline

The figure below illustrates the package details for the Si5383/84. The table below lists the values for the dimensions shown in the illustration.

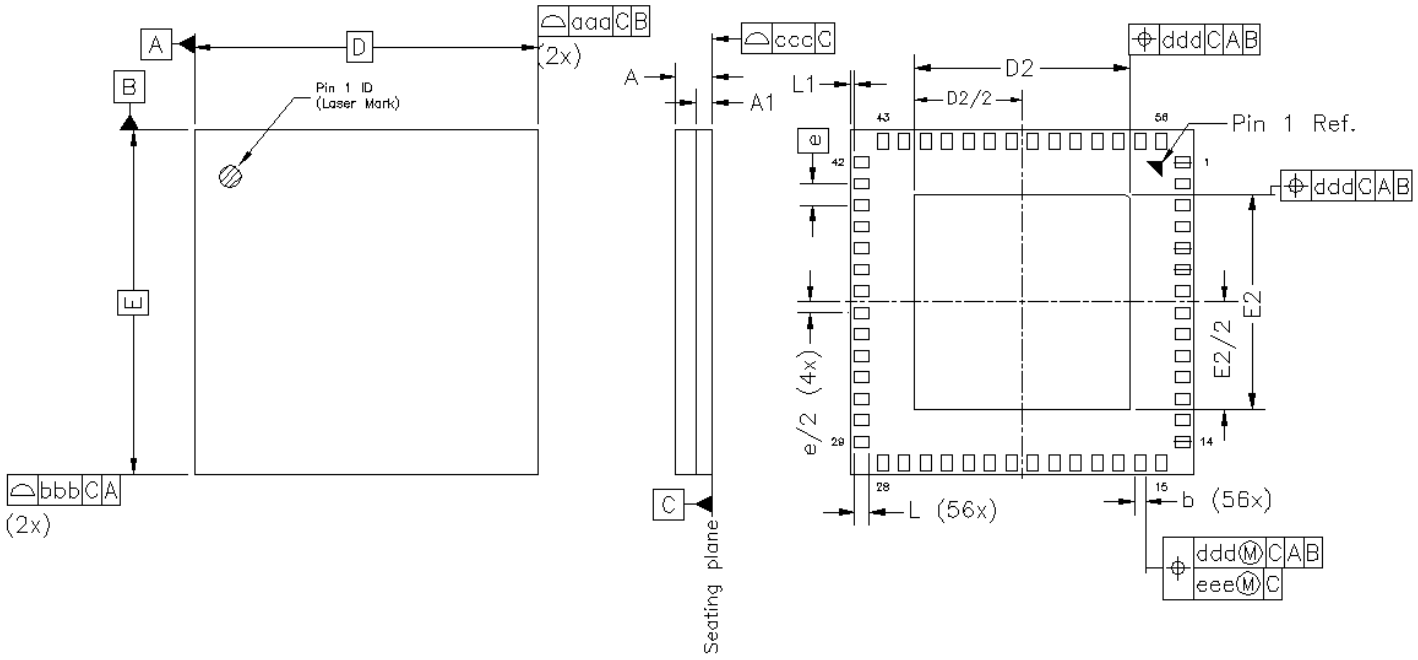


Figure 10.1. Si5383/84 8x8 mm 56-Pin LGA

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.22	0.26	0.30
b	0.20	0.25	0.30
D		8.00 BSC	
D2	4.80	4.90	5.00
e		0.50 BSC	
E		8.00 BSC	
E2	4.80	4.90	5.00
L		0.363 BSC	
L1	0.00	0.12	0.18
aaa	—	—	0.10
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.15
eee	—	—	0.05

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration. Refer to the *Si5383/84 Reference Manual* for information about thermal via recommendations.

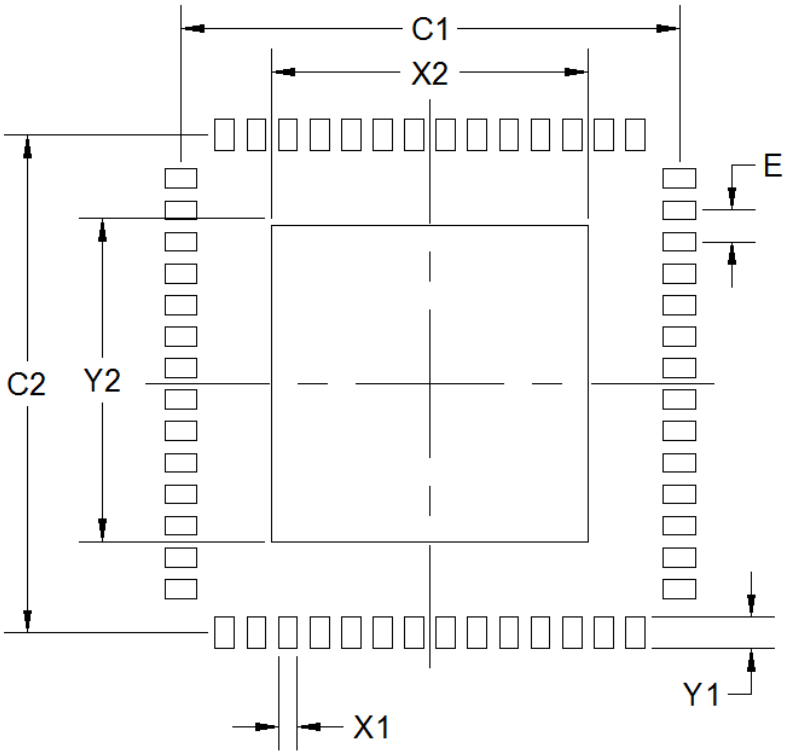


Figure 11.1. Si5383/84 PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5383/84 IPC-7351 (Max)	Si5383/84 Alternative Dimensions with Larger Pads (Max)[1]
C1	7.50	7.90
C2	7.50	7.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.45	0.85
X2	4.95	4.95
Y2	4.95	4.95

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. LGA package solder stencil design should match the respective ground pads as shown in the Package outline.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Alternative Land Pattern

1. This alternative land pattern may be used if desired to facilitate easier rework and/or manual soldering

12. Top Marking

Figure 12.1. Si5383 Top Marking

Figure 12.2. Si5384 Top Marking

Table 12.1. Top Marking

Line	Characters	Description
1	Si5383g- Si5384g-	Base part number and Device Grade. Si5383: 3-PLL Packet Network Synchronizer for SyncE/1588 Si5384: 1-PLL Packet Network Synchronizer for SyncE/1588 g = Device Grade. See Chapter 2. Ordering Guide for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (See Chapter 2. Ordering Guide for current revision.) xxxxx = Customer specific NVM sequence number or firmware revision number. -GM = Package (LGA) and temperature range (–40 to +85 °C).
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm diameter	Pin 1 indicator; left-justified
	e4	Pb-free symbol; Center-Justified
	TW	TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

14. Revision History

Revision 1.1

June, 2019

- Updated Figure 3.5 Crystal Resonator Connections on page 12.
  - Updated Crystal Resonator Connection diagram and added connection diagrams for Differential XO/Clock and Single-Ended XO.
- Updated Figure 3.6 External Reference Connections on page 13.
  - Updated diagram with addition information on input divider circuity to attenuate input to not exceed spec limit.
- Updated Figure 3.19 Supported Differential Output Terminations on page 24.
  - Updated AC-Coupled LVDS/LVPECL figure to clarify LVDS and LVPECL Vddo voltage support.
- Updated 3.10.8 LVCMOS Output Polarity.
  - Clarified language used to describe that LVCMOS output polarity is configurable, enabling either in-phase or complementary clock generation.
- Updated 5. Electrical Specifications.
  - Updated Table 5.3 Input Clock Specifications on page 31.
    - Removed LVCMOS from Standard Input Buffer with Differential or Single-Ended Configuration description to be more in line with other Silabs products.
    - Input Capacitance, C_{IN} changed to 2.4pf to match IBIS model.
    - Input Frequency parameter changes.
      - Change f_{IN_PULSED} to f_{IN_CMOS}.
      - Changed Standard Mode Test Condition to LVCMOS Mode.
      - Added Pulsed CMOS Mode Test Condition and spec limits.
    - Minimum Pulse Width parameter changes.
      - Changed Standard Mode to LVCMOS CMOS Mode (250 MHz @ 40% Duty Cycle).
      - Added Pulsed CMOS (1 MHz @ 5% Duty Cycle) test condition and spec limits.
    - Duty Cycle parameter added.
      - Added Duty Cycle Test Conditions and spec limits for LVCMOS and Pulsed CMOS.
  - Updated Table 5.4 Control Input Pin Specifications on page 33.
    - Input Capacitance, C_{IN} changed to 1.5 pF to match IBIS model.
  - Updated Table 5.5 Differential Clock Output Specifications on page 34.
    - Duty Cycle (DC) – 2nd row of Test Condition table - 712.5 MHz changed to 718.5 MHz.
    - Vpp_diff = 2*Vpp_se diagram – Moved diagram under Note 1.
  - Updated Table 5.6 LVCMOS Clock Output Specifications on page 35
    - Output Voltage Low Parameter – Removed reference to Note 3, it does not apply.
  - Updated Table 5.7 Output Status Pin Specifications on page 37.
    - Removed VDDO = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5% from conditions at top of table.
  - Updated Table 5.8 Performance Characteristics on page 37.
    - Updated PLL Lock Time Parameter.
      - Added f_{IN} = 19.44 MHz; Ramped Exit from Holdover enabled (recommended) Test Condition and 1900 s typical spec added to reflect typical lock time when recommended Ramped Exit from Holdover setting is used.
      - 1 pps Mode[8] Phase error < 10 ns Test Condition and typical 25 s spec added. Note 8 added at bottom of table.
      - 1 pps Mode[9] Test Condition updated with “Fully Locked”, max spec removed, and typical spec of 2 min added to reflect typical lock time under conditions of Note 9 at bottom of table.
      - Added Note 10 to f_{IN} = 19.44 MHz; Ramped Exit from Holdover enabled (recommended)[10].
      - Pull-in Range[6] Parameter – Standard mode test condition spec changed to 500 ppm typical to reflect spec limits of similar Silabs products.
      - Input-to-Output Delay Variation[8] Parameter, $t_{IODELAY}$ – Specification Removed - Under high device junction temperatures, it is possible that all of the output Multisynths may not start exactly at the same time. This effect may be different after each reset or power cycle at high temperatures.

- Updated 9. Pin Descriptions.
  - Updated Table 9.1 Si5383/84 Pin Descriptions [1] on page 46.
    - Added Note 3 to OUT2 and OUT2b Pin names.
- Updated 10. Package Outline.
  - Updated Table 10.1 Package Dimensions on page 49.
    - Dimension A Min spec changed to 0.80 and Nom. Spec changed to 0.90. Both specification changes reflect a lower overall package height than was originally on the datasheet. These dimension were incorrect when datasheet was released.
- Updated 11. PCB Land Pattern.
  - Updated Table 11.1 PCB Land Pattern Dimensions on page 52.
    - Stencil Design Note 4 changed to reflect recommendation for an LGA package. Original Note 4 applied to QFN package.

Revision 1.0

April, 2017

- Updated 1. Feature List.
- Updated OPN information in 2. Ordering Guide and 2.1 Ordering Part Number Fields.
- Added text about device reset recommendations in 3.5.1 Initialization and Reset.
- Added 3.10.9 Output Enable/Disable and 3.10.13 Synchronous/Asynchronous Output Disable.
- Updated values and added new test conditions to Table 5.2 DC Characteristics on page 29.
- Updated values in Table 5.5 Differential Clock Output Specifications on page 34.
- Update values and added new test conditions and footnotes 7-9 in Table 5.8 Performance Characteristics on page 37.
- Updated values in Table 5.11 Thermal Characteristics on page 40.
- Removed $t_{VD:DAT}$ from Figure 5.3 I^2C Serial Port Timing Standard and Fast Modes on page 39.
- Updated and added new diagrams in section 6. Typical Application Diagrams.
- Updated 7. Detailed Block Diagram.
- Updated Figure 8.1 F_{IN} = 19.44 MHz; F_{OUT} = 156.25 MHz, 3.3 V LVPECL with Rakon 12.8 MHz Reference, 48 MHz Crystal on page 45.
- Corrected the name of pin 19 in Figure 9.1 Si5383 Pins on page 46 and Figure 9.2 Si5384 Pins on page 46.

Revision 0.8

November, 2016

- Added Si5384 part number and related specifications to all tables and figures.
- Updated description on front page.
- Updated values in Table 2.1.
- Updated text and corrected typographical errors in Section 3.
- Updated Figure 3.1 and Figure 3.4.
- Updated resistor values in Figure 3.8.
- Added Section 3.8.6 and 3.10.15.
- Updated Figures 3.14, 3.15, and 3.16.
- Removed a figure that incorrectly described OEb functionality.
- Added Section 3.12
- Updated values in Table 5.1, Table 5.2, Table 5.3, Table 5.4, Table 5.5, Table 5.6, Table 5.7, Table 5.8, Table 5.9, Table 5.10, Table 5.11, and Table 5.12.
- Updated Figure 6.1.
- Added Figure 6.2.
- Updated Figure 7.1.
- Added Figure 8.1.
- Updated Figure 9.1.
- Added Figure 9.2.
- Updated pin descriptions in Table 9.1.
- Updated Figure 10.1.
- Updated Table 10.1.
- Updated Table 11.1.
- Updated Figure 12.1.
- Added Figure 12.2.
- Updated Table 12.1.

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