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FAIRCHILD SEMICONDUCTOR®

January 2014

FDMC7660S

N-Channel Power Trench® SyncFET™

30 V, 20 A, 2.2 mΩ

Features

- Max $r_{DS(on)}$ = 2.2 mΩ at V_{GS} = 10 V, I_D = 20 A
- Max $r_{DS(on)}$ = 2.95 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

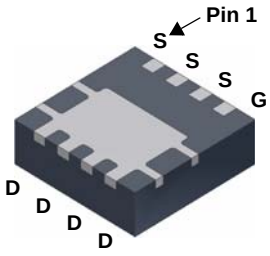
General Description

The FDMC7660S has been designed to minimize losses in power conversion applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

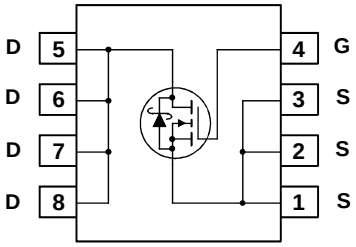
- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification

Top



Bottom

Power 33



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage		(Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		40	A
	-Continuous (Silicon limited)	T_C = 25 °C		100	
	-Continuous	T_A = 25 °C	(Note 1a)	20	
	-Pulsed			200	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	128	mJ
P_D	Power Dissipation			41	W
	Power Dissipation		(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

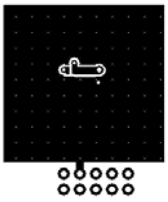
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7660S	FDMC7660S	Power 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25 °C		13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.6	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25 °C		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A		1.7	2.2	mΩ
		V_{GS} = 4.5 V, I_D = 18 A		2.5	2.95	
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C		2.2	3.1	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 20 A		129		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		3250	4325	pF
C_{oss}	Output Capacitance			1260	1680	pF
C_{rss}	Reverse Transfer Capacitance			105	160	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 20 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		14	25	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
t_f	Fall Time			3.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 20 A		47	66	nC
	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D = 20 A		21	29	nC
Q_{gs}	Total Gate Charge	V_{DD} = 15 V, I_D = 20 A		9.5		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15 V, I_D = 20 A		5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A (Note 2)		0.8	1.2	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.4	0.7	
t_{rr}	Reverse Recovery Time	I_F = 20 A, di/dt = 300 A/μs		31	50	ns
Q_{rr}	Reverse Recovery Charge			39	62	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1in^2 pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. Starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 16 A, V_{DD} = 27 V, V_{GS} = 10 V.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

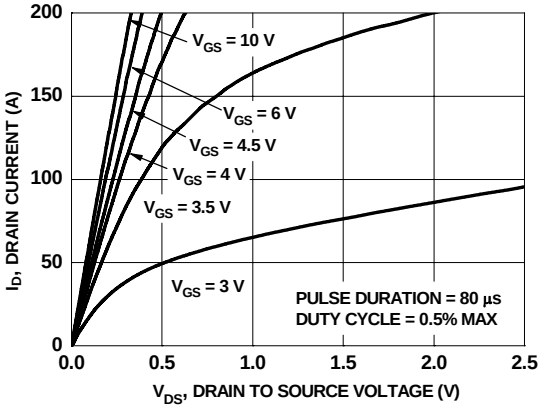


Figure 1. On-Region Characteristics

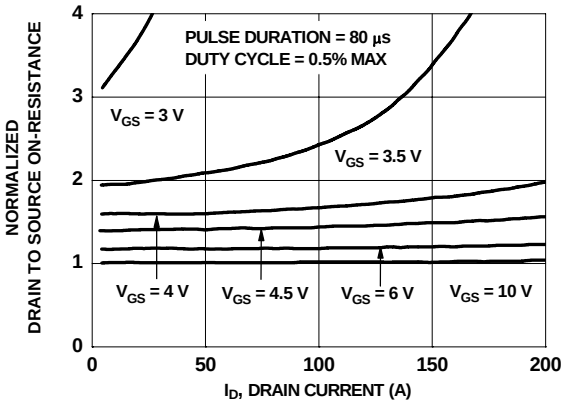


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

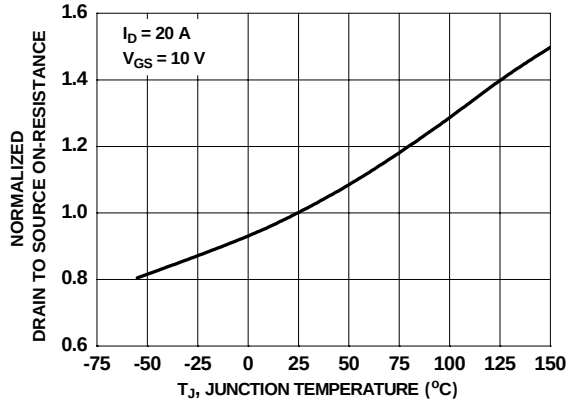


Figure 3. Normalized On-Resistance vs Junction Temperature

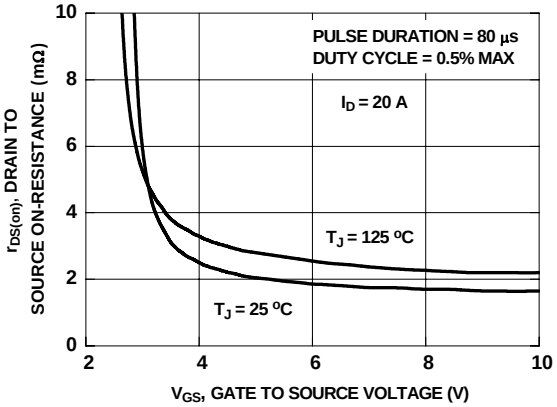


Figure 4. On-Resistance vs Gate to Source Voltage

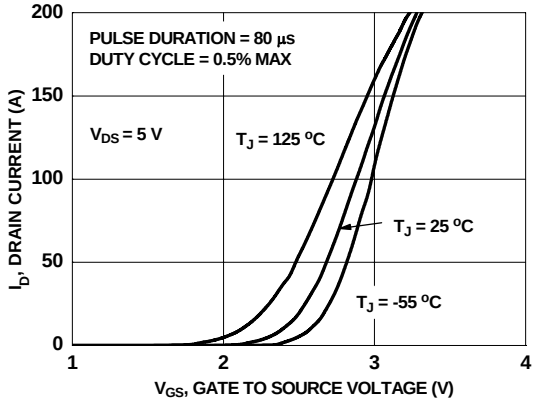


Figure 5. Transfer Characteristics

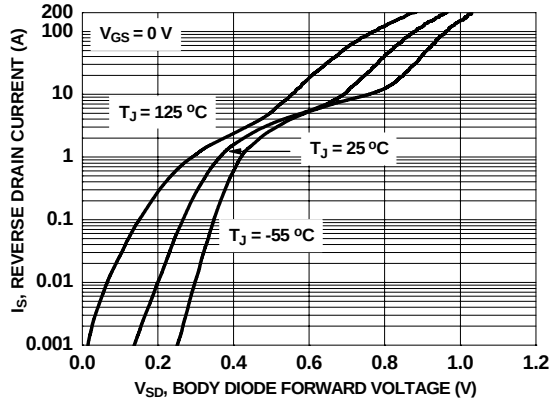


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

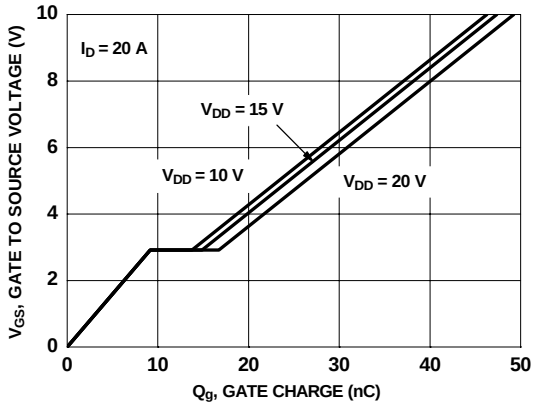


Figure 7. Gate Charge Characteristics

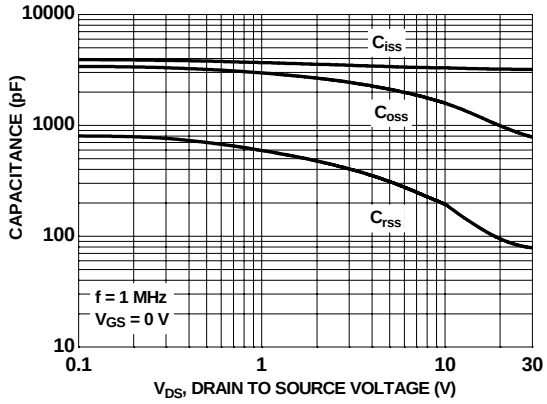


Figure 8. Capacitance vs Drain to Source Voltage

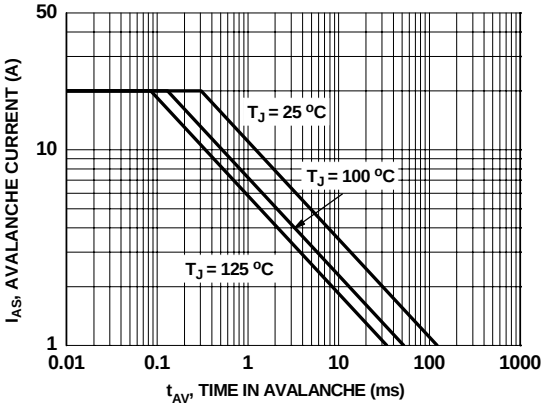


Figure 9. Unclamped Inductive Switching Capability

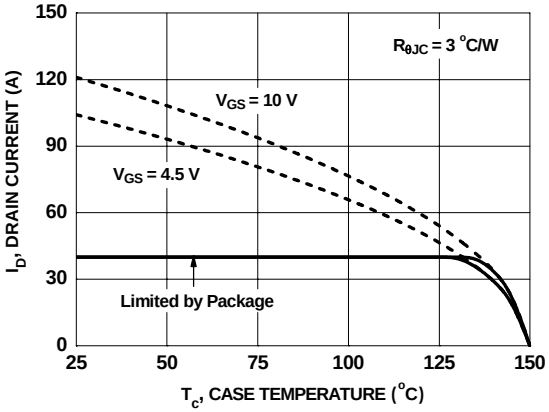


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

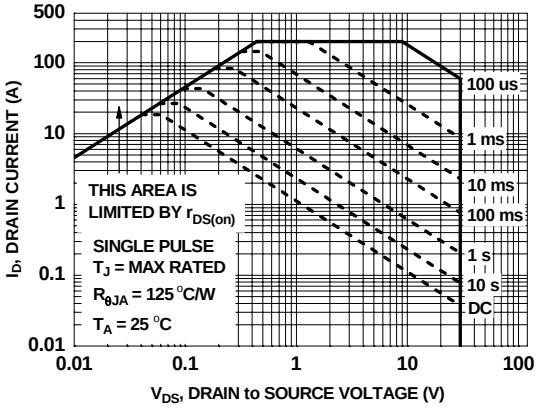


Figure 11. Forward Bias Safe Operating Area

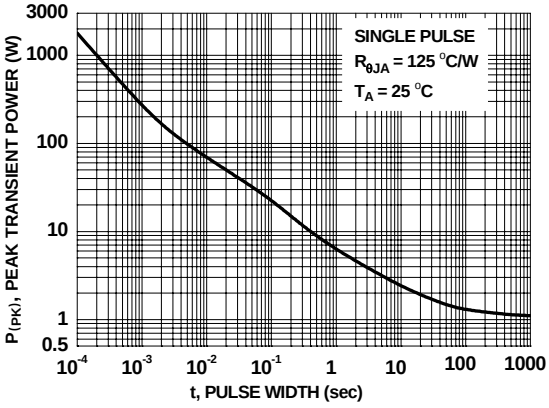


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

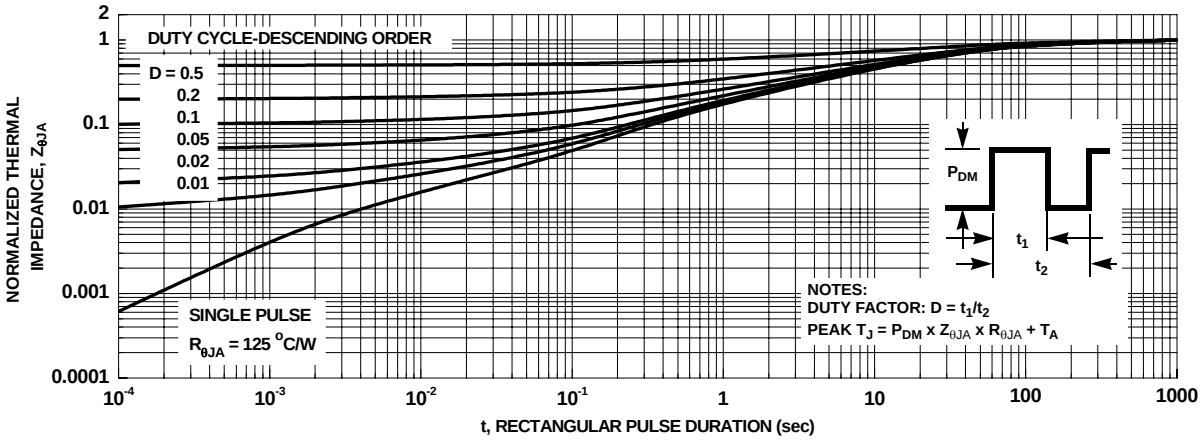


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMC7660S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

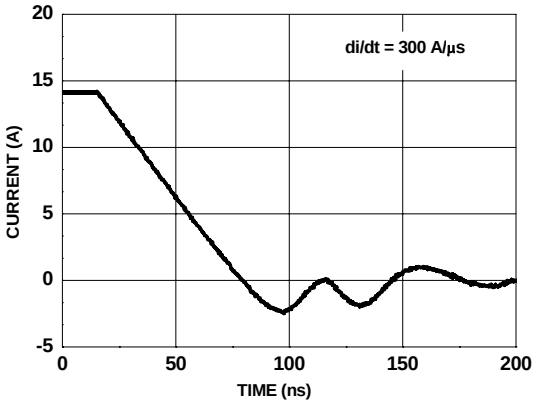


Figure 14. FDMC7660S SyncFET body diode reverse recovery characteristic

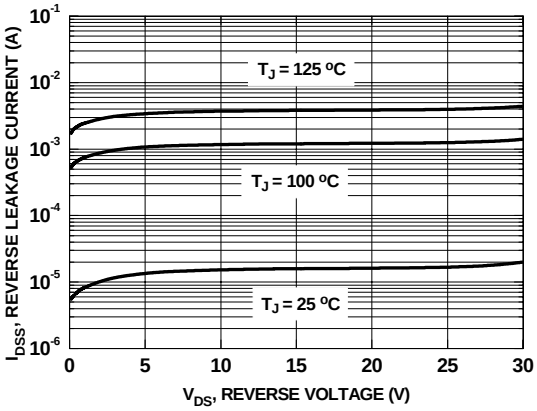
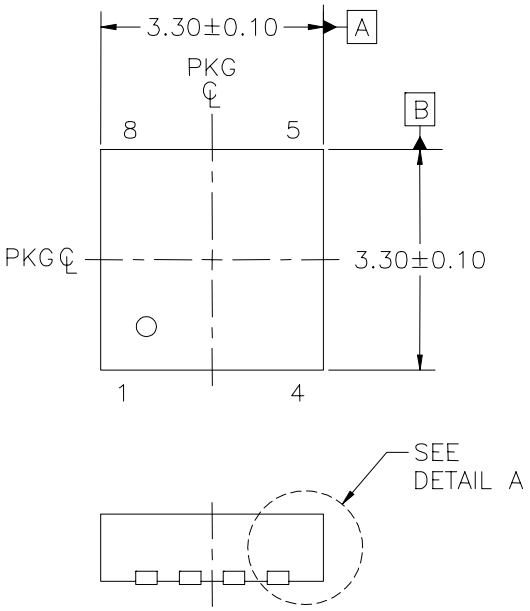
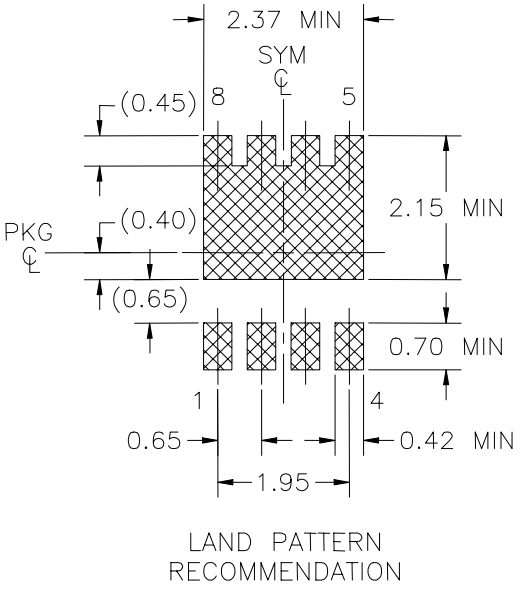


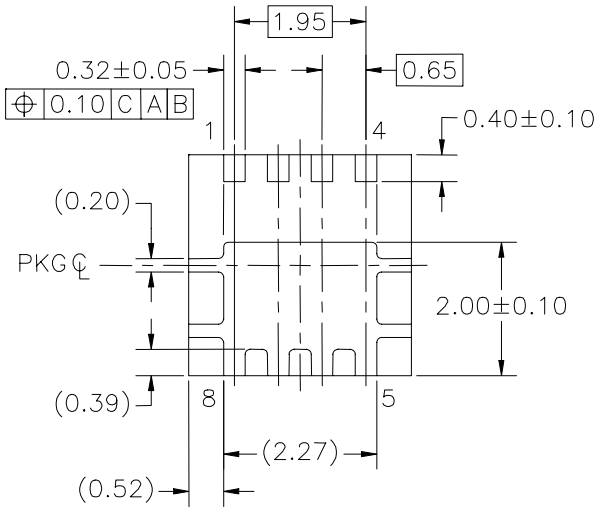
Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

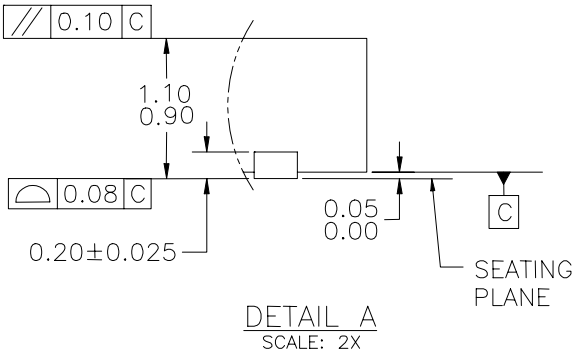
Dimensional Outline and Pad Layout





LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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