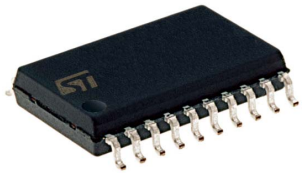
STCMB1

TM PFC with X-cap discharge and LLC resonant combo controller

Datasheet - production data



SO20W

Applications

- Ac-dc adapter, open frame SMPS
- SMPS for LED TV, desktop and all-in-one PC
- Consumer and industrial SMPS compliant with “Energy Using Product” directive (EuP) Lot 6, DOE and European CoC ver. 5, Tier 2
- LED street lighting

Features

- Common features
  - SO20W package
  - 800 V high voltage start-up with integrated input voltage sensing
  - Active input filter capacitor discharge circuitry for reduced standby power compliant with IEC 62368-1 and UL Demko certified
  - Independent debug mode for both converters
- PFC controller features
  - Enhanced constant on-time PFC with input voltage feedforward, THD optimizer
  - Complete set of protections: ac brown-in/out, inrush control, OVP, OCP, inductor saturation, feedback disconnection
- LLC controller features
  - Proprietary timeshift control for improved input ripple rejection and dynamic response
  - Half-bridge operation up to 750 kHz with self-adjusting deadtime
  - Complete set of protections: dc brown-out, two-level OCP, hard switching prevention (HSP) function for anti-capacitive mode protection and safe start-up
  - Synchronous burst mode operation with PFC enhances light-load efficiency

Contents

1 Description

The STCMB1 device embodies a transition mode (TM) PFC, a high voltage double-ended controller for LLC resonant half-bridge, an 800 V-rated high voltage section and the glue logic that supervises the operation of these three blocks.

The PFC section uses a proprietary constant on-time control methodology that does not require a sinusoidal input reference, thereby reducing the system cost and external component count.

It includes also a complete set of protections: a cycle-by-cycle overcurrent (OCP), an output overvoltage (OVP), a feedback failure (FFP, latch-mode), an ac brown-out, boost inductor saturation and inrush current detection both at the start-up and after mains sags or missing cycles.

The half-bridge (HB) section provides two complementary outputs that drive the high-side and low-side MOSFET 180° out-of-phase. The deadtime inserted between the turn-off of an either switch and the turn-on of the other is automatically adjusted to ensure zero voltage switching and higher efficiency from low to full load.

A proprietary control method, timeshift control - TSC, improves dynamic behavior and input ripple rejection resulting in a cleaner output voltage.

At the light-load the IC can be forced to enter a controlled burst mode operation where both the HB and the PFC work intermittently synchronized one to another. This helps to reduce the average switching frequency, thus keeping converter input consumption as low as possible.

At the start-up, in addition to the traditional soft-start based on the frequency-shift, a proprietary hard switching prevention (HSP) function controls the half-bridge to prevent hard switching in the initial cycles. Additionally, the HSP function prevents the converter from working in or too close to the capacitive mode to ensure soft-switching.

The HB is provided with a two-level OCP. The first level is with the frequency shift and delayed shutdown with an automatic restart. A fast shutdown with an automatic restart occurs if this first-level protection cannot limit the primary current. Finally, the device embeds the logic circuitry to coordinate the operation of the PFC, HB and HV start-up generator; in particular: the power-on/off sequencing, X-capacitor discharge, fault handling and synchronous burst mode operation. For the application debug purposes it is possible to externally disable one section at a time and have the other section working standalone.

2 Block diagrams

Figure 1. STCMB1 block diagram

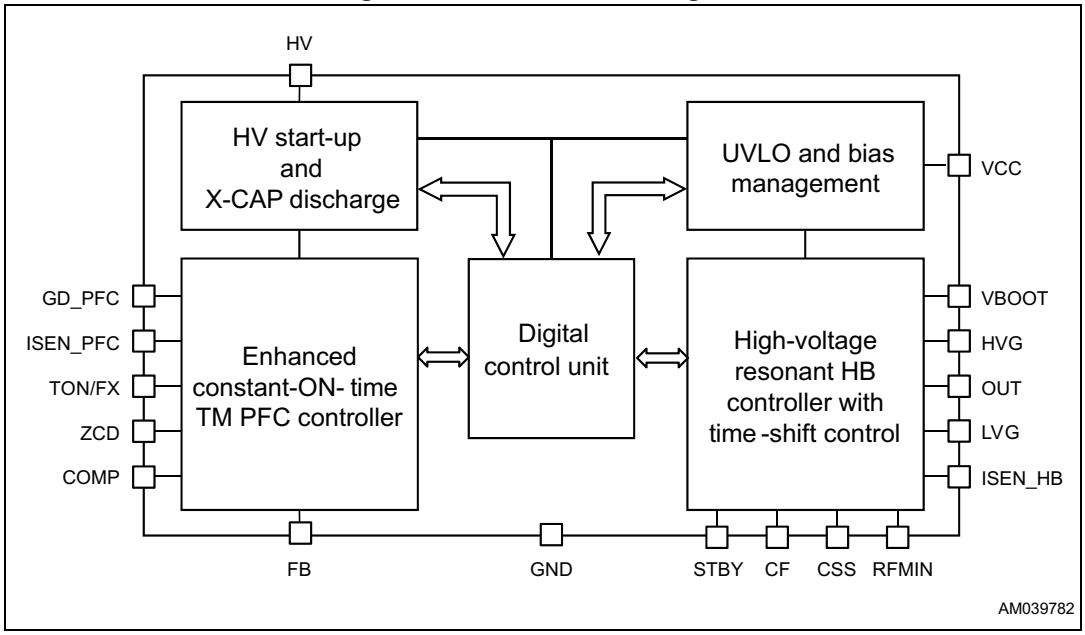
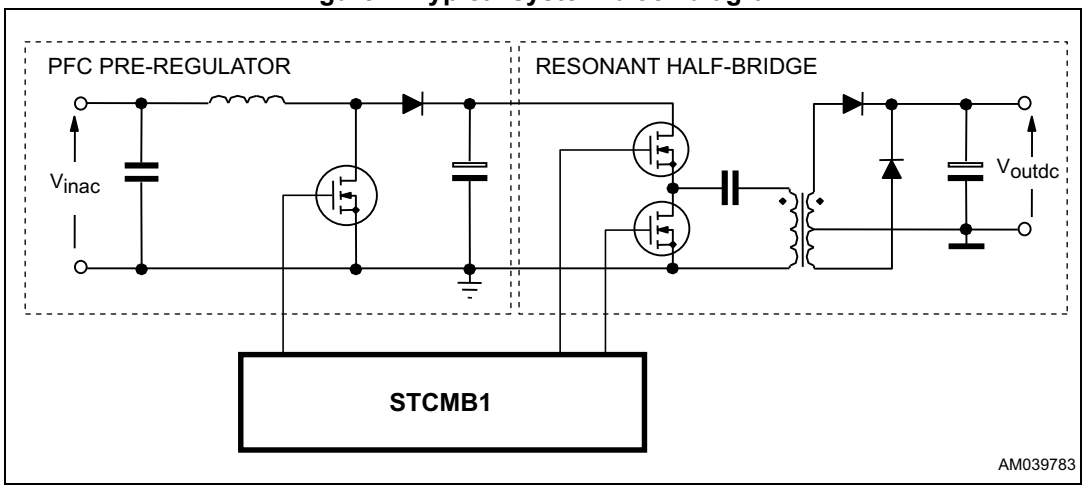


Figure 2. Typical system block diagram



3 Pin connections and description

Figure 3. Pin connections, top view

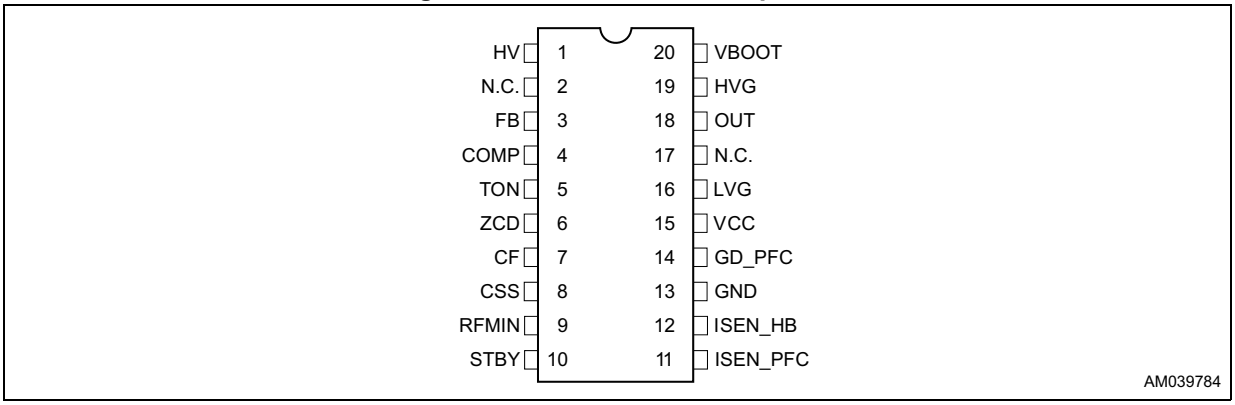


Table 1. Pin description

Pin no.	Name	Function
1	HV	High voltage start-up generator / ac voltage sensing input. The pin, able to withstand 800 V, has to be connected to the ac side of the input bridge via a pair of diodes (1N400x type) to sense the ac input voltage. If the voltage on the pin is higher than 20 V (typical value), an internal pull-up circuit charges the capacitor connected between the VCC pin and GND. Initially the current is low for safety in case of a shorted VCC, and then it goes to the normal level as far as the VCC pin reaches the start-up threshold. To reduce the hold-up requirement on the VCC cap, the generator is turned off when the half-bridge section starts up. In case of a fault that prevents the half-bridge from starting up, the HV generator is shut down after a timeout of 80 ms. The generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold. In case of a latched shutdown, when the VCC cycles between the start-up threshold and the UVLO threshold, the current is reduced to keep power dissipation low. The same occurs in case of a restart after a fault to create a longer restart delay. The pin is used also to sense the ac voltage, which is used by the input voltage feedforward and the ac brown-out functions. When a brown-out condition is detected any latched protection converging on the FB pin is cleared. An internal logic circuit detects that the unit has been detached from the power line and activates the high voltage start-up generator to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulations (such as IEC 61010-1 or IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitor, thus saving the associated power losses and enabling ultra-low consumption in standby conditions. A series resistor between 3 kΩ and 9 kΩ has to be mandatorily inserted in series to the pin.
2, 17	N.C.	High voltage spacer. These pins are not internally connected to isolate the high voltage sections and ease compliance with safety regulations (creepage distance) on the PCB.

Table 1. Pin description (continued)

Pin no.	Name	Function
3	FB	Being the pin uncommitted, its voltage is proportional to the instantaneous output voltage of the PFC stage. Under steady state conditions the voltage on the pin sits at the internal reference of the error amplifier (2.5 V). If the voltage exceeds the steady state value by 7% (e.g.: due to an output voltage overshoot) switching is stopped until it gets back close to it. If the FB voltage falls below 0.5 V, a failure of the output divider is assumed and both the PFC stage and the half-bridge are latched off. The HV start-up generator is intermittently turned on to keep the device supplied. To restart the device it is necessary to disconnect the unit from the input source. As the input voltage monitor for the half-bridge, the pin handles power-on and power-off sequencing. As the device is turned on, the PFC stage starts first and the half-bridge is kept disabled until the FB voltage exceeds 2.4 V. In case the voltage is already above 2.4 V as the PFC starts, the half-bridge waits 0.2 ms before starting, so to have always consistent power-on sequencing. The half-bridge is again inhibited as the voltage on the pin falls below 1.75 V (dc brown-out).
4	COMP	To avoid an uncontrolled rise of the output voltage at the zero load, when the voltage on the pin falls below 1 V (typical value) the gate driver output will be inhibited (burst mode operation).
5	TON	Maximum on-time of the PFC MOSFET. A resistor and a capacitor in parallel are connected from this pin to ground. When the MOSFET of the PFC stage is ON an internal current generator produces a ramp that, along with the voltage on the COMP pin, determines the turn-off instant of the MOSFET.
6	ZCD	Boost inductor's demagnetization sensing input. A negative-going edge triggers the PFC MOSFET's turn-on. The pin can be connected to an auxiliary winding of the boost inductor through a resistor or to the drain of the MOSFET via an RC series.
7	CF	Timing capacitor for HB oscillator. A capacitor connected from this pin to GND is charged by an internal current generator programmed by the external network connected to the RFMIN pin. In each half cycle the ramp starts as the tank current (sensed through the ISEN_HB pin) and the applied square wave voltage has the same sign (e.g.: ISEN_HB positive during the high-side MOSFET on-time and ISEN_HB negative during low-side MOSFET on-time). The ramp is reset as a fixed peak value is reached. This also causes the HB to be toggled.
8	CSS	HB soft-start. This pin connects an external capacitor to GND and a resistor to the RFMIN pin that set both the initial oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (VCC < UVLO, FB < 1.75 V, ISEN_HB > 1.5 V) to make sure it will be soft-started next. Additionally the switch is activated when the voltage on the current sense pin (ISEN) exceeds 0.8 V or when the converter is working in the capacitive mode operation. As long as the voltage on the pin is lower than 0.3 V, the burst mode operation and second level OCP protection are inhibited.
9	RFMIN	Timeshift setting. This pin provides an accurate 2 V reference, and a resistor connected from this pin to GND defines a current that is used to set the maximum timeshift. To close the feedback loop that regulates the converter output voltage by modulating the timeshift, the phototransistor of an optocoupler will be connected to this pin through a resistor. The value of this resistor will set the minimum timeshift. An R-C series connected from this pin to GND sets the timeshift at the start-up to prevent an excessive energy inrush (soft-start).

Table 1. Pin description (continued)

Pin no.	Name	Function
10	STBY	Burst mode operation threshold for the HB. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.25 V). If the voltage on the pin is lower than the reference, the IC stops switching, enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 40 mV. Soft-start is not invoked. When the HB is stopped the PFC is stopped as well; while the HB is switching the PFC stage is enabled and it switches or not depending on the level of the COMP pin. Tie the pin to RFMIN if the burst mode operation is not used. An RC filter is mandatory, with R > 100 Ω and C > 100 pF. Please note that the time constant of the RC filter enters in the loop transfer function, when the pin is directly fed by the phototransistor of the optocoupler.
11	ISEN_PFC	The inductor current is sensed through a resistor RS on the current return side and the resulting negative voltage is applied to this pin through a limiting resistor. When the power MOSFET is turned on an internal comparator enables the PWM ramp to start only when the voltage on the pin is lower than -25 mV (typical value), e.g.: when the inductor current is slightly positive. If the voltage on the pin goes below -0.5 V the internal overcurrent comparator is triggered and terminates the conduction cycle of the external power MOSFET before the normal PWM circuit does. In this way, the peak inductor current is limited at a maximum of 0.5/RS. A voltage on this pin higher than -25 mV (typical value) enables both power MOSFET's turn-on when a cycle is initiated by the demagnetization sensing circuit and when it is initiated by the internal starter. In this way, the unit stops during the current surges occurring at power up or after a mains dip or a missing cycle and restarts switching only when the surge is over. An RC filter is mandatory at the pin, R > 100 Ω and C > 100 pF. The overall time constant should give a negligible delay with respect to the typical operating frequencies of the PFC. The value of the resistor also defines the effect of the THD optimizer (enhanced COT): THD is usually optimized with a value between 100 Ω and 300 Ω.
12	ISEN_HB	Current sense input for the HB. The pin senses the resonant current through a sense resistor or a capacitive divider for lossless sensing. If the voltage exceeds a 0.8 V threshold the soft-start capacitor connected to the CSS pin is internally discharged: the frequency increases hence limiting the power throughput. Under the output short-circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time internally set at 40 ms minimum. If the current keeps on building up despite this frequency increase, a second comparator referenced to 1.5 V disables switching immediately. In both cases VCC is recycled before restarting (see the HV pin). As long as the voltage on the CSS pin is lower than 0.3 V, this second comparator is inhibited. The pin is used also by the hard switching prevention (HSP) function. Do not short the pin to ground; this would prevent the device from operating correctly. An RC filter is recommended to reduce the noise level at the pin, with R > 50 Ω and C > 100 pF. The overall time constant should give a negligible delay with respect to the typical operating frequencies of the LLC.
13	GND	Ground. Current return for signal parts of the IC, the PFC gate driver and the low-side gate driver of the half-bridge. Keep the PCB trace that goes from this pin to the sources of the PFC and the low-side MOSFETs separate from the trace that collects the grounding of the bias components.
14	GD_PFC	PFC gate driver output. The totem pole output stage is able to drive power MOSFETs and IGBTs. It is capable of a 0.6 A source current and a 0.8 A sink current (minimum values). The pin is actively pulled to GND during UVLO.

Table 1. Pin description (continued)

Pin no.	Name	Function
15	VCC	Supply voltage of the signal part of the IC. An electrolytic capacitor of at least 22 µF (typ. value) must be connected between the pin and GND. Sometimes a small bypass capacitor (0.1 µF typ.) in parallel to the ELCAP might be useful to get a clean bias voltage for the signal part of the IC.
16	LVG	Low-side gate drive output. The driver is capable of a 0.3 A source and a 0.8 A sink peak current (minimum values) to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
18	OUT	High-side gate drive floating ground. Current return for the high-side gate drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
19	HVG	High-side gate drive output. The driver is capable of a 0.3 A source and a 0.8 A sink peak current (minimum values) to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to OUT ensures that the pin is not floating during UVLO.
20	BOOT	High-side gate drive floating supply voltage. The bootstrap capacitor connected between this pin and OUT is fed by an internal synchronous bootstrap diode driven in phase with the low-side gate drive. This patented structure replaces the normally used external diode.

4 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Pin no.	Parameter	Value	Unit
V_{HV}	1	Voltage range (referred to GND)	-1 to 800	V
-	3, 5, 7, 8, 9, 10	Analog inputs and outputs voltage range	-0.3 to 3.6	V
-	4, 6	Analog inputs and outputs voltage range	-0.3 to 5.5	V
I_{ZCD}	6	Zero current detector input max. current	3	mA
I_{RFMIN}	9	Maximum source current	2	mA
V_{ISEN_PFC}	11	Current sensing inputs voltage range	-3 to 3.6	V
V_{ISEN_HB}	12	Current sensing inputs voltage range	-3 to 5.5	V
V_{GD_PFC}, V_{LVG}	14, 16	Ground-referenced gate drivers	-0.3 to V_{VCC}	V
V_{VCC}	15	IC supply voltage	-0.3 to 21	V
V_{OUT}	18	Floating ground voltage	-3 up to a value included in the range V_{BOOT} -21 and V_{BOOT}	V
d_{VOUT} /dt	18	Floating ground max. slew rate	50	V/ns
V_{HVG}	19	High-side (floating) gate driver	V_{OUT} - 0.3 to V_{VBOOT} + 0.3	V
V_{BOOT}	20	Floating supply voltage (referred to GND)	-1 to 620	V
ESD HBM	18,19	According to ANSI/ESDA/JEDEC JS-001-2014	± 900	V
	1, 3 to 16, 20		± 2000	

5 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction to ambient	90	°C/W
P_{tot}	Power dissipation at T_{amb} = 70 °C	0.6	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

6 Electrical data

T_j = -40 °C to +125 °C, V_{VCC} = V_{VBOOT} = 15 V[a], C_F = 470 pF; R_{RFMIN} = 22.5 kΩ; C_{HVG} = C_{LVG} = C_{GD_PFC} = 1 nF, C_{TON} = 470 pF unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC supply voltage						
V_{VCC}	Operating range	After turn-on	10	-	20	V
V_{VCCOn}	Turn-on threshold	(1)Voltage rising	15.5	16.5	17.5	V
V_{VCCOff}	Turn-off threshold	(1)Voltage falling	9	9.5	10	V
Supply current						
I_q	Quiescent current after turn-on	V_{FB} = 1 V	-	1.5	2.2	mA
		V_{FB} = 2.5 V	-	3	4	
		Idle during burst mode T_j = 25 °C	-	0.7	0.94	
		IC latched off	-	-	1.2	
I_{CC}	Operating supply current at f_{sw} = 75 kHz	V_{FB} = 1 V, GD_PFC only	-	2.8	3.6	mA
		V_{FB} = 2.5 V, all drivers	-	4.5	6	
High voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	800	-	-	V
$V_{HVstart}$	Start voltage (rising)	(1)I_{VCC} < 100 µA	10	18	25	V
V_{VCC_SO}	VCC switchover threshold	-	1	1.5	2	V
$I_{HV, ON}$	ON-state charge current	V_{HV} > $V_{HVstart}$, V_{VCC} < V_{VCC_SO}	0.5	1	1.6	mA
		V_{HV} > $V_{HVstart}$, V_{VCC} > V_{VCC_SO}	5	8	11	
		IC latched off or restart after overload timeout	3.5	4.5	5.5	
$I_{HV, OFF}$	Off-state leakage current	V_{HV} = 400 V	-	20	24	µA
T_{TOUT}	Generator shutdown timeout	After V_{VCC} exceeds V_{VCCOn}	64	80	96	ms
IC debug functions						
V_{ZCD_D}	PFC disable threshold	At turn-on, voltage rising	-	2.4	-	V
$V_{ISEN\_HB\_D}$	HB disable threshold	At turn-on, voltage rising	-	2.4	-	V
X-capacitor discharge function						
V_{HVmin}	Peak residual voltage	$I_{HV, DIS}$ > 4.2 mA	-	-	45	V
$I_{HV, DIS}$	Discharge current	V_{HV} > 45 V	4.2	-	-	mA

a. Adjust V_{VCC} above V_{VCCOn} before setting at 15 V.

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PFC - ac brown-out protection						
V_{HVpk_BO}	Brown-out threshold	(1)Peak voltage falling LLC in continuous switching, no burst mode. RHV series = 5.6 KΩ	92	98	104	V
V_{HVpk_BI}	Brown-in threshold	(1)Peak voltage rising LLC in continuous switching, no burst mode. RHV series = 5.6 KΩ	106	113	120	V
T_{DB}	Brown-out debounce time	-	32	40	48	ms
PFC - zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	2.8	3.3	-	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = -2.5 mA	-0.3	-	0	V
V_{ZCDA}	Arming voltage	(1)Positive-going edge	-	0.5	-	V
V_{ZCDT}	Triggering voltage	(1)Negative-going edge	-	0.25	-	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 2.2 V	-	-	5	µA
PFC - maximum on-time						
I_{TON}	Charge current	V_{TON} = 3 V, V_{HV_pk} = 160 V dc	180	200	220	µA
		V_{TON} = 3 V, V_{HV_pk} = 320 V dc	640	800	960	
V_{TON}	Linear operating range	-	0	-	3	V
V_{TON}	On-time reference level	GD_PFC goes low V_{COMP} = 3 V	-	2	-	V
R_{DSC}	Discharge resistance	-	-	60	200	Ω
PFC - transconductance error amplifier						
V_{ref}	Internal voltage reference	T_j = 25 °C	2.475	2.5	2.525	V
		(1)10 V < V_{VCC} < 21 V	2.44	-	2.58	
I_{FB}	Input bias current	V_{FB} = 0 to 3 V	-1	-0.2	1	µA
$V_{COMPSAT}$	Upper clamp voltage	I_{SOURCE} = 20 µA	4.0	4.3	-	V
		I_{SOURCE} = 20 µA, T_j > °0	4.2	4.5	-	
I_{COMP}	Max. sink/source current	V_{COMP} = 3 V, V_{FB} = 2.3 V	150	200	-	µA
g_m	Transconductance	V_{FB} = V_{ref}	160	200	240	µS
Ro	Output impedance	-	2	-	-	MΩ
PFC - dynamic and static OVP protections						
V_{FB_S}	D_OVP threshold	T_j = 25 °C	2.595	2.675	2.755	V
		(1)10 V < V_{VCC} < 21 V	2.568	-	2.782	
V_{FB_R}	Restart voltage after D_OVP	(1)	2.47	2.55	2.63	V
T_{DB}	D_OVP debounce time	-	40	50	65	µs
V_{COMP_S}	S_OVP threshold	(1)Voltage falling	0.9	1	1.1	V
V_{COMP_R}	Restart voltage after S_OVP	(1)Voltage rising	0.92	1.02	1.15	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PFC - feedback failure protection (FFP)						
V_{FB_D}	Disable threshold	(1)Voltage falling	0.42	0.46	0.5	V
T_{DB}	FFP debounce time	-	40	50	65	µs
PFC - current sensing comparators						
I_{ISEN_PFC}	Input bias current	VISEN_PFC = -0.5 V	-	-	4.8	µA
V_{ISEN_PFC}	OCP threshold	(1)VCOMP = upper clamp	-0.46	-0.5	-0.54	V
$td_{(H-L)}$	Delay to output	-	-	220	280	ns
$V_{ISEN\_PFC\_Z}$	ZCD anticipation level and THD optimizer threshold	-	-	-25	-	mV
PFC - internal start-up timer						
t_{START_DEL}	Start-up delay	After $V_{ISEN\_PFC} > V_{ISEN\_PFC\_Z}$	8	10	13	µs
PFC - GATE DRIVER						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	0.4	0.7	V
V_{OH}	Output high voltage	I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
	UVLO saturation	V_{VCC} = 0 to V_{VCCon}, I_{sink} = 1 mA	-	-	1.1	V
HB - high-side floating gate drive supply						
$R_{DS(on)}$	Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH	-	230	-	Ω
HB - input voltage sensing (dc brown-out)						
V_{FB_E}	Enable voltage	(1)Voltage rising	2.34	2.4	2.49	V
V_{FB_D}	Disable voltage	(1)Voltage falling	1.7	1.75	1.8	V
HB - oscillator						
V_{CFp}	Ramp peak	(1)V_{STBY} > 1.34 V	1.44	1.5	1.56	V
		(1)V_{STBY} < 1.26 V	1.775	1.85	1.925	
V_{CFv}	Ramp valley	-	0	-	20	mV
V_{RFMIN}	Voltage reference	(1)	1.93	2	2.08	V
		(1)I_{RFMIN} = -2 mA	1.93	2	2.08	
D	Output duty cycle (HVG and LVG)(2)	V_{STBY} = 2 V R_{RFMIN} = 5.15 kΩ	49	50	51	%
T_{SH}	Time-shift	R_{RFMIN} = 22.5 kΩ	8.5	9	9.5	µs
		R_{RFMIN} = 5.15 kΩ	2.1	2.25	2.4	
f_{HB}	Max. operating frequency	-	500	-	-	kHz
K_M	Mirroring ratio I_{CF} / I_{RFMIN}	-	0.97	1	1.03	-
R_{RFMIN}	Timing resistor range	-	1	-	100	kΩ

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
HB - adaptive deadtime function						
T_{D_max}	Maximum deadtime	-	0.7	-	-	µs
T_{D_min}	Minimum deadtime	-	-	-	270	µs
HB - zero-current comparator						
V_{ISEN_Z}	Threshold voltage	Negative-going edge	-	-35	-	mV
		Positive-going edge	-	35	-	
HB - overcurrent comparator and overload delays						
I_{ISEN_HB}	Input bias current	V_{ISEN_HB} = 0 to 1.4 V	-1	-	1	nA
$V_{ISEN\_HB\_x}$	Frequency shift threshold	(1)Voltage rising	0.76	0.80	0.84	V
$V_{ISEN\_HB\_dis}$	Immediate stop threshold	(1)Voltage rising	1.42	1.5	1.58	V
HB - soft-start function						
I_{leak}	Open state current	V_{CSS} = 2 V	-	-	0.5	µA
R	Discharge resistance	-	-	120	220	Ω
T_{DISCH}	Css discharge duration	$V_{ISEN\_HB} > V_{ISEN\_HBx}$	-	6	-	µs
$V_{thHSP-SS}$	SS discharge enable (HSP)	(1)Voltage rising	1.77	1.85	1.94	V
HB - standby function						
I_{STBY}	Input bias current	V_{STBY} = 1.3 V	-1	-	1	µA
V_H	V_{CFp} change threshold	(1)Voltage falling	1.26	1.3	1.34	V
$V_{H,Hys}$	V_H hysteresis	Voltage rising	30	40	50	mV
V_L	Disable threshold	(1)Voltage falling	1.21	1.25	1.29	V
$V_{L,Hys}$	V_L hysteresis	Voltage rising	30	45	60	mV
Low-side gate driver (voltages referred to GND)						
V_{OL}	Output low voltage	I_{sink} = 50 mA	-	0.5	0.9	V
V_{OH}	Output high voltage	I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
	UVLO saturation	V_{VCC} = 0 to V_{VCCon}, I_{sink} = 1 mA	-	0.9	1.1	V
High-side gate driver (voltages referred to OUT)						
V_{OL}	Output low voltage	I_{sink} = 50 mA	-	0.5	0.9	V
V_{OH}	Output high voltage	V_{BOOT} = V_{CC} V, I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
-	HVG-OUT pull-down	-	21	27	36	kΩ

1. Parameters tracking each other.
2. $D_{HVG} + D_{LVG}$ = 100%.

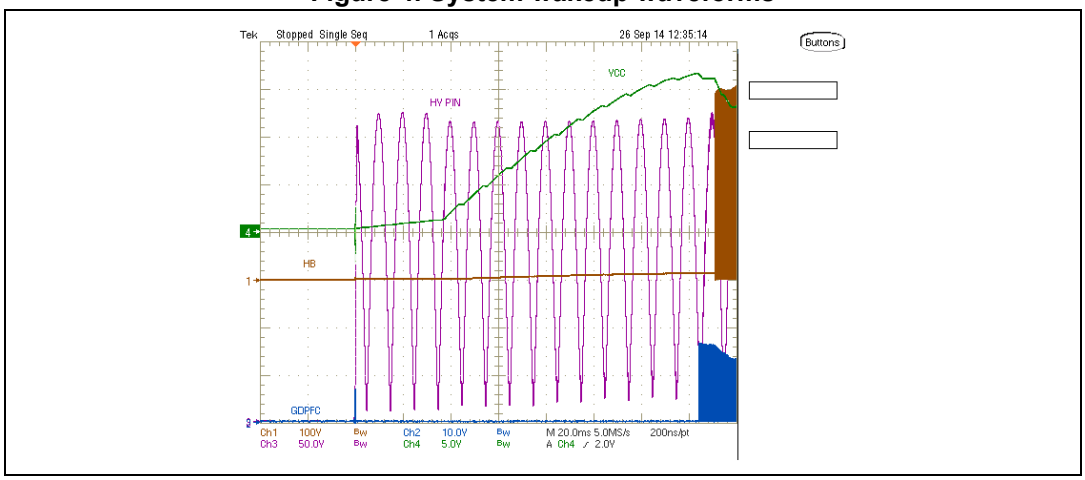
7 Application information

7.1 HV start-up

The STCMB1 is equipped with internal HV start-up circuitry dedicated to supply the IC during the initial start-up phase, before the self-supply winding is operating. An external electrolytic capacitor connected to the VCC pin is charged by the HV start-up circuitry, connected to the HV pin.

As soon as the voltage on the HV pin is higher than $V_{HVstart}$ (18 V typ.), the HV start-up system turns on and the external V_{CC} capacitor is charged up to the turn-on threshold (V_{CCOn}, 16.5 V typ.), then to guarantee a reliable start-up of the STCMB1, the HV start-up system is turned off only after the half-bridge section starts up. In case of a fault that prevents the half-bridge section from starting up, the HV start-up system is automatically shut down after a timeout T_{TOUT} = 80 ms.

Figure 4. System wakeup waveforms



If for any reason the self-supply circuitry cannot power the STCMB1 the HV start-up will be reactivated once the V_{CC} reaches the turn-off threshold ($V_{VCCOff,}$ 9.5 V typ.).

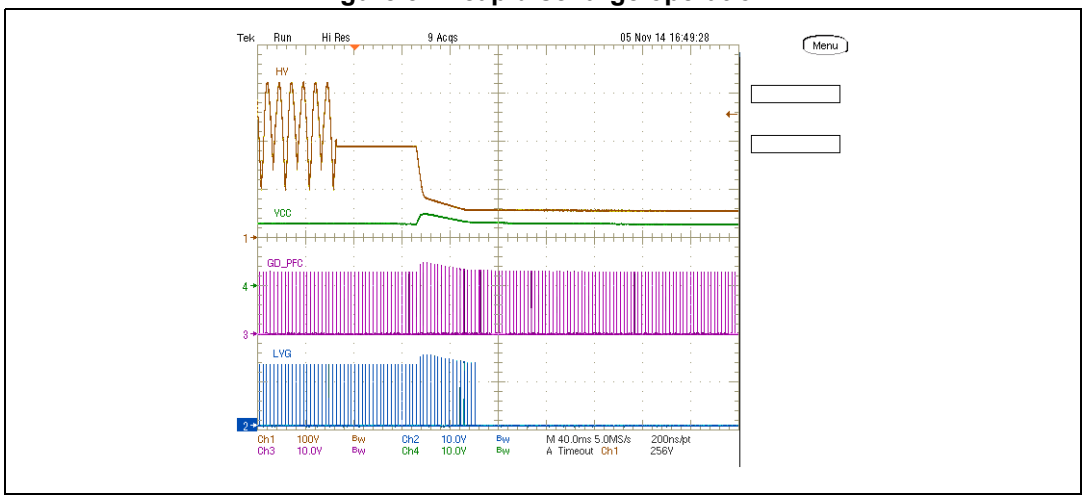
The HV start-up system performs an R-C charge of the VCC pin. A double time constant depending on the voltage value on the VCC pin is implemented to prevent damaging in case of shorts to GND of the V_{CC} circuitry.

The HV startup generator is activated also after detection of the PFC feedback failure, ac brown-out or X-cap discharge condition. Different values of the charging current (IHV,ON) are supplied to the VCC pin according to the state, see *Table 4: Electrical characteristics on page 11*.

7.2 X-cap discharge

The compliance of consumer equipment with the safety regulation such as IEC 61010-1, IEC 62368-1, and others, requires that, when the converter mains connector is removed from the plug, the EMI filter capacitors connected across the line between the phase and the neutral wires (the so called X-caps) have to be discharged bringing their voltage at a safe level to avoid the user any risk of the electrical shock due to the energy stored in the capacitors. This requirement is mandatory in case the total capacitance before the input bridge exceeds 100 nF.

Figure 5. X-cap discharge operation



Typically this function is performed by means of a resistor in parallel but this method cannot be applied in case the converter requires very low power consumption during the light-load or no load operation, because the losses of the X-cap discharging resistor would be too high.

To overcome this issue, enabling the user to design a high performance power supply the STCMB1 device does this operation by means of the HV start-up system, allowing the removal of the traditional X-cap discharge resistor. The STCMB1 internal circuits detect the ac mains plug disconnection by sensing the voltage on the HV pin. After a detection time of 64 ms typical from the mains disconnection, the X-cap discharge operation is triggered and the HV start-up system is turned on: a discharge current (4.2 mA minimum) is drawn from the HV pin ensuring the X-cap discharge until the voltage on the HV pin falls below a safe level (45 V maximum), within the regulation maximum discharging time. The current from the HV pin will flow out from the VCC pin, to keep the IC correctly supplied until the end of the discharge. An internal 15 V clamp is activated to limit the voltage on the VCC pin by sinking the discharge current in excess of the IC consumption.

None additional component is needed by this function, totally embedded in the STCMB1.

7.3 Ac brown-out protection

The STCMB1 device is equipped with brown-out protection to prevent the operation at too low ac input voltage (typically when it falls below 70 V ac). When the brown-out protection is activated, the PFC and HB sections are both turned off, the V_{CC} start falling because no more sustained by the on-board self-supply. When V_{CC} reaches the turn-off threshold (V_{VCCoff}), the HV start-up is turned on and VCC is charged up to VCCon. The HV start-up is then turned off and VCC falls again toward VCCoff, since the switching activity is forbidden by the brown-out protection. The charge and discharge of VCC goes on as long as the abnormal ac mains condition lasts. The brown-out protection is deasserted when the ac voltage goes above the brown-in threshold (typically 80 V ac).

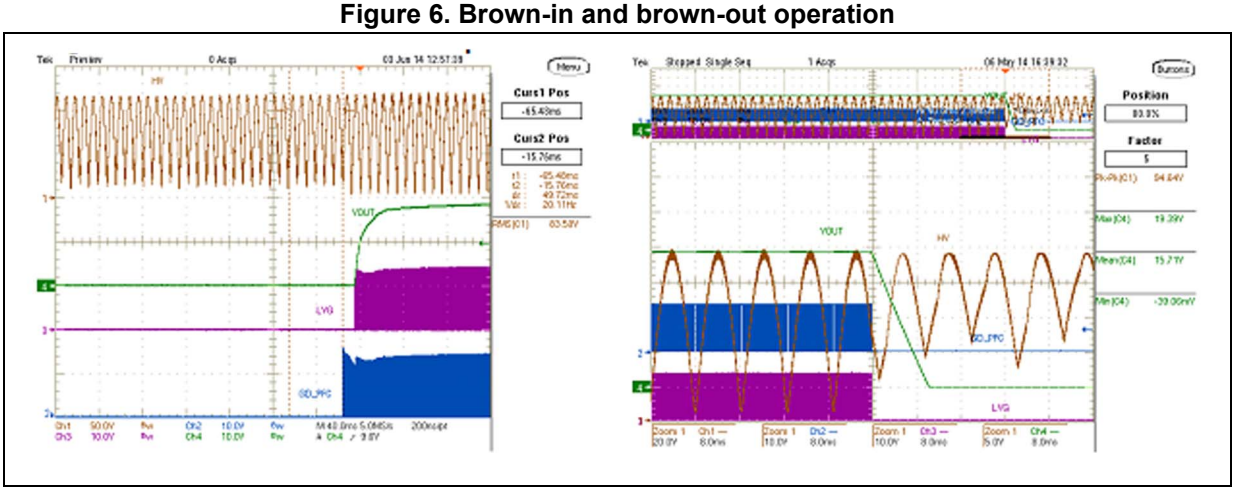
In order to avoid unexpected intervention of AC brown-out protection in case of missing cycles or short dips of the ac mains, a debounce time, T_{DB}, has been introduced: in practice, an AC brown-out condition has to last a time equal to T_{DB} (32 ms, typ.) to stop the converter operation.

To allow correct behavior of the brown-in and brown-out protections, accordingly to the threshold values given in *Table 4 on page 11*, a resistor with value between 3 kΩ and 9 kΩ, in series with the HV pin is mandatory.

The brown-in threshold has to be intended as the voltage at the HV pin right before the adapter turn-on (first GDPFC pulse, in general), when the mains voltage is slowly increased. In detail, before the brown-in, VCC is charged by the HV start-up generator and naturally discharged. During the charge phase, the voltage at the HV pin is about the actual mains voltage minus the drop on the series resistor. When VCC = VCCon, the HV start-up generator is turned off, the voltage drop is reduced to zero and the voltage at the HV pin becomes equal to the actual mains voltage. So, the converter turn-on by brown-in will occur when the mains voltage is above the threshold and the charge phase of VCC is finished.

Conversely, because of the debounce time, the brown-out threshold has to be intended as the last peak voltage at the HV pin at about one debounce time before the adapter turns off (PFC and LLC simultaneously turn off, in general), when the mains voltage is slowly decreased. Note that before the brown-out, the converter is working, so VCC is generated on the board and the HV start-up generator is off; consequently, the voltage at the HV pin is about the actual mains voltage. When the brown-out is triggered, the converter is turned off and the VCC is naturally discharged up to VCCoff when the HV start-up generator is turned on and the charge / discharge operation of VCC starts to maintain the protected condition.

Figure 6. Brown-in and brown-out operation



7.4 VCC pin

This pin is the supply voltage of the IC. An electrolytic capacitor of at least 22 µF (typ. value) must be connected between the pin and GND in order to sustain the voltage during the start-up phase and supply the IC, before the self-supply circuitry from the half-bridge transformer deliver enough voltage. Place also a ceramic capacitor (0.1 µF typ.) in parallel to the electrolytic capacitor to bypass the high frequency noise to GND and supply the STCMB1 device with a proper clean voltage.

The V_{CC} voltage is used also to supply the MOSFET gate drivers, not having a dedicated clamping, supplying the STCMB1 from the auxiliary (self-supply) winding from the resonant transformer may need a small BJT voltage regulator to keep the supply voltage regulated and avoid the aging of the gate oxide due to an excessive V_{CC}, or limit transients that could damage the IC as in case of dead shorts.

A typical V_{CC} operating voltage is 12 - 13 V.

7.5 PFC section

The STCMB1 device implements a transition mode (TM) PFC section that uses a proprietary “Constant On-Time” (COT) control methodology termed “Enhanced Constant On-Time” (ECOT). Like the COT, this control mode does not require a sinusoidal input reference, thereby reducing the system cost and external component count, while providing a distortion of the input current at the same level as current mode control.

It includes also a complete set of protections: the cycle-by-cycle overcurrent (OCP), output overvoltage (OVP), feedback failure (FFP), boost inductor saturation and inrush current detection both at the start-up and after mains sags or missing cycles.

The output voltage (Vout) is controlled by mean of a transconductance error amplifier and an accurate internal voltage reference; “Zero Current Detection” (ZCD) by sensing the voltage on the auxiliary winding on the PFC inductor enables the TM operation.

The current sense on the return path allows continuous monitoring of the inductor current. THD optimization is implemented too.

A “two-level” line voltage feedforward function helps to reduce the changes in the system gain due to changes in input voltage.

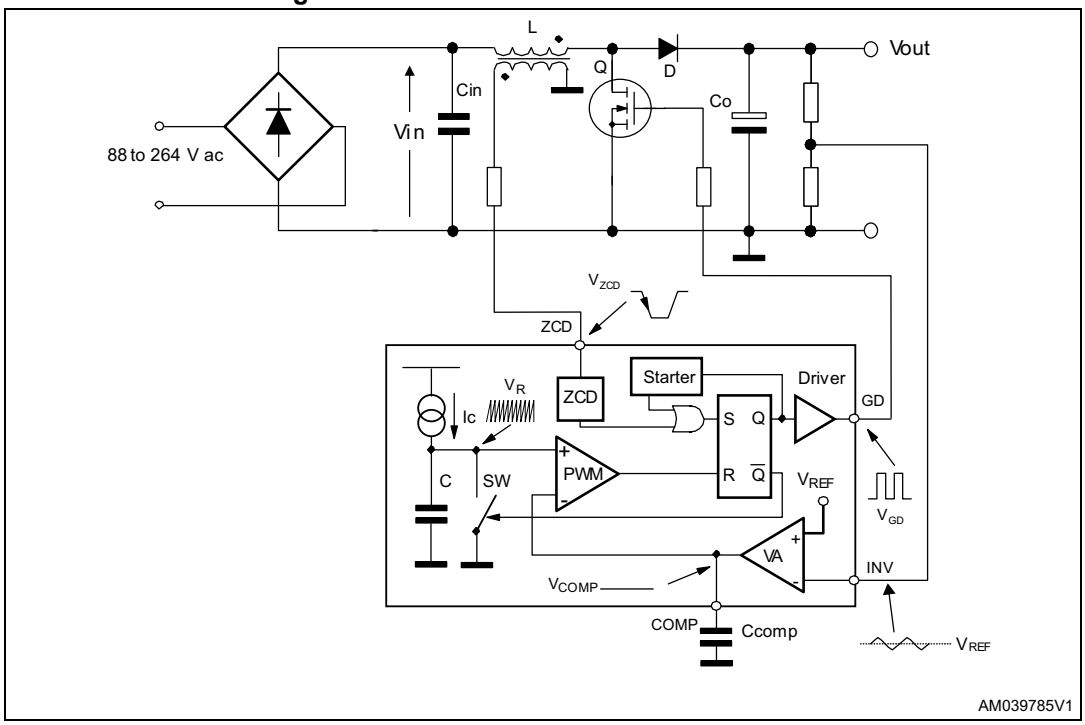
7.6 PFC: enhanced constant on-time control with THD optimizer

TM-operated PFCs are characterized by good efficiency even if the large input current ripple requires bigger EMI filters.

The COT is a common control technique where the turn-on of the power transistor in each cycle is commanded when the current through the boost inductor falls to zero and the turn-off is commanded when the duration of the on-time has reached the value programmed by the control loop. It is well-known that if this on-time is constant or even slowly varying during each line cycle, the converter draws an ideally sinusoidal current from the line.

The combination of the TM operation and COT control is a very popular solution used in several PFC controllers for output power up to 300 W. The block diagram and key waveforms of the traditional approach are shown in *Figure 7* and *Figure 8* respectively.

Figure 7. Conventional COT controlled PFC



Since the slope of the inductor current during the on-time is proportional to the input voltage, there is a perfect linear relation between the instantaneous AC voltage and the current drawn by the circuit, which would ideally provide a perfect unity power factor and no distortion when the on-time is kept constant along a line cycle.

Unfortunately, parasitic elements (essentially, the parasitic capacitance of the drain node, C_{drain}) cause a negative offset in the inductor current shape as can be seen in *Figure 8*. In particular, the negative peak current I_{Lvy} can be calculated as follows:

Equation 1

$$I_{Lvy} = -\left(V_{out} - V_{in\_pk}\, sin\,\theta\right)\sqrt{\frac{C_{drain}}{L}}$$

Approximating the inductor current with a triangular waveshape, the commanded peak current is:

Equation 2

$$I_{Lpk} = I_{Lvy} + \frac{V_{in\_pk}\, sin\,\theta}{L} T_{ON}$$

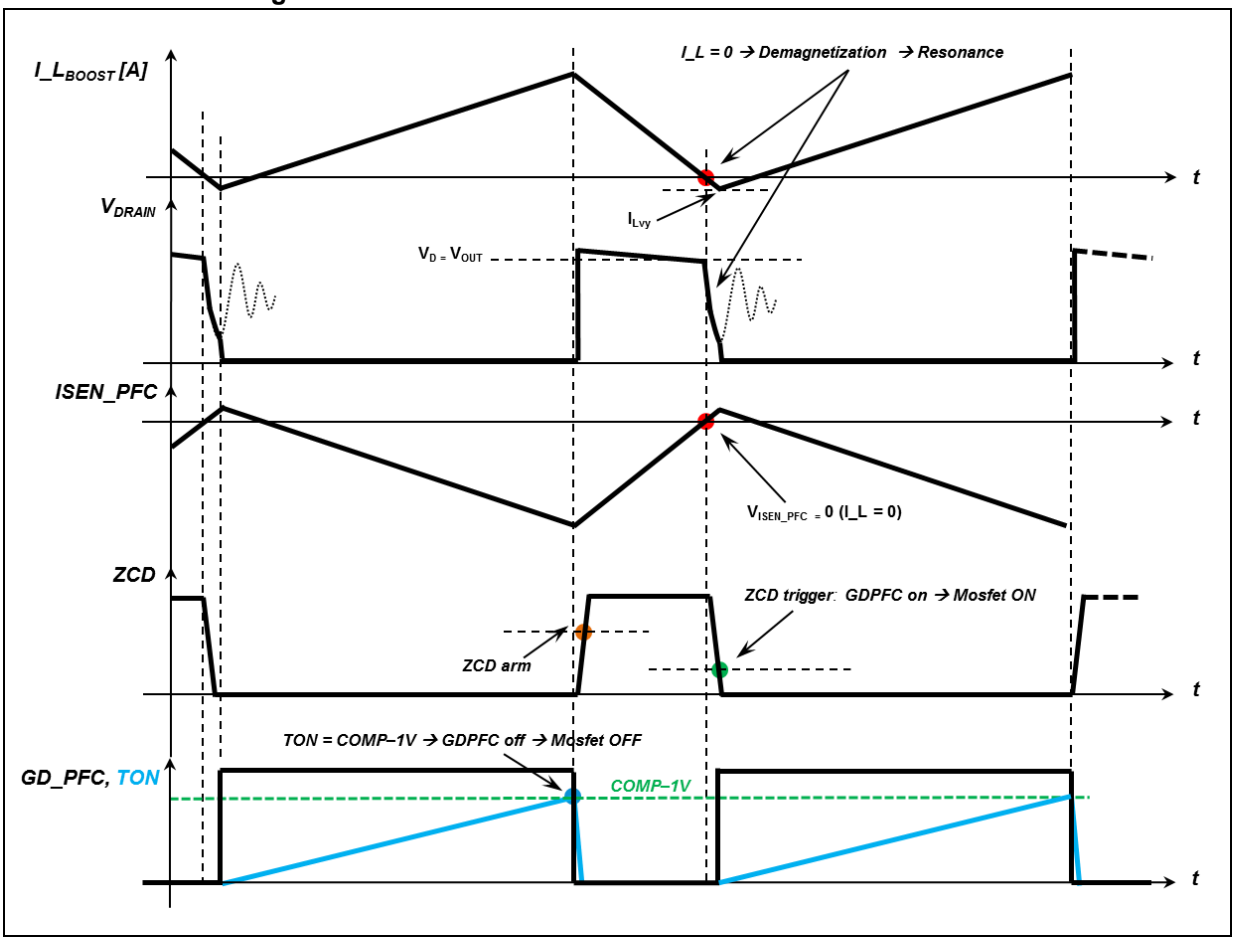
and its average value in a switching cycle is:

Equation 3

$$\left\langle I_L \right\rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{V_{in\_pk}\, sin\,\theta}{2\,L} T_{ON} + V_{in\_pk}\, sin\,\theta \sqrt{\frac{C_{drain}}{L}} - V_{out}\sqrt{\frac{C_{drain}}{L}} \quad (x)$$

The last term *"(x)"* in *Equation 3* is non-sinusoidal (constant) and causes distortion in the input current.

Figure 8. Conventional COT controlled TM PFC waveforms



The enhanced constant on-time (ECOT) control integrated in the STCMB1 is a proprietary solution that outperforms the typical THD performance of the conventional COT control. The idea is to cancel out the constant term "(x)" in *Equation 3* with a corresponding positive term. This can be done by delaying the instant start of the timer that sets the on-time until the inductor current reaches a preset value I_{Lth}. In this way it is no longer the ON-time T_{ON} of the power switch that is controlled (and kept constant) but the time T_{ON_C} defined as:

Equation 4

$$I_{Lpk} = I_{Lth} + \frac{V_{in\_pk}\, sin\,\theta}{L} T_{ON\_C} \quad \text{(y)}$$

Of course, the on-time T_{ON} will no longer be constant as in the conventional COT:

Equation 5

$$T_{ON} = T_{ON\_C} + \frac{I_{Lth} - I_{Lvy}}{V_{in\_pk}\, sin\,\theta} L$$

It is possible to prove that, when choosing:

Equation 6

$$I_{Lth} = V_{out}\sqrt{\frac{C_{drain}}{L}}$$

the average value of the inductor current in a switching cycle will be:

Equation 7

$$\langle I_L \rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{1}{2}\left(\frac{1}{L}T_{ON\_C} + \sqrt{\frac{C_{drain}}{L}}\right)V_{in\_pk}\,sin\,\theta \quad (z)$$

The block diagram and the relevant waveforms of the ECOT-controlled TM PFC are shown in *Figure 9* and *Figure 10*.

On the one hand, a negative threshold is placed on the current sensing pin ISEN_PFC ($V_{ISEN\_PFC\_Z}$ = -25 mV, typ.): the on-time generator (ramp at pin TON) starts as the (negative) voltage on the pin ISEN_PFC goes below $V_{ISEN\_PFC\_Z}$. This is equivalent to having $I_{Lth} = V_{ISEN\_PFC\_Z}/Rs$, where Rs is the current sensing resistor.

On the other hand, when the threshold $V_{ISEN\_PFC\_Z}$ is crossed by the rising signal on the pin ISEN_PFC at the end of the off-time, an internal generator (Ios = 50 µA typ.) is turned on, which sources the current out of the pin ISEN_PFC. This becomes a positive offset voltage on the pin itself, because of the external series resistor Ros (part of the RC filter of the pin). In this way, the crossing of the threshold $V_{ISEN\_PFC\_Z}$ by the negative-going signal can be further delayed and the equivalent current threshold I_{Lth} set at:

Equation 8

$$I_{Lth} = \frac{\left|V_{ISEN\_PFC\_Z}\right| + I_{OS}\,R_{OS}}{Rs}$$

The value of the series resistor Ros can be adjusted to find the optimum I_{Lth}. As a starting point, one can select Ros based on the theoretical compensation condition:

Equation 9

$$R_{OS} = \frac{Rs\,V_{out}\sqrt{\frac{C_{drain}}{L}} - \left|V_{ISEN\_PFC\_Z}\right|}{I_{OS}}$$

Note in *Figure 10* the effect of this offset in the region $V_{ISEN\_PFC} > V_{ISENPFC\_Z}$ (green portion of the inductor current waveform), compared to the unaffected waveform that would occur with Ros = 0 (black portion of the same waveform in the previous cycle).

Figure 9. Enhanced COT controlled TM PFC block diagram

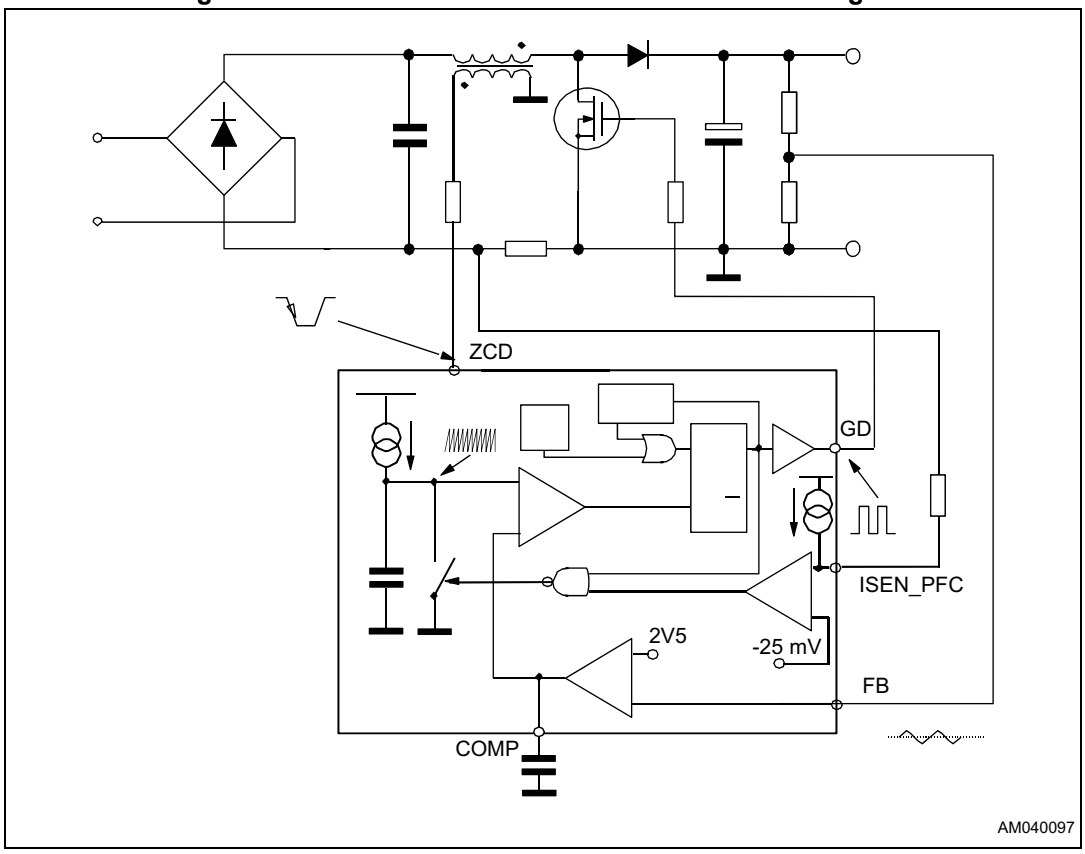
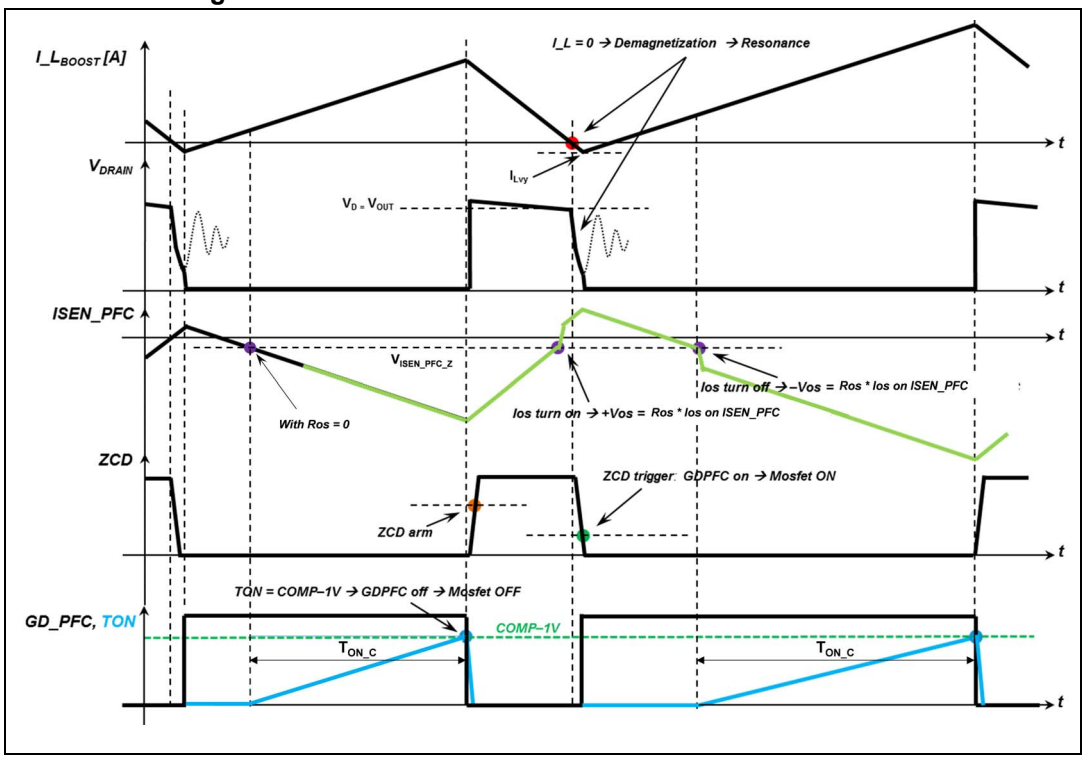


Figure 10. Enhanced COT controlled TM PFC waveforms



7.7 PFC: error amplifier, regulation loop and V_{FF}

The STCMB1 regulation loop keeps the output voltage regulated by means of a transconductance amplifier having an internal 2.5 V reference and a typical gain bandwidth product of 1 MHz. Its inverting input (FB, pin #3) has to be connected to the PFC bulk capacitor via a resistor divider. Since the voltage on this pin is proportional to the PFC output voltage, some other monitoring circuitries are connected to this pin. Because of its high impedance, the FB pin has to be filtered locally by a ceramic capacitor to get a clean and stable voltage. Typical filtering capacitor values are in the range from some nF up to few ten nF.

The error amplifier output (COMP, pin #4), offset by -1 V, is then compared with the Ton ramp signal by the PWM comparator. Thus, the PWM comparator stops the on-time when $V_{TON} = V_{COMP} - 1$ V. The error amplifier output can swing from 1 V (burst mode threshold) up to 4.5 V (upper value).

The on-time generator delivers a constant current charging an external capacitor connected to the Ton pin (#5) used to determine the MOSFET on-time each cycle.

To keep the maximum output power deliverable by the PFC almost constant with respect to the ac input voltage, a two-level, discrete voltage feedforward (VFF) is integrated in the STCMB1. The ac input voltage is monitored via the HV pin (#1) and the signal is fed into a peak detector. This information is used to properly set the value of the current ITON sourced by the TON pin during the normal operation to determine the on-time of the power switch. The threshold aimed to select the proper value of the current ITON is set between 145 and 160 Vac_rms. The proper operation of the PFC, with the right ITON current, is guaranteed below 145 Vac_rms and above 160 Vac_rms.

Whereas mains voltage rises are detected immediately, mains voltage drops are detected after a latency of 16 ms.

Because of this latency, particular attention in the design of the application must be paid to account for line transients that span across the mains ranges. To avoid that the half-bridge shuts down due to the dc brown-out function being triggered (see *Section 7.16: Dc brown-out function (HB enable and disable) on page 30*), the following relationship has to be fulfilled:

Equation 10

$$C_{bulk} \frac{\Delta V_{OUT}}{I_{LOAD}} > 16 \text{ ms}$$

where:

a) C_{bulk} is the output capacitor of the PFC stage.

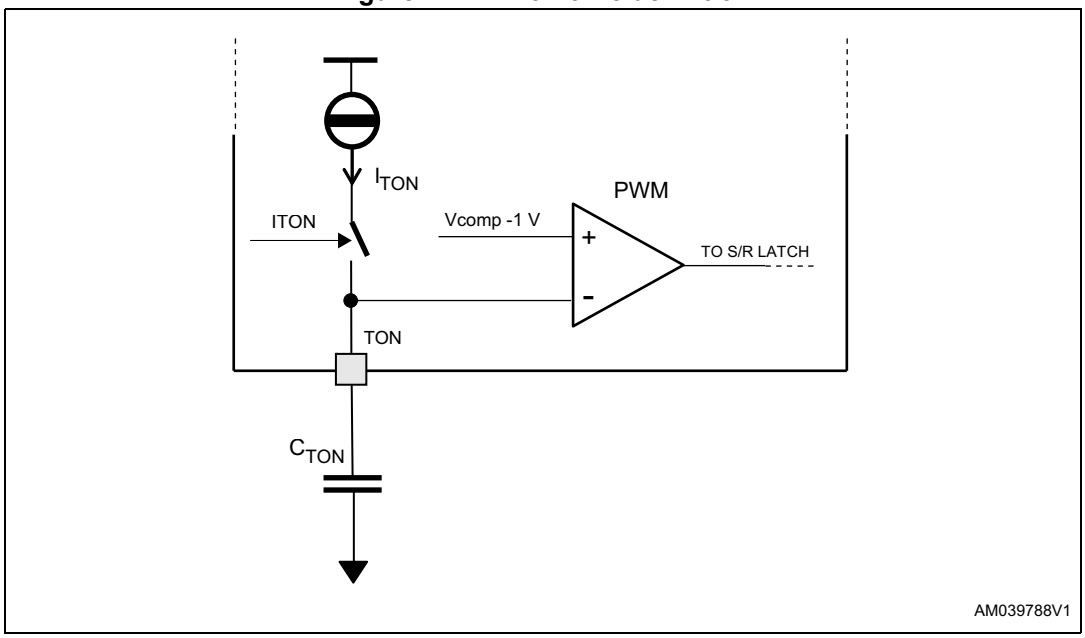
b) ΔV_{OUT} is the maximum allowed output voltage drop (the difference between the regulated output voltage V_{REG} and the dc brown-out threshold (280 V if V_{REG} = 400 V).

c) $I_{LOAD} = P_{OUT}/V_{REG}$ is the output current delivered by the PFC stage and provided to the downstream half-bridge.

7.8 PFC: C_{TON} calculation

Figure 11 shows how the PFC on-time is defined by the PWM comparator, as explained in *Section 7.7: PFC: error amplifier, regulation loop and V_{FF}*.

Figure 11. PFC on-time definition



In detail, C_{TON} must be larger than the maximum on-time T_{ON_MAX} required to carry the maximum power demanded by the load of the PFC stage with the minimum specified ac voltage. The T_{ON_MAX} is a known parameter once the power stage has been designed, in fact:

Equation 11

$$T_{ON\_MAX} = L \frac{ILPk}{\sqrt{2}\ VACmin}$$

The maximum programmable on-time is achieved when the output of the error amplifier is saturated high. This must occur even when the saturation voltage spreads at its minimum value ($V_{COMPSAT\_MIN}$ = 4.2 V for a consumer temperature range design, 4 V for an extended temperature range design).

Therefore, since during the on-time (GD_PFC high) the current generator I_{TON} raises the voltage V(TON) across the capacitor C_{TON}, it is possible to find the minimum C_{TON} value according to the following relationship:

Equation 12

$$C_{TON\_MIN} = T_{ON\_MAX} \cdot \frac{I_{TON\_MAX}}{V_{COMPSAT\_MIN} - 1V}$$

Since this relationship is referred to the minimum input voltage, the appropriate value of I_{TON_MAX} must be used: I_{TON} = 200 µA (I_{TON_MAX} = 220 µA) in US, Japan, or wide-range mains applications, I_{TON} = 800 µA (I_{TON_MAX} = 960 µA) in European mains applications (these value are reported in *Table 4 on page 11*).

7.9 PFC: light-load operation

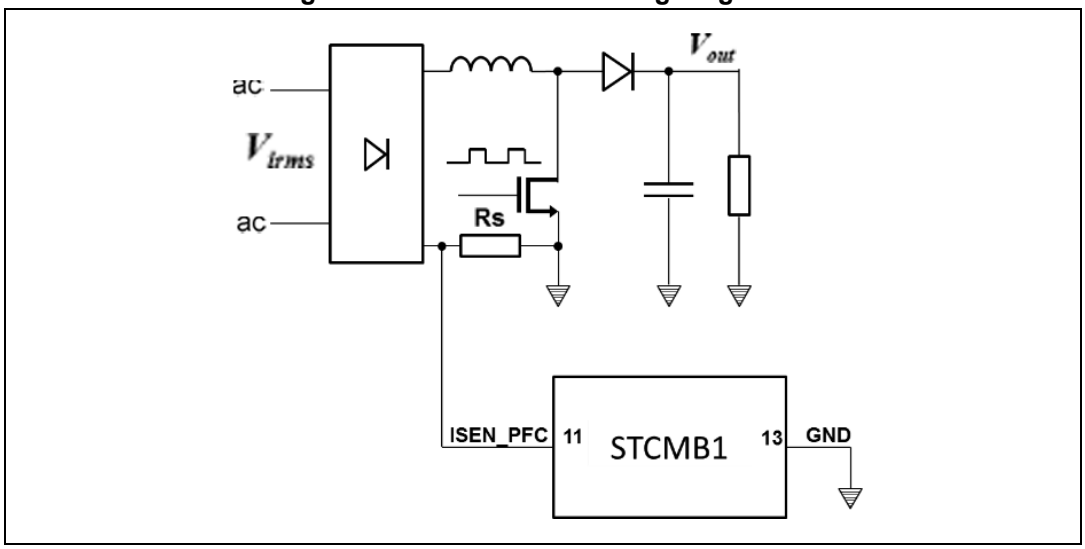
In case of the light-load operation the PFC can work in the burst mode in two ways:

1. If the output of the error amplifier decreases to 1 V an internal comparator stops the switching activity, independently by the HB stage. This burst mode is intended to be used in case of the light-load operation at high mains, in case the burst mode of the HB resonant stage is not used or has a threshold set at the very low load.
2. If the HB resonant stage detects a light-load and begins working in the burst mode will force the PFC working synchronized in the burst mode too. In detail, when the LLC enters in the idle state of the burst mode, the last PFC pulse is reset, in its natural way, by TON reaching COMP - 1 V. Conversely, when the LLC restarts switching, at the end of the idle state, the first PFC pulse is delayed of about 10 µs with respect to the first LLC pulse. Further details in *Section 7.20: HB: improved burst mode operation at light-load on page 37*.

Note that the connection of an oscilloscope probes to the COMP pin, when the PFC is in the deep burst mode, could modify the proper operation of the PFC.

7.10 PFC: inductor current sensing on ground return and PFC OCP

Figure 12. PFC current sensing on ground



The STCMB1 implements the PFC current sensing on the ground return path, by means of the ISEN_PFC pin. In this way the signal fed into that pin has the information of the current level during the entire switching period, differently from other systems monitoring the current during the PFC MOSFET on-time only.

Monitoring the current during the whole switching period allows safe handling of inductor saturation conditions: an internal comparator enables the MOSFET to be turned on only if the inductor has completed its demagnetization, not before. This mechanism prevents the MOSFET from turning on with incomplete inductor demagnetization, for example following a mains dip or during an inrush current charging the bulk capacitor. Both these situations might result in very dangerous condition for the MOSFET because of the very low impedance of a saturated coil.

The PFC OCP is integrated on the ISEN_PFC pin too: it is equipped with an OCP comparator, stopping the MOSFET conduction time in case the current reaches the threshold V_{ISEN_PFC} (-0.5 V typ.), realizing a pulse-by-pulse current limiting.

Calculation of the sensing resistor can be done according to the following procedure:

1. Calculate the maximum peak current in the PFC inductor/MOSFET/diode:

Equation 13

$$I_{L\_pk\_\max} = I_{Lth} + \frac{V_{in\_pk\_\min}}{L} T_{ON\_c\_\max}$$

2. Calculate the maximum sense resistor value:

Equation 14

$$Rs \leq \frac{V_{ISEN\_PFC\_\min}}{I_{L\_pk\_\max}}$$

3. Select the commercial value Rs, next to Rsx.
4. Calculate the ILrms current:

Equation 15

$$I_{Lrms} = \frac{1}{\sqrt{6}} \left(I_{L\_pk\_\max} + I_{Lvy} \right)$$

5. Calculate the sensing resistor(s) power dissipation:

Equation 16

$$P = Rs \bullet ILrms^2$$

7.11 PFC: zero-current detector

The PFC embedded in the STCMB1 uses the ZCD pin as the boost inductor's demagnetization sensing input. A negative-going edge triggers the PFC MOSFET's turn-on. The pin is provided with two clamps to protect the pin from voltage above its rating, so it can be connected to an auxiliary winding of the boost inductor through a resistor. A series limiting resistor has to be provided to limit the current injected in the pin voltage clamps. The demagnetization can also be sensed via an RC series connected to the MOSFET.

For debug purposes it is possible disable the PFC stage by pulling this pin over 2.4 V at the start-up, thus allowing the half-bridge section to work standalone.

7.12 Starter

Because any transition mode PFC is basically a self-oscillating converter, using a self-generated signal for the MOSFET to turn-on, a starter signal is necessary to start the operation at power-on or restart the operation after an idle state, when the ZCD signal is not present.

The STCMB1 device is provided with an internal starter having a 10 µs period and working at wake-up, at the burst mode restart, after OVP or inrush current protection intervention.

7.13 PFC: Dynamic OVP and feedback failure protection (latched)

The STCMB1 is equipped with PFC protections to prevent failures due to an excessive PFC voltage.

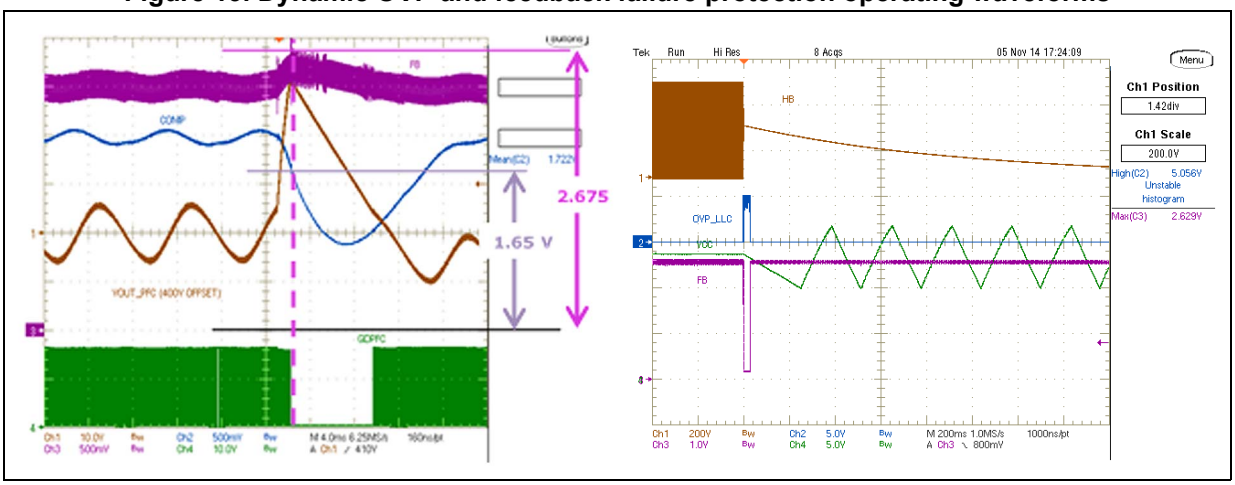
The dynamic overvoltage protection (OVP) is non-latch protection dedicated to prevent an excessive increasing of the PFC output voltage caused by load transients that may happen because of the typically limited bandwidth of the PFC output voltage regulation loop. In this case an internal comparator monitoring the PFC output voltage via the FB pin (#3) stops the switching activity if the voltage at the pin reaches the threshold V_{FB_S} (2.675 V typ.) and will allow the restarting if the voltage on the pin decreases to V_{FB_R} (2.55 V typ.).

An additional protection against overvoltages caused by a PFC loop failure (disconnection) is also integrated in the STCMB1 device: in case the voltage on the FB pin (#3) drops to the threshold V_{FB_D} (0.45 V typ.) an internal comparator stops the switching activity of both converters, latching the IC operation. The HV start-up is activated to keep the latch condition. The latch condition will be cleared by unplugging the power supply from the mains.

In case a latch protection is needed for other purposes as the LLC open loop or OTP it is possible latch the whole STCMB1 by tie the FB pin to GND by an open collector or an open drain transistor.

The mentioned protection thresholds are in tracking with the internal reference of the IC and therefore will have a similar tolerance as the PFC error amplifier reference.

Figure 13. Dynamic OVP and feedback failure protection operating waveforms



In *Figure 14* the waveforms in case of the Dynamic OVP and feedback failure protection intervention have been captured. In case of the intervention of Dynamic OVP (left picture) we can see a case of load disconnection: the error amplifier output starts decreasing but the narrow bandwidth of the loop do not allow a fast response, in the meantime the PFC output voltage has increased. The FB pin voltage has increased proportionally and when that voltage has crossed the threshold the PFC has stopped the switching activity. We can also see on the picture that the COMP pin level is well above the burst mode threshold and therefore the stopping of switching activity is not due to the burst mode comparator. The PFC restarts switching when the FB voltage decreases at 2.55 V. Considering the nominal PFC output voltage we can calculate the Dynamic OVP threshold as:

$$V_{PFC\_DOVP} = V_{PFC} \bullet 1.06.$$

In the left picture a feedback disconnection event has been captured: we can see that when the FB pin drops below the threshold the converters stops switching and the HV start-up is activated keeping the STCMB1 correctly powered to retain the latch condition. The latch condition can be cleared by unplugging the ac mains voltage.

7.14 PFC gate driver

The GD_PFC gate driver has a DMOS structure driving the MOSFET gate. The current capability is 0.3 A at the MOSFET turn-on and 0.7 A at turn-off, giving typical rise and fall times of 60 ns and 30 ns respectively, so it is able to drive MOSFETs with suitable size for high efficiency transition mode PFCs.

The driver has no any voltage clamping of the gate voltage thus the MOSFET will be driven with a driving voltage at the V_{CC} level. For this reason the V_{CC} will have to be limited in all operating or fault condition to a safe level, to avoid any premature aging or damaging of the MOSFETs gate oxide.

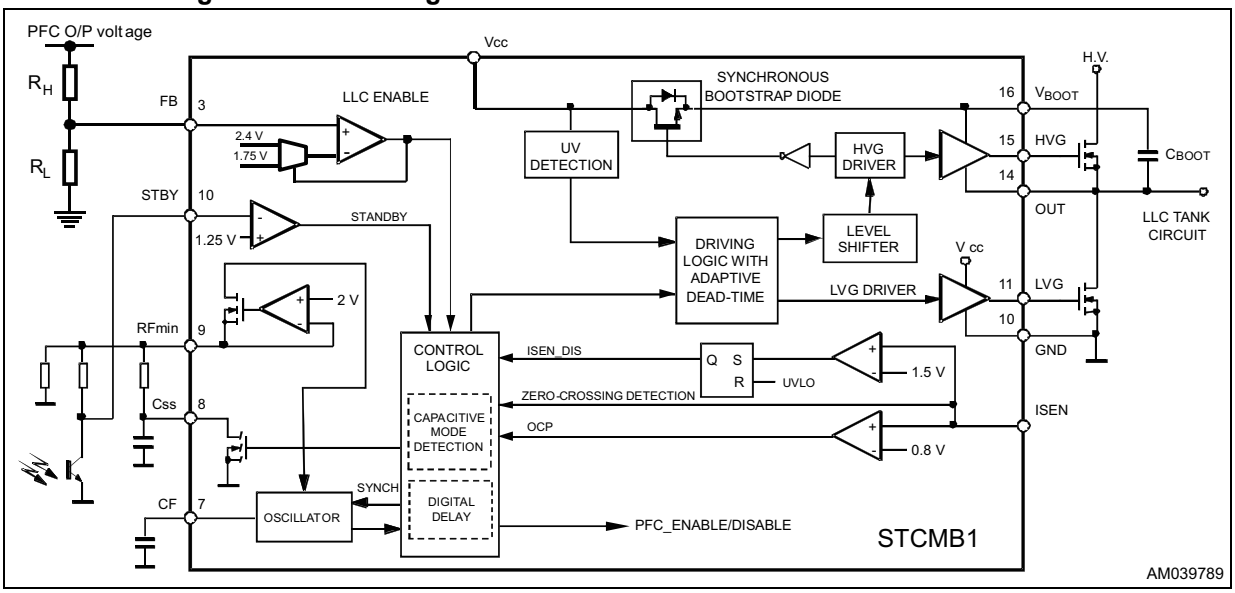
Active pull-down circuitry prevents any undesired MOSFET turn-on that might occur in very noisy environment and allows removing the typical gate-source resistance or using a higher value.

7.15 Resonant HB section

The STCMB1 embeds an advanced double-ended controller specific for the resonant half-bridge topology. Its detailed block diagram is illustrated in *Figure 7 on page 19*.

Normally, in this converter the MOSFETs of the half-bridge leg are alternately switched on and off (180 ° out-of-phase) for exactly the same time. This is commonly referred to as an operation at “50% duty cycle”, although the real duty cycle, e.g.: the ratio of the on-time of either switch to the switching period, is actually less than 50%. The reason is that there is a deadtime TD inserted between the turn-off of either MOSFET and the turn-on of the other one, where both MOSFETs are off. This deadtime is essential in order for the converter to work correctly: it enables soft-switching and, then, the high frequency operation with high efficiency and low EMI emissions.

Figure 14. Block diagram of the HB resonant controller in the STCMB1



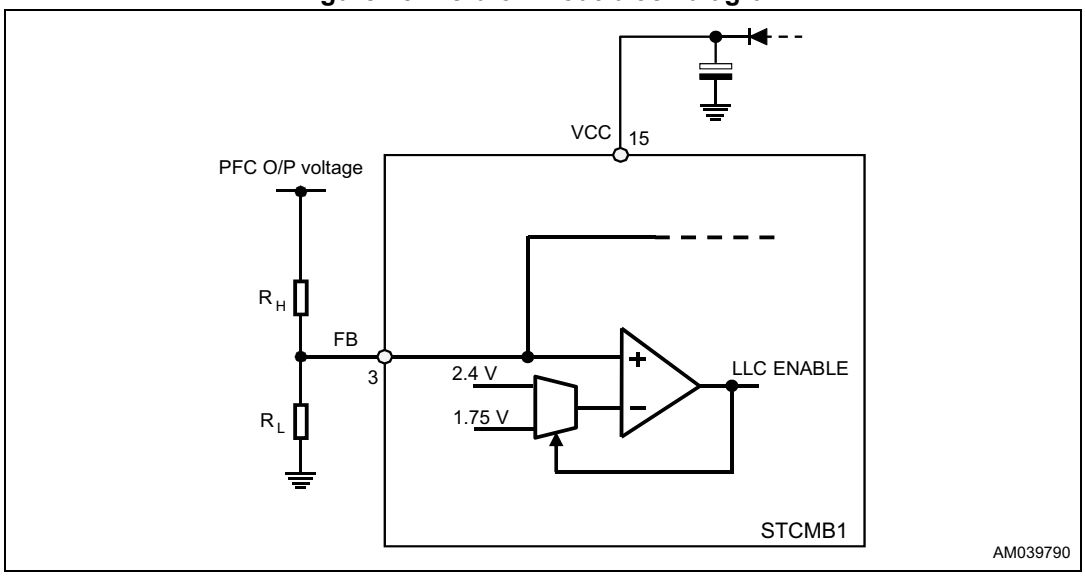
A special feature of this IC is that it is able to automatically adjust TD within a range so that it best fits the transition time of the half-bridge midpoint (adaptive deadtime). This allows the user to optimize the design of the resonant tank so that soft-switching can be achieved with a lower level of reactive energy (e.g.: magnetizing current), hence optimizing efficiency under a broader load range, from full to the light-load.

To perform converter's output voltage regulation the device is able to operate in different modes, depending on the load conditions:

1. Variable frequency with 50% duty cycle at the heavy and medium load. A relaxation oscillator (see *Section 7.18: HB: oscillator on page 33* for more details) generates a sawtooth, which MOSFETs' switching is locked to. The frequency of this waveform is regulated by:
   a) A current that is modulated by the feedback circuitry (as in DFC systems)
   b) A control of the amount of time elapsing from a zero crossing of the tank current to the next switching of the half-bridge (timeshift control - TSC)
2. Burst mode with no or a very light-load. When the load falls below a value, the converter enters a controlled intermittent operation, where series of a few switching cycles at a nearly fixed frequency (bursts) are spaced out by idle periods where both MOSFETs are in off-state. A further load decrease will be translated into shorter bursts and longer idle periods and then into a reduction of the average switching frequency.

7.16 Dc brown-out function (HB enable and disable)

Figure 15. Dc brown-out block diagram



The dc brown-out is a function dedicated to manage the correct sequencing of the converters at the power-on and shutdown. This function is necessary to ensure that the resonant HB stage starts after the PFC has started up, and PFC output voltage is close to the nominal level. The function also guarantees that at power-off the resonant HB stops the operation at a precise input voltage level, thus allowing to properly manage the hold-up requirements of the power supply. Actually, the PFC bulk capacitor acts as a reservoir battery and powers the resonant stage when the ac mains disappears.

The function monitors the PFC output voltage on the FB pin and enables the resonant HB stage operation as the pin voltage reaches 2.4 V (V_{FB_E} typ. value). The resonant stage is then stopped if the voltage on the FB pin drops to 1.75 V (V_{FB_D} typ. value). The resonant HB is re-enabled as the voltage on the FB pin rises again above the enable voltage reference V_{FB_E}.

Considering a PFC delivering a typical 390 V output voltage at nominal V_{ref}, we can easily calculate the resonant HB stage enable and disable voltages:

Equation 17

$$V_{PFC} = 390V$$

$$V_{ref} = 2.5V$$

$$V_{FB-E} = 2.4V$$

$$V_{FB-D} = 1.75V$$

$$V_{HB-Start} = V_{PFC} \bullet \frac{V_{FB-E}}{V_{ref}} = 374.4V$$

$$V_{HB-Stop} = V_{PFC} \bullet \frac{V_{FB-D}}{V_{ref}} = 273V$$

The calculated voltage V_{HB_Stop} will have to be guaranteed by the bulk capacitors after the hold-up time and will be the minimum voltage at which the resonant HB converter will work, and therefore it will be dimensioned according to that minimum voltage.

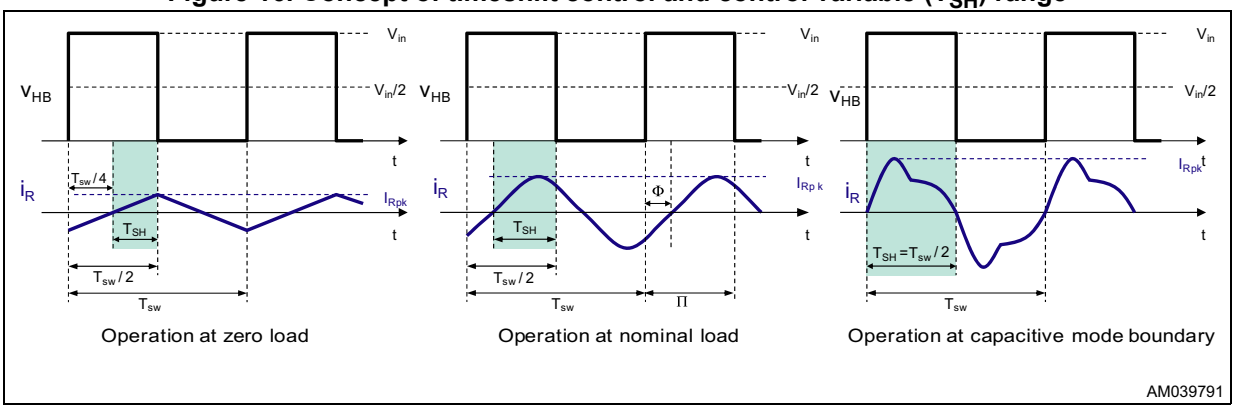
Since the PFC stage is typically designed at the minimum input voltage (and maximum output load), a DC brown-out event could occur at heavy loads, when the input voltage is between the minimum input voltage and the AC brown-out threshold. In fact, in this condition, the PFC is limiting the power delivered and its output voltage could decrease up to the DC brown-out threshold at which the LLC stage is turned off: VOUT will drop and VCC will be discharged. As VCC reaches VCCon, the HV start-up is activated, VCC recharged and operations restarted as VCC reaches VCCon.

To avoid the occurrence of a DC brown-out event before the AC brown-out, at the full load, the PFC stage has to be designed at the ACBO threshold rather than at the minimum input voltage.

7.17 HB: timeshift control basic concept

The TSC methodology consists in controlling the amount of time T_{SH} elapsing from a zero crossing of the tank current to the next toggling of the half-bridge, as shown in *Figure 16*. The edge of the square wave voltage commanded at the end of T_{SH} has the opposite sense with respect to that of the current zero crossing that initiated T_{SH}. This ensures that the tank current lags behind the applied square wave voltage and, therefore, that the MOSFETs of the half-bridge work with soft-switching. *Figure 16* shows, for example,
a negative-going edge of the square wave voltage commanded after a positive-going zero crossing of the tank current (highlighted in blue).

Figure 16. Concept of timeshift control and control variable (T_{SH}) range



Denoting with the phase shift of the tank current with respect to the applied square wave voltage, *Equation 18* relates the timeshift to operating frequency f_{sw}:

Equation 18

$$T_{SH} = \frac{\pi \quad \Phi}{2\pi \quad f_{sw}}$$

Under no load conditions, the operating frequency reaches the maximum value f_{swmax}, the switching period is $T_{swmin} = 1/f_{swmax}$ and the tank current is in quadrature to the voltage ($\Phi = \pi/2$; *Figure 16*, left-hand side), so it is $T_{SH} = T_{swmin} / 4$. On the opposite side, at the boundary with the capacitive mode operation, when the current and voltage are in phase

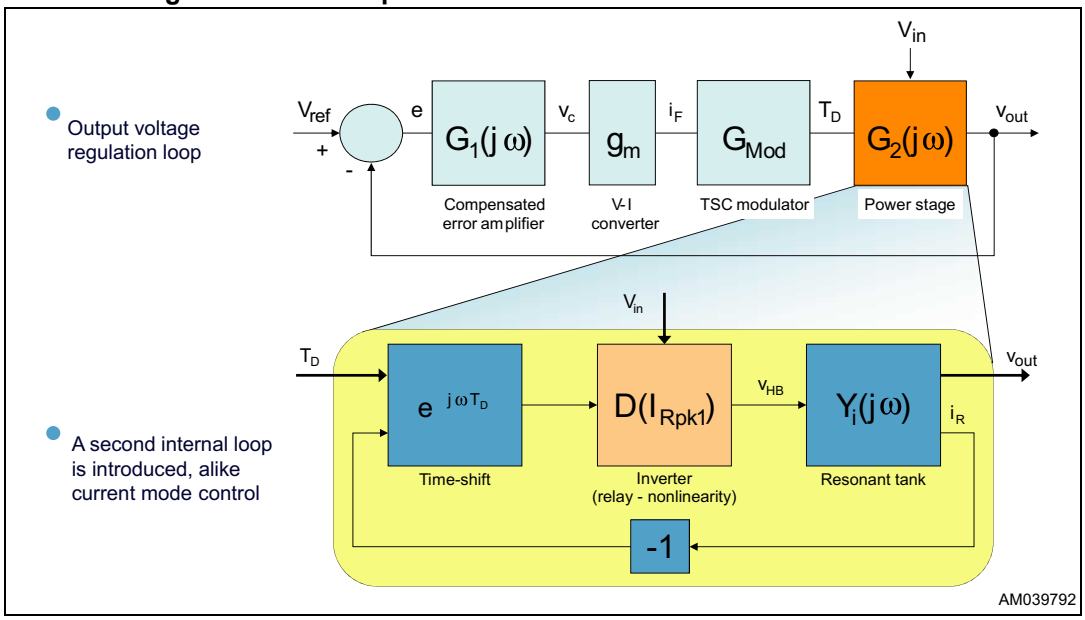
(*Figure 16*, right-hand side), it is $\Phi = 0$, the operating frequency reaches the critical value f_{swcm}, the switching period is $T_{swcm} = 1/f_{swcm}$ and $T_{SH} = T_{swcm} / 2$.

Therefore, in a properly designed converter the range of T_{SH} is included between $T_{swmin} / 4$ and $T_{swmax} / 2$, with $T_{swmax} < T_{swcm}$.

Conceptually, with TSC an inner loop is closed, and the outer loop that regulates the output voltage provides the reference T_{SH} for the inner loop. This is schematically illustrated in *Figure 17*.

The feedback variable in the inner loop is the tank current i_R, whose zero crossings are used as the starting point for T_{SH}, while the input quantity to the tank circuit is the applied square wave voltage v_{HB}. From the control point of view, converter's input voltage Vin can be seen as a disturbance that affects the inverter block (the half-bridge leg that generates the square wave voltage applied to the resonant tank).

Figure 17. Dual-loop structure of a resonant converter with TSC



Since the tank circuit responds primarily to the first harmonic of the applied square wave voltage v_{HB} and negligibly to the higher order harmonics, the inner loop can be analyzed using the describing function approach. The result of the stability analysis is that the loop is absolutely stable as long as the control variable is included in the range:
($T_{swmin} / 4$, $T_{swcm} / 2$).

The open-loop dynamic behavior of an LLC converter with TSC has been found to be that of a low Q second-order system, that is, a system with two real, well separated poles. Therefore, it is possible to use dominant pole approximation at frequencies below crossover and, from the practical point of view, treat it as a first-order system.

There is a number of benefits resulting from these properties, which can be summarized as follows:

- Converter dynamics is very close to that of a first-order system: frequency compensation is considerably simpler (a standard type 2 compensation scheme can be used for optimum results) and its natural response to perturbations is overdamped. This makes the system less prone to those small subharmonic oscillations that can be sometimes observed as a result of switching noise or when secondary synchronous rectification is used.
- Load transient is considerably improved: overshoots and undershoots are significantly smaller, settling times significantly shorter.
- Input ripple rejection is improved: because of the simpler dynamics, the low frequency gain of the feedback loop can be considerably larger (at least 15 - 20 dB), with a corresponding reduction of the residual 100/120 Hz ripple on the output voltage.
- Hard switchings at the start-up are prevented: it's inherent in the control methodology to ensure that the half-bridge toggles when the tank current has the right sign in order for the MOSFETs to achieve soft-switching.

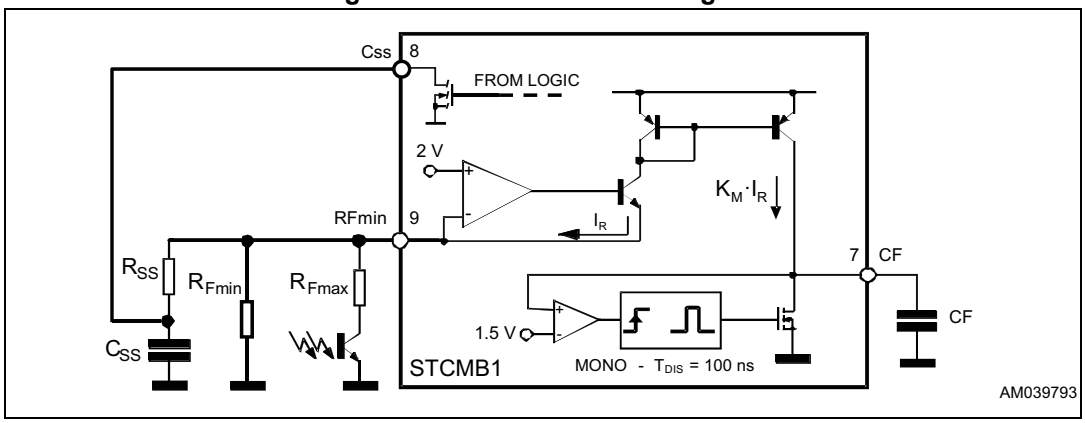
For more information on the methodology, please refer to *Section 11: Reference on page 56*.

7.18 HB: oscillator

The oscillator is programmed externally by means of a capacitor (C_F), connected from the CF pin to ground, and the network connected to the RFmin pin. The capacitor C_F is charged with a constant current starting from zero up to a peak value (= 1.5 V in continuous switching) and then quickly discharged, thus originating a triangular sawtooth. The network connected to the RFmin defines the charging current for the C_F.

The RFmin pin provides an accurate 2 V reference capable of sourcing up to 2 mA; the current I_R sourced by the pin is internally mirrored and output from the CF pin. The mirroring ratio, K_M is typically 1. Therefore, the higher I_R is, the faster C_F is charged. The simplified block diagram of the oscillator is shown in *Figure 18*. The circuitry that locks and synchronizes the actual set of the oscillator ramp to the zero crossing of the tank current, sensed at the ISEN_HB pin, is not shown for the sake of simplicity.

Figure 18. Oscillator block diagram



The network connected to the RFmin pin generally comprises three branches:

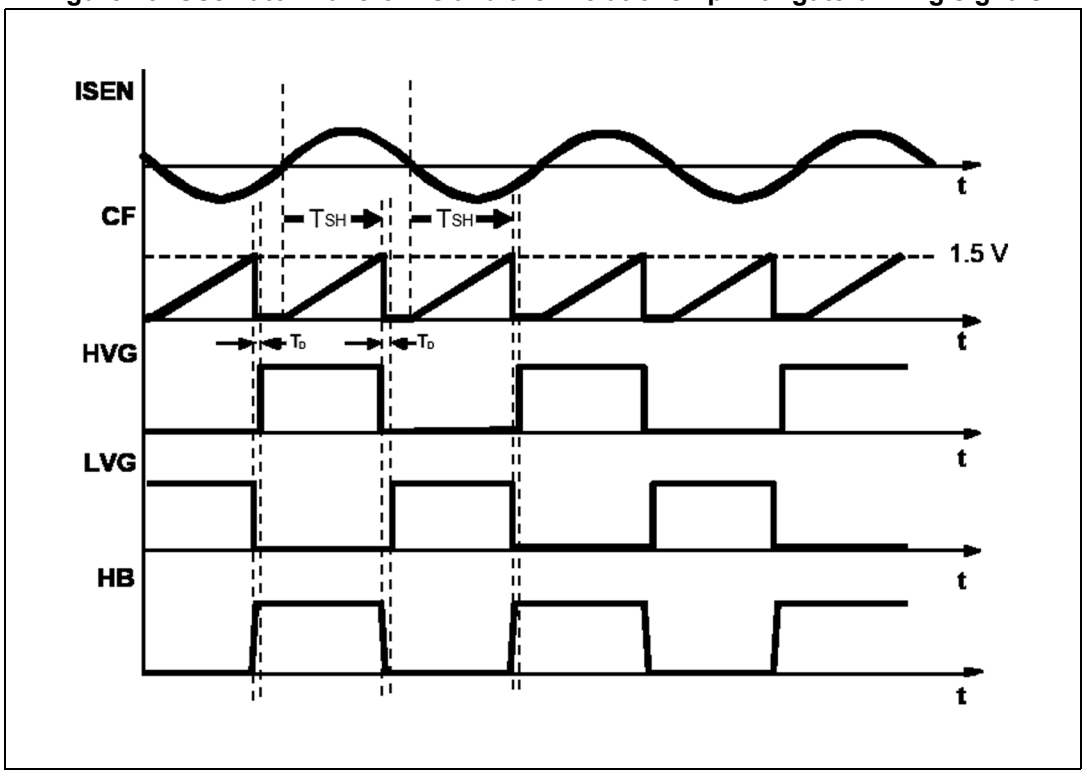
1. A resistor RF_{min} connected between the pin and ground that determines the minimum oscillator frequency
2. A resistor RF_{max} connected between the pin and the collector of the (emitter-grounded) phototransistor that transfers the feedback signal from the secondary side back to the primary side; while in the operation, the phototransistor will modulate the current through this branch - hence modulating the oscillator frequency - to perform output voltage regulation; the value of RF_{max} determines the maximum oscillation frequency when the phototransistor is fully saturated
3. An R-C series circuit (C_{SS} + R_{SS}) connected between the pin and ground that enables to set up a frequency shift at the start-up. Note that the contribution of this branch is zero during the steady state operation.

Because of the time shift control implementation, the on-time of the half bridge is defined not only by the oscillator ramp, but also by the time the current takes to arrive to zero from the switched value, since the oscillator ramp is actually set by the signal at the ISEN_HB pin crossing zero.

In the end, the oscillator frequency is always twice the half bridge frequency, being its period given by the sum of the time the tank current, sensed at the ISEN_HB pin, takes from its switched value to its zero crossing and the time length of the ramp, that is defined by the external capacitor on the CF pin and by the current the control loop pulls from the RFMIN pin.

From this point, we will refer to the switching frequency of the half-bridge, it being understood that the oscillator frequency is always twice as much.

Figure 19. Oscillator waveforms and their relationship with gate-driving signals



In spite of the time-shift control, the calculation of the oscillator components can be easily done taking into account the limits of the operating frequency range of the converter, used for the resonant converter calculation. Therefore, after fixing CF in the hundred pF or in the nF range (consistent with the maximum source capability of the RFmin pin and trading this off against the total consumption of the device), the value of RFmin and RFmax will be selected so that the oscillator frequency is able to cover the entire range needed for regulation, from the minimum value fmin (at minimum input voltage and maximum load) to the maximum value fmax (at maximum input voltage and minimum load):

Equation 19

$$Rfmin = \frac{2V}{3VC_F \cdot f_{min}} \qquad Rfmax = \frac{2V - V_{CEsat}}{3VC_F \cdot (2f_{max} - fmin)}$$

V_{CEsat} is the saturation voltage of the phototransistor.

The above RFmax formula has to be considered for calculation in case the resonant stage does not need working in the burst mode, in that case the STBY pin (#10) will have to be connected to the RFmin (pin #9).

If the burst mode has to be implemented *Equation 20* has to be used.

Equation 20

$$Rfmax_{BM} = \frac{1V}{4V \cdot C_F \cdot (2f_{max} - f_{min})}$$

7.19 HB: Soft-start

The soft-start function is simply realized by the addition of an R-C series circuit from the pin 9 (RFmin) to ground (see *Figure 20*, left). The middle point of the RC is also connected to the pin 8 (CSS).

Initially, the capacitor C_{SS} is totally discharged, so that the series resistor R_{SS} is effectively in parallel to R_{Fmin} and the resulting initial frequency is determined by R_{SS} and R_{Fmin} only, since the optocoupler's phototransistor is cut off (as long as the output voltage is not too far away from the regulated value):

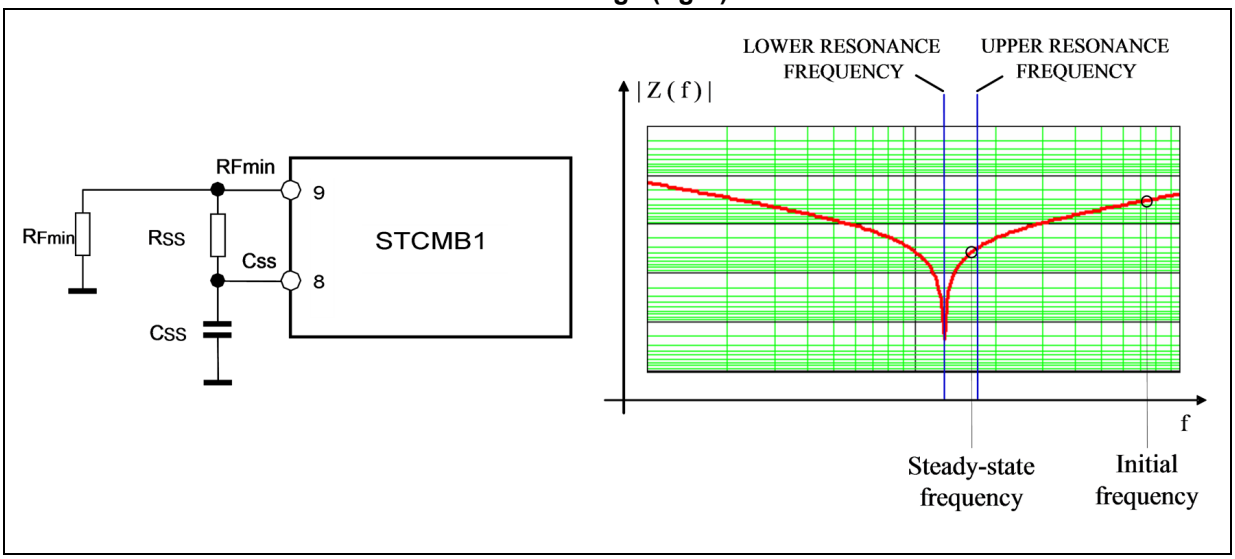
Equation 21

$$f_{start} = \frac{1}{3 \cdot CF \cdot \left(RF_{min} // R_{SS} \right)}$$

The C_{SS} capacitor is progressively charged until its voltage reaches the reference voltage (2 V) and, consequently, the current through the R_{SS} goes to zero. This conventionally takes 5 times constants $R_{SS} \cdot C_{SS}$ however, the soft-start phase really ends when the output voltage has got close to the regulated value and the feedback loop taken over, so that the operating frequency is essentially determined by the current sunk by the optocoupler's phototransistor.

During this frequency sweep phase the operating frequency will decay following the exponential charge of the C_{SS}: then, it initially changes relatively quickly but the rate of the change gets slower and slower. This counteracts the non-linear frequency dependence of the tank circuit that makes the converter's input impedance change little as frequency is away from resonance, and the change very quickly as frequency approaches resonance frequency (see *Figure 20*, right).

Figure 20. Soft-start circuit (left) and input impedance vs. frequency curve in an LLC resonant half-bridge (right)



As a result, the dc input current will smoothly increase, without peaks that might occur because of the resonant tank transfer function, and the output voltage will reach the regulated value with almost no overshoot.

Typically, the R_{SS} and C_{SS} will be selected based on the following relationships:

Equation 22

$$R_{SS} = \frac{RF_{min}}{\frac{f_{start}}{f_{min}} - 1} \quad ; \quad C_{SS} = \frac{3 \cdot 10^{-3}}{R_{SS}}$$

where f_{start} is recommended to be at least 4 times f_{min}. These criteria are quite empirical and a workaround checking the waveforms and fine tuning of the R_{SS} and C_{SS} values might be required.

It is recommended that the resonant current has no severe overshoots that might trigger the OCP1 threshold (ISEN_HB ≥ 0.8 V) in the first half bridge pulses, because the proper charge of the C_{SS} would be negatively prevented.

Please note also that an internal switch will discharge the C_{SS} capacitor every time the chip turns off (VCC < UVLO, FB < 1.75 V, ISEN_HB > 1.5 V) to make sure it will be soft-started at the following restart. Additionally, the switch is activated when the voltage on the current sense pin (ISEN) exceeds 0.8 V or when the converter is working in the capacitive mode operation.

As long as the voltage on the pin is lower than 0.3 V, the burst mode operation and second level OCP protection are inhibited.

7.20 HB: improved burst mode operation at light-load

Despite the optimization of the LLC tank circuit allowed by the adaptive deadtime function and the anti-capacitive protection function (see *Section 7.21: HB: adaptive deadtime (ADT)*), the latest requirements on energy saving are so demanding that a significant optimization effort is still needed to fulfill them.

To reduce this effort, the STCMB1 device implements a novel concept of the burst mode operation that significantly increases the amount of energy carried by the converter in each switching cycle. As a result, the average values of the switching frequency and the residual magnetizing current are dramatically reduced and light-load efficiency further boosted.

While output power decreases, switching frequency increases up to a programmed level fmax; the maximum frequency value fmax is reached when the voltage on the STBY pin equals the internal voltage threshold V_L (1.25 V typ.). When $V_{STBY} \leq V_L$ the STCMB1 enters in idle state, its quiescent current consumption is reduced and the internal threshold is shifted up to the restart value V_L + Hys (= 1.25 V + 40 mV).

In detail, the LLC is stopped as STBY goes below VL and restarted as STBY goes above V_L + HYS. Furthermore, it is practically the master on the PFC whose the last pulse in the switching packet is naturally stopped by TON = COMP - 1 V, while it is turned on with a certain delay (10 µs typ.) with respect to the first LLC pulse of the switching packet.

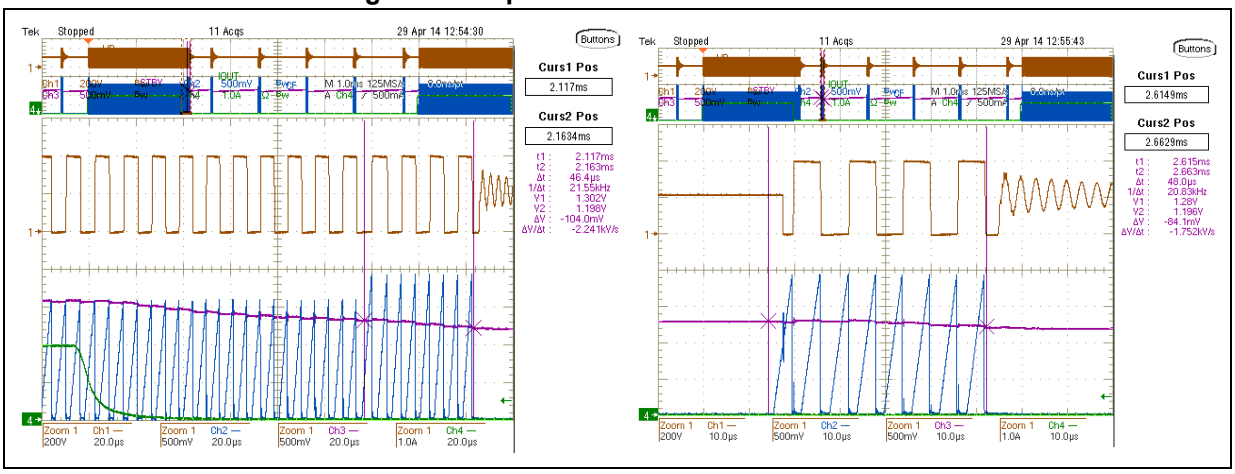
The novelty consists in an additional threshold located slightly over V_H. When the voltage on the STBY pin falls below this threshold the oscillator ramp peak value V_{CFp} is increased. This is clearly noticeable in the left side picture of *Figure 21*. In this way the average switching frequency is reduced as long as voltage on the STBY pin remains between V_H and V_L, and the converter efficiency is increased.

In other words, it is possible to obtain very short switching packets, but with a significant energy content: so short that an inherent limit of having the LLC master on the PFC could be highlighted. In fact, when the PFC is driven by the burst mode of the LLC, its loop is open and its output voltage is defined by the energy transfer, from the mains to the bulk capacitor, allowed by the length and the period of the switching packets. To overcome this problem, as said, the last PFC pulse in the switching packet is reset by its natural mechanism (TON = COMP - 1 V).

During the HB burst mode, the stop and restart are accurately controlled: the last cycle before switching stoppage ends with a complete HVG pulse and the first cycle after restarting is the LVG pulse (with half duration) to minimize the perturbations on the dc voltage across the resonant capacitor Cr.

If the burst mode is not used connect the STBY pin (#10) to the RFmin (pin #9).

Figure 21. Improved burst mode waveforms



7.21 HB: adaptive deadtime (ADT)

A deadtime T_D is inserted between the turn-off of either switch and the turn-on of the complementary one, where both switches are in the OFF state. This is essential to achieve soft-switching: its value has to be larger than the time T_T needed for the rail-to-rail swing of the half-bridge leg midpoint (HB). This duration T_T depends on the total parasitic capacitance of the node HB (CHB) that has to be completely charged or depleted and on the value of the resonant tank current during the transition.

With good approximation, the tank current during the transition time T_T can be considered constant and equal to the “switched current” IS, e.g.: the value of the tank current as the transition begins. If C_{HB} denotes the total parasitic capacitance of the half-bridge midpoint (it includes the Coss of the MOSFETs, the transformer's primary winding parasitic capacitance, plus other stray contributors), the condition for soft-switching is:

Equation 23

$$T_T = \frac{C_{HB}}{I_S} \quad V_{in} \leq T_D$$

which should be met under all operating conditions. This suggests that T_D should be large enough to always exceed T_T, especially with maximum Vin and at no load, where I_S is at a minimum and T_T at a maximum. However, fixing a too long deadtime may lead to losing soft-switching too: in fact, the tank current must not change sign within the deadtime, which could lead to turn-on either the MOSFET with a non-zero drain-to-source voltage or, even worse, with the body diode of the other MOSFET conducting (see *Section 7.22: HB: hard switching prevention (HSP) and anti-capacitive mode protection (ACP) on page 41* for more details). This might occur at the maximum load and minimum Vin, especially when the tank circuit is designed for a low magnetizing current to optimize light-load efficiency. Additionally, a too long deadtime might increase conduction losses in the body diodes and significantly limit the operating frequency of the half-bridge.

A good approach is to automatically adjust T_D so that it tracks T_T, keeping $T_D \geq T_T$ under all operating conditions. This is the objective of the adaptive deadtime function in the STCMB1.

Figure 23 shows the principle schematic and its key waveforms. An edge detector (the |d/dt| block) senses that the node HB (connected to the OUT pin) is swinging from B+ to ground or vice versa. The output of the |d/dt| block is high as long as the OUT pin is swinging and, as

the transition is completed, the output goes low. A monostable circuit, sensitive to negative-going edges, releases a pulse that marks the end of the deadtime.

The derivative of HB voltage needed for the ADT function is implemented sensing the signal current flowing through both the intrinsic C_{gd} capacitor of the external power MOS and the LVG pin.

The signal current ($i_{source/sink}$) is proportional to the derivative of HB voltage and C_{gd} value:

Equation 24

$$i_{source/sink} = i_{Cgd} = C_{gd} \frac{dV_{HB}}{dt}$$

In order to ensure the right behavior of the ADT function, this current signal has to fulfill the following:

Equation 25

$$i_{source/sink} > S_{diff} \; (S_{diffMAX} \approx 4 \text{ mA})$$

where S_{diff} is the minimum current signal which can be detected by the edge detector.

C_{gd} is a function of drain-source voltage of the LVG power MOS and the HB voltage slope is not constant but it depends on the value of the current flowing in the resonant tank. Therefore, in view of obtain reliable derivative detection, the following relationship has to be fulfilled at least at the end of HB transition:

Equation 26

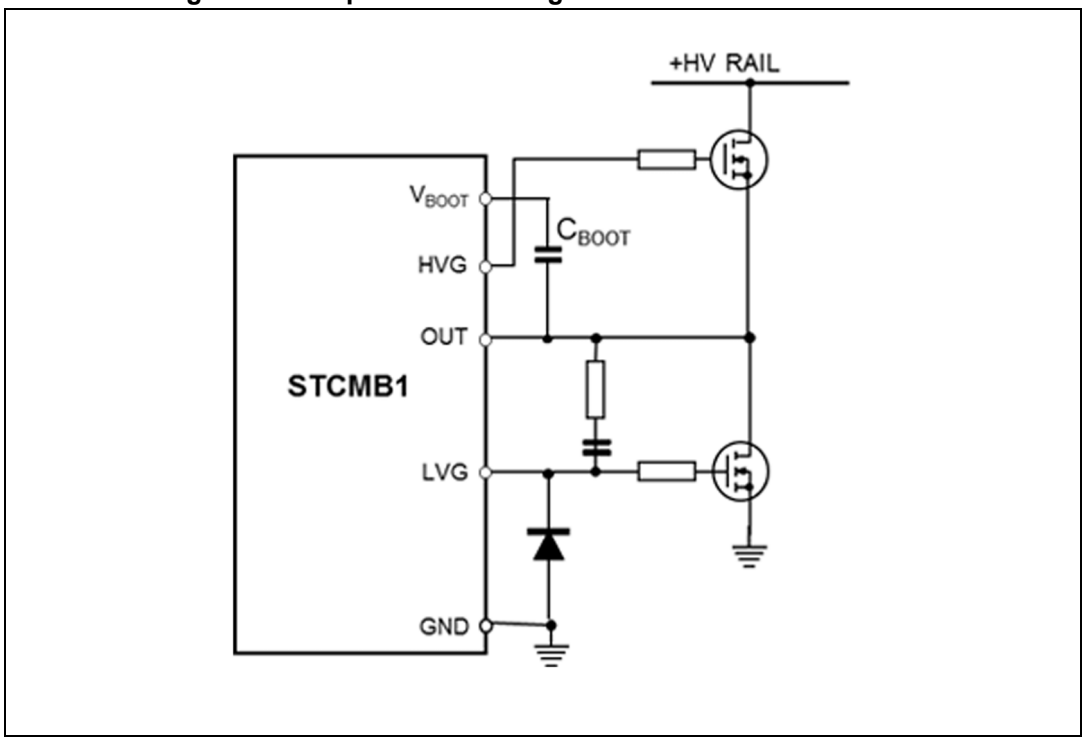
$$i_{source\,/\,simk} = i_{Cgd}\left(V_{HB}, I_{TANK}\right) = C_{gd}\left(V_{HB}\right) \frac{dV_{HB}}{dt}\left(I_{TANK}\right) \geq S_{diff}$$

The adaptive dead time generator gives a minimum dead time of 220 ns (max.) and a maximum dead time of 700 ns (min.), depending on the slope of the half bridge node. The actual minimum observable dead time is about 120 ns, defined and limited by the internal propagation delay. If, for some reason, the end of the half bridge transition were not detected, then the dead time would last indefinitely.

To avoid this stall condition, a timeout of about 1µs on the dead time is applied: unless the anti-capacitive protection mechanism is active (dead time made longer to let the current to take the right sign), the turn-on of the MOSFET is forced at about 1 µs from the turn-off of the other.

According to *Equation 26*, a MOSFET with the small Crss and small switched tank current could induce the unwanted generation of a minimum dead time to which a hard switch event could be associated (MOSFET turns on before the end of the half bridge transition, but no cross conduction). In these cases, a ceramic capacitor, up to 10 pF, between the drain of the low side MOSFET and the LVG pin can solve this adaptive dead time generation issue. A resistor, up to some kΩ, in series with the added capacitor and a Schottky diode, for instance the BAV21, between the LVG and GND, will made the solution more robust. The ceramic capacitor has to be high voltage rating. *Figure 22* shows the proposed solution.

Figure 22. Adaptive dead time generation made more robust



Details of the adaptive dead time generator and its operation are given in the following.

The actual dead time TD that can be observed during the operation does not depend only on the adjustment circuit of *Figure 20 on page 36*. This fact can be explained with the aid of the oscilloscope picture shown in *Figure 21 on page 38*.

It shows a detailed view of the low-to-high transition of the half-bridge midpoint (waveform labeled HB) along with the high-side gate drive (HVG) and the low-side gate drive (LVG). Clearly, the comments that follow apply to the high-to-low transition as well.

There are three contributors to T_D:

- The turn-off delay t_{OFF} of the power MOSFET, which depends on the input characteristics of the specific MOSFET and the speed its gate is driven
- The transition time T_T the half-bridge midpoint takes for a rail-to-rail swing
- The detection time t_{det} that elapses from the end of the half-bridge midpoint swing to the gate drive signal of the other MOSFET going high; this includes the detection time as well as the propagation delay along the downstream logic circuitry up to the driver output.

It is important to point out that the value of T_{D_MIN} specified in the electrical characteristics is essentially t_{det}: therefore the minimum observable T_D will always be longer. T_{D_MAX}, instead, is counted starting from the negative-going edge of the gate drive signal.

Figure 23. Adaptive deadtime: principle schematic (left) and relevant timing diagrams (right)

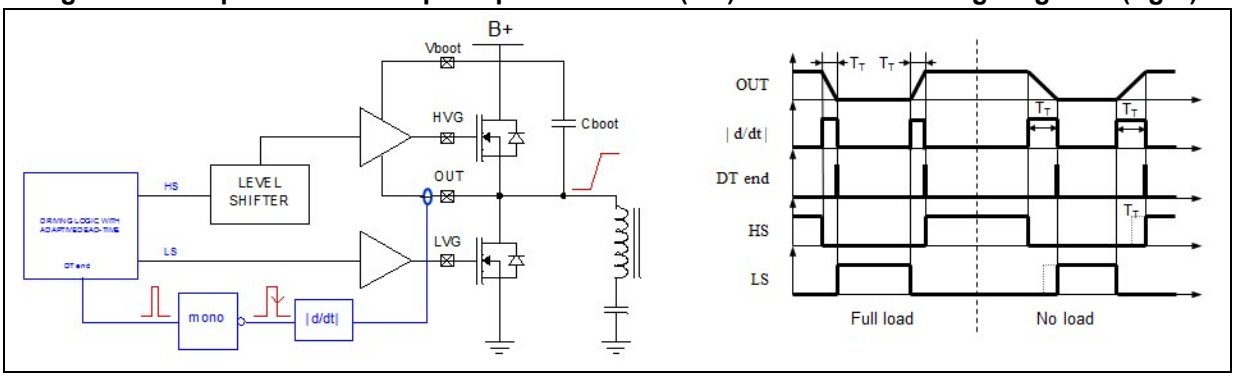
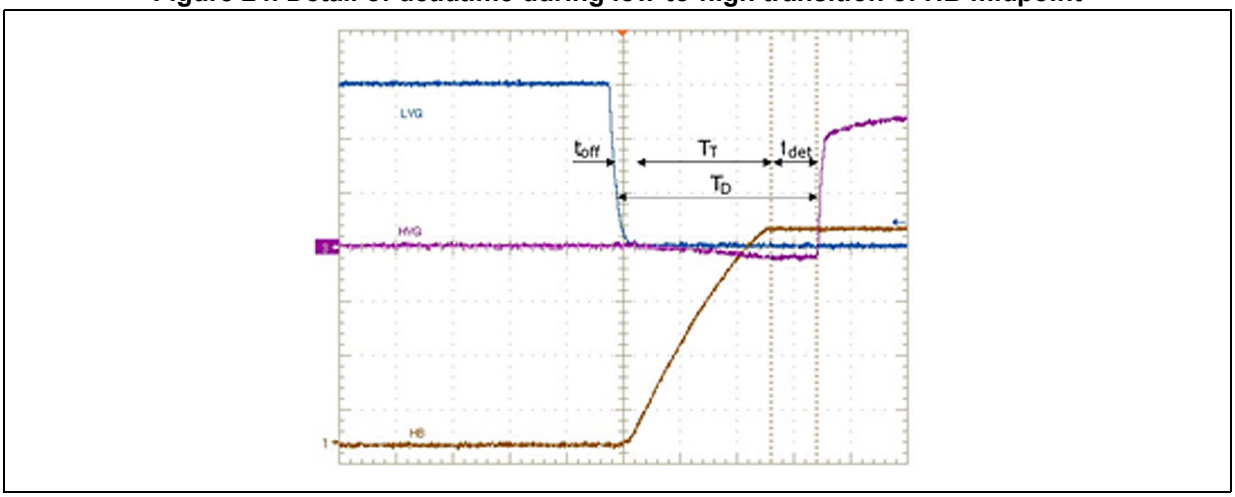


Figure 24. Detail of deadtime during low-to-high transition of HB midpoint



Finally, it is worth stating that the adaptive deadtime function does not significantly increase efficiency by itself. It is a degree of freedom that has to be exploited to this purpose when designing the resonant tank. Essentially, it allows the use of a higher magnetizing inductance in the transformer, which minimizes the magnetizing current and, then, the conduction losses associated to it. Additionally, this may reduce the switched current I_S to the minimum required to achieve soft-switching, thus reducing turn-off switching losses in MOSFETs. Efficiency at the medium and light-load will maximally benefit from this optimization.

7.22 HB: hard switching prevention (HSP) and anti-capacitive mode protection (ACP)

Resonant converters work in the capacitive mode when their switching frequency falls below a critical value that depends on the loading conditions and the input-to-output voltage ratio. They are especially prone to run into the capacitive mode when the input voltage is lower than the minimum specified and/or the output is overloaded or short-circuited. Designing a converter so that it never works in the capacitive mode, even under abnormal operating conditions, is definitely possible but this might pose unacceptable design constraints in some cases (e.g.: a transformer magnetizing current too big to comply with light-load efficiency targets).

The HSP and ACP functions in the STCMB1 help to prevent the severe drawbacks of the capacitive mode operation, while enabling a design that needs to ensure the inductive mode operation only in the specified operating range, neglecting abnormal operating conditions.

- If the phase shift of the tank current approaches zero, which is indicative of the impending capacitive mode operation, at some point the tank current will cross the zero current band within the deadtime. Therefore, the ACP circuit will find an anomalous condition and will extend the deadtime until the tank current changes the sign. Additionally, the soft-start capacitor is discharged, so that the resulting frequency rise pushes the operation away from that dangerous condition.
- If the phase relationship reverses abruptly (which may happen in case of dead short at the converter's output), the HSP will find it has the wrong sign and extend the duration of that conduction cycle until the tank current changes the sign.

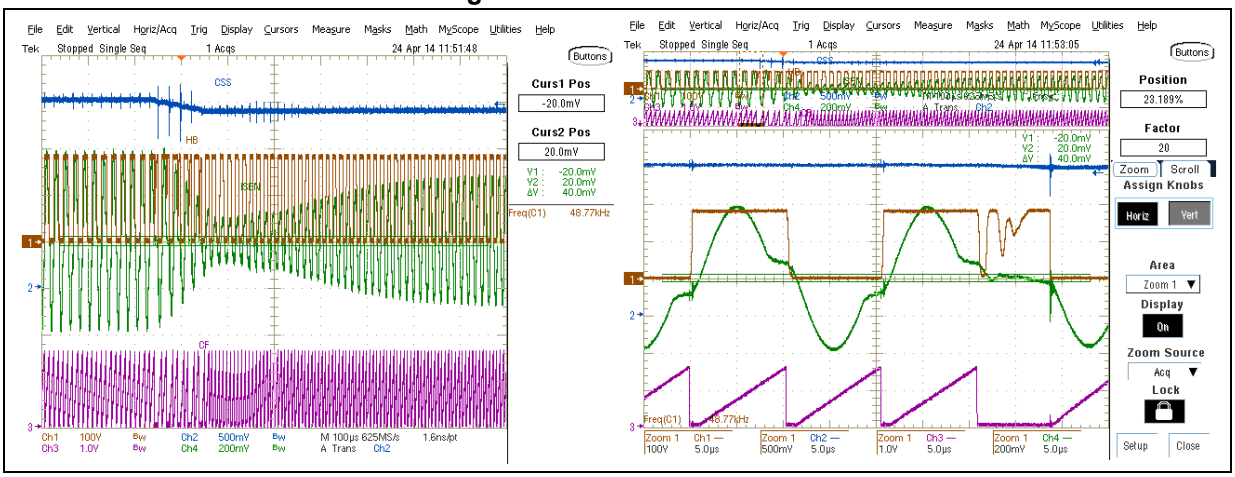
The HSP control method helps to avoid hard switching condition at MOSFET's turning-on, confirming the ISEN_HB sign is coherent with the driver is going to be turned-on. **It checks the sign of the ISEN_HB before the driver is turned-off.** When the ramp of the oscillator reaches the peak value VCFp, if the sign of the ISEN_HB signal is correct (positive with HS on and LS off, negative with LS on and HS off), the driver currently active is turned off and the deadtime starts. Otherwise, if the sign of the ISEN_HB is not correct the HSP acts resetting the oscillator and letting the driver currently active on until the ISEN_HB sign becomes correct.

The ACP (anti-capacitive mode protection) **works monitoring the sign of the ISEN_HB voltage signal at the end of the deadtime**. If the sign on the ISEN_HB pin has not correct polarity with respect to the driver is going to be turned-on (positive after LVG turn-off or negative after HVG turn-off), a capacitive mode (CM) condition is asserted. Hence the oscillator is reset and the drivers are kept off until the ISEN_HB sign returns to be consistent with the proper HB operation, preventing the hard switching condition. During CM condition the CSS capacitor is discharged, in this way increasing frequency as long as CM conditions end.

The half-bridge current sign definition is resulting from the use of two comparators monitoring the ISEN_HB signal. The sign of the current is considered positive when the voltage on that pin exceeds $-V_{ISEN\_Z}$, negative when it falls below V_{ISEN_Z} ($|V_{ISEN\_Z}|$ = 20 mV typ.)

During the start-up, the CSS discharge is disabled as long as the CSS pin voltage reaches 1.85 V to prevent deadlock conditions. For the same reason, the CSS discharge is disabled for about 50 µs after that the HB exits from the idle state of the burst mode operation.

Figure 25. ACP intervention



7.23 HB: Smooth start-up function

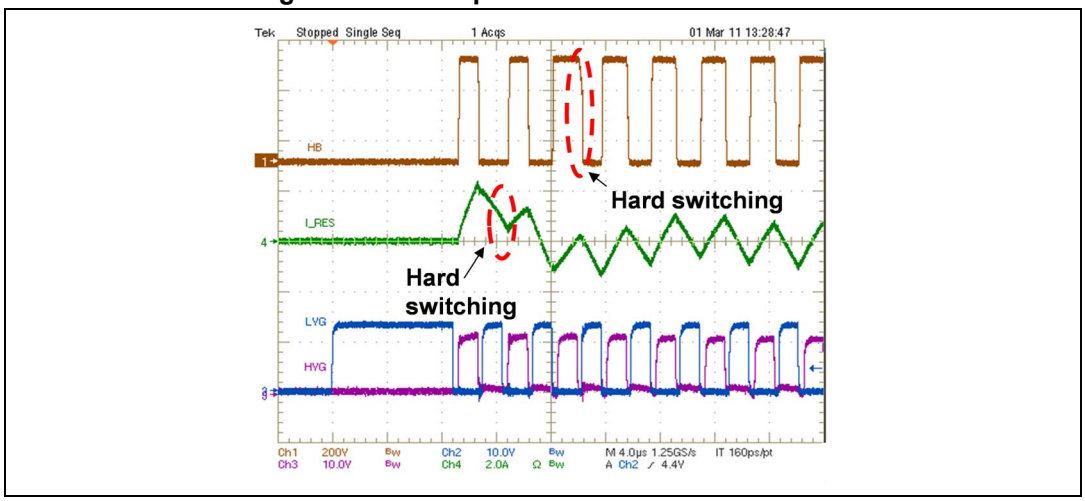
The timeshift control allows the prevention of any hard switching at the start-up: it's inherent in the control methodology to ensure that the half-bridge toggles when the tank current has the right sign in order for the MOSFETs to achieve soft-switching, which is not ensured by the usual soft-start procedure.

Sweeping the operating frequency from an initial high value down to the point where the control loop takes over, which is commonly referred to as soft-start, has a twofold benefit. On the one hand, since the deliverable power depends inversely on frequency, it progressively increases the converter's power capability, thus avoiding the excessive inrush current. On the other hand, it makes the converter to initially work at frequencies higher than the upper resonance frequency of the LLC tank circuit, which ensures the inductive mode operation (e.g.: with the tank current lagging the square wave voltage generated by the half-bridge) and, therefore, soft-switching.

However, the last statement is true under a quasi-static approximation, e.g.: when the operating point of the resonant tank is slowly varying around steady state condition. This approximation is not correct during the very first switching cycles of the half-bridge, where the initial conditions of the tank circuit can be away from those under steady state. Therefore, hard switching is possible during the transient period needed to reach the slowly varying steady state condition dictated by the soft-start action. A non-zero initial voltage on the resonant capacitor Cr and transformer flux imbalance during the previously mentioned transient period are the possible causes of hard switching in the initial cycles.

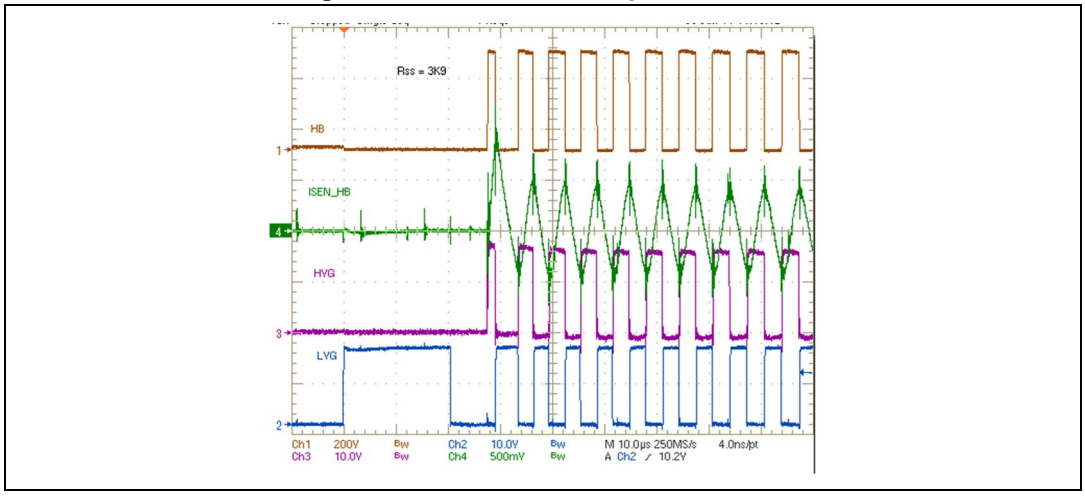
In high voltage half-bridge controllers it is customary to start switching activity by turning on the low-side MOSFET for a preset time to pre-charge the bootstrap capacitor and ensure proper driving of the high-side MOSFET since the first cycle. In traditional controllers, normal switching starts right at the end of the pre-charge time, as shown in *Figure 26*.

Figure 26. Start-up with traditional controllers



A non-zero initial voltage on the resonant capacitor may cause the very first turn-on of the high-side MOSFET to occur with non-zero drain-to-source voltage while the body diode of the low-side MOSFET is conducting, thus invoking its reverse recovery. More hard switching cycles may follow. These events are few but potentially hazardous: they could cause both MOSFETs destruction, should the resulting dV/dt across the low-side MOSFET exceed its maximum rating. To understand the origin of transformer flux imbalance it is worth reminding that normally the half-bridge is driven with the 50% duty cycle. This implies that, under steady state conditions, the voltage across the resonant capacitor Cr has a dc component equal to Vin/2.

Figure 27. STCMB1 start-up waveforms



Consequently, the transformer's primary winding is symmetrically driven by a ± Vin/2 square wave.

At the start-up, however, the voltage across the Cr is often quite different from Vin/2 and it takes some time for its dc component to reach this value. During this transient, the transformer is not driven symmetrically in voltage and, then, with the 50% duty cycle there is a significant V • s imbalance in two consecutive half-cycles. This causes a significant difference in the up and down slopes of the tank current and, being the duration of the two half-cycles the same, the current may not reverse in a switching half-cycle, as shown in the

left-hand picture in *Figure 12 on page 25*. Once again, one MOSFET can be turned on while the body diode of the other is conducting and this may happen for a few cycles.

This is automatically prevented with timeshift control. In fact, being the oscillator ramps synchronized to the zero crossings of the tank current, a ramp in a half-cycle starts only after the tank current has reversed in that half-cycle. As a result, the duty cycle of the initial cycles is less than 50% until the dc voltage across the Cr reaches Vin/2, which eliminates the initial V • s imbalance and ensures soft-switching. The picture of *Figure 27* shows the start-up waveforms of a resonant converter driven by the STCMB1.

7.24 HB: OCP management with internal digital delay and restart

In the STCMB1 the current sense input ISEN_HB pin senses the current flowing in the resonant tank to perform two tasks:

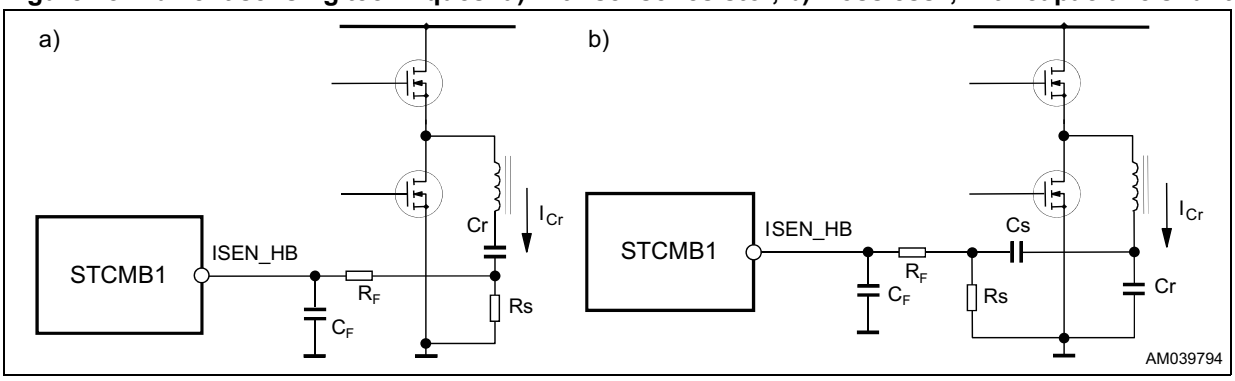
1. Primary overcurrent protection (OCP function)
2. Hard switching cycle prevention

In this section the discussion is focused on the OCP function.

Unlike PWM controlled converters, where the energy flow is controlled by the duty cycle of the primary switch (or switches), in a resonant HB the duty cycle is fixed and the energy flow is controlled by its switching frequency. Thus, in resonant HB converters the most efficient way to reduce an excessive current level is the increasing of the switching frequency.

In *Figure 28* a couple of current sensing methods are illustrated that will be described here following.

Figure 28. Current sensing techniques: a) with sense resistor, b) "lossless", with capacitive shunt



In the circuit shown in *Figure 28*a, Rs is placed directly in series to the resonant tank. Its value can be determined using *Equation 27*.

Equation 27

$$R_S = \frac{0.76V}{I_{RES \cdot pk}}$$

where $I_{RES.pk}$ is the maximum expected peak current flowing through the resonant capacitor and the primary winding of the transformer, with the maximum load and the minimum input voltage. The power dissipation in Rs can be approximately found with:

Equation 28

$$P_D = 0.4 I_{RES \cdot pk}$$

Differently, the proposed circuit shown in *Figure 28*b operates as a capacitive current divider; Cs will be typically selected equal to Cr/100 or less and will be a low-loss type, and the sense resistor Rs will be selected as:

Equation 29

$$R_S = \frac{0.76V}{I_{RES \cdot pk}} \cdot \left(1 + \frac{Cr}{Cs}\right)$$

With this solution the associated power dissipation will be reduced by a factor (1 + Cr / Cs). This circuit is then recommended when the efficiency target is very high.

For proper operation of the LLC, the STCMB1 must sense the instantaneous tank current for the proper operation of the hard switching prevention function. As shown in *Figure 25*, an RC filter close to the ISEN_HB pin is recommended to reduce the noise level on the pin, but the delay it introduces has to be negligible with respect to the operating frequency of the LLC. As a rule of the thumb, the following can be considered: time constant R • C should be no more than few hundred ns (400 ns) when the LLC frequency is about 100 kHz.

Because the RC filter on the pin introduces a phase delay of the signal on the ISEN_HB pin with respect to the current flowing in the resonant tank, it might happen that the anti-capacitive mode protection do not reveal the incorrect situation because the protection does not see the real phase among the voltage and current in the resonant tank. Therefore, with longer time constants it is recommended that the converter operation close to the capacitive mode boundary and during the short-circuit should be checked for possible hard switching cycles.

The ISEN_HB pin, which is able to withstand also negative voltages, is internally connected to the input of a first comparator, referenced to the V_{ISENx} (first level protection threshold for frequency-shift, set at 0.8 V typ.), and to that of a second comparator referenced to the $V_{ISENdis}$ (second level protection threshold for immediate stop, set to 1.5 V typ.).

7.24.1 First OCP protection

If the voltage at the ISEN_HB pin exceeds the $V_{ISEN\_HB\_x}$ (frequency shift threshold) referenced at 0.8 V (typ.), a comparator is tripped causing the activation of the C_{SS} discharging the internal switch for 5 µs (OCP1 event). The discharge of the soft-start capacitor quickly increases the oscillator frequency, limiting the energy transfer to the output and reducing the peak resonant current. After the discharge time (5 µs), if the overload is still there, the switching frequency will decrease again and the resonant current will increase. If the ISEN_HB pin voltage reaches the $V_{ISEN\_HB\_x}$ again the operation described above will be repeated. Under the overload condition, this operation results in a peak primary current that periodically oscillates around the maximum value allowed by the sense resistor on the ISEN_HB pin, the R_S, above calculated in *Equation 29*.

This overcurrent protection is effective in limiting the primary-to-secondary energy flow in case of overload. In spite of this, the output current through the secondary winding and rectifiers under these conditions might be high enough to jeopardize converter's safety if continuously flowing.

In order to prevent the converter damaging, the operation during the overload described above will have limited duration; afterward the converter will have to be forced to work intermittently, which brings the average output current to values such that the thermal stress of the transformer and the rectifier is within safe limits.

The operation of the converter in the overload is limited in time by a mechanism based on a pair of internal counters: one is a modulo 128 cyclical counter, clocked by the switching frequency of the LLC, and the other is a modulo 20 K counter, clocked by the internal reference at about 1 MHz. The first OCP1 event (first time Visen_hb ≥ 800 mV, typ.) turns on the two counters.

If a second OCP1 event occurs within 128 cycles of the LLC from the first OCP1 event, then the cyclical counter is reset and restarted, while the modulo 20 K is left free running on its clock.

If no OCP1 event occurs within 128 cycles of the LLC from the last OCP1 events, that is the cyclical, the counter reaches its EoC, then the value of the modulo 20 K counter is decreased of 32 and frozen.

The value of the modulo 20 K counter is decreased of 32 and frozen, each time the modulo 128 cyclical counter reaches its EoC (no OCP1 event within 128 cycles of the LLC from the last EoC). When the value of the modulo 20 K counter reaches 0 (because of consecutive decrements), the modulo 128 cyclical counter is reset and stopped.

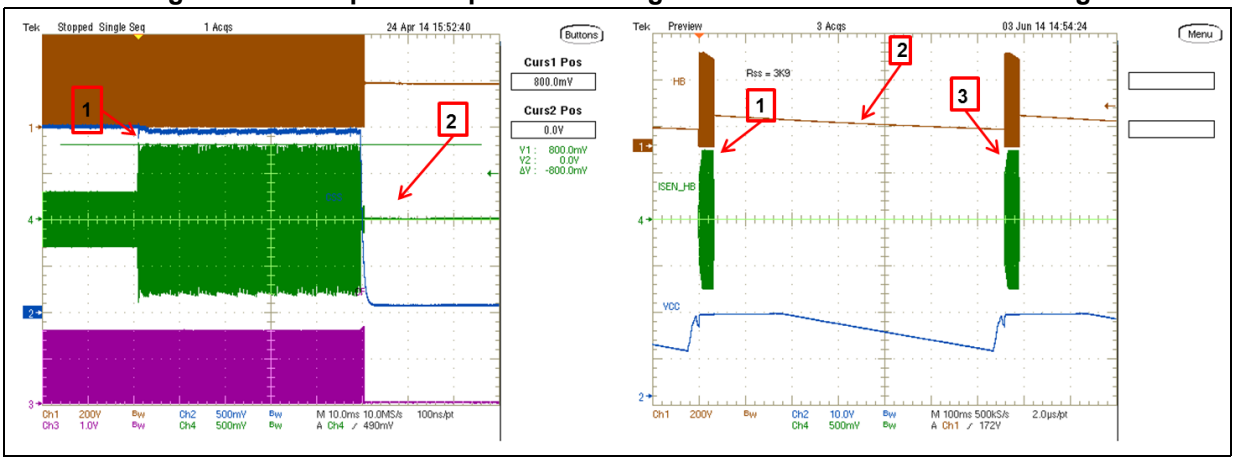
Conversely, when an OCP1 event occurs while the modulo 20 K counter is frozen (OCP1 event occurring within 128 cycles of the LLC from the last EoC), its counting is restarted and the modulo 128 cyclical counter is reset. When the modulo 20 K counter reaches its EoC, a soft-stop procedure is activated (and the counters are reset and stopped).

The soft-stop procedure consists of a controlled turn-off of the LLC stage in 128 cycles: the soft-start capacitor is completely discharged to increase the switching frequency so that the energy in the resonant tank is minimized. After the shutdown, the adapter will be driven by the natural discharge and recharge by the HVSU of the VCC pin. If the overload condition is permanent, then the adapter will operate in the hiccup mode.

In practice, the modulo 20 K counter will reach its EoC in 20 ms (18 ms min.) in case of the output short-circuit, if the latter does not trigger the OCP2, or when the overload is above a certain current level and/or time length.

Waveforms of the converter operation at the first shutdown by the soft-stop procedure and during the hiccup mode are given in *Figure 29*. Detailed operation is described below *Figure 29*.

Figure 29. Hiccup mode operation during OVL and detail of current limiting



1. As the overload is applied (1, in the left picture), the OCP1 is triggered: the output power is limited by the periodic discharge of the soft-start capacitor and the internal counting system starts.
2. In about 50 ms, the modulo 20 K counter reaches its EoC, triggering the soft-start procedure (2, in the left picture): the CSS is completely discharged and the LLC stopped after 128 cycles and VCC is naturally discharged.
3. The STCMB1 remains in the OFF state until VCC drops to VCCoff: here, the HV start-up generator is activated and charges VCC. As VCCon is reached, the STCMB1 will restart operations via a soft-start procedure (CSS has been previously discharged).
4. Because of the permanent overload, the OCP1 is triggered again and the above sequence will be repeated: the soft-stop in about 50 ms (1, in the right picture), VCC discharges (2, in the right picture), VCC recharges and the converter restarts (3, in the right picture).
5. The hiccup operation will last for the time the overload condition is kept. As it is removed, the converter will restart the normal operation at the first VCC recharge after the removal of the overload condition.

7.24.2 Second level OCP protection

In case of particularly severe dead shorts the current in the resonant tank can rise very quickly to very high levels. In such cases it would be dangerous for the converters to wait the timing set up by the procedure described above, so the STCMB1 is equipped with an additional comparator referenced at 1.5 V (typ. level, V_{ISEN_HB}). In case of dead shorts if the signal on the ISEN_HB pin reaches the V_{ISEN_HB} the converter is stopped immediately after terminating the current cycle and the internal C_{SS} discharging switch is forced continuously on.

The resonant HB will restart the operation after the V_{CC} has dropped below the V_{VCCOff}, and then risen to the V_{VCCON} by the activation of the HV start-up as during normal power-on. The converter operation will result in a continuous intermittent operation (hiccup mode) until the fault is removed.

In order to prevent the intervention of this protection at the start-up due to any initial transient or spike, this second level OCP protection is inhibited until the voltage on Css is higher than 0.3 V.

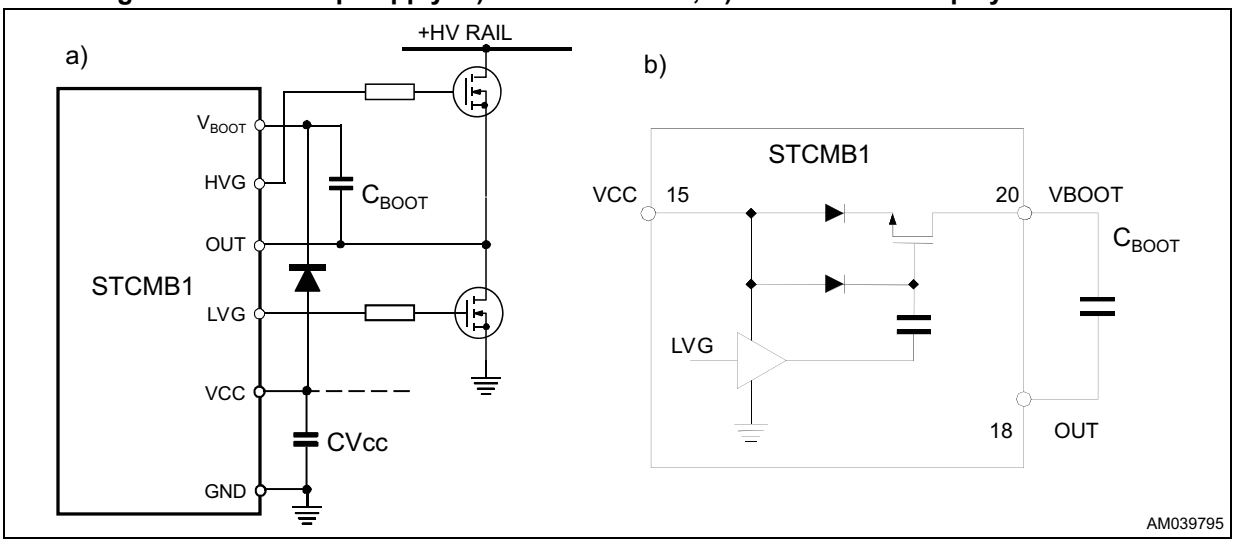
7.25 HB: high voltage bootstrap section and HB gate drivers (HVG and LVG)

The supply of the floating high-side section is obtained by means of bootstrap circuitry. This solution normally requires a high voltage fast recovery diode to charge the bootstrap capacitor C_{BOOT}, as shown in *Figure 30*a. In the STCMB1 a patented integrated structure replaces this external diode. It is realized by means of a high voltage DMOS, working in the third quadrant and driven synchronously with the low-side driver (LVG), with a diode in series to the source, as shown in *Figure 30*b.

The diode prevents any current can flow from the VBOOT pin back to V_{CC} in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged. To drive the synchronous DMOS it is necessary a voltage higher than the supply voltage V_{CC}. This voltage is obtained by means of an internal charge pump.

The bootstrap structure introduces a voltage drop while recharging CBOOT (e.g.: when the low-side driver is on), which increases with the operating frequency and with the size of the external power MOS. It is the sum of the drop across the $R_{(DS)ON}$ and the forward drop across the series diode. At low frequency this drop is very small and can be neglected but, as the operating frequency increases, it must be taken into account. In fact, the drop reduces the amplitude of the driving signal and can significantly increase the $R_{(DS)ON}$ of the external high-side MOSFET and then its conductive loss.

Figure 30. Bootstrap supply: a) standard circuit; b) internal bootstrap synchronous



This concern applies to converters designed with a high resonance frequency (indicatively, > 150 kHz), so that they run at high frequency also at the full load. Otherwise, the converter will run at high frequency at the light-load, where the current flowing in the MOSFETs of the half-bridge leg is low, so that, generally, a slight $R_{(DS)ON}$ rise is not an issue. However, it is wise to check this point anyway and *Equation 30* is useful to estimate the drop on the bootstrap driver.

Equation 30

$$V_{Drop} = I_{charge} R_{(DS)\,on} + V_F = \frac{Q_g}{T_{charge}} R_{(DS)\,on} + V_F$$

where *Qg* is the gate charge of the external power MOSFET, $R_{(DS)on}$ is the on-resistance of the bootstrap DMOS (230 Ω, typ.) and T_{charge} is the on-time of the bootstrap driver, which equals about a half switching period minus the deadtime T_D. For example, using a MOSFET with a total gate charge of 30 nC, the drop on the bootstrap driver is about 3 V at a switching frequency of 200 kHz:

Equation 31

$$V_{Drop} = \frac{30\ \ 10^{9}}{2.5\ \ 10^{6}\ \ \ 0.3\ \ 10^{6}} 230 + 0.6 = 3.7\ V$$

A typical range of the bootstrap capacitor (Cboot) is from 100 to 470 nF.

If a significant drop on the bootstrap driver is an issue, an external ultrafast diode can be used, thus saving the drop on the $R_{(DS)ON}$ of the internal DMOS. In this case it is also recommended to add a small resistor (in the ten Ω) in series to the diode to prevent the

bootstrap capacitor from being charged to a voltage exceeding the absolute maximum rating (21 V), in case of significant negative spikes on the half-bridge midpoint when the high-side MOSFET turns off.

Both high-side and low gate drivers have a DMOS structure driving the MOSFET gates. The current capability is 0.3 A at the MOSFET turn-on and 0.6 A at turn off, giving typical rise and fall times of 60 ns and 30 ns respectively.

Both drivers have pull-down circuitry active before the start-up to keep the MOSFETs safely off against an unwanted turn-on due to the environment noise: the HVG has an internal pull-down resistor (27 kΩ typ.) connected among the HVG and OUT pin, while the LVG driver has active pull-down circuitry. Both them allow removing the typical gate-source resistance or using a higher value.

It has to be noted that the drivers have no any voltage clamping of the gate voltage. Therefore the MOSFETs will be driven with a driving voltage at the V_{CC} level. For this reason the V_{CC} will have to be limited in all operating or fault condition to a safe level, to avoid any premature aging or damaging of the MOSFETs gate oxide.

8 Debug modes

For debugging purposes the STCMB1 has the possibility to disable one stage a time.

At power-on, when the V_{CC} voltage reaches the turn-on threshold, the internal logic checks the level of some signals at the pin, and can disable the PFC or the HB stage as detailed here following:

- If the device is turned on with the voltage on the pin **ZCD > 2.4 V, the PFC section is disable**d so that the HB resonant stage can work standalone.
  In this debug mode the STCMB1 must be supplied by a dc voltage connected to the PFC bulk cap and by an external VCC > V_{VCCOn}, because the HV start-up is disabled. After the start-up, if the self-supply circuitry is working properly, the resonant stage can work self-supplied and the external V_{CC} can be removed.
  The dc brown-out function is disabled; therefore the resonant stage can work also with an input voltage much lower than the nominal PFC output. In this case any of the HB stage protections could work because of the abnormal condition.
- If the device is turned on with the voltage on the pin **HISEN_HB > 2.4 V, the HB resonant section is disabled** so that the PFC resonant stage can work standalone. The HV start-up in this case can work charging the V_{CC} capacitor but an external V_{CC} voltage from a dc supply is necessary for powering the STCMB1 after the start-up phase. All other protections like the brown-in, brown-out, OCP, Dynamic OVP, FFP are enabled.

9 STCMB1 layout hints

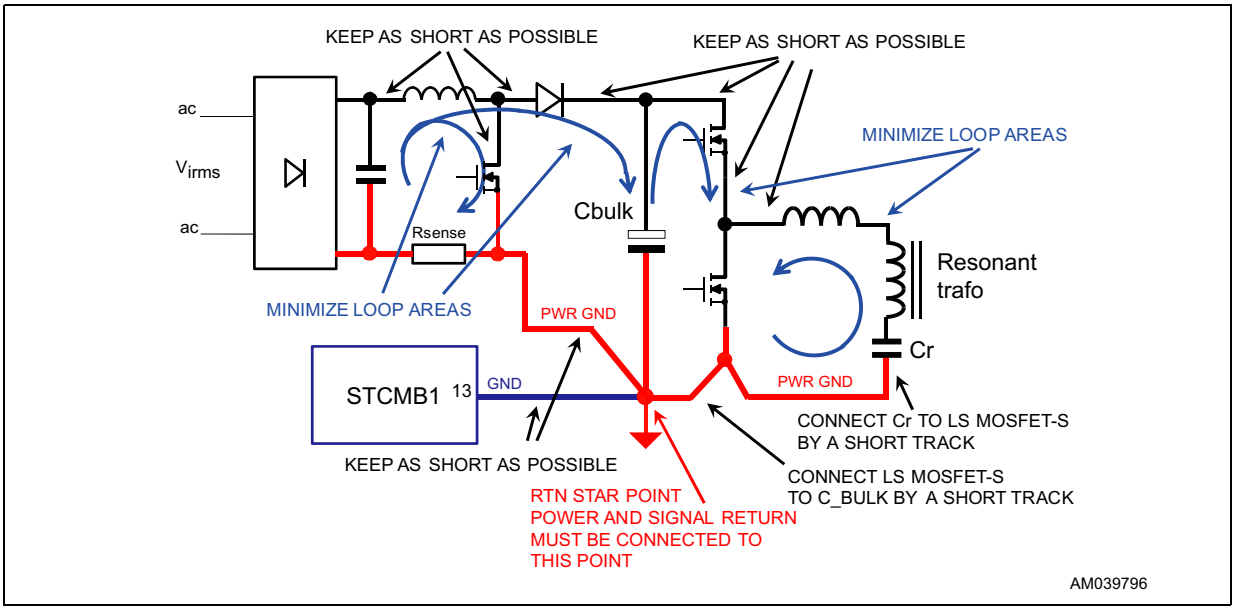
The layout of any converter is a very important phase in the design process needing the required attention by the engineers. **Even if it the layout phase looks sometimes time consuming, a good layout surely saves time during the functional debugging and the qualification phases and increases the robustness against the susceptibility tests. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages, so it will allow a consistent saving of the BOM cost.**

The STCMB1 does not need to follow any special layout instruction, just following the general layout rules for any power converter have to be applied wisely, especially for the ground connections. The main, basic hints are indicated here following; they can be implemented even if a single side PCB is used.

1. **Keep power RTN separated by the signal RTN.** Connect the return pins of the component carrying the high current switched at high frequency such as the PFC sense resistor, PFC MOSFET source, resonant capacitor, LLC low-side MOSFET source as close as possible and converging on the latter. This point will be the RTN star point. In case the half-bridge is far away from the PFC output bulk capacitor, this last can be split in two capacitors located near the two stages, one capacitor close to the PFC power section, the second one should be positioned close to the half-bridge MOSFETs. This placement minimizes the differential mode noise produced by both sections.

2. **Connect the pin #13 (GND) to the RTN star point making the connections as short as possible and using a track width suitable to minimize its impedance (larger than 1 mm).** Keep this connection separated from any other GND connection, especially if carrying high currents.
3. **PCB tracks carrying high dV/dt signals have to be as short as possible.** This minimizes the noise radiation that might affect high impedance points working with low level signals. Therefore, the PCB tracks connected to the boost inductor, PFC MOSFET drain, PFC rectifier and LLC resonant tank MOSFETs and transformer have to be routed as short as possible and their width has to be at least 1.5 mm, in order to minimize their parasitic inductance. Pay attention also to the insulation creepage distance.

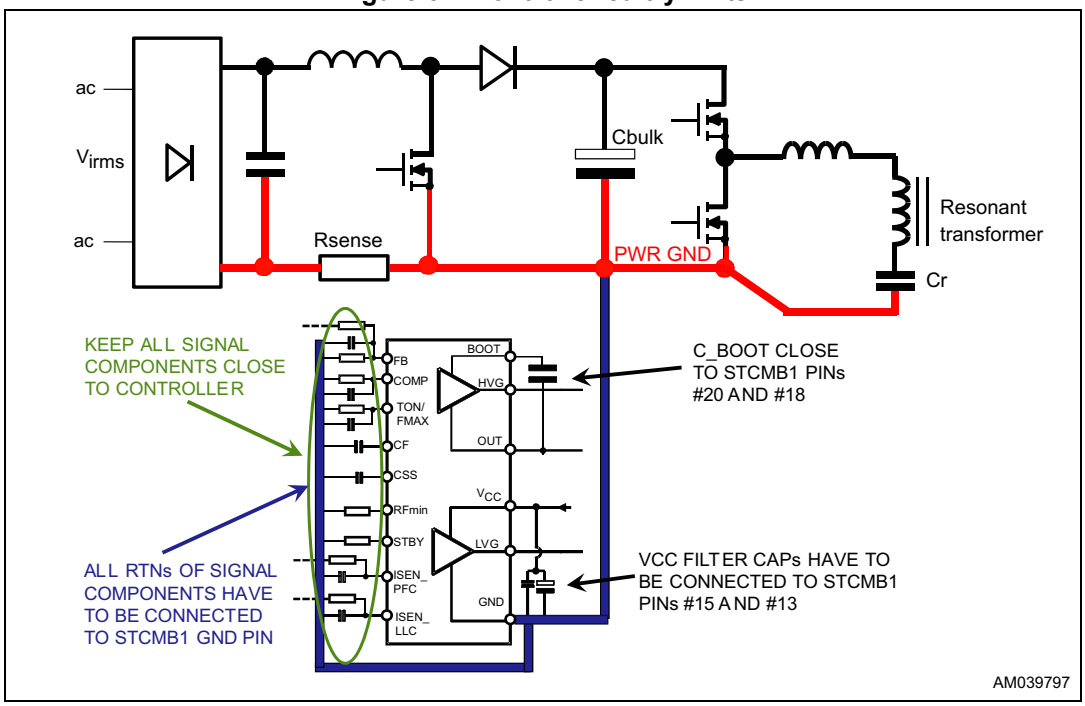
Figure 31. STCMB1 power section and RTN connections



4. **Place the VCC filter capacitor (ceramic, 470 nF ÷ 1 µF) close to the STCMB1** connecting it to the VCC pin (pin #15) and to the GND (pin #13).
5. **Keep signal components as close as possible to the relevant pins.** Connect the components relevant to the FB (pin #3), COMP (pin #4), TON (pin #5) CF (pin #7), CSS (pin #8) RFMIN (pin #9), STBY (pin #10) close to the GND pin of the STCMB1 (pin #13). All components and traces connected to the mentioned pins have to be placed far from traces and connections carrying signals with high dV/dt.
6. **The tracks relevant to the whole net of the pin #3 (FB) have to be as short as possible and far from high dV/dt signal tracks**. Because of its high impedance, the pin could pick up noise affecting the PFC operation. If an additional circuit is needed to pull-down the pin to latch the STCMB1 in case of OTP or the open loop, it has to be placed close to the pin itself.
7. **Place the RC filtering components of the PFC and LLC current sensing as close as possible to the relevant pins, ISEN_PFC and ISEN_HB.** Filtering resistors in series have to be placed nearby the pins as well. The filtering capacitors ground connection have to be near to the pin #13 (GND), on the signal ground connection. Components and traces connected to the mentioned pins have to be placed far from traces and connections carrying signals with high dV/dt.

8. **Connect the RTN of signal components directly to the STCMB1 GND pin (pin #13).** RTN of signal components relevant to the pins FB (pin #3), COMP (pin #4), TON (pin #5) CF (pin #7), CSS (pin #8) RFMIN (pin #9), STBY (pin #10) must not be involved in any different return path, it must be kept separated. Use ground tracks width more than 1 mm.

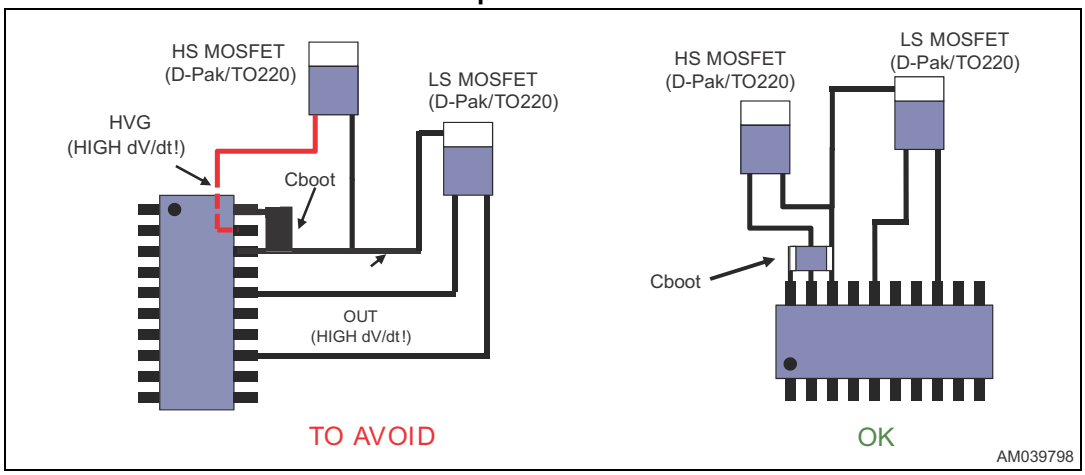
Figure 32. Control circuitry hints



9. **Connect the feedback optocoupler emitter to the signal RTN, close to the GND connection of oscillator components.** Both optocoupler tracks have to be placed far from traces and pins operating with high voltage and high dV/dt.
10. **Connect heatsinks to Power GND close to each relevant MOSFET source.** Connect the PFC MOSFET heatsink to primary GND, close to the PFC MOSFET source. Connect the half-bridge MOSFETs heatsink, if present, to primary GND too and close to the LLC low-side MOSFET source. Never leave heatsinks floating.
11. **Place an external copper band contacting the ferrite core of the boost inductor and connect it to GND.** Grounding the core of the PFC inductor decreases the EMI (radiated noise) from the PFC inductor caused by the dV/dt; it improves the EMC performance of the SMPS.
12. **Place the bootstrap capacitor close to the pins #20 and #18 of STCMB1.** Do not place tracks relevant to the pins VBOOT, HVG an OUT close to signal pins or tracks, especially CF and other oscillator pins may be affected by disturbances because such pins operates with high voltage and high dV/dt. Furthermore,
    a) Minimum insulation distances of these tracks and relevant components, with respect to other low voltage parts, have be checked too.
    b) If an external bootstrap diode is needed, please locate it close to the STCMB1 pins minimizing the length of the tracks.

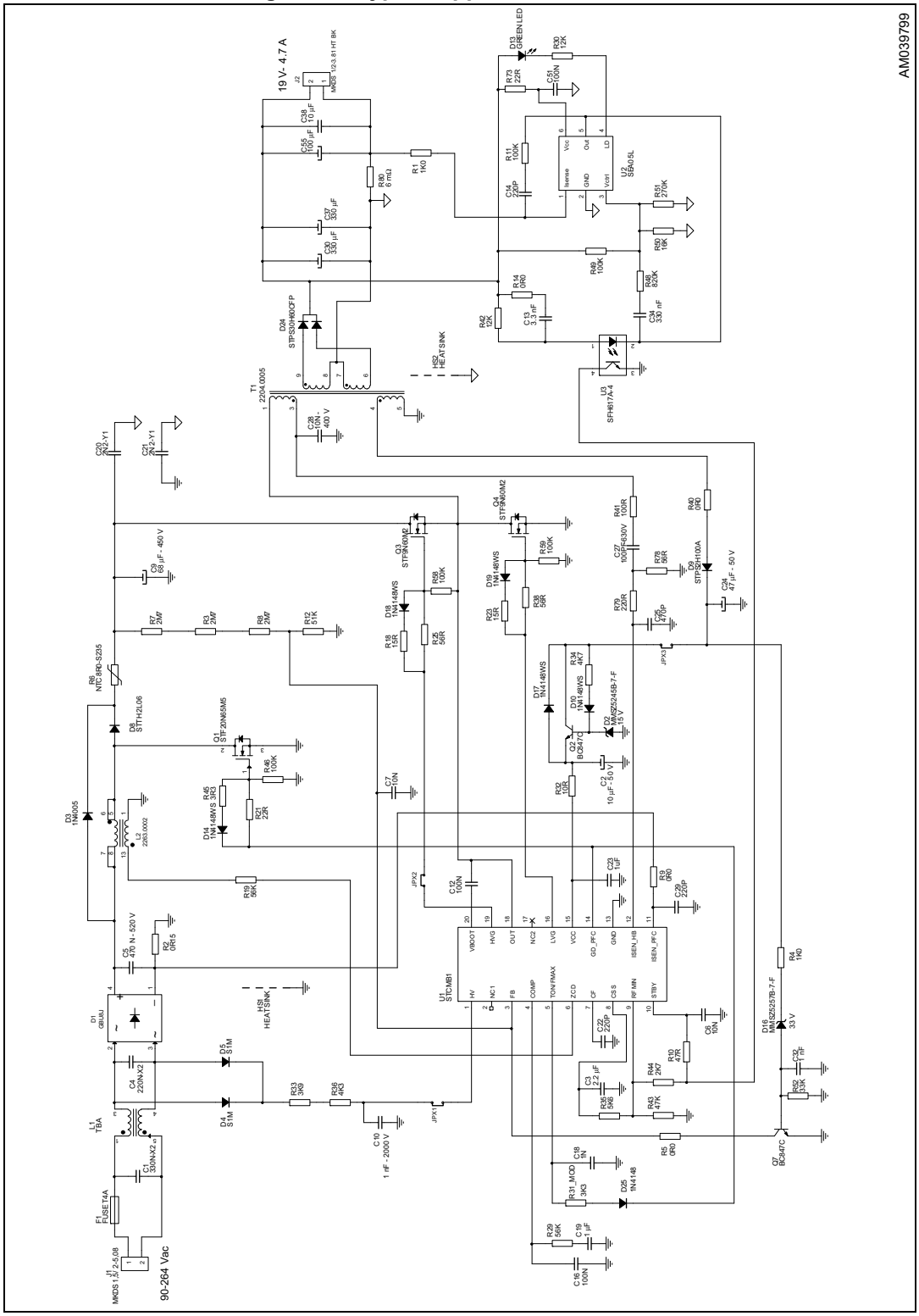
13. **It is better do avoid the HVG trace under the IC, between pin rows** (see *Figure 33*). This layout solution should be avoided because the high dV/dt of the HV traces might affect the low signal pins. It is a better practice using a suitable SMT package for the bootstrap capacitor and route the HVG track below, as on the right side. The IC and MOSFETs positioning like in the sketch here below on the left should be avoided because the trace length cannot be minimized.

Figure 33. Critical (left) and preferred (right) MOSFETs and Cboot routing and placement



10 Typical application schematic

Figure 34. Typical application schematic



11 Reference

C. Adragna, “Time-shift control of LLC resonant converters”, Proc. of 29th PCIM Europe International Exhibition and Conference, 2010, paper # 113, pp. 661 - 666, Nuremberg, Germany.

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

This package has a lead-free second level interconnect. The category of the second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

12.1 SO20W package information

Figure 35. SO20W package outline

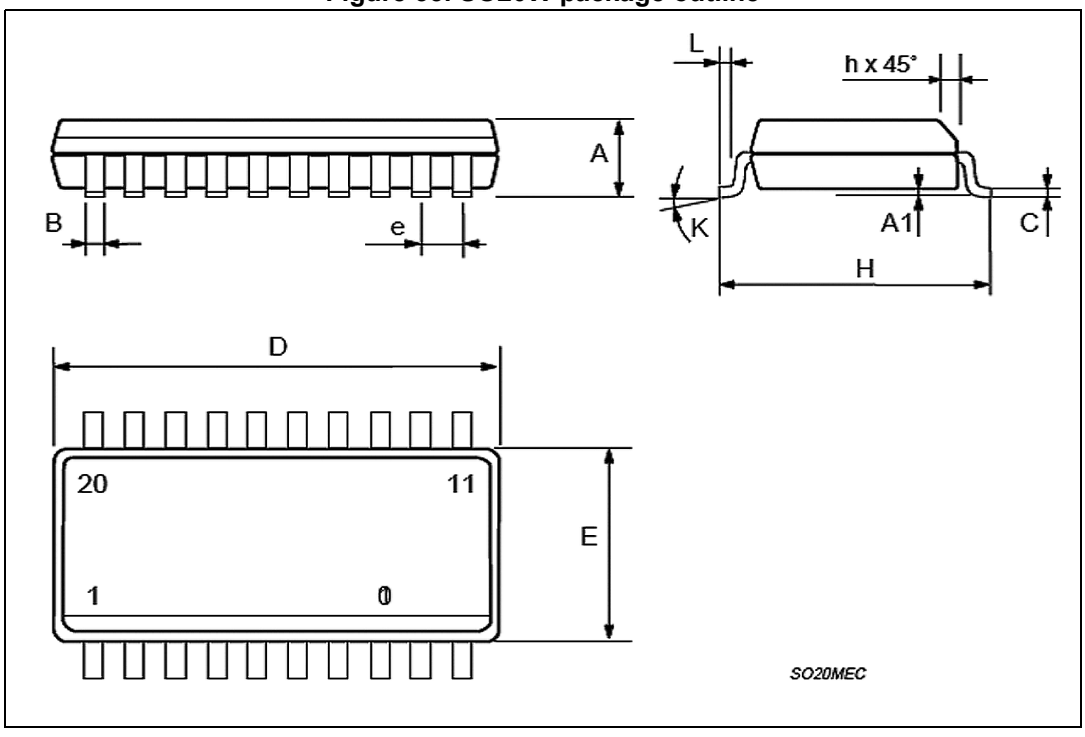


Table 5. SO20W package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	-	0.51	0.013	-	0.200
C	0.23	-	0.32	0.009	-	0.013
D	12.60	-	13.00	0.496	-	0.512
E	7.40	-	7.60	0.291	-	0.299
e	-	1.27	-	-	0.050	-
H	10.00	-	10.65	0.394	-	0.419
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
k	0° (min.), 8° (max.)					

13 Revision history

Table 6. Document revision history

Date	Revision	Changes
03-Feb-2016	1	Initial release.
15-Feb-2016	2	Updated document status to *Datasheet - production data on page 1*.
20-Jun-2017	3	Updated *Section : Features on page 1* (added “and UL Demko certified”). Updated *Table 1 on page 6* (updated HV, TON, STBY, ISEN_PFC, and ISEN_HB pins). Updated *Table 2 on page 10* (updated V_{OUT} pin, added ESD and ESD HBM rows). Updated *Table 4 on page 11* (updated I_q, V_{HVPK_BO}, V_{HVPK_BI}, I_{TON}, T_{D_MIN}, $V_{COMPSAT}$, HVG-OUT pull-down, removed T_{OVL}). Updated *Section 7 on page 15* (updated text, replaced by new figures from *Figure 7 on page 19* to *Figure 11 on page 24*, *Figure 19 on page 34*, and *Figure 20 on page 36*), added *Section 7.19 on page 35*. Updated *Section 9 on page 51* (updated text). Minor modifications throughout document.
15-Jan-2018	4	Updated *Table 4 on page 11* (updated max. limit of the parameter I_{ISEN_PFC}). Minor modifications throughout document.

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