

FEATURES

- Overvoltage protection up to -55 V and $+55 \text{ V}$
- Power-off protection up to -55 V and $+55 \text{ V}$
- Overvoltage detection on source pins
- Low charge injection (Q_{INJ}): -0.4 pC
- Low on capacitance
 - ADG5208F:** 20 pF
 - ADG5209F:** 14 pF
- Latch-up immune under any circumstance
- Known state without digital inputs present
- V_{SS} to V_{DD} analog signal range
 - $\pm 5 \text{ V}$ to $\pm 22 \text{ V}$ dual-supply operation
 - 8 V to 44 V single-supply operation
- Fully specified at $\pm 15 \text{ V}$, $\pm 20 \text{ V}$, $+12 \text{ V}$, and $+36 \text{ V}$

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The **ADG5208F** and **ADG5209F** are 8:1 and dual 4:1 analog multiplexers. The **ADG5208F** switches one of eight inputs to a common output, and the **ADG5209F** switches one of four differential inputs to a common differential output. An EN input on both devices enables or disables the device. Each channel conducts equally well in both directions when on, and each channel has an input signal range that extends to the supplies. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

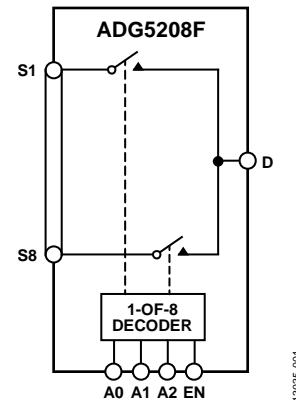
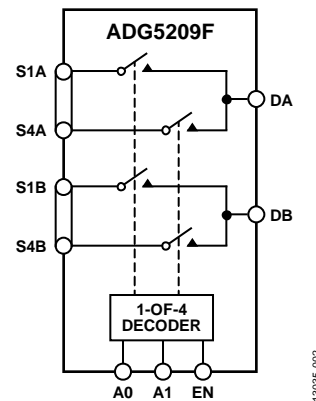
When no power supplies are present, the channel remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any S_x pin exceed positive fault voltage (V_{DD}) or negative fault voltage (V_{SS}) by a threshold voltage (V_T), the channel turns off and that S_x pin becomes high impedance. If the fault channel is selected, the drain pin is pulled to the secondary supply voltage that was exceeded.

Rev. A

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FUNCTIONAL BLOCK DIAGRAMS


 Figure 1. **ADG5208F** Functional Block Diagram

 Figure 2. **ADG5209F** Functional Block Diagram

Input signal levels of up to -55 V or $+55 \text{ V}$ relative to ground are blocked, in both the powered and unpowered conditions.

The low capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch switching and fast settling times are required.

PRODUCT HIGHLIGHTS

1. The source pins are protected against voltages greater than the supply rails, up to -55 V and $+55 \text{ V}$.
2. The source pins are protected against voltages between -55 V and $+55 \text{ V}$ in an unpowered state.
3. Trench isolation guards against latch-up.
4. Optimized for low charge injection and on capacitance.
5. The **ADG5208F/ADG5209F** can be operated from a dual supply of $\pm 5 \text{ V}$ up to $\pm 22 \text{ V}$ or a single power supply of 8 V up to 44 V .

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REVISION HISTORY

3/16—Rev. 0 to Rev. A

| | |
|---|-----------|
| Added 16-Lead LFCSP..... | Universal |
| Changes to General Description Section | 1 |
| Changes to Table 5..... | 11 |
| Changes to Table 6..... | 12 |
| Added Figure 4; Renumbered Sequentially | 13 |
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| Changes to Ordering Guide | 27 |

4/15—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, see Figure 38 |
| On Resistance, R_{ON} | 250 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| | 250 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 2.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| | 2.5 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 6.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 8 | 9 | 9 | Ω max | |
| | 1.5 | | | Ω typ | $V_S = \pm 9\text{ V}$, $I_S = -1\text{ mA}$ |
| | 3.5 | 4 | 4 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 1 | ± 2 | ± 5 | nA max | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 36 |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 66 | | ± 78 | μA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | ± 40 | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| | ± 50 | ± 70 | ± 90 | nA max | |
| Power Supplies Grounded | ± 500 | | | nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| | ± 700 | ± 700 | ± 700 | nA max | |
| Power Supplies Floating | ± 50 | ± 50 | ± 50 | μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} | | | 2.0 | V min | |
| Input Voltage Low, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | ± 1.1 | | ± 1.2 | μA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------|----------------|-----------------|---------|--|
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{\text{TRANSITION}}$ | 180 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 230 | 245 | 260 | ns max | $V_S = 8\text{ V}$, see Figure 47 |
| t_{ON} (EN) | 180 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 235 | 250 | 260 | ns max | $V_S = 10\text{ V}$, see Figure 46 |
| t_{OFF} (EN) | 95 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 125 | 145 | 145 | ns max | $V_S = 10\text{ V}$, see Figure 46 |
| Break-Before-Make Time Delay, t_D | 130 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | | | 90 | ns min | $V_S = 10\text{ V}$, see Figure 45 |
| Overvoltage Response Time, t_{RESPONSE} | 90 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 43 |
| | 115 | 130 | 130 | ns max | |
| Overvoltage Recovery Time, t_{RECOVERY} | 745 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 44 |
| | 945 | 965 | 970 | ns max | |
| Charge Injection, Q_{INJ} | -0.4 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$, see Figure 48 |
| Off Isolation | -76 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 40 |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 42 |
| Adjacent Channels | -75 | | | dB typ | |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.005 | | | % typ | $R_L = 10\text{ k}\Omega$, $V_S = 15\text{ V p-p}$, $f = 20\text{ Hz to }20\text{ kHz}$, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, see Figure 41 |
| ADG5208F | 190 | | | MHz typ | |
| ADG5209F | 290 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 41 |
| C_S (Off) | 4 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5208F | 13 | | | pF typ | |
| ADG5209F | 8 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5208F | 20 | | | pF typ | |
| ADG5209F | 14 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| | | | | | $V_{\text{DD}} = +16.5\text{ V}$; $V_{\text{SS}} = -16.5\text{ V}$; $\text{GND} = 0\text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.3 | | | mA typ | |
| | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.25 | | 1.25 | mA max | |
| I_{SS} | 0.65 | | | mA typ | |
| | 0.8 | | 0.85 | mA max | |
| Fault Mode | | | | | $V_S = \pm 55\text{ V}$ |
| I_{DD} | 1.6 | | | mA typ | |
| | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.65 | | | mA typ | |
| | 1.0 | | 1.1 | mA max | |
| $V_{\text{DD}}/V_{\text{SS}}$ | | | ± 5 | V min | $\text{GND} = 0\text{ V}$ |
| | | | ± 22 | V max | $\text{GND} = 0\text{ V}$ |

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = 20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | | $V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$, see Figure 38 |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 260 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 280 | 345 | 405 | Ω max | |
| | 250 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 2.5 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| | 2.5 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 12 | 13 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 12.5 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 14 | 15 | 15 | Ω max | |
| | 1.5 | | | Ω typ | $V_S = \pm 13.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 3.5 | 4 | 4 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 36 |
| | ± 1 | ± 2 | ± 5 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = \pm 15\text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 66 | | | μA typ | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| | ± 2 | ± 2 | ± 2 | μA max | |
| Power Supplies Grounded | ± 500 | | | nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| | ± 700 | ± 700 | ± 700 | nA max | |
| Power Supplies Floating | ± 50 | ± 50 | ± 50 | μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} | | | 2.0 | V min | |
| Input Voltage Low, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | ± 1.1 | | ± 1.2 | μA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------|----------------|-----------------|---------|--|
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{\text{TRANSITION}}$ | 190 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 245 | 270 | 285 | ns max | $V_S = 10 \text{ V}$, see Figure 47 |
| t_{ON} (EN) | 185 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 250 | 270 | 280 | ns max | $V_S = 10 \text{ V}$, see Figure 46 |
| t_{OFF} (EN) | 95 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 120 | 145 | 145 | ns max | $V_S = 10 \text{ V}$, see Figure 46 |
| Break-Before-Make Time Delay, t_D | 140 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | | | 90 | ns min | $V_S = 10 \text{ V}$, see Figure 45 |
| Overvoltage Response Time, t_{RESPONSE} | 75 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 5 \text{ pF}$, see Figure 43 |
| | 105 | 105 | 105 | ns max | |
| Overvoltage Recovery Time, t_{RECOVERY} | 820 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 5 \text{ pF}$, see Figure 44 |
| | 1100 | 1250 | 1400 | ns max | |
| Charge Injection, Q_{INJ} | -0.8 | | | pC typ | $V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$, see Figure 48 |
| Off Isolation | -76 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 40 |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 42 |
| Adjacent Channels | -75 | | | dB typ | |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.005 | | | % typ | $R_L = 10 \text{ k}\Omega$, $V_S = 20 \text{ V p-p}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, see Figure 41 |
| ADG5208F | 190 | | | MHz typ | |
| ADG5209F | 290 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 41 |
| C_S (Off) | 4 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5208F | 12 | | | pF typ | |
| ADG5209F | 8 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5208F | 19 | | | pF typ | |
| ADG5209F | 14 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| | | | | | $V_{\text{DD}} = +22 \text{ V}$; $V_{\text{SS}} = -22 \text{ V}$; $\text{GND} = 0 \text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.3 | | | mA typ | |
| | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.25 | | 1.25 | mA max | |
| I_{SS} | 0.65 | | | mA typ | |
| | 0.8 | | 0.85 | mA max | |
| Fault Mode | | | | | $V_S = \pm 55 \text{ V}$ |
| I_{DD} | 1.6 | | | mA typ | |
| | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.65 | | | mA typ | |
| | 1.0 | | 1.1 | mA max | |
| $V_{\text{DD}}/V_{\text{SS}}$ | | | ± 5 | V min | $\text{GND} = 0 \text{ V}$ |
| | | | ± 22 | V max | $\text{GND} = 0 \text{ V}$ |

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

Table 3.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|-----------------|-------------------|--|
| ANALOG SWITCH | | | | | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$, see Figure 38 |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 630 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 690 | 710 | 730 | Ω max | |
| | 270 | | | Ω typ | $V_S = 3.5\text{ V to }8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 290 | 355 | 410 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 6 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 17 | 19 | 19 | Ω max | |
| | 3 | | | Ω typ | $V_S = 3.5\text{ V to }8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6.5 | 11 | 12 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 380 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 440 | 460 | 460 | Ω max | |
| | 25 | | | Ω typ | $V_S = 3.5\text{ V to }8.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 27 | 28 | 28 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 36 |
| | ± 1 | ± 2 | ± 5 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = 1\text{ V}/10\text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 63 | | | μA typ | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | | μA typ | $V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, see Figure 35 |
| | ± 50 | ± 70 | ± 90 | nA max | |
| Power Supplies Grounded | ± 500 | | | nA typ | $V_{DD} = 0\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| | ± 700 | ± 700 | ± 700 | nA max | |
| Power Supplies Floating | ± 50 | ± 50 | ± 50 | μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0\text{ V}$, $V_S = \pm 55\text{ V}$, $A_X = 0\text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} | | | 2.0 | V min | |
| Input Voltage Low, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | ± 1.1 | | ± 1.2 | μA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------|----------------|-----------------|---------|--|
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{\text{TRANSITION}}$ | 160 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 200 | 215 | 230 | ns max | $V_S = 8\text{ V}$, see Figure 47 |
| t_{ON} (EN) | 160 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 200 | 220 | 235 | ns max | $V_S = 8\text{ V}$, see Figure 46 |
| t_{OFF} (EN) | 130 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | 155 | 160 | 160 | ns max | $V_S = 8\text{ V}$, see Figure 46 |
| Break-Before-Make Time Delay, t_D | 95 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ |
| | | | 65 | ns min | $V_S = 8\text{ V}$, see Figure 45 |
| Overvoltage Response Time, t_{RESPONSE} | 110 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 43 |
| | 145 | 145 | 145 | ns max | |
| Overvoltage Recovery Time, t_{RECOVERY} | 500 | | | ns typ | $R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$, see Figure 44 |
| | 655 | 720 | 765 | ns max | |
| Charge Injection, Q_{INU} | 0.9 | | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$, see Figure 48 |
| Off Isolation | -74 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 40 |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 42 |
| Adjacent Channels | -75 | | | dB typ | |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.044 | | | % typ | $R_L = 10\text{ k}\Omega$, $V_S = 6\text{ V p-p}$, $f = 20\text{ Hz to }20\text{ kHz}$, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, see Figure 41 |
| ADG5208F | 175 | | | MHz typ | |
| ADG5209F | 270 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 41 |
| C_S (Off) | 4 | | | pF typ | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5208F | 14 | | | pF typ | |
| ADG5209F | 8 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| ADG5208F | 21 | | | pF typ | |
| ADG5209F | 14 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| | | | | | $V_{\text{DD}} = 13.2\text{ V}$; $V_{\text{SS}} = 0\text{ V}$; $\text{GND} = 0\text{ V}$; digital inputs = 0 V, 5 V, or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.3 | | | mA typ | |
| | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.4 | | 1.4 | mA max | |
| I_{SS} | 0.5 | | | mA typ | |
| | 0.65 | | 0.7 | mA max | |
| Fault Mode | | | | | $V_S = \pm 55\text{ V}$ |
| I_{DD} | 1.6 | | | mA typ | |
| | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.65 | | | mA typ | Digital inputs = 5 V |
| | 1.0 | | 1.1 | mA max | $V_S = \pm 55\text{ V}$, $V_D = 0\text{ V}$ |
| V_{DD} | | | 8 | V min | $\text{GND} = 0\text{ V}$ |
| | | | 44 | V max | $\text{GND} = 0\text{ V}$ |

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $C_{DECOUPLING} = 0.1 \mu\text{F}$, unless otherwise noted.

Table 4.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-----------|----------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | $V_{DD} = 32.4 \text{ V}$, $V_{SS} = 0 \text{ V}$, see Figure 38 |
| On Resistance, R_{ON} | 310 | | | Ω typ | $V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 335 | 415 | 480 | Ω max | |
| | 250 | | | Ω typ | $V_S = 4.5 \text{ V to } 28 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 270 | 335 | 395 | Ω max | |
| On-Resistance Match Between Channels, ΔR_{ON} | 3 | | | Ω typ | $V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 7 | 16 | 18 | Ω max | |
| | 3 | | | Ω typ | $V_S = 4.5 \text{ V to } 28 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 6.5 | 11 | 12 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 62 | | | Ω typ | $V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 70 | 85 | 100 | Ω max | |
| | 1.5 | | | Ω typ | $V_S = 4.5 \text{ V to } 28 \text{ V}$, $I_S = -1 \text{ mA}$ |
| | 3.5 | 4 | 4 | Ω max | |
| Threshold Voltage, V_T | 0.7 | | | V typ | See Figure 30 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_{DD} = 39.6 \text{ V}$, $V_{SS} = 0 \text{ V}$ |
| | ± 1 | ± 2 | ± 5 | nA max | $V_S = 1 \text{ V/ } 30 \text{ V}$, $V_D = 30 \text{ V/ } 1 \text{ V}$, see Figure 36 |
| Drain Off Leakage, I_D (Off) | ± 0.1 | | | nA typ | $V_S = 1 \text{ V/ } 30 \text{ V}$, $V_D = 30 \text{ V/ } 1 \text{ V}$, see Figure 36 |
| | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.3 | | | nA typ | $V_S = V_D = 1 \text{ V/ } 30 \text{ V}$, see Figure 37 |
| | ± 1.5 | ± 20 | ± 25 | nA max | |
| FAULT | | | | | |
| Source Leakage Current, I_S With Overvoltage | ± 58 | | | μA typ | $V_{DD} = +39.6 \text{ V}$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $V_S = +55 \text{ V}$, -40 V , see Figure 35 |
| Power Supplies Grounded or Floating | ± 25 | | | μA typ | $V_{DD} = 0 \text{ V}$ or floating, $V_{SS} = 0 \text{ V}$ or floating, $GND = 0 \text{ V}$, $A_X = 0 \text{ V}$ or floating, $V_S = \pm 55 \text{ V}$, see Figure 34 |
| Drain Leakage Current, I_D With Overvoltage | ± 10 | | | nA typ | $V_{DD} = 39.6 \text{ V}$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $V_S = \pm 55 \text{ V}$, see Figure 35 |
| | ± 50 | ± 70 | ± 90 | nA max | |
| Power Supplies Grounded | ± 500 | | | nA typ | $V_{DD} = 0 \text{ V}$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $V_S = +55 \text{ V}$, -40 V , $A_X = 0 \text{ V}$, see Figure 34 |
| | ± 700 | ± 700 | ± 700 | nA max | |
| Power Supplies Floating | ± 50 | ± 50 | ± 50 | μA typ | $V_{DD} = \text{floating}$, $V_{SS} = \text{floating}$, $GND = 0 \text{ V}$, $V_S = \pm 55 \text{ V}$, $A_X = 0 \text{ V}$, see Figure 34 |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{INH} | | | 2.0 | V min | |
| Input Voltage Low, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 0.7 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | ± 1.1 | | ± 1.2 | μA max | |
| Digital Input Capacitance, C_{IN} | 5.0 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------|----------------|-----------------|---------|---|
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{\text{TRANSITION}}$ | 180 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 230 | 245 | 255 | ns max | $V_S = 18 \text{ V}$, see Figure 47 |
| t_{ON} (EN) | 175 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 225 | 245 | 260 | ns max | $V_S = 18 \text{ V}$, see Figure 46 |
| t_{OFF} (EN) | 105 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | 135 | 150 | 150 | ns max | $V_S = 18 \text{ V}$, see Figure 45 |
| Break-Before-Make Time Delay, t_D | 105 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$ |
| | | | 65 | ns min | $V_S = 18 \text{ V}$, see Figure 45 |
| Overvoltage Response Time, t_{RESPONSE} | 60 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 5 \text{ pF}$, see Figure 43 |
| | 80 | 85 | 85 | ns max | |
| Overvoltage Recovery Time, t_{RECOVERY} | 1400 | | | ns typ | $R_L = 1 \text{ k}\Omega$, $C_L = 5 \text{ pF}$, see Figure 44 |
| | 1900 | 2100 | 2200 | ns max | |
| Charge Injection, Q_{INJ} | -0.9 | | | pC typ | $V_S = 18 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$, see Figure 48 |
| Off Isolation | -75 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 40 |
| Channel-to-Channel Crosstalk | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 42 |
| Adjacent Channels | -75 | | | dB typ | |
| Nonadjacent Channels | -88 | | | dB typ | |
| Total Harmonic Distortion Plus Noise, THD + N | 0.007 | | | % typ | $R_L = 10 \text{ k}\Omega$, $V_S = 18 \text{ V p-p}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 39 |
| -3 dB Bandwidth | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, see Figure 41 |
| ADG5208F | 200 | | | MHz typ | |
| ADG5209F | 300 | | | MHz typ | |
| Insertion Loss | 10.5 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 41 |
| C_S (Off) | 3 | | | pF typ | $V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$ |
| C_D (Off) | | | | | $V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5208F | 12 | | | pF typ | |
| ADG5209F | 7 | | | pF typ | |
| C_D (On), C_S (On) | | | | | $V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$ |
| ADG5208F | 19 | | | pF typ | |
| ADG5209F | 12 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| | | | | | $V_{\text{DD}} = 39.6 \text{ V}$; $V_{\text{SS}} = 0 \text{ V}$; $\text{GND} = 0 \text{ V}$; digital inputs = 0 V , 5 V , or V_{DD} |
| Normal Mode | | | | | |
| I_{DD} | 1.3 | | | mA typ | |
| | 2 | | 2 | mA max | |
| I_{GND} | 0.75 | | | mA typ | |
| | 1.4 | | 1.4 | mA max | |
| I_{SS} | 0.5 | | | mA typ | |
| | 0.65 | | 0.7 | mA max | |
| Fault Mode | | | | | $V_S = +55 \text{ V}$, -40 V |
| I_{DD} | 1.6 | | | mA typ | |
| | 2.2 | | 2.3 | mA max | |
| I_{GND} | 0.9 | | | mA typ | |
| | 1.6 | | 1.7 | mA max | |
| I_{SS} | 0.65 | | | mA typ | |
| | 1.0 | | 1.1 | mA max | |
| V_{DD} | | | 8 | V min | $\text{GND} = 0 \text{ V}$ |
| | | | 44 | V max | $\text{GND} = 0 \text{ V}$ |

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S_x, D, OR D_x

Table 5.

| Parameter | 25°C | 85°C | 125°C | Unit | Test Conditions/Comments |
|--|------|------|-------|--------|---|
| ADG5208F | | | | | |
| 16-Lead TSSOP, $\theta_{JA} = 112.6^{\circ}\text{C/W}$ | 27 | 16 | 8 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 16 | 11 | 7 | mA max | $V_S = V_{SS}$ to V_{DD} |
| 16-Lead LFCSP, $\theta_{JA} = 30.4^{\circ}\text{C/W}$ | 48 | 25 | 11 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 27 | 17 | 9 | mA max | $V_S = V_{SS}$ to V_{DD} |
| ADG5209F | | | | | |
| 16-Lead TSSOP, $\theta_{JA} = 112.6^{\circ}\text{C/W}$ | 20 | 13 | 8 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 12 | 8 | 6 | mA max | $V_S = V_{SS}$ to V_{DD} |
| 16-Lead LFCSP, $\theta_{JA} = 30.4^{\circ}\text{C/W}$ | 36 | 20 | 10 | mA max | $V_S = V_{SS}$ to $V_{DD} - 4.5\text{ V}$ |
| | 21 | 13 | 8 | mA max | $V_S = V_{SS}$ to V_{DD} |

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

| Parameter | Rating |
|---|--|
| V _{DD} to V _{SS} | 48 V |
| V _{DD} to GND | −0.3 V to +48 V |
| V _{SS} to GND | −48 V to +0.3 V |
| Sx Pins | −55 V to +55 V |
| Sx to V _{DD} or V _{SS} | 80 V |
| V _S to V _D | 80 V |
| D or Dx Pins ¹ | V _{SS} − 0.7 V to V _{DD} + 0.7 V or 30 mA, whichever occurs first |
| Digital Inputs ² | GND − 0.7 V to 48 V or 30 mA, whichever occurs first |
| Peak Current, Sx, D, or Dx Pins | 72.5 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, Sx, D, or Dx Pins | Data ³ + 15% |
| D or Dx Pins, Overvoltage State, Load Current | 1 mA |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Impedance, θ _{JA} (4-Layer Board) | |
| 16-Lead TSSOP | 112.6°C/W |
| 16-Lead LFCSP | 30.4°C/W |
| Reflow Soldering Peak Temperature, Pb-Free | As per JEDEC J-STD-020 |

¹ Overvoltages at the D or Dx pins are clamped by internal diodes. Limit the current to the maximum ratings given.

² The digital inputs are the EN and Ax pins.

³ See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



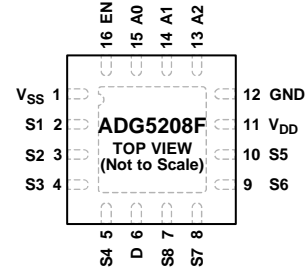
ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 3. ADG5208F Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 4. ADG5208F Pin Configuration (LFCSP)

Table 7. ADG5208F Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|------------------|-------|-----------------|---|
| TSSOP | LFCSP | | |
| 1 | 15 | A0 | Logic Control Input. |
| 2 | 16 | EN | Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 2 | S1 | Overvoltage Protected Source Terminal 1. This pin can be an input or an output. |
| 5 | 3 | S2 | Overvoltage Protected Source Terminal 2. This pin can be an input or an output. |
| 6 | 4 | S3 | Overvoltage Protected Source Terminal 3. This pin can be an input or an output. |
| 7 | 5 | S4 | Overvoltage Protected Source Terminal 4. This pin can be an input or an output. |
| 8 | 6 | D | Drain Terminal. This pin can be an input or an output. |
| 9 | 7 | S8 | Overvoltage Protected Source Terminal 8. This pin can be an input or an output. |
| 10 | 8 | S7 | Overvoltage Protected Source Terminal 7. This pin can be an input or an output. |
| 11 | 9 | S6 | Overvoltage Protected Source Terminal 6. This pin can be an input or an output. |
| 12 | 10 | S5 | Overvoltage Protected Source Terminal 5. This pin can be an input or an output. |
| 13 | 11 | V _{DD} | Most Positive Power Supply Potential. |
| 14 | 12 | GND | Ground (0 V) Reference. |
| 15 | 13 | A2 | Logic Control Input. |
| 16 | 14 | A1 | Logic Control Input. |
| N/A ¹ | 0 | EPAD | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

¹ N/A means not applicable.

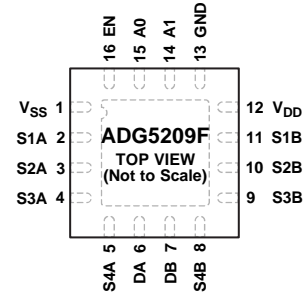
Table 8. ADG5208F Truth Table

| A2 | A1 | A0 | EN | On Switch |
|----------------|----------------|----------------|----|-----------|
| X ¹ | X ¹ | X ¹ | 0 | None |
| 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 1 | 1 | S2 |
| 0 | 1 | 0 | 1 | S3 |
| 0 | 1 | 1 | 1 | S4 |
| 1 | 0 | 0 | 1 | S5 |
| 1 | 0 | 1 | 1 | S6 |
| 1 | 1 | 0 | 1 | S7 |
| 1 | 1 | 1 | 1 | S8 |

¹ X is don't care.



Figure 5. ADG5209F Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 6. ADG5209F Pin Configuration (LFCSP)

Table 9. ADG5209F Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|------------------|-------|-----------------|---|
| TSSOP | LFCSP | | |
| 1 | 15 | A0 | Logic Control Input. |
| 2 | 16 | EN | Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 2 | S1A | Overvoltage Protected Source Terminal 1A. This pin can be an input or an output. |
| 5 | 3 | S2A | Overvoltage Protected Source Terminal 2A. This pin can be an input or an output. |
| 6 | 4 | S3A | Overvoltage Protected Source Terminal 3A. This pin can be an input or an output. |
| 7 | 5 | S4A | Overvoltage Protected Source Terminal 4A. This pin can be an input or an output. |
| 8 | 6 | DA | Drain Terminal A. This pin can be an input or an output. |
| 9 | 7 | DB | Drain Terminal B. This pin can be an input or an output. |
| 10 | 8 | S4B | Overvoltage Protected Source Terminal 4B. This pin can be an input or an output. |
| 11 | 9 | S3B | Overvoltage Protected Source Terminal 3B. This pin can be an input or an output. |
| 12 | 10 | S2B | Overvoltage Protected Source Terminal 2B. This pin can be an input or an output. |
| 13 | 11 | S1B | Overvoltage Protected Source Terminal 1B. This pin can be an input or an output. |
| 14 | 12 | V _{DD} | Most Positive Power Supply Potential. |
| 15 | 13 | GND | Ground (0 V) Reference. |
| 16 | 14 | A1 | Logic Control Input. |
| N/A ¹ | 0 | EPAD | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

¹ N/A means not applicable.

Table 10. ADG5209F Truth Table

| A1 | A0 | EN | On Switch Pair |
|----------------|----------------|----|----------------|
| X ¹ | X ¹ | 0 | None |
| 0 | 0 | 1 | S1x |
| 0 | 1 | 1 | S2x |
| 1 | 0 | 1 | S3x |
| 1 | 1 | 1 | S4x |

¹ X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 7. R_{ON} as a Function of V_S, V_D , Dual Supply



Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 15 V Dual Supply

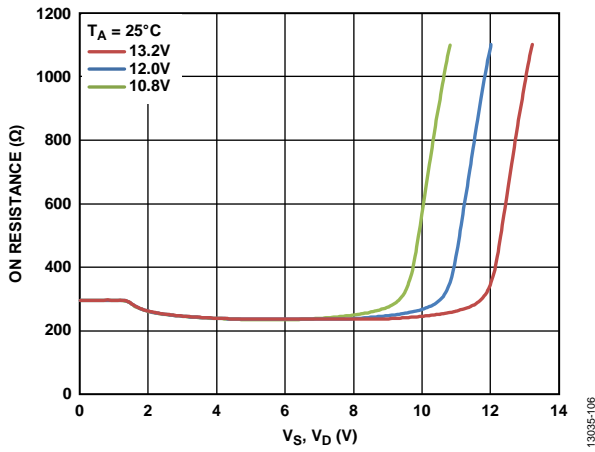


Figure 8. R_{ON} as a Function of V_S, V_D , 12 V Single Supply



Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, ± 20 V Dual Supply

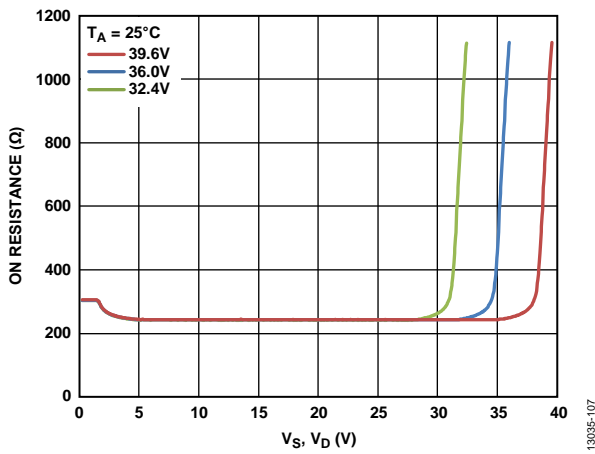


Figure 9. R_{ON} as a Function of V_S, V_D , 36 V Single Supply

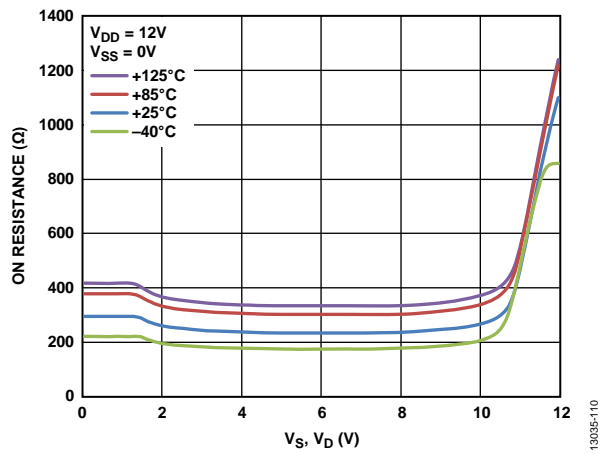


Figure 12. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply



Figure 13. R_{ON} as a Function of V_S , V_D for Different Temperatures, 36 V Single Supply



Figure 16. Leakage Current vs. Temperature, 12 V Single Supply



Figure 14. Leakage Current vs. Temperature, ±15 V Dual Supply



Figure 17. Leakage Current vs. Temperature, 36 V Single Supply

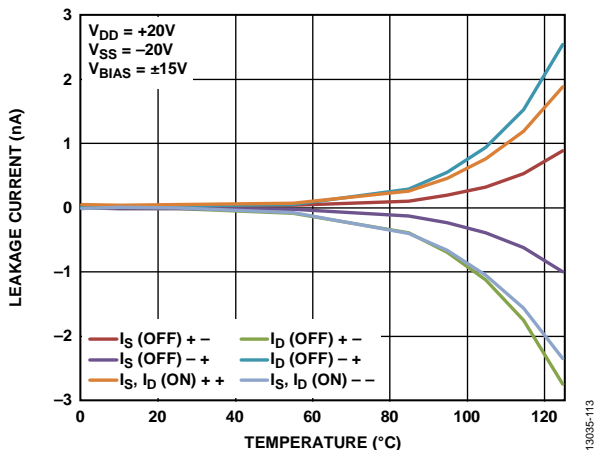


Figure 15. Leakage Current vs. Temperature, ±20 V Dual Supply

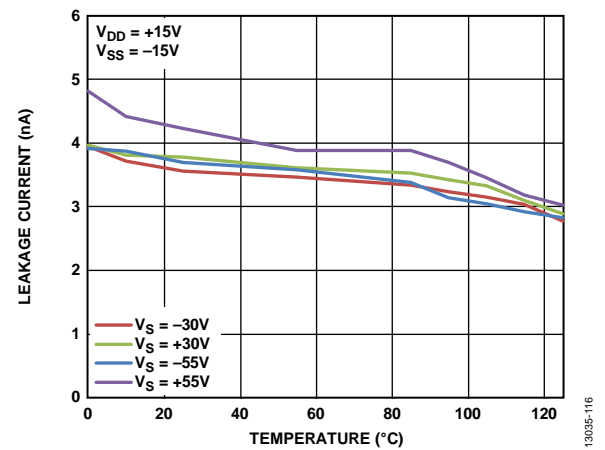


Figure 18. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply



Figure 19. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply



Figure 22. Off Isolation vs. Frequency, ±15 V Dual Supply



Figure 20. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply



Figure 23. Crosstalk vs. Frequency, ±15 V Dual Supply



Figure 21. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply



Figure 24. Charge Injection vs. Source Voltage (V_s), Single Supply



Figure 25. Charge Injection vs. Source Voltage (V_S), Dual Supply



Figure 28. Bandwidth vs. Frequency



Figure 26. ACPSRR vs. Frequency, ± 15 V Dual Supply



Figure 29. $t_{TRANSITION}$ vs. Temperature

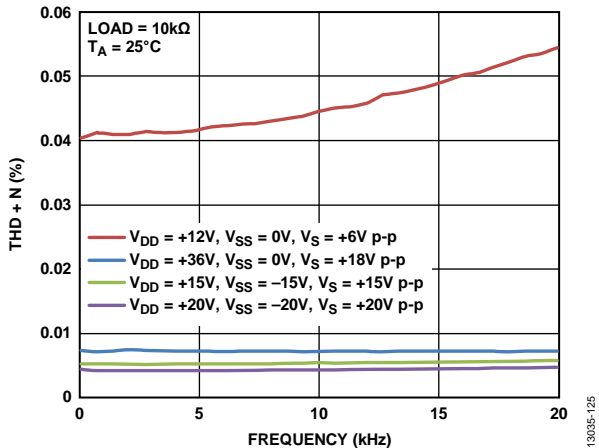


Figure 27. THD + N vs. Frequency

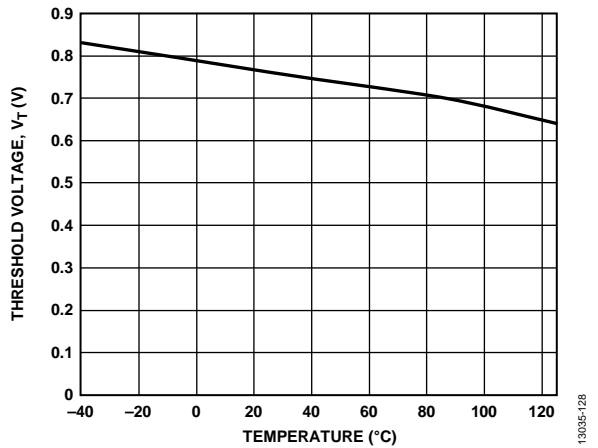


Figure 30. Threshold Voltage (V_T) vs. Temperature

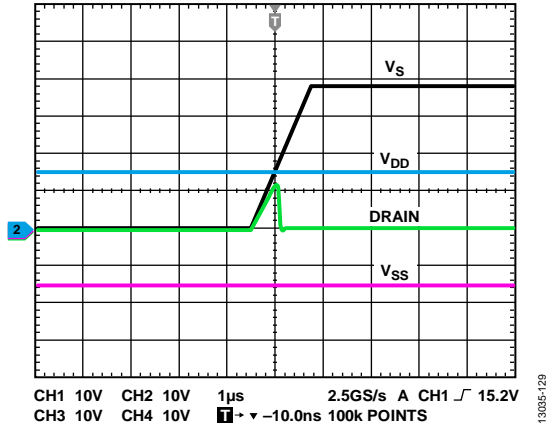


Figure 31. Drain Output Response to Positive Overvoltage

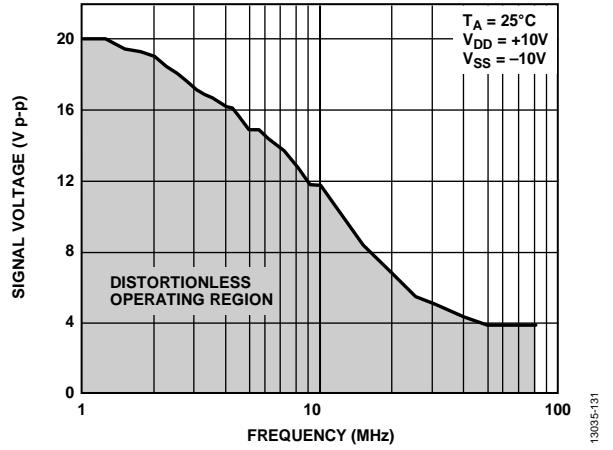


Figure 33. Large Voltage Signal Tracking vs. Frequency

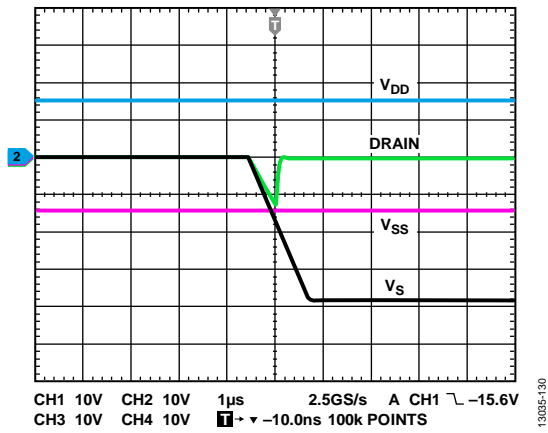


Figure 32. Drain Output Response to Negative Overvoltage

TEST CIRCUITS



Figure 34. Switch Unpowered Leakage



Figure 35. Switch Overvoltage Leakage



Figure 36. Off Leakage



Figure 37. On Leakage

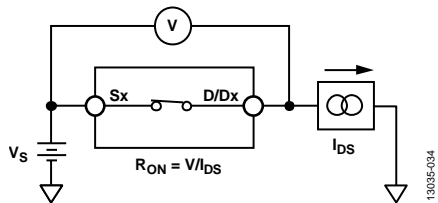


Figure 38. On Resistance



Figure 39. THD + N



Figure 40. Off Isolation

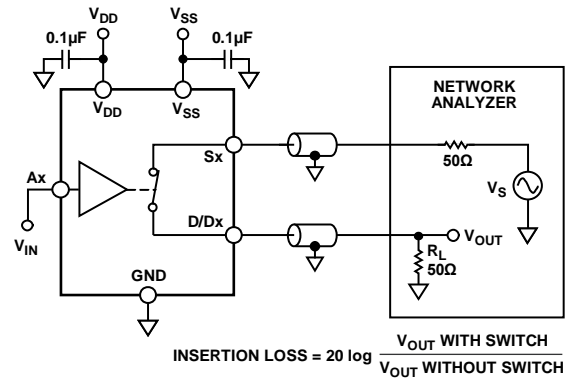


Figure 41. Bandwidth

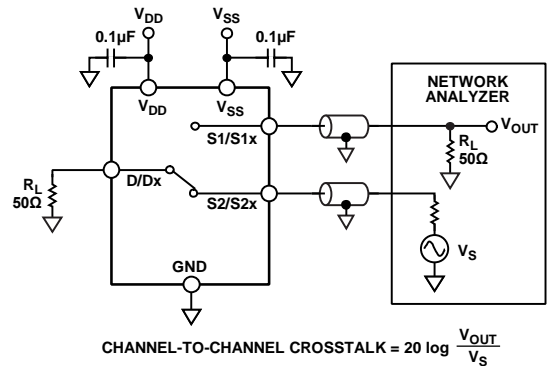


Figure 42. Channel-to-Channel Crosstalk



NOTES

1. THE OUTPUT PULLS TO V_{DD} WITHOUT A 1kΩ RESISTOR (INTERNAL 40kΩ PULL-UP RESISTOR TO THE SUPPLY RAIL DURING A FAULT).

Figure 43. Overvoltage Response Time, $t_{RESPONSE}$

13035-043

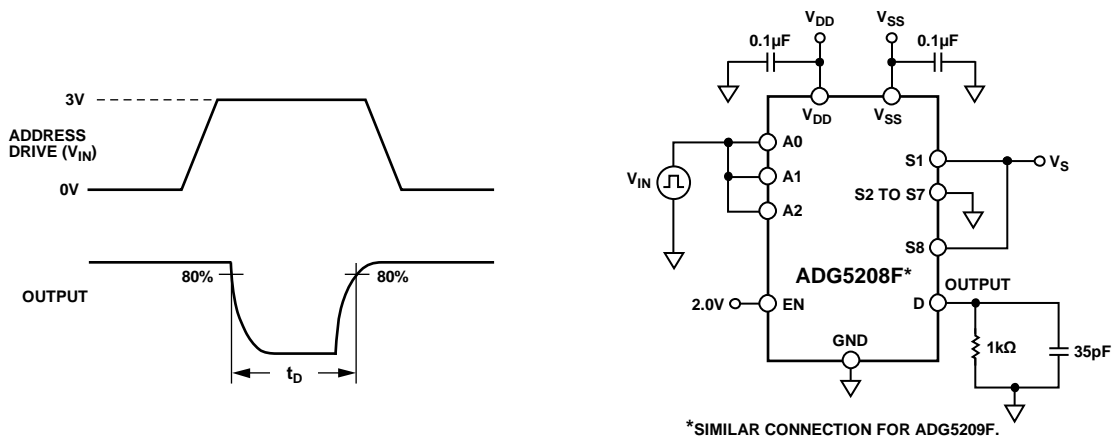


NOTES

1. THE OUTPUT STARTS FROM THE V_{DD} CLAMP LEVEL WITHOUT A 1kΩ RESISTOR (INTERNAL 40kΩ PULL-UP RESISTOR TO THE SUPPLY RAIL DURING A FAULT).

Figure 44. Overvoltage Recovery Time, $t_{RECOVERY}$

13035-044



*SIMILAR CONNECTION FOR ADG5209F.

Figure 45. Break-Before-Make Time Delay, t_D

13035-045



Figure 46. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

13035-046

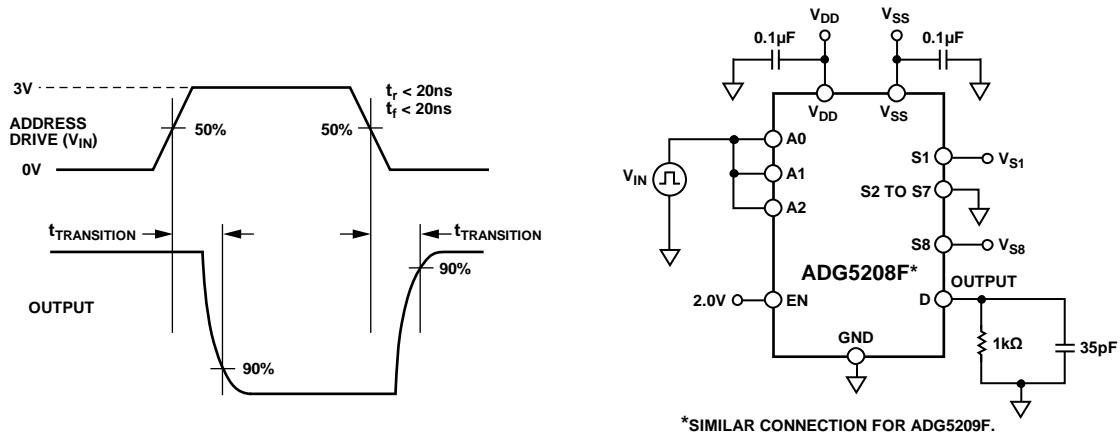


Figure 47. Address to Output Switching Time, $t_{TRANSITION}$

13035-047

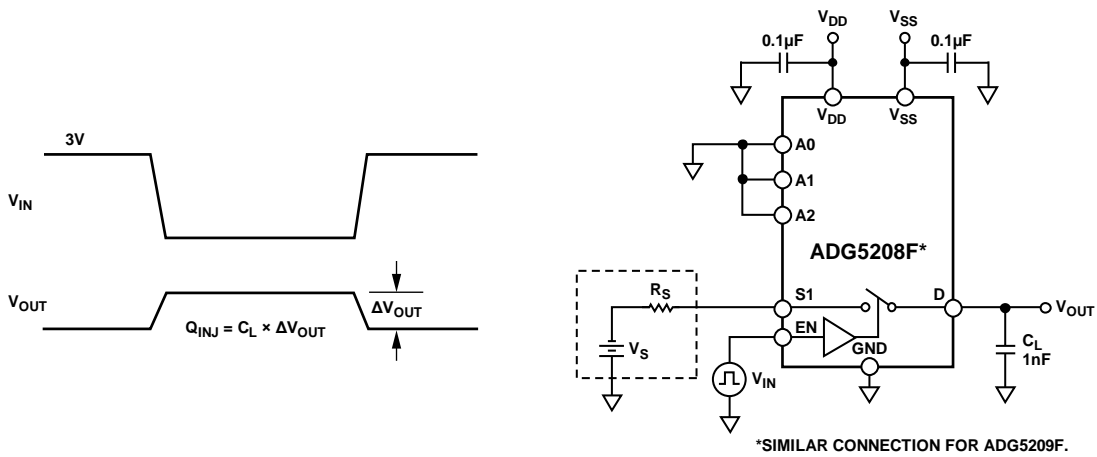


Figure 48. Charge Injection, Q_{INJ}

13035-048

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on the D or Dx pins and the Sx pins, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between the D or Dx pins and the Sx pins.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

I_S (off) is the source leakage current with the switch off.

I_D (Off)

I_D (off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (on) and I_S (on) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (on) and C_S (on) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) represents the delay between applying the digital control input and the output switching on (see Figure 46).

t_{OFF} (EN)

t_{OFF} (EN) represents the delay between applying the digital control input and the output switching off (see Figure 46).

$t_{TRANSITION}$

$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 90% points of both switches when switching from one address state to another.

$t_{RESPONSE}$

$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 50% of its peak voltage.

$t_{RECOVERY}$

$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 50% of its peak voltage.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

-3 dB Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

On Response

On response is the frequency response of the on switch.

V_T

V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 30).

Total Harmonic Distortion Plus Noise (THD + N)

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the ADG5208F/ADG5209F consists of a parallel pair of NDMOS and PDMOS transistors. This construction provides excellent performance across the signal range. The ADG5208F/ADG5209F channels operate as standard switches when input signals with a voltage between V_{SS} and V_{DD} are applied. For example, the on resistance is 250 Ω typically and opening or closing the switch is controlled using the appropriate address pins.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on a source pin with V_{DD} and V_{SS} . A signal is considered overvoltage if it exceeds the supply voltages by the voltage threshold, V_T . The threshold voltage is typically 0.7 V, but can range from 0.8 V at -40°C down to 0.6 V at $+125^\circ\text{C}$. See Figure 30 to see the change in V_T with operating temperature.

The voltage range that can be applied to any source input is $+55\text{ V}$ to -55 V . When the device is powered using a single supply of 25 V or greater, the minimum signal level increases from -55 V to -40 V at $V_{DD} = +40\text{ V}$ to remain within the 80 V maximum rating. Construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

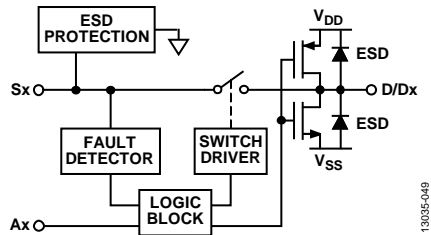


Figure 49. Switch Channel and Control Function

Overvoltage Reaction

When an overvoltage condition is detected on a source pin, the switch automatically opens regardless of the digital logic state. The source pin becomes high impedance and, if that source pin is selected, the drain pin is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{DD} , then the drain output pulls to V_{DD} , similarly for V_{SS} . In Figure 31, the voltage on the drain pin can be seen to follow the voltage on the source pin until the switch turns off completely. The drain pin then pulls to GND due to the 1 k Ω load resistor; otherwise, it pulls to the V_{DD} supply. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the pin.

During overvoltage conditions, the leakage current into and out of the source pins is limited to tens of microamperes. If the source pin is unselected, only nanoamperes of leakage appear on the drain pin. However, if the source is selected, the pin is pulled to the supply rail. The device that pulls the drain pin to the rail has an impedance of approximately 40 k Ω ; thus, the D or Dx pin current is limited to approximately 1 mA during a shorted load condition. This internal impedance also determines the minimum external load resistance required to ensure that the drain pin is pulled to the desired voltage level during a fault. When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The drain pins have ESD protection diodes to the rails and the voltage at these pins must not exceed the supply voltage. The source pins have specialized ESD protection that allows the signal voltage to reach $\pm 55\text{ V}$ regardless of supply voltage level. See Figure 49 for an overview of the switch channel function.

Trench Isolation

In the ADG5208F and ADG5209F, an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances.



Figure 50. Trench Isolation

FAULT PROTECTION

When the voltages at the source inputs exceed V_{DD} or V_{SS} by V_T , the switch turns off or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state and if it is selected, the drain pulls to either V_{DD} or V_{SS} . Signal levels up to +55 V and -55 V are blocked in both the powered and unpowered condition as long as the 80 V limitation between the source and supply pins is met.

Power-On Protection

The following three conditions must be satisfied for the switch to be in the on condition:

- V_{DD} to $V_{SS} \geq 8$ V
- The input signal is between $V_{SS} - V_T$ and $V_{DD} + V_T$
- The digital logic control input is active

When the switch is turned on, signal levels up to the supply rails are passed.

The switch responds to an analog input that exceeds V_{DD} or V_{SS} by a threshold voltage, V_T , by turning off. The absolute input voltage limits are -55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the source pin returns to between V_{DD} and V_{SS} .

The fault response time ($t_{RESPONSE}$) when powered by a ± 15 V dual supply is typically 90 ns and the fault recovery time ($t_{RECOVERY}$) is 745 ns. These vary with supply voltages and output load conditions.

Exceeding ± 55 V on any source input may damage the ESD protection circuitry on the device.

The maximum stress across the switch channel is 80 V, therefore, the user must pay close attention to this limit under a fault condition.

For example, consider the case where the device is set up as shown in Figure 51.

- $V_{DD}/V_{SS} = \pm 22$ V, S1 = +22 V, S1 is selected
- S2 has a -55 V fault and S3 has a +55 V fault
- The voltage between S2 and D = +22 V - (-55 V) = +77 V
- The voltage between S3 and D = 55 V - 22 V = 33 V

These calculations are all within device specifications: a 55 V maximum fault on the source inputs and a maximum of 80 V across the off switch channel.

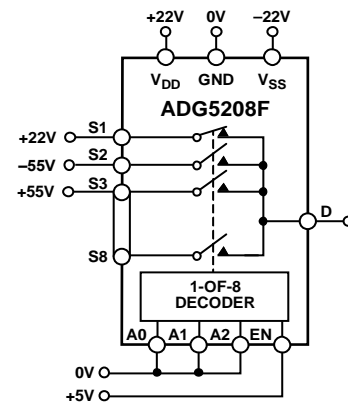


Figure 51. ADG5208F in an Overvoltage Condition

Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ± 55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5208F and the ADG5209F can tolerate digital input signals being present on the device without power. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults of up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provides robust solutions for instrumentation, industrial, automotive, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 μF decoupling capacitors are required.

The [ADG5208F](#) and the [ADG5209F](#) can operate with bipolar supplies between $\pm 5\text{ V}$ and $\pm 22\text{ V}$. The supplies on V_{DD} and V_{SS} need not be symmetrical, but the V_{DD} to V_{SS} range must not exceed 44 V. The [ADG5208F](#) and the [ADG5209F](#) can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

These devices are fully specified at $\pm 15\text{ V}$, $\pm 20\text{ V}$, $+12\text{ V}$, and $+36\text{ V}$ supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the devices are unpowered and signals from -55 V to $+55\text{ V}$ can be applied without damaging the devices. The switch channel closes only when the supplies are connected, a suitable digital control signal is placed on the address pins, and the signal is within normal operating range. Placing the [ADG5208F/ADG5209F](#) between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins before the supply voltages are available.

SIGNAL RANGE

The [ADG5208F/ADG5209F](#) switches have overvoltage detection circuitry on their inputs that compares the voltage levels at the source terminals with V_{DD} and V_{SS} . To protect downstream circuitry from overvoltages, supply the [ADG5208F/ADG5209F](#) with voltages that match the intended signal range. The additional protection architecture allows the signals up to the supply rails to be passed and only a signal that exceeds the supply rail by the threshold voltage is then blocked. This signal block offers protection to both the device and any downstream circuitry.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 52. The [ADP7118](#) and [ADP7182](#) can be used to generate clean positive and negative rails from the [ADP5070](#) (dual switching regulator) output. These rails can be used to power the [ADG5208F/ADG5209F](#) amplifier, and/or a precision converter in a typical signal chain.

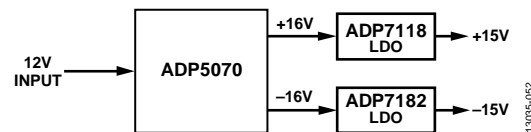


Figure 52. Bipolar Power Solution

Table 11. Recommended Power Management Devices

| Product | Description |
|-------------------------|--|
| ADP5070 | 1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs |
| ADP7118 | 20 V, 200 mA, low noise, CMOS LDO |
| ADP7142 | 40 V, 200 mA, low noise, CMOS LDO |
| ADP7182 | -28 V , -200 mA , low noise, linear regulator |

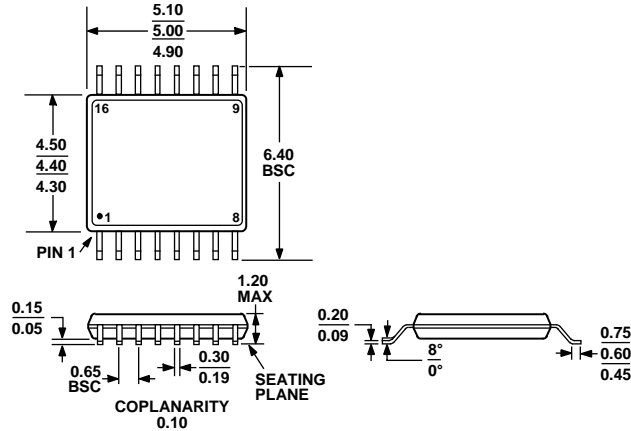
HIGH VOLTAGE SURGE SUPPRESSION

The [ADG5208F/ADG5209F](#) are not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltages exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar devices.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

Figure 33 illustrates the voltage range and frequencies that the [ADG5208F/ADG5209F](#) can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD} , keep the frequency below 1 MHz. If the required frequency is greater than 1 MHz, decrease the signal range appropriately to ensure signal integrity.

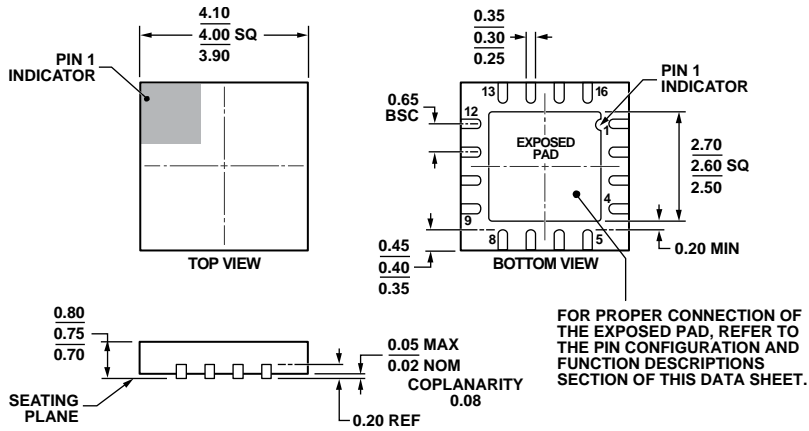
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 53. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body and 0.75 mm Package Height (CP-16-17)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG5208FBCPZ-RL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-17 |
| ADG5208FBRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG5208FBRUZ-RL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG5209FBCPZ-RL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-17 |
| ADG5209FBRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG5209FBRUZ-RL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

¹ Z = RoHS Compliant Part.

08-16-2010-C

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9