IS61NLP12832B
IS61NLP12836B/IS61NVP12836B
IS61NLP25618A/IS61NVP25618A

128K x 32, 128K x 36, and 256K x 18
4Mb, PIPELINE 'NO WAIT' STATE BUS SRAM

SEPTEMBER 2007

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{CKE}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 165-ball PBGA and 119-ball PBGA packages
- Power supply:
  NVP: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
  NLP: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 4 Meg 'NLP/NVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 128K words by 32 bits, 128K words by 36 bits, and 256K words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CKE}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

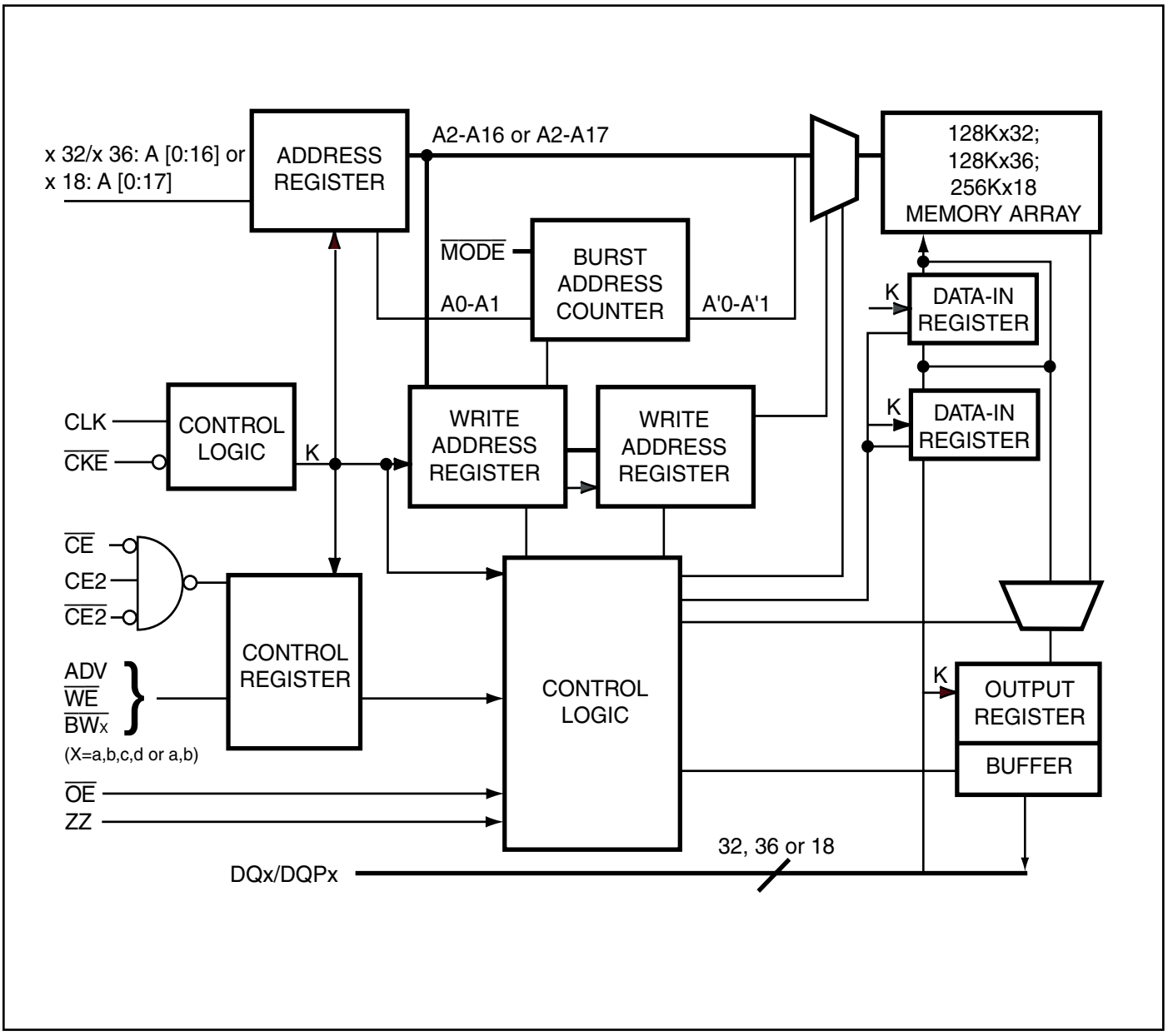
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written.

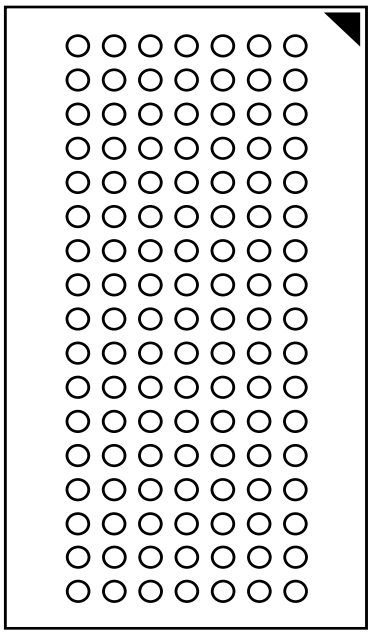
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

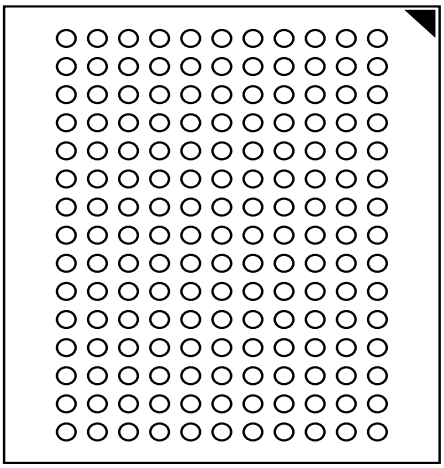
Symbol	Parameter	-250	-200	Units
t_{KQ}	Clock Access Time	2.6	3.1	ns
t_{KC}	Cycle Time	4	5	ns
	Frequency	250	200	MHz

BLOCK DIAGRAM





Bottom View
119-Ball, 14 mm x 22 mm BGA
1 mm Ball Pitch, 7 x 17 Ball Array



Bottom View
165-Ball, 13 mm x 15mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array

PIN CONFIGURATION — 128K x 36, 165-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BW}$c	$\overline{BW}$b	$\overline{CE}$2	$\overline{CKE}$	ADV	NC	A	NC
B	NC	A	CE2	$\overline{BW}$d	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	NC	A1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A0*	NC	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/ Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$x (x=a-d)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V_{DD}	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
V_{DDQ}	Isolated output Power Supply 3.3V/2.5V
V_{SS}	Ground

119-PIN PBGA PACKAGE CONFIGURATION —128K x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	$\overline{CE}2$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	Vss	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE}$	Vss	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	Vss	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BW}$c	NC	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	Vss	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	NC	$\overline{BW}$a	DQa	DQa
M	V_{DDQ}	DQd	VSS	$\overline{CKE}$	Vss	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A_1*	Vss	DQa	DQa
P	DQd	DQPd	V_{SS}	A_0*	Vss	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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A	Address Inputs
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CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BW}$x (x=a-d)	Synchronous Byte Write Inputs

$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Parity Data I/O
V_{DDQ}	Output Power Supply

165-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BW}$b	NC	$\overline{CE}$2	$\overline{CKE}$	ADV	NC	A	A
B	NC	A	CE2	NC	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	NC	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	Vss	NC	NC	NC	Vss	V_{DDQ}	NC	NC
P	NC	NC	A	A	NC	A_1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A_0*	NC	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

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A	Address Inputs
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CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V_{DD}	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
V_{DDQ}	Isolated output Power Supply 3.3V/2.5V
Vss	Ground

119-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	$\overline{CE}2$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	Vss	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CE}$	Vss	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	Vss	DQa	V_{DDQ}
G	NC	DQb	$\overline{BW}b$	NC	NC	NC	DQa
H	DQb	NC	Vss	$\overline{WE}$	Vss	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	Vss	NC	DQa
L	DQb	NC	NC	NC	$\overline{BW}a$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{CKE}$	Vss	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	Vss	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	Vss	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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A	Address Inputs
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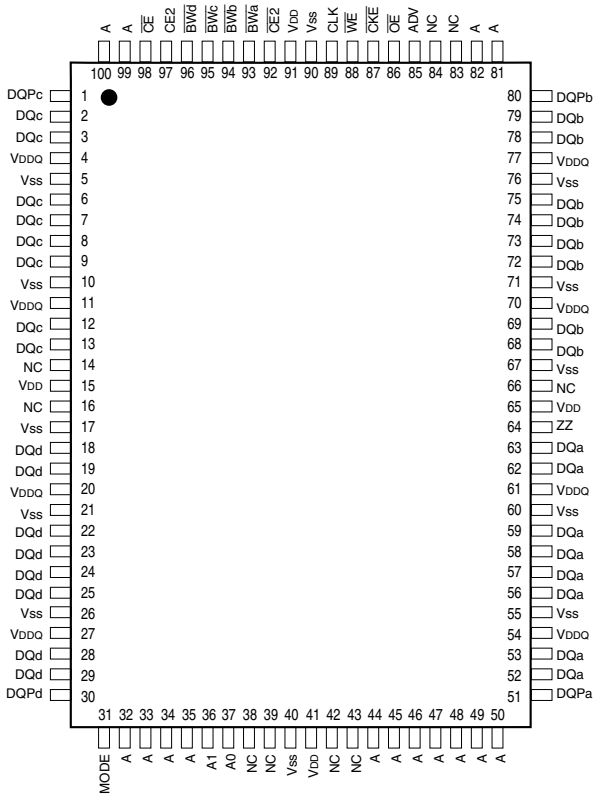
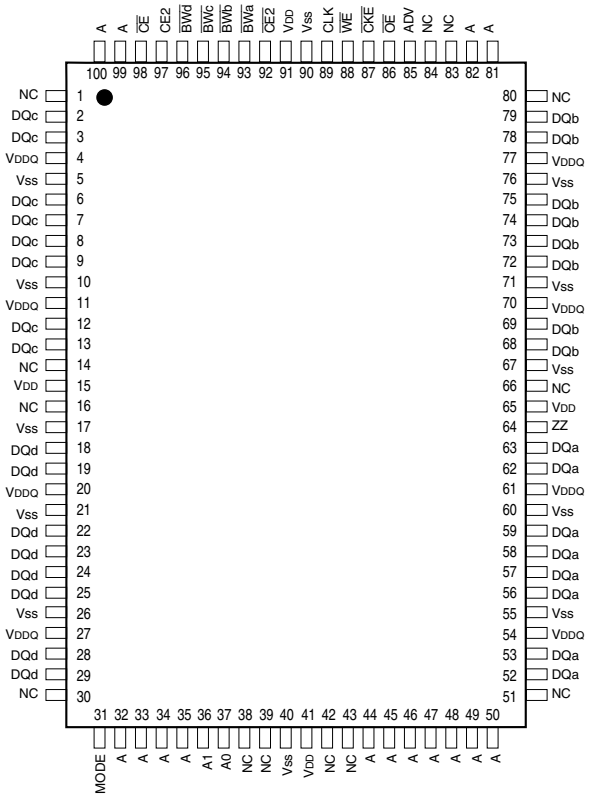
$\overline{CKE}$	Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Inputs

$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Parity Data I/O
V_{DDQ}	Output Power Supply

PIN CONFIGURATION
100-Pin TQFP



128K x 36



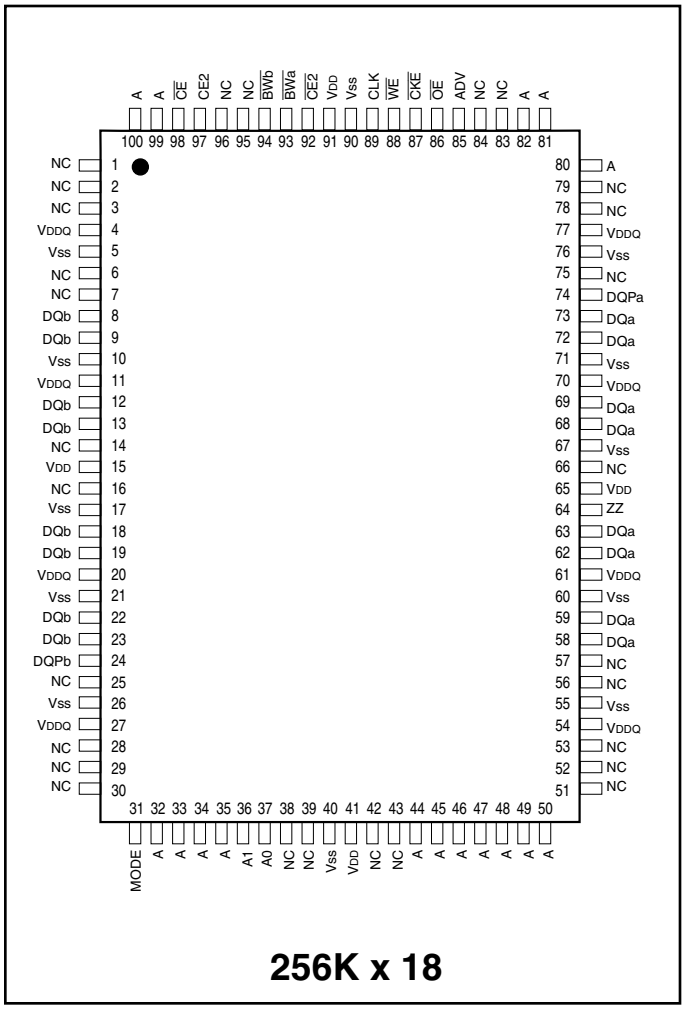
128K x 32

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BW}$a-$\overline{BW}$d	Synchronous Byte Write Enable
$\overline{WE}$	Write Enable
$\overline{CKE}$	Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data I/O
MODE	Burst Sequence Selection
V_{DD}	+3.3V/2.5V Power Supply
V_{SS}	Ground for output Buffer
V_{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

PIN CONFIGURATION
100-Pin TQFP



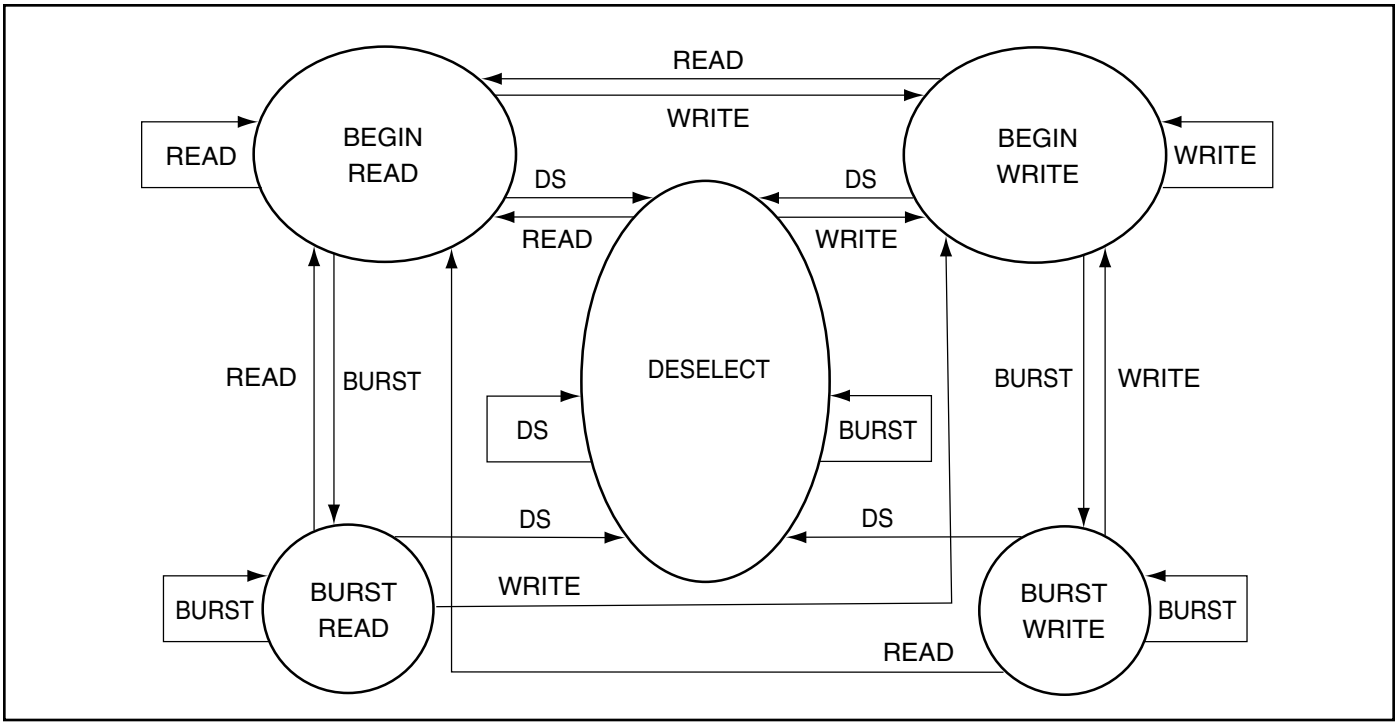
256K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BW}$a-$\overline{BW}$d	Synchronous Byte Write Enable
$\overline{WE}$	Write Enable
$\overline{CKE}$	Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data I/O
MODE	Burst Sequence Selection
V_{DD}	+3.3V/2.5V Power Supply
V_{SS}	Ground for output Buffer
V_{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE(1)

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE(1)

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x32/x36)

Operation	$\overline{WE}$	$\overline{BW}a$	$\overline{BW}b$	$\overline{BW}c$	$\overline{BW}d$
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

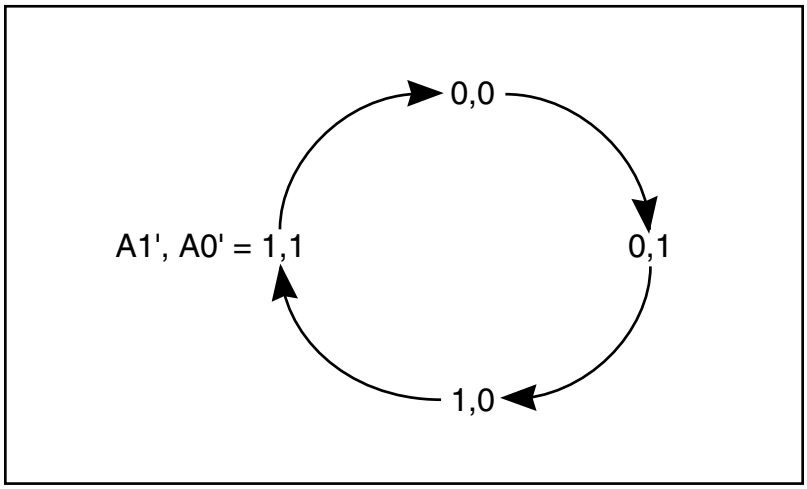
Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to V_{SS} for I/O Pins	–0.5 to V_{DDQ} + 0.5	V
V_{IN}	Voltage Relative to V_{SS} for for Address and Control Inputs	–0.5 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	3.3V Min.	3.3V Max.	2.5V Min.	2.5V Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V)	2.4	—	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}(1)	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$(1)	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE} = V_{IH}$	–5	5	–5	5	µA

Note:
1. Overshoot: V_{IH} (AC) < V_{DD} + 2.0V (Pulse width less than t_{KC}/2). Undershoot: V_{IL} (AC) > -2V (Pulse width less than t_{KC}/2).

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-250 MAX x18	-250 MAX x32/x36	-200 MAX x18	-200 MAX x32/x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com. Ind.	225 250	225 250	200 210	200 210	mA
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com. Ind.	90 100	90 100	90 100	90 100	mA
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., $V_{IN} \le V_{SS}$ + 0.2V or ≥V_{DD} – 0.2V f = 0	Com. Ind. typ.(2)	70 75	70 75 40	70 75	70 75	mA
I_{SB2}	Sleep Mode	ZZ>V_{IH}	Com. Ind. typ.(2)	30 35	30 35 20	30 35	30 35	mA

Note:
1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100µA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

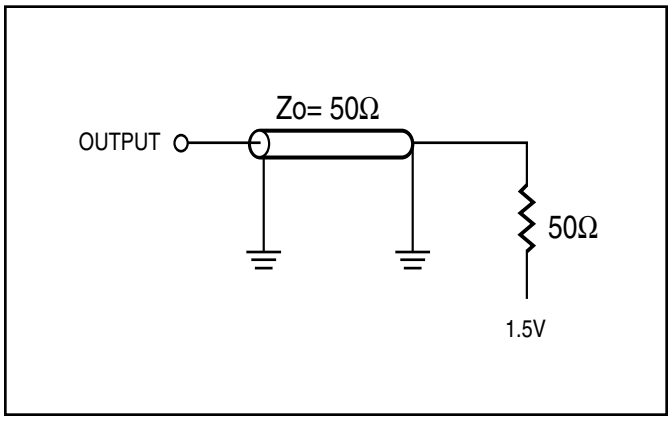


Figure 1

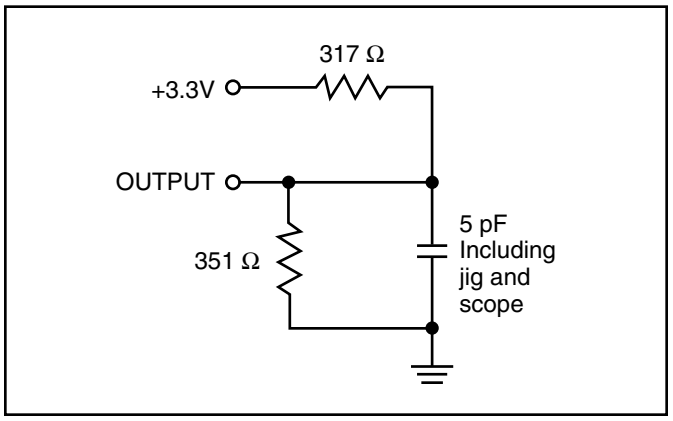


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

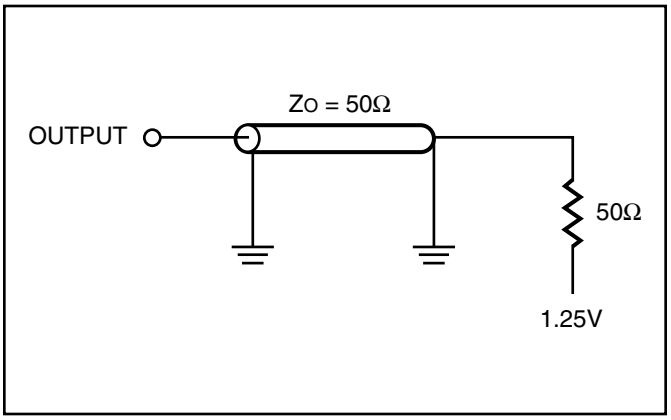


Figure 3

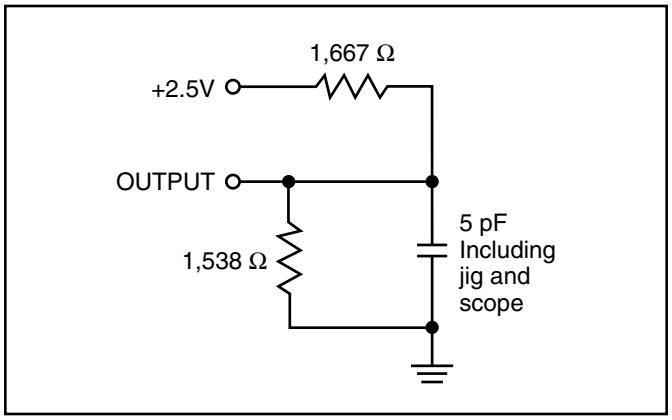


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

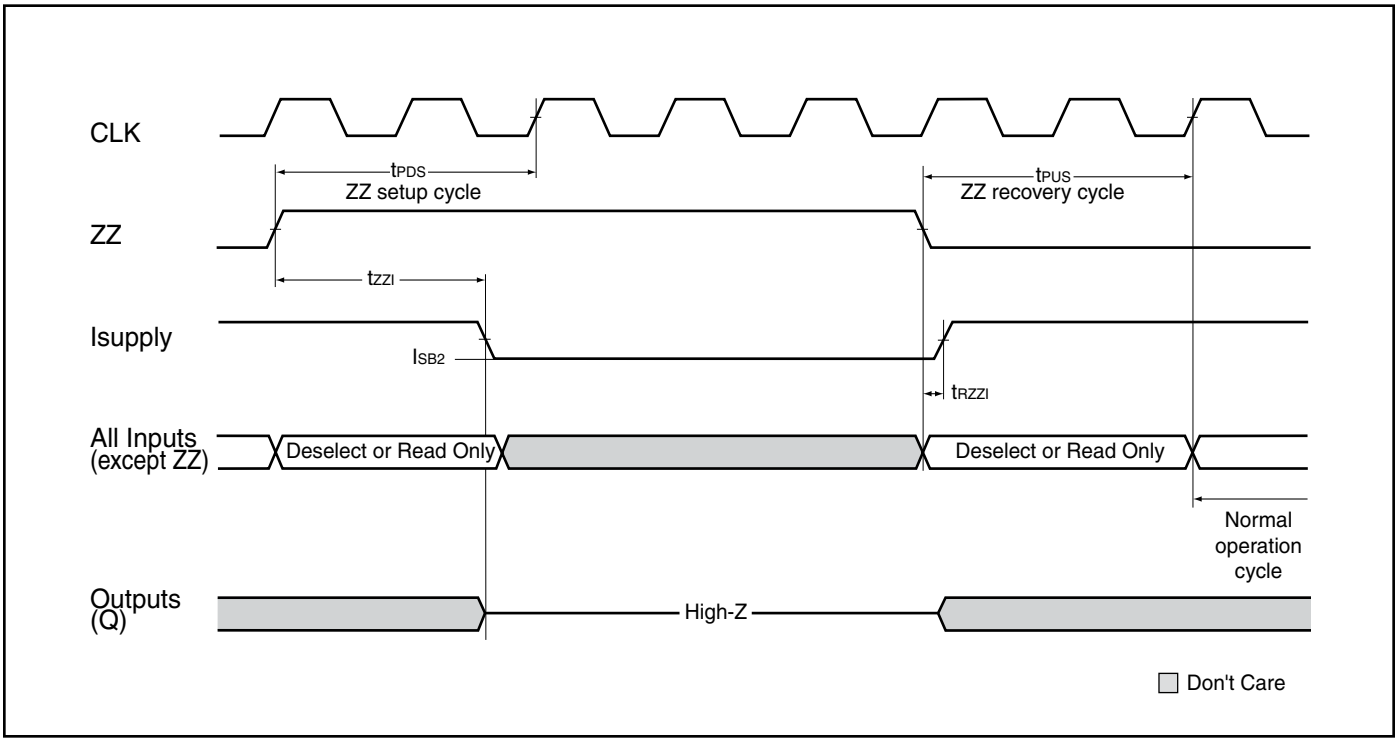
Symbol	Parameter	-250 Min.	-250 Max.	-200 Min.	-200 Max.	Unit
fmax	Clock Frequency	—	250	—	200	MHz
t_{KC}	Cycle Time	4.0	—	5	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	ns
t_{KL}	Clock Low Time	1.7	—	2	—	ns
t_{KQ}	Clock Access Time	—	2.6	—	3.1	ns
t_{KQX}[2]	Clock High to Output Invalid	0.8	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0.8	—	1	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	2.6	—	3.0	ns
t_{OEQ}	Output Enable to Output Valid	—	2.8	—	3.1	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	2.6	—	3.0	ns
t_{AS}	Address Setup Time	1.2	—	1.4	—	ns
t_{WS}	Read/Write Setup Time	1.2	—	1.4	—	ns
t_{CES}	Chip Enable Setup Time	1.2	—	1.4	—	ns
t_{SE}	Clock Enable Setup Time	1.2	—	1.4	—	ns
t_{ADVS}	Address Advance Setup Time	1.2	—	1.4	—	ns
t_{DS}	Data Setup Time	1.2	—	1.4	—	ns
t_{AH}	Address Hold Time	0.3	—	0.4	—	ns
t_{HE}	Clock Enable Hold Time	0.3	—	0.4	—	ns
t_{WH}	Write Hold Time	0.3	—	0.4	—	ns
t_{CEH}	Chip Enable Hold Time	0.3	—	0.4	—	ns
t_{ADVH}	Address Advance Hold Time	0.3	—	0.4	—	ns
t_{DH}	Data Hold Time	0.3	—	0.4	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

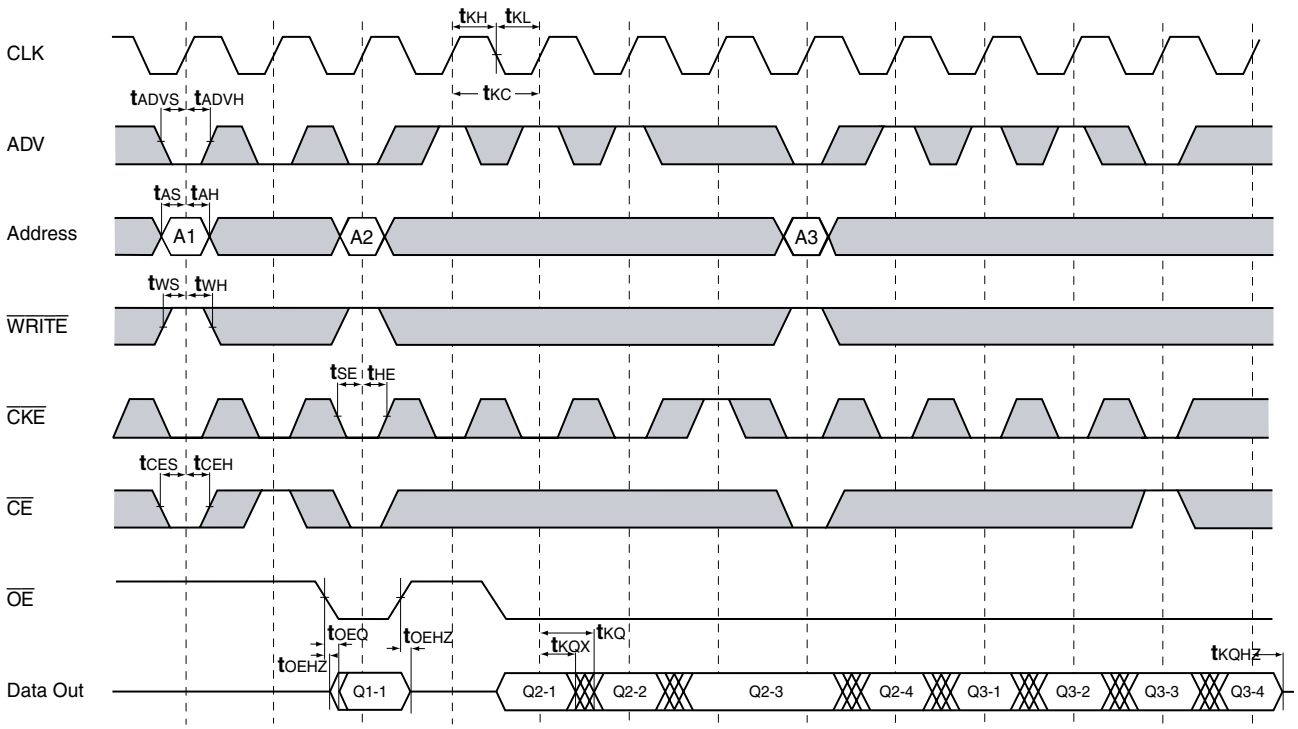
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SLEEP MODE	ZZ ≥ V_{IH}		35	mA
t_{PDS}	ZZ active to input ignored		2		cycle
t_{PUS}	ZZ inactive to input sampled		2		cycle
t_{ZZI}	ZZ active to SLEEP current		2		cycle
t_{RZZI}	ZZ inactive to exit SLEEP current		0		ns

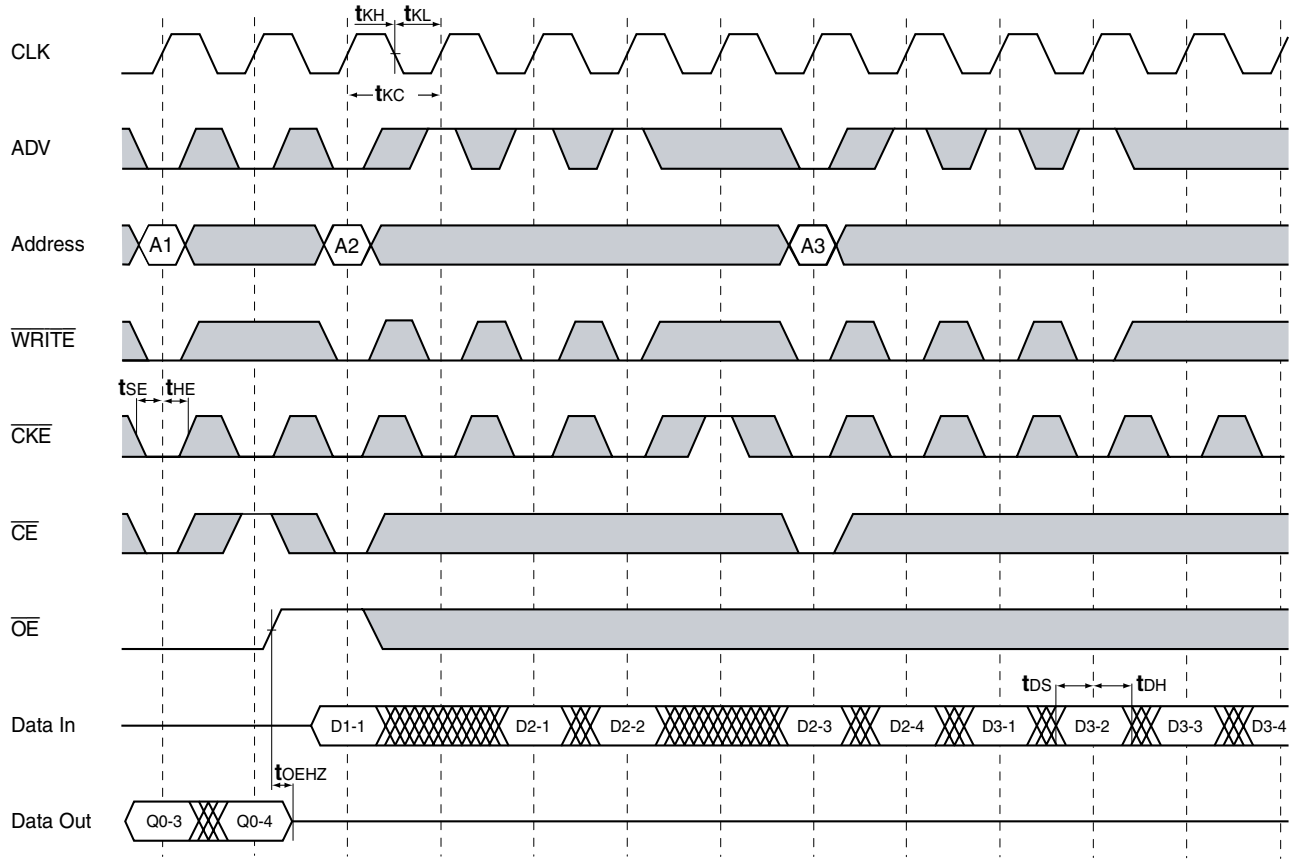
SLEEP MODE TIMING



READ CYCLE TIMING

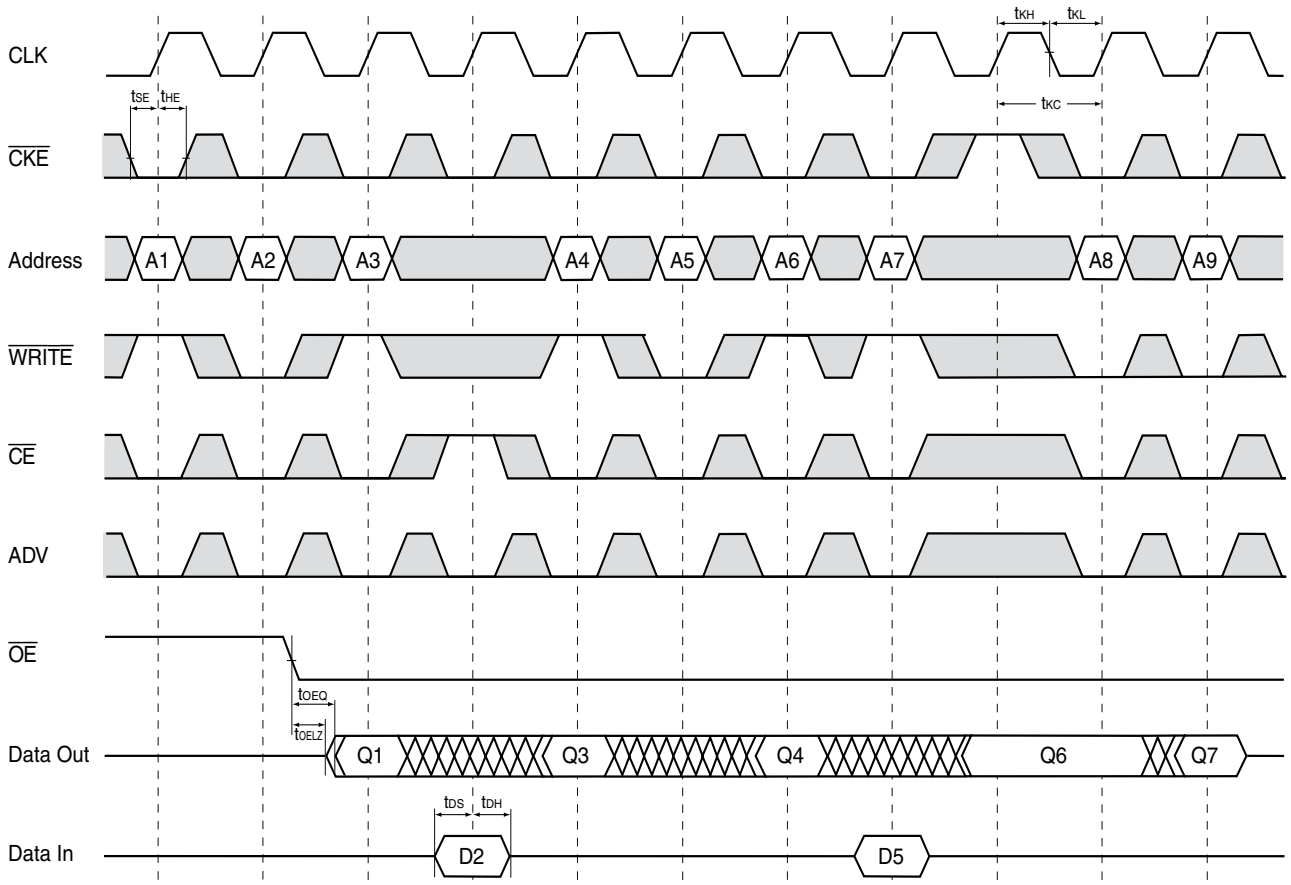


WRITE CYCLE TIMING

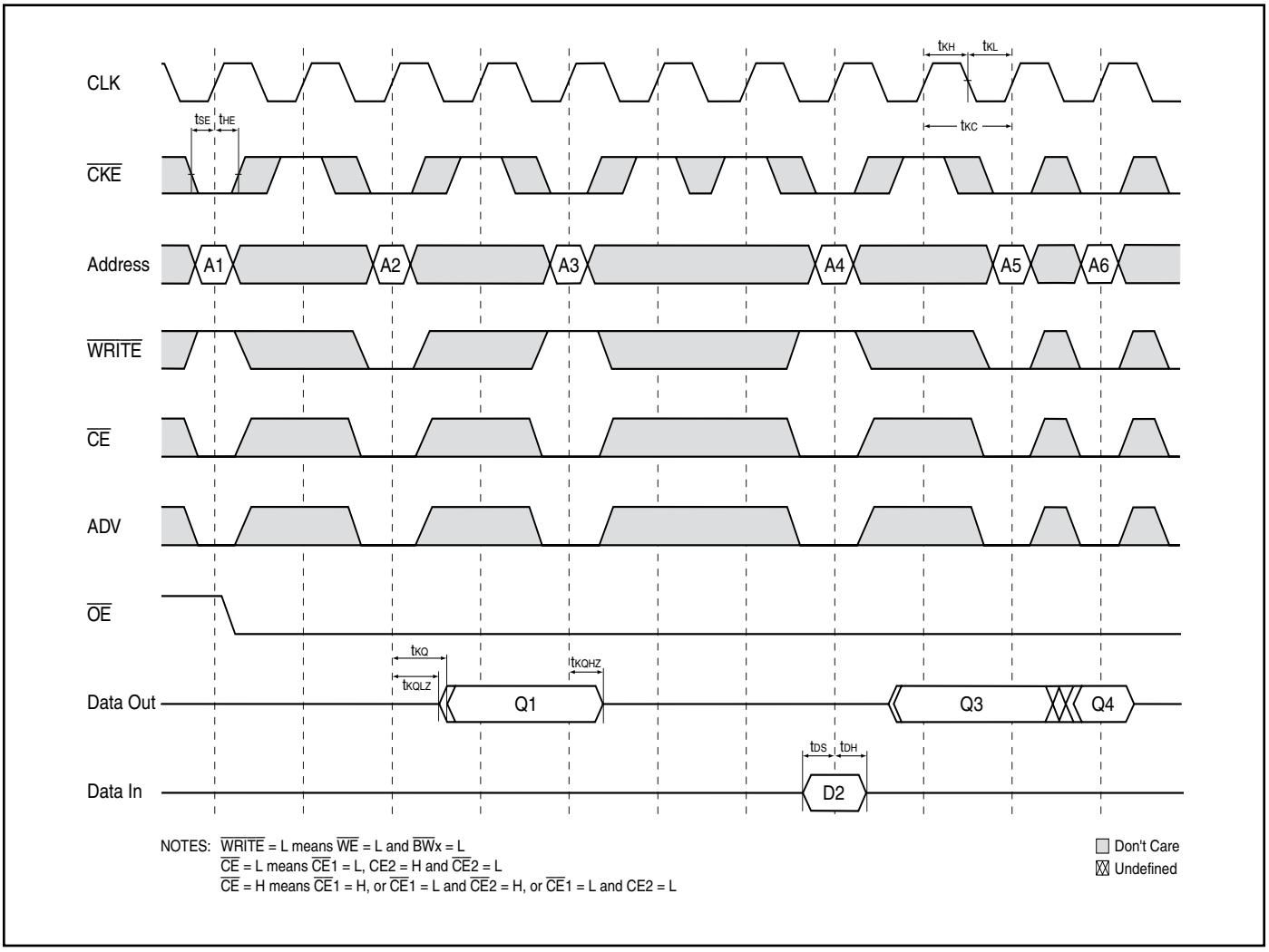


NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L and $\overline{BW}$x = L
$\overline{WE}$ = L and $\overline{BW}$X = L
$\overline{CE}$ = L means $\overline{CE}$1 = L, CE2 = H and $\overline{CE}$2 = L
$\overline{CE}$ = H means $\overline{CE}$1 = H, or $\overline{CE}$1 = L and $\overline{CE}$2 = H, or $\overline{CE}$1 = L and CE2 = L

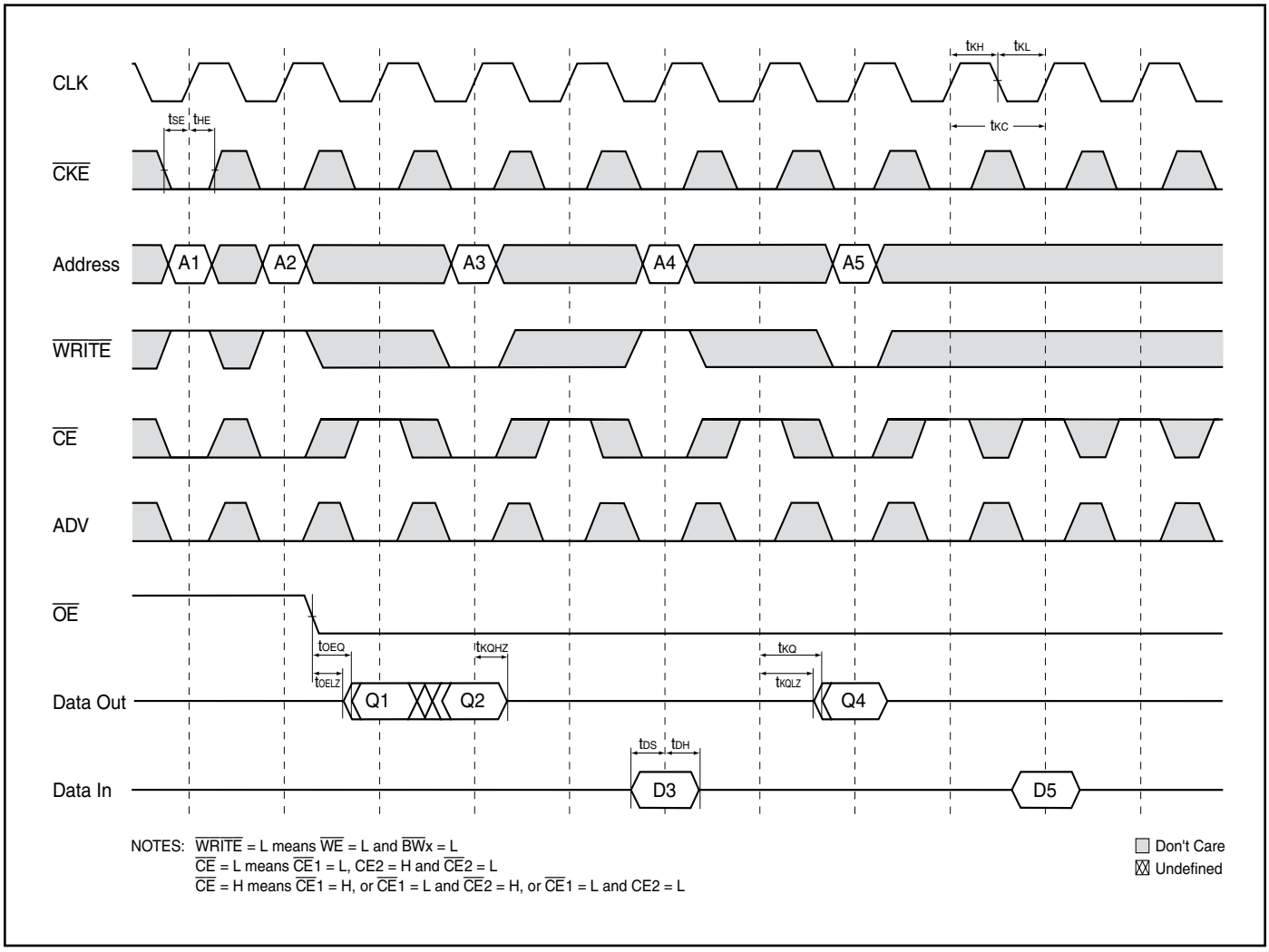
SINGLE READ/WRITE CYCLE TIMING



$\overline{CKE}$ OPERATION TIMING



$\overline{CE}$ OPERATION TIMING



ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)
Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
	128Kx32	
250	IS61NLP12832B-250TQ	100 TQFP
	IS61NLP12832B-250B3	165 PBGA
	IS61NLP12832B-250B2	119 PBGA
200	IS61NLP12832B-200TQ	100 TQFP
	IS61NLP12832B-200B3	165 PBGA
	IS61NLP12832B-200B2	119 PBGA
	128Kx36	
250	IS61NLP12836B-250TQ	100 TQFP
	IS61NLP12836B-250B3	165 PBGA
	IS61NLP12836B-250B2	119 PBGA
200	IS61NLP12836B-200TQ	100 TQFP
	IS61NLP12836B-200B3	165 PBGA
	IS61NLP12836B-200B2	119 PBGA
	256Kx18	
250	IS61NLP25618A-250TQ	100 TQFP
	IS61NLP25618A-250B3	165 PBGA
	IS61NLP25618A-250B2	119 PBGA
200	IS61NLP25618A-200TQ	100 TQFP
	IS61NLP25618A-200B3	165 PBGA
	IS61NLP25618A-200B2	119 PBGA

ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)
Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
	128Kx32	
250	IS61NLP12832B-250TQI	100 TQFP
	IS61NLP12832B-250B3I	165 PBGA
	IS61NLP12832B-250B2I	119 PBGA
200	IS61NLP12832B-200TQI	100 TQFP
	IS61NLP12832B-200TQLI	100 TQFP, Lead-free
	IS61NLP12832B-200B3I	165 PBGA
	IS61NLP12832B-200B2I	119 PBGA
	128Kx36	
250	IS61NLP12836B-250TQI	100 TQFP
	IS61NLP12836B-250B3I	165 PBGA
	IS61NLP12836B-250B2I	119 PBGA
200	IS61NLP12836B-200TQI	100 TQFP
	IS61NLP12836B-200TQLI	100 TQFP, Lead-free
	IS61NLP12836B-200B3I	165 PBGA
	IS61NLP12836B-200B2I	119 PBGA
	IS61NLP12836B-200B2LI	119 PBGA, Lead-free
	256Kx18	
250	IS61NLP25618A-250TQI	100 TQFP
	IS61NLP25618A-250B3I	165 PBGA
	IS61NLP25618A-250B2I	119 PBGA
200	IS61NLP25618A-200TQI	100 TQFP
	IS61NLP25618A-200TQLI	100 TQFP, Lead-free
	IS61NLP25618A-200B3I	165 PBGA
	IS61NLP25618A-200B3LI	165 PBGA, Lead-free
	IS61NLP25618A-200B2I	119 PBGA

ORDERING INFORMATION (V_{DD} = 2.5V/V_{DDQ} = 2.5V)

Commercial Range: 0°C to +70°C

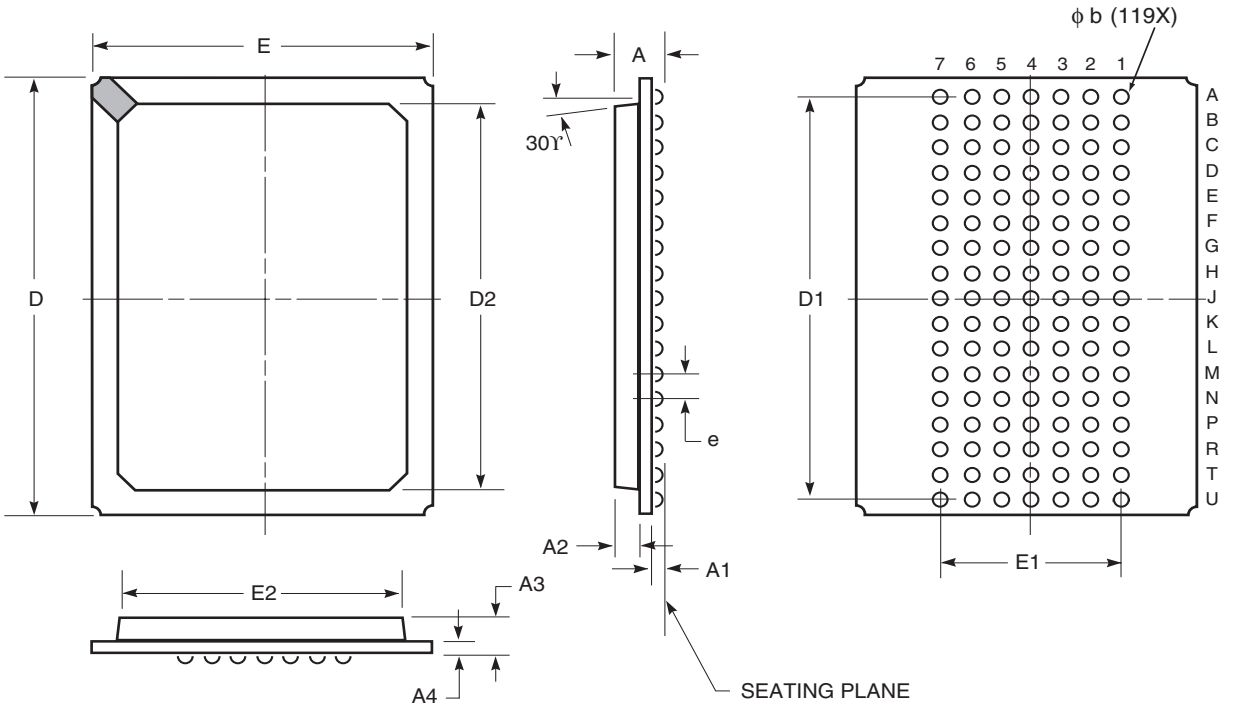
Access Time	Order Part Number	Package
	128Kx36	
250	IS61NVP12836B-250TQ	100 TQFP
	IS61NVP12836B-250B3	165 PBGA
	IS61NVP12836B-250B2	119 PBGA
200	IS61NVP12836B-200TQ	100 TQFP
	IS61NVP12836B-200B3	165 PBGA
	IS61NVP12836B-200B2	119 PBGA
	256Kx18	
250	IS61NVP25618A-250TQ	100 TQFP
	IS61NVP25618A-250B3	165 PBGA
	IS61NVP25618A-250B2	119 PBGA
200	IS61NVP25618A-200TQ	100 TQFP
	IS61NVP25618A-200B3	165 PBGA
	IS61NVP25618A-200B2	119 PBGA

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
	128Kx36	
250	IS61NVP12836B-250TQI	100 TQFP
	IS61NVP12836B-250B3I	165 PBGA
	IS61NVP12836B-250B2I	119 PBGA
200	IS61NVP12836B-200TQI	100 TQFP
	IS61NVP12836B-200B3I	165 PBGA
	IS61NVP12836B-200B2I	119 PBGA
	256Kx18	
250	IS61NVP25618A-250TQI	100 TQFP
	IS61NVP25618A-250B3I	165 PBGA
	IS61NVP25618A-250B2I	119 PBGA
200	IS61NVP25618A-200TQI	100 TQFP
	IS61NVP25618A-200B3I	165 PBGA
	IS61NVP25618A-200B2I	119 PBGA

PACKAGING INFORMATION

Plastic Ball Grid Array
Package Code: B (119-pin)



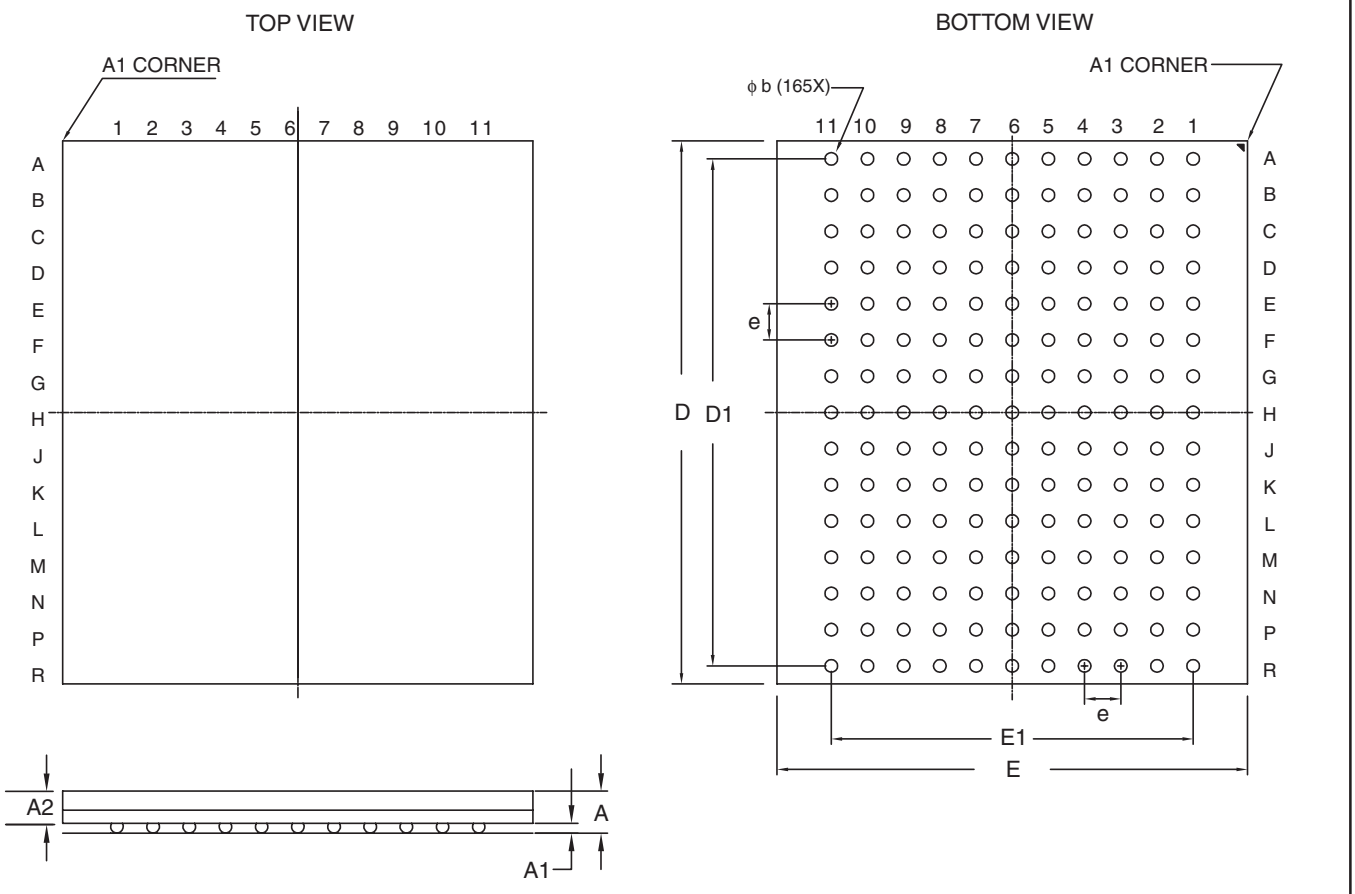
	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
N0. Leads		**119**		
A	—	2.41	—	0.095
A1	0.50	0.70	0.020	0.028
A2	0.80	1.00	0.032	0.039
A3	1.30	1.70	0.051	0.067
A4	0.56 BSC		0.022 BSC	
b	0.60	0.90	0.024	0.035
D	21.80	22.20	0.858	0.874
D1	20.32 BSC		0.800 BSC	
D2	19.40	19.60	0.764	0.772
E	13.80	14.20	0.543	0.559
E1	7.62 BSC		0.300 BSC	
E2	11.90	12.10	0.469	0.476
e	1.27 BSC		0.050 BSC	

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Ball Grid Array
Package Code: B (165-pin)



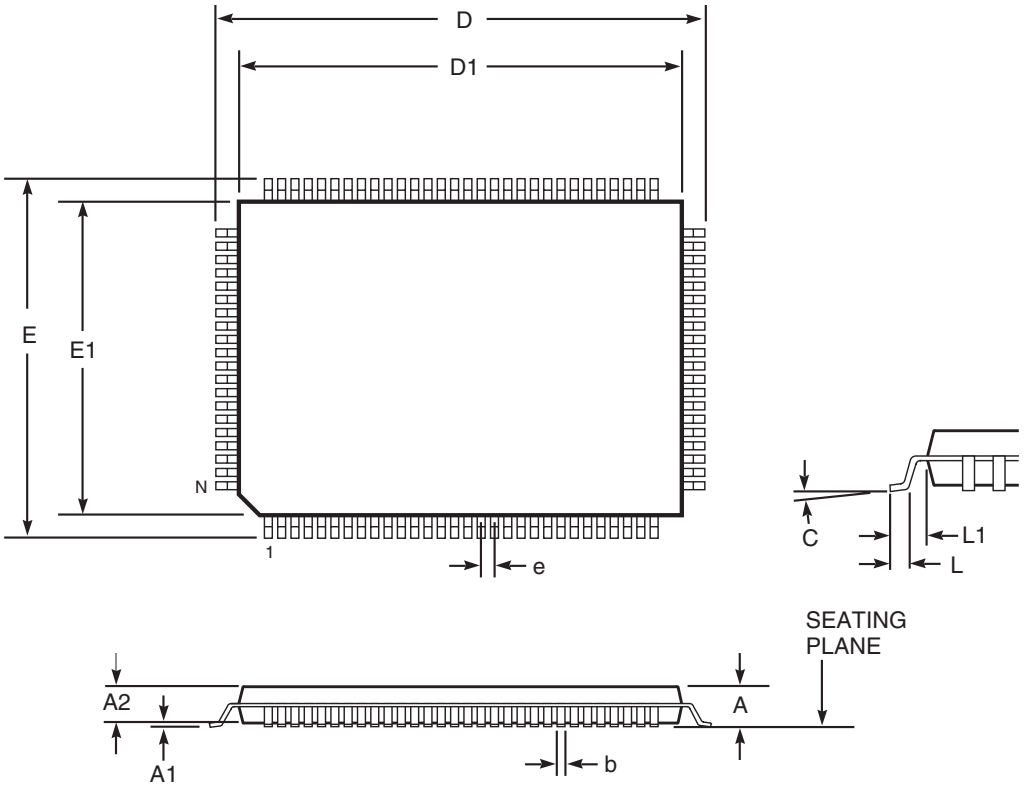
BGA - 13mm x 15mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
N0. Leads		**165**			**165**	
A	—	—	1.20	—	—	0.047
A1	0.25	0.33	0.40	0.010	0.013	0.016
A2	—	0.79	—	—	0.031	—
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	—	1.00	—	—	0.039	—
b	0.40	0.45	0.50	0.016	0.018	0.020

Notes:
1. Controlling dimensions are in millimeters.

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flat Pack (TQ)								
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads (N)	100				128			
A	—	1.60	—	0.063	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°	0°	7°	0°	7°

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.

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