

## Inverter Grade Thyristors (PUK Version), 620 A



TO-200AB (E-PUK)

### FEATURES

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- International standard case TO-200AB (E-PUK)
- High surge current capability
- Low thermal impedance
- High speed performance
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### PRODUCT SUMMARY

Package	TO-200AB (E-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	620 A
$V_{DRM}/V_{RRM}$	400 V, 800 V, 1000 V, 1200 V
$V_{TM}$	2.16 V
$I_{TSM}$ at 50 Hz	7950 A
$I_{TSM}$ at 60 Hz	8320 A
$I_{GT}$	200 mA
$T_C/T_{hs}$	55 °C

### TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

### MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		620	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		1180	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	7950	A
	60 Hz	8320	
$I^2t$	50 Hz	316	kA <sup>2</sup> s
	60 Hz	289	
$V_{DRM}/V_{RRM}$		400 to 1200	V
$t_q$	Range	10 to 30	µs
$T_J$		-40 to 125	°C

#### Note

- $t_q = 10 \mu s$  to  $20 \mu s$  for 400 V to 800 V devices
- $t_q = 15 \mu s$  to  $30 \mu s$  for 1000 V to 1200 V devices



**ELECTRICAL SPECIFICATIONS**

<b>VOLTAGE RATINGS</b>				
TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST303C..C	04	400	500	50
	08	800	900	
	10	1000	1100	
	12	1200	1300	

<b>CURRENT CARRYING CAPABILITY</b>							
FREQUENCY							UNITS
50 Hz	1314	1130	2070	1940	6930	6270	A
400 Hz	1260	1040	2190	1880	3440	2960	
1000 Hz	900	700	1900	1590	1850	1540	
2500 Hz	340	230	910	710	740	560	
Recovery voltage $V_r$	50		50		50		V
Voltage before turn-on $V_d$	$V_{DRM}$		$V_{DRM}$		$V_{DRM}$		
Rise of on-state current $di/dt$	50		-		-		A/ $\mu$ s
Heatsink temperature	40	55	40	55	40	55	$^{\circ}$ C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		$\Omega/\mu$ F

<b>ON-STATE CONDUCTION</b>						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180 $^{\circ}$ conduction, half sine wave double side (single side) cooled			620 (230)	A
					55 (85)	$^{\circ}$ C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 $^{\circ}$ C heatsink temperature double side cooled			1180	
Maximum peak, one half cycle, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	7950	A
		t = 8.3 ms			8320	
		t = 10 ms	100 % $V_{RRM}$ reapplied		6690	
		t = 8.3 ms			7000	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied		316	$kA^2s$
		t = 8.3 ms			289	
		t = 10 ms	100 % $V_{RRM}$ reapplied		224	
		t = 8.3 ms			204	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			3160	$kIA^2\sqrt{s}$
Maximum peak on-state voltage	$V_{TM}$	$I_{TM} = 1255$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse			2.16	V
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			1.44	
High level value of threshold voltage	$V_{T(TO)2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			1.48	
Low level value of forward slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.57	m $\Omega$
High level value of forward slope resistance	$r_{t2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum			0.56	
Maximum holding current	$I_H$	$T_J = 25$ $^{\circ}$ C, $I_T > 30$ A			600	mA
Typical latching current	$I_L$	$T_J = 25$ $^{\circ}$ C, $V_A = 12$ V, $R_a = 6$ $\Omega$ , $I_G = 1$ A			1000	



<b>SWITCHING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	dl/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times dl/dt$	1000	A/ $\mu$ s
Typical delay time	$t_d$	$T_J = 25^\circ\text{C}$ , $V_{DM} = \text{Rated } V_{DRM}$ , $I_{TM} = 50 \text{ A DC}$ , $t_p = 1 \mu\text{s}$ Resistive load, gate pulse: 10 V, 5 $\Omega$ source	0.83	$\mu$ s
Maximum turn-off time <sup>(1)</sup>	minimum	$T_J = T_J$ maximum, $I_{TM} = 550 \text{ A}$ , commutating $dl/dt = 40 \text{ A}/\mu\text{s}$ $V_R = 50 \text{ V}$ , $t_p = 500 \mu\text{s}$ , $dV/dt$ : See table in device code	10	
	maximum		30	

**Note**

<sup>(1)</sup>  $t_q = 10 \mu\text{s}$  to  $20 \mu\text{s}$  for 400 V to 800 V devices;  $t_q = 15 \mu\text{s}$  to  $30 \mu\text{s}$  for 1000 V to 1200 V devices

<b>BLOCKING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % $V_{DRM}$ , higher value available on request	500	V/ $\mu$ s
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied	50	mA

<b>TRIGGERING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $f = 50 \text{ Hz}$ , $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5 \text{ ms}$	10	A
Maximum peak positive gate voltage	+ $V_{GM}$		20	V
Maximum peak negative gate voltage	- $V_{GM}$		5	
Maximum DC gate current required to trigger	$I_{GT}$	$T_J = 25^\circ\text{C}$ , $V_A = 12 \text{ V}$ , $R_a = 6 \Omega$	200	mA
Maximum DC gate voltage required to trigger	$V_{GT}$		3	V
Maximum DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied	20	mA
Maximum DC gate voltage not to trigger	$V_{GD}$		0.25	V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	$T_J$		-40 to 125	$^\circ\text{C}$
Maximum storage temperature range	$T_{Stg}$		-40 to 150	
Maximum thermal resistance, junction to heatsink	$R_{thJ-hs}$	DC operation single side cooled	0.09	K/W
		DC operation double side cooled	0.04	
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$	DC operation single side cooled	0.020	
		DC operation double side cooled	0.010	
Mounting force, $\pm 10 \%$			9800 (1000)	N (kg)
Approximate weight			83	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (E-PUK)	



<b><math>\Delta R_{thJ-hs}</math> CONDUCTION</b>						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.010	0.010	0.007	0.007	T <sub>J</sub> = T <sub>J</sub> max.	K/W
120°	0.012	0.012	0.012	0.013		
90°	0.015	0.015	0.016	0.017		
60°	0.022	0.022	0.023	0.023		
30°	0.036	0.036	0.036	0.037		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJ-hs}$  when devices operate at different conduction angles than DC

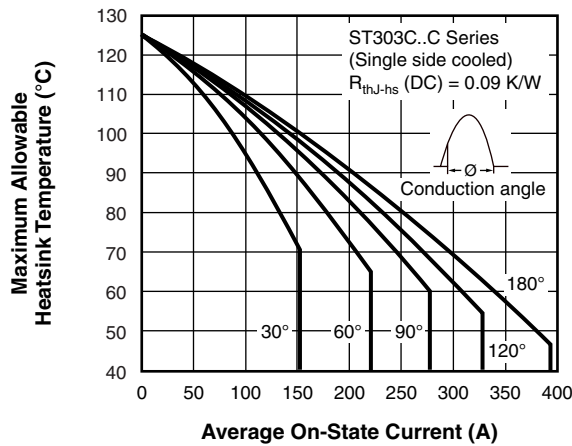


Fig. 1 - Current Ratings Characteristics

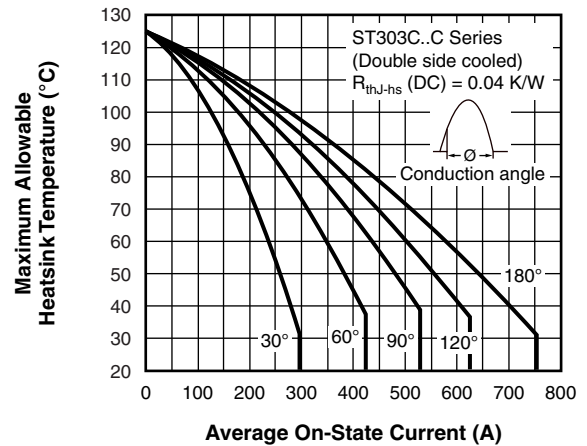


Fig. 3 - Current Ratings Characteristics

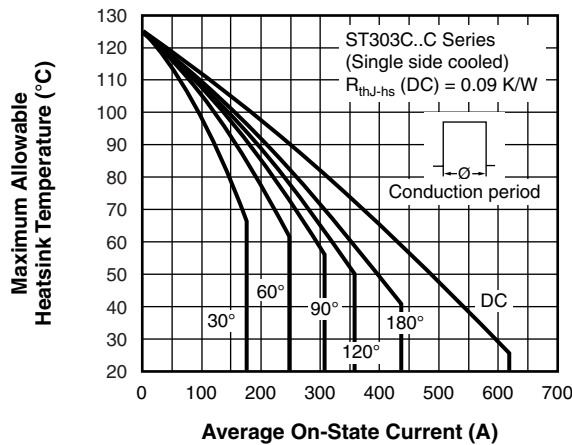


Fig. 2 - Current Ratings Characteristics

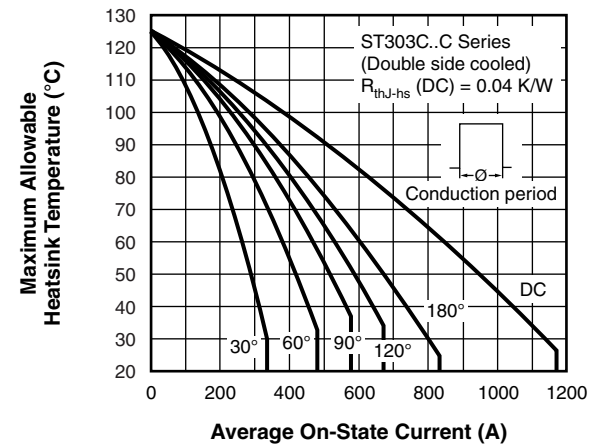


Fig. 4 - Current Ratings Characteristics

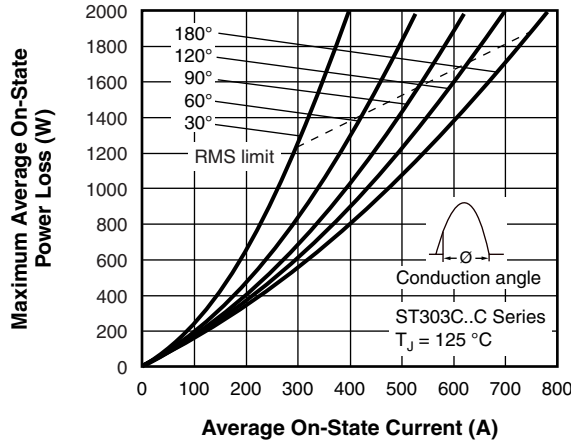


Fig. 5 - On-State Power Loss Characteristics

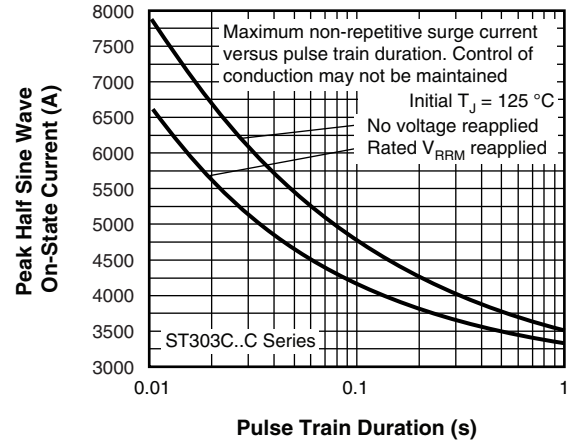


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

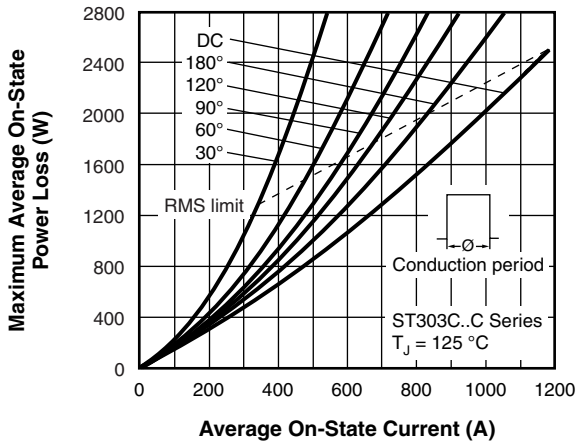


Fig. 6 - On-State Power Loss Characteristics

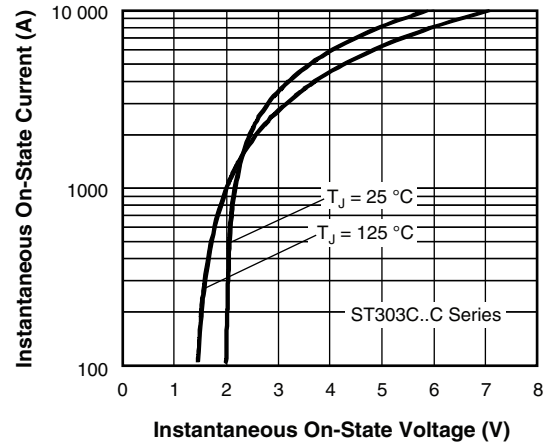


Fig. 9 - On-State Voltage Drop Characteristics

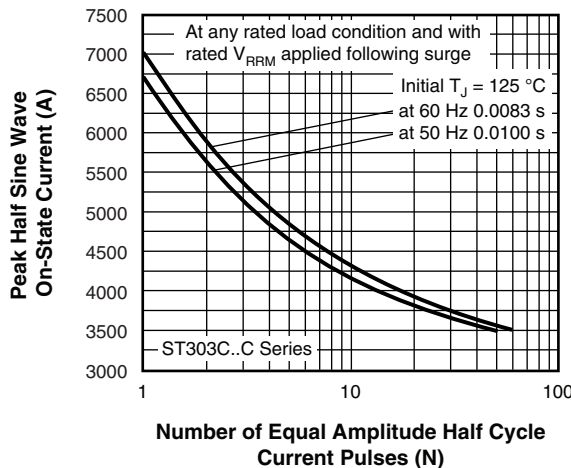


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

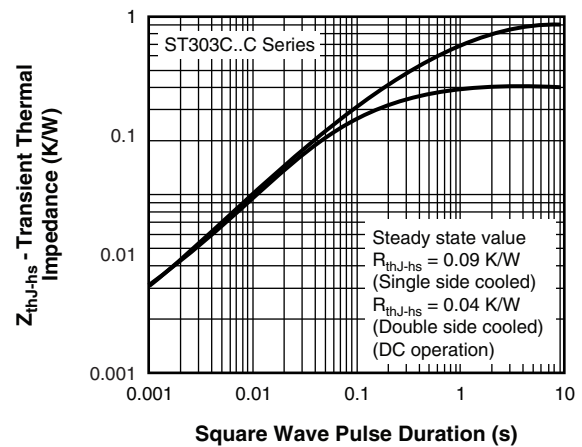


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

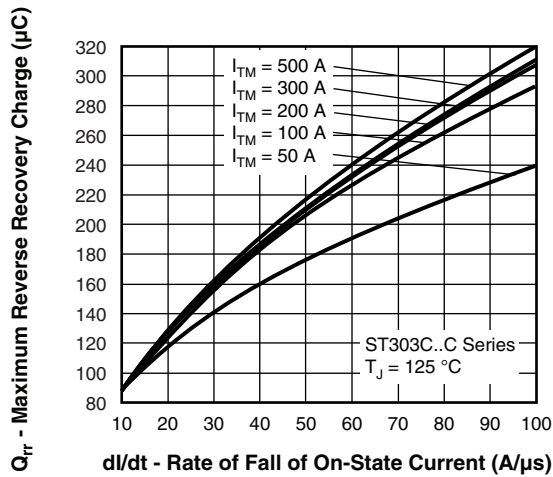


Fig. 11 - Reverse Recovered Charge Characteristics

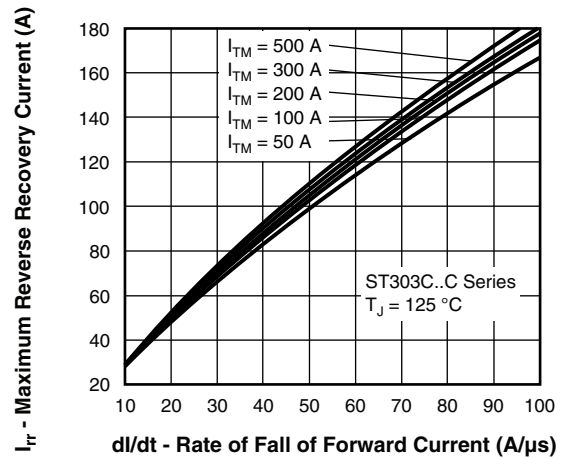


Fig. 12 - Reverse Recovered Current Characteristics

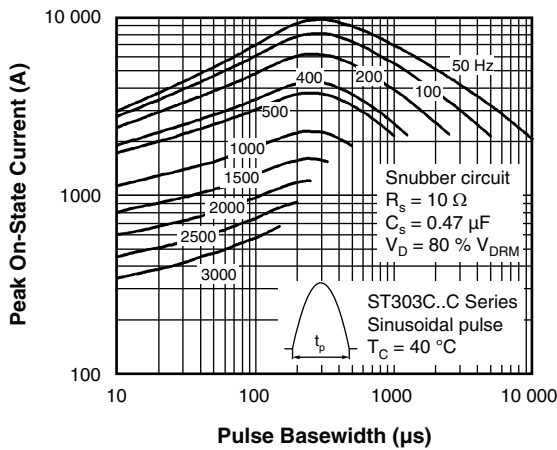


Fig. 13 - Frequency Characteristics

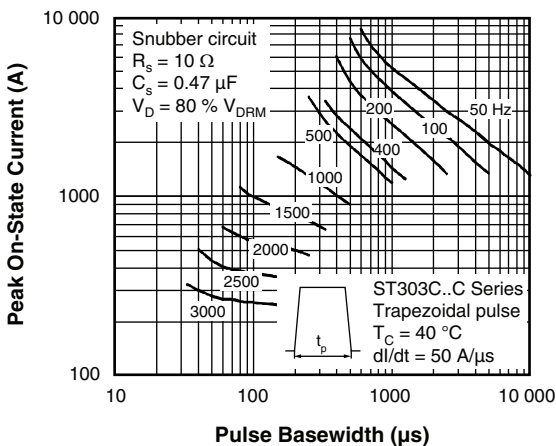
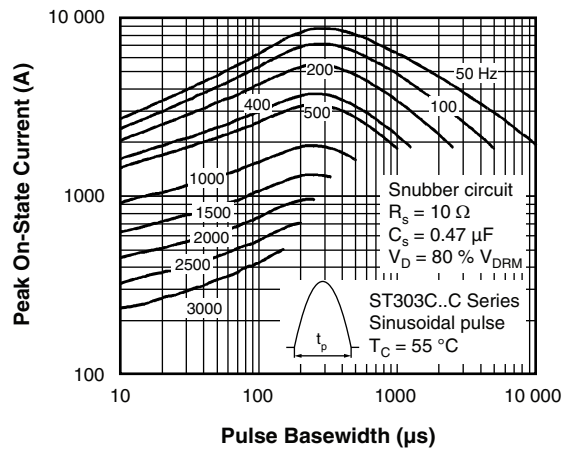
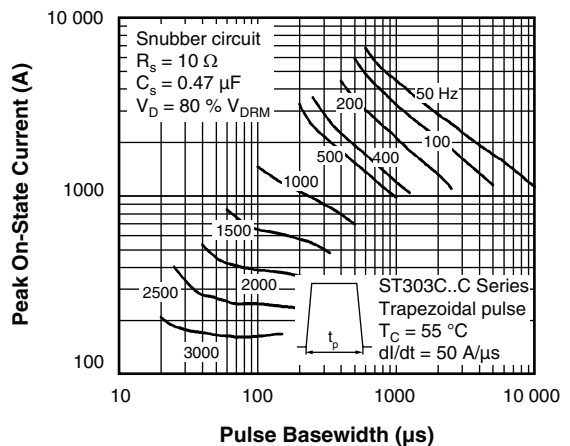


Fig. 14 - Frequency Characteristics



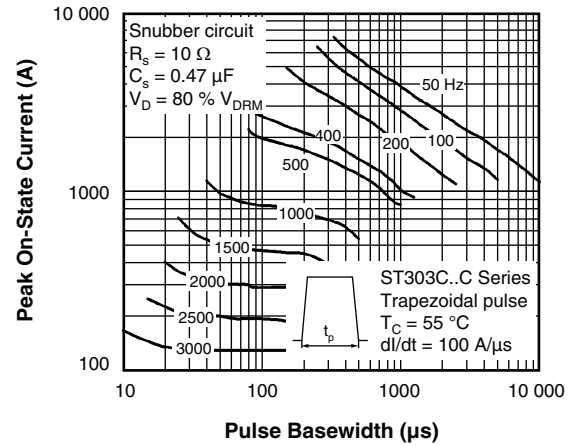
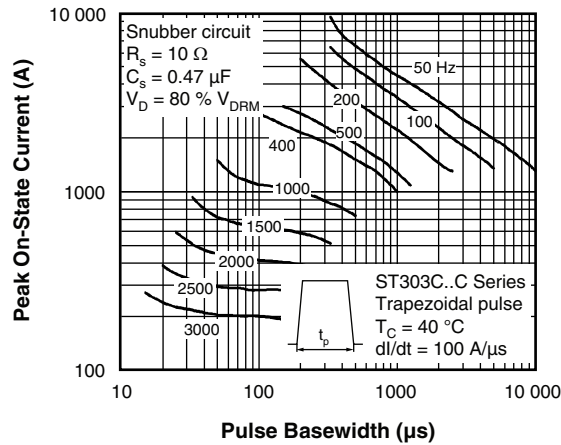


Fig. 15 - Frequency Characteristics

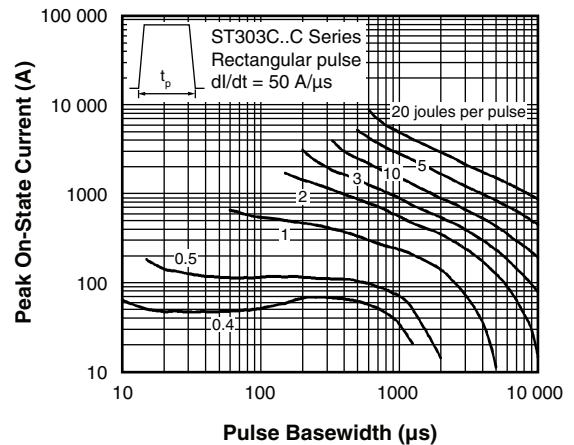
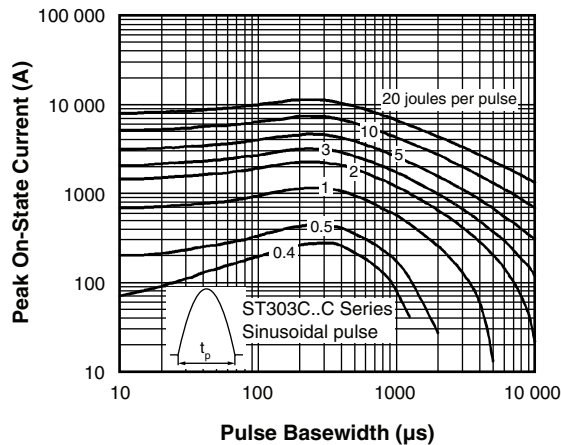


Fig. 16 - Maximum On-State Energy Power Loss Characteristics

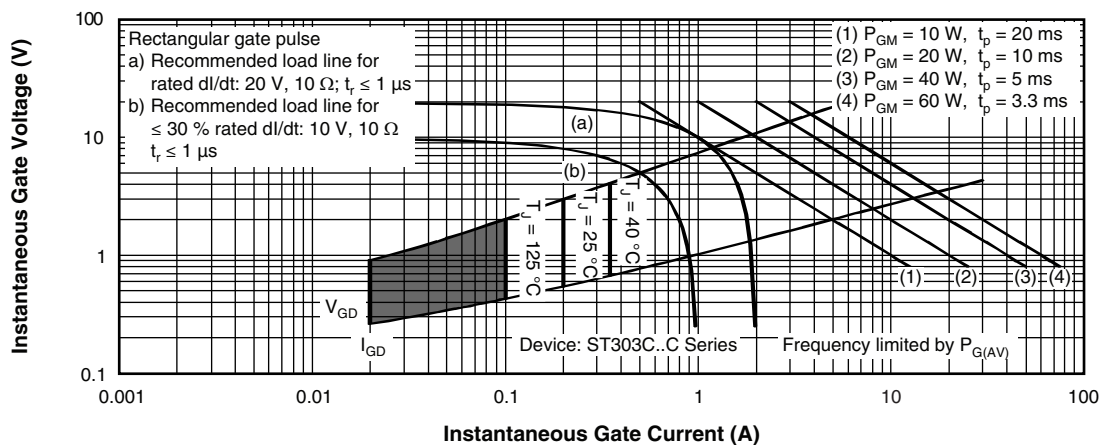


Fig. 17 - Gate Characteristics



**ORDERING INFORMATION TABLE**

Device code	<b>VS-</b>	<b>ST</b>	<b>30</b>	<b>3</b>	<b>C</b>	<b>12</b>	<b>C</b>	<b>H</b>	<b>K</b>	<b>1</b>	<b>-</b>
	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = Fast turn-off
- 5** - C = Ceramic PUK
- 6** - Voltage code x 100 =  $V_{RRM}$   
(see Voltage Ratings table)
- 7** - C = PUK case TO-200AB (E-PUK)
- 8** - Reapplied dV/dt code (for  $t_q$  test condition)
- 9** -  $t_q$  code
- 10** - 0 = Eyelet terminals  
(gate and aux. cathode unsoldered leads)  
1 = Fast-on terminals  
(gate and aux. cathode unsoldered leads)  
2 = Eyelet terminals  
(gate and aux. cathode soldered leads)  
3 = Fast-on terminals  
(gate and aux. cathode soldered leads)
- 11** - Critical dV/dt:
  - None = 500 V/ $\mu$ s (standard value)
  - L = 1000 V/ $\mu$ s (special selection)

dV/dt - $t_q$ combinations available						
		dV/dt (V/ $\mu$ s)				
		20	50	100	200	400
$t_q$ ( $\mu$ s) up to 800 V	10	CN	DN	EN	<b>FN*</b>	HN
	12	CM	DM	EM	FM	HM
	15	CL	DL	EL	<b>FL*</b>	HL
	20	CK	DK	EK	<b>FK*</b>	HK
$t_q$ ( $\mu$ s) only for 1000 V/1200 V	15	CL	-	-	-	-
	18	CP	DP	-	-	-
	20	CK	DK	EK	<b>FK*</b>	HK
	25	CJ	DJ	EJ	<b>FJ*</b>	HJ
	30	-	DH	EH	FH	HH

\* Standard part number.  
All other types available only on request.

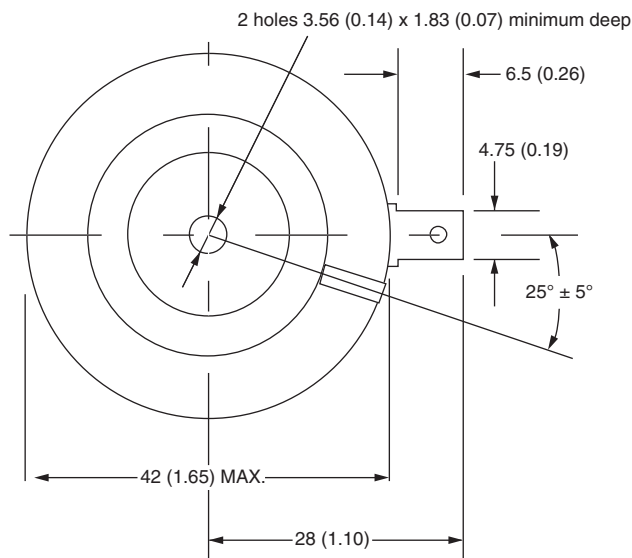
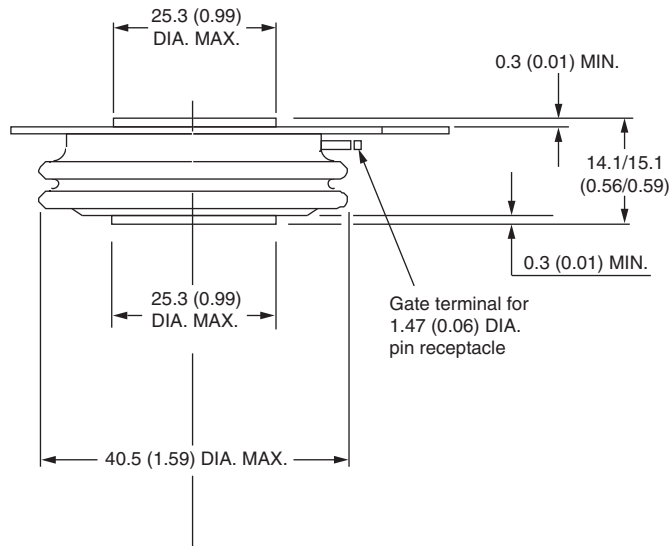
LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95075">http://www.vishay.com/doc?95075</a>



## TO-200AB (E-PUK)

**DIMENSIONS** in millimeters (inches)

Anode to gate  
 Creepage distance: 11.18 (0.44) minimum  
 Strike distance: 7.62 (0.30) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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