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74LCX760

Low Voltage Buffer/Line Driver with 5V Tolerant Inputs and Open Drain Outputs

General Description

The LCX760 is the Open Drain version of the LCX244. The LCX760 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX760 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX760 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- Open drain version of the LCX244
- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 8.0 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- 24 mA output drive ($V_{CC} = 3.0V$)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD performance:
Human body model > 2000V
Machine model > 200V

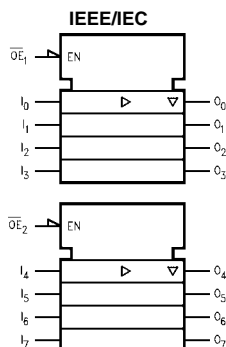
Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

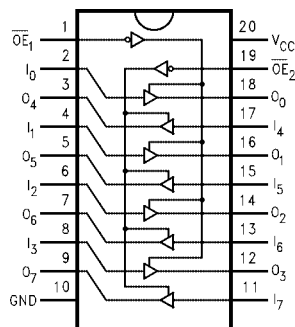
Order Number	Package Number	Package Description
74LCX760WWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX760SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX760MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX760MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



74LCX760 Low Voltage Buffer/Line Driver with 5V Tolerant Inputs and Open Drain Outputs

Pin Descriptions

Pin Names	Description
$\overline{\text{OE}}_1, \overline{\text{OE}}_2$	3-STATE Output Enable Inputs
$\text{I}_0\text{--}\text{I}_7$	Inputs
$\text{O}_0\text{--}\text{O}_7$	Outputs

Truth Tables

Inputs		Outputs
$\overline{\text{OE}}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{\text{OE}}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Absolute Maximum Ratings ^(Note 2)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Sink Current	50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	Operating Data Retention	2.0 3.6 3.6	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage	0	5.5	V
I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V V _{CC} = 2.7V – 3.0V V _{CC} = 2.3V – 2.7V	24 12 8	mA
T _A	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = −40°C to +85°C		Units
			(V)	Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0		0.2 0.6 0.4 0.4 0.55	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND 3.6V ≤ V _I , V _O ≤ 5.5V (Note 5)	2.3 – 3.6 2.3 – 3.6		10 ±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} −0.6V	2.3 – 3.6		500	μA
I _{OHZ}	Off State Current	V _O = 5.5	2 - 3.6		10	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PZL}	Propagation Delay	0.5	8.0	0.5	9.0	0.5	10.0	ns
t _{PLZ}	Data to Output	0.5	7.0	0.5	8.0	0.5	8.4	
t _{PZL}	Output Enable Time OE _n to Out	0.5	8.0	0.5	9.0	0.5	10.0	ns
t _{PLZ}	Output Disable Time OE _n to Out	0.5	7.0	0.5	8.0	0.5	8.4	ns
t _{OSHL}	Output to Output Skew		1.0					ns
t _{OSLH}	(Note 6)		1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^{\circ}\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	0.8 0.6	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	-0.8 -0.6	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	10	pF

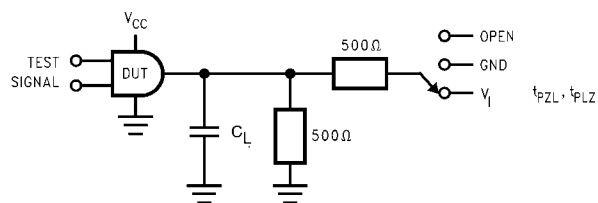


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

Test	Switch
t _{PZL} , t _{PLZ}	6V at V _{CC} = 3.3 ± 0.3V V _{CC} x 2 at V _{CC} = 2.5 ± 0.2V

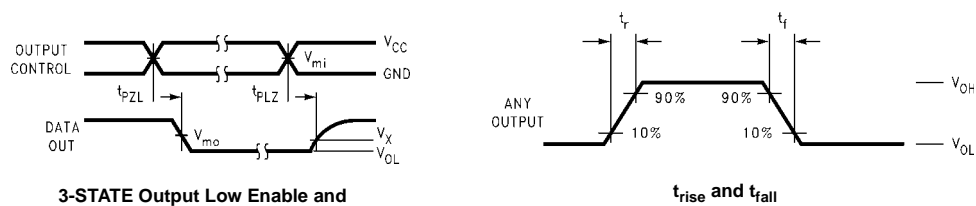


FIGURE 2. Waveforms
(Input Characteristics; $f = 1\text{MHz}$, $t_r = t_f = 3\text{ns}$)

Symbol	V _{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V _{mi}	1.5V	1.5V	V _{CC} /2
V _{mo}	1.5V	1.5V	V _{CC} /2
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V
V _y	V _{OH} - 0.3V	V _{OH} - 0.3V	V _{OH} - 0.15V

Schematic Diagram Generic for LCX Family (output pull-up circuitry is not applicable to open drain versions)

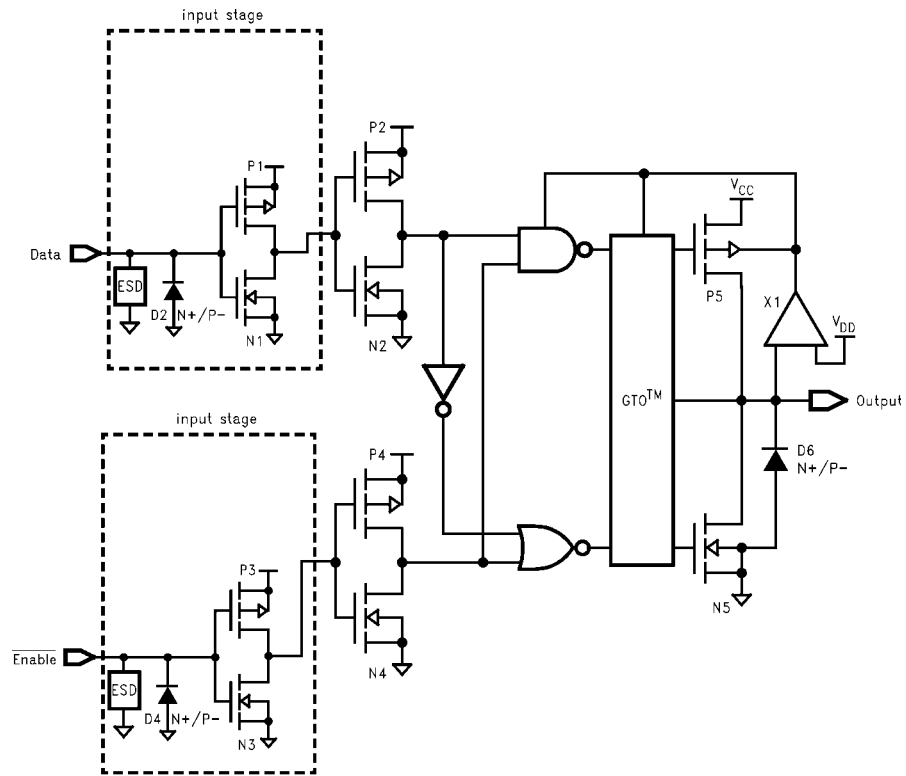
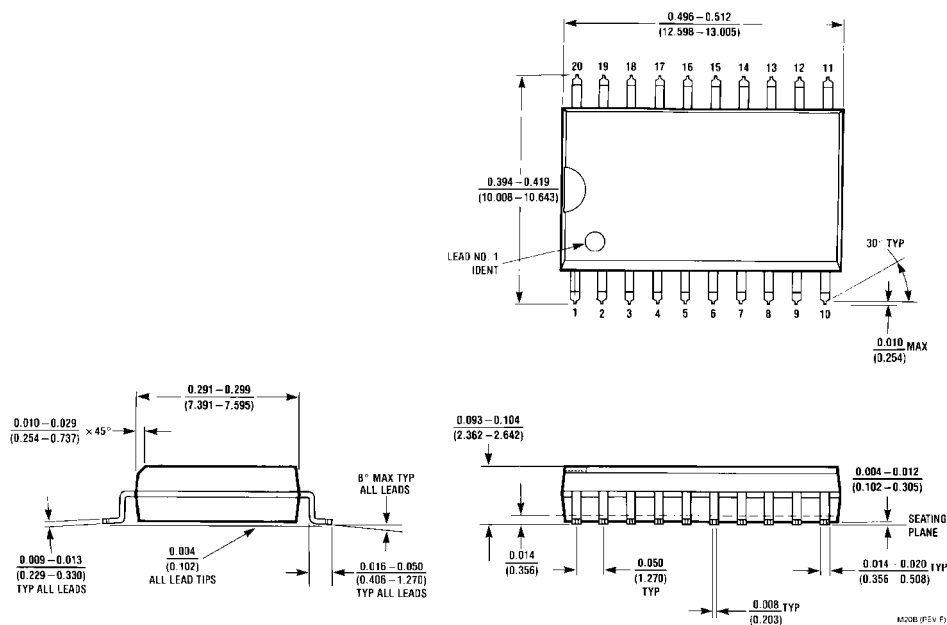
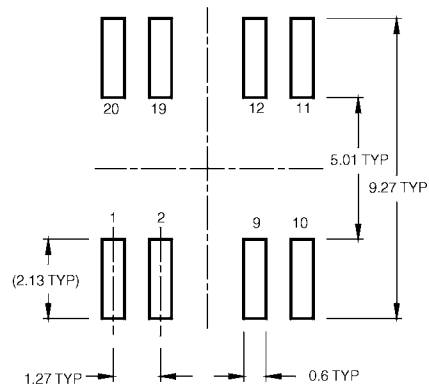


FIGURE 3.

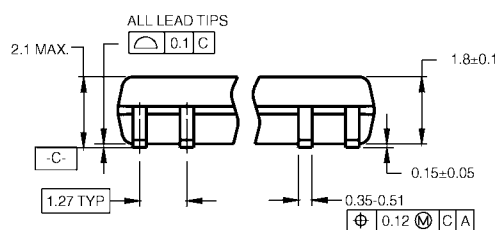
Physical Dimensions inches (millimeters) unless otherwise noted



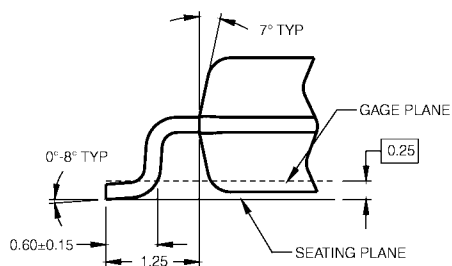
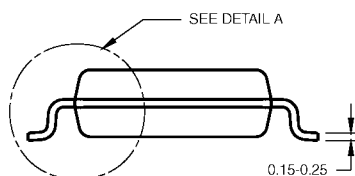
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.

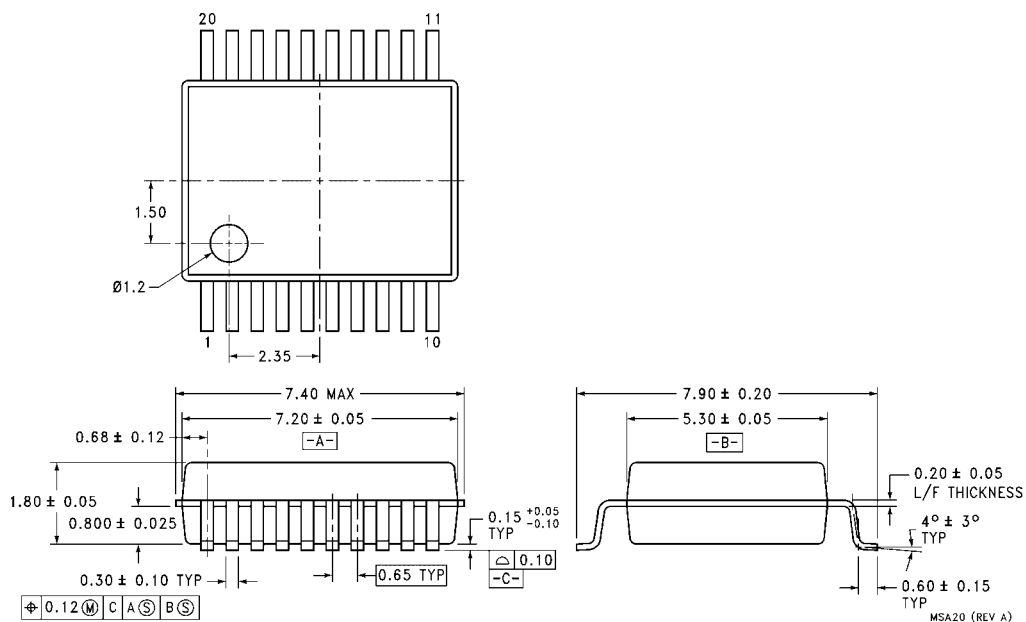
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

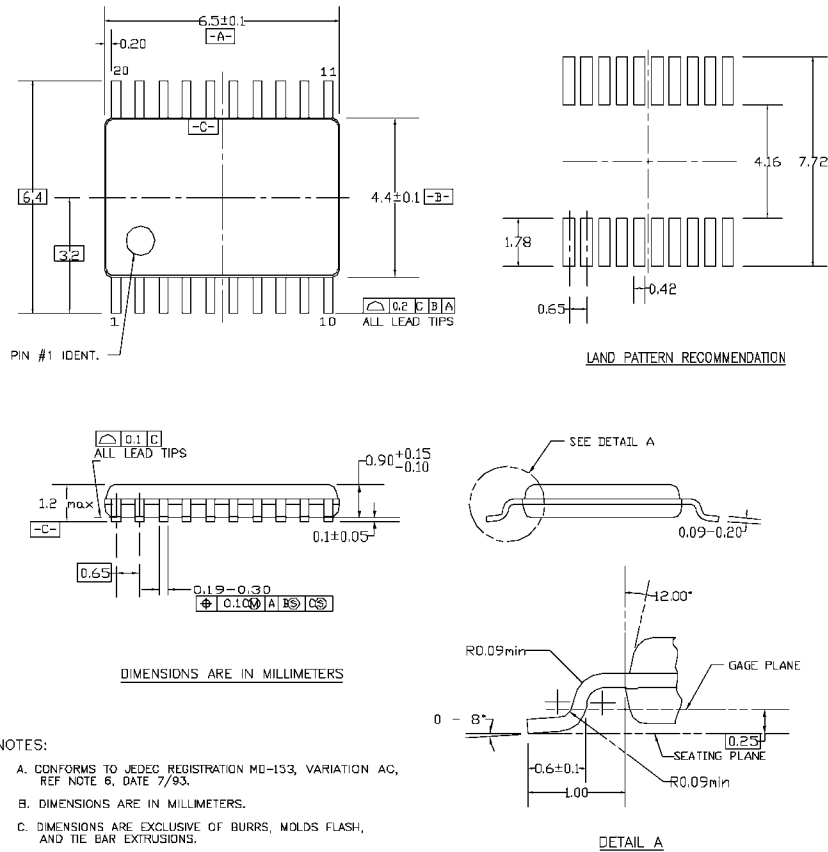
**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC20REV D1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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