

## 2.7V Dual Channel 12-Bit A/D Converter with SPI Serial Interface

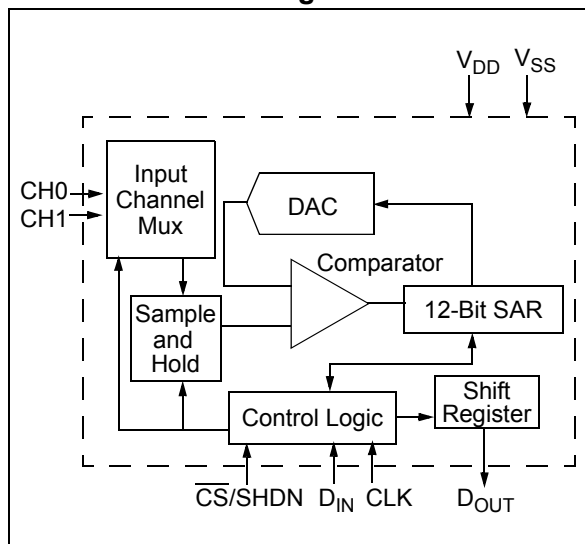
### Features

- 12-bit resolution
- $\pm 1$  LSB maximum DNL
- $\pm 1$  LSB maximum INL (MCP3202-B)
- $\pm 2$  LSB maximum INL (MCP3202-C)
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI Serial Interface (Modes 0,0 and 1,1)
- Single supply operation: 2.7V-5.5V
- 100 ksp/s maximum sampling rate at  $V_{DD} = 5V$
- 50 ksp/s maximum sampling rate at  $V_{DD} = 2.7V$
- Low power CMOS technology
- 500 nA typical standby current, 5  $\mu A$  maximum
- 550  $\mu A$  maximum active current at 5V
- Industrial temp range:  $-40^{\circ}C$  to  $+85^{\circ}C$
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

### Applications

- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

### Functional Block Diagram



### Description

The MCP3202 is a successive approximation 12-bit analog-to-digital (A/D) converter with on-board sample and hold circuitry.

The MCP3202 is programmable to provide a single pseudo-differential input pair or dual single-ended inputs. Differential Nonlinearity (DNL) is specified at  $\pm 1$  LSB, and Integral Nonlinearity (INL) is offered in  $\pm 1$  LSB (MCP3202-B) and  $\pm 2$  LSB (MCP3202-C) versions.

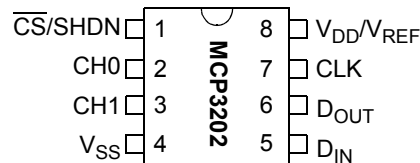
Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of conversion rates of up to 100 ksp/s at 5V and 50 ksp/s at 2.7V.

The MCP3202 operates over a broad voltage range, 2.7V to 5.5V. Low-current design permits operation with typical standby and active currents of only 500 nA and 375  $\mu A$ , respectively.

The MCP3202 is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

### Package Types

#### PDIP, MSOP, SOIC, TSSOP



# MCP3202

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

|                                              |                          |
|----------------------------------------------|--------------------------|
| $V_{DD} - V_{SS}$ .....                      | 7.0V                     |
| All Inputs and Outputs w.r.t. $V_{SS}$ ..... | -0.6V to $V_{DD} + 0.6V$ |
| Storage Temperature.....                     | -65°C to +150°C          |
| Ambient temperature with power applied.....  | -65°C to +150°C          |
| Maximum Junction Temperature ( $T_J$ ) ..... | +150°C                   |
| ESD Protection On All Pins (HBM) .....       | ≥ 4 kV                   |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

| <b>Electrical Characteristics:</b> Unless otherwise noted, all parameters apply at $V_{DD} = 5.5V$ , $V_{SS} = 0V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $f_{SAMPLE} = 100$ ksp/s and $f_{CLK} = 18 \cdot f_{SAMPLE}$ . |              |                 |                       |                    |                |                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------------|-----------------------|--------------------|----------------|------------------------------------------------------|
| Parameter                                                                                                                                                                                                                    | Sym          | Min.            | Typ.                  | Max.               | Units          | Conditions                                           |
| <b>Conversion Rate:</b>                                                                                                                                                                                                      |              |                 |                       |                    |                |                                                      |
| Conversion Time                                                                                                                                                                                                              | $t_{CONV}$   | —               | —                     | 12                 | clock cycles   |                                                      |
| Analog Input Sample Time                                                                                                                                                                                                     | $t_{SAMPLE}$ | 1.5             |                       |                    | clock cycles   |                                                      |
| Throughput Rate                                                                                                                                                                                                              | $f_{SAMPL}$  | —               | —                     | 100<br>50          | ksp/s<br>ksp/s | $V_{DD} = V_{REF} = 5V$<br>$V_{DD} = V_{REF} = 2.7V$ |
| <b>DC Accuracy:</b>                                                                                                                                                                                                          |              |                 |                       |                    |                |                                                      |
| Resolution                                                                                                                                                                                                                   |              | 12              |                       |                    | bits           |                                                      |
| Integral Nonlinearity                                                                                                                                                                                                        | INL          | —               | $\pm 0.75$<br>$\pm 1$ | $\pm 1$<br>$\pm 2$ | LSB<br>LSB     | MCP3202-B<br>MCP3202-C                               |
| Differential Nonlinearity                                                                                                                                                                                                    | DNL          | —               | $\pm 0.5$             | $\pm 1$            | LSB            | No missing codes over temperature                    |
| Offset Error                                                                                                                                                                                                                 |              | —               | $\pm 1.25$            | $\pm 3$            | LSB            |                                                      |
| Gain Error                                                                                                                                                                                                                   |              | —               | $\pm 1.25$            | $\pm 5$            | LSB            |                                                      |
| <b>Dynamic Performance:</b>                                                                                                                                                                                                  |              |                 |                       |                    |                |                                                      |
| Total Harmonic Distortion                                                                                                                                                                                                    | THD          | —               | -82                   | —                  | dB             | $V_{IN} = 0.1V$ to $4.9V@1$ kHz                      |
| Signal-to-Noise and Distortion (SINAD)                                                                                                                                                                                       | SINAD        | —               | 72                    | —                  | dB             | $V_{IN} = 0.1V$ to $4.9V@1$ kHz                      |
| Spurious Free Dynamic Range                                                                                                                                                                                                  | SFDR         | —               | 86                    | —                  | dB             | $V_{IN} = 0.1V$ to $4.9V@1$ kHz                      |
| <b>Analog Inputs:</b>                                                                                                                                                                                                        |              |                 |                       |                    |                |                                                      |
| Input Voltage Range for CH0 or CH1 in Single-Ended Mode                                                                                                                                                                      |              | $V_{SS}$        | —                     | $V_{DD}$           | V              |                                                      |
| Input Voltage Range for IN+ in Pseudo-Differential Mode                                                                                                                                                                      | IN+          | IN-             | —                     | $V_{DD} + IN-$     |                | See Sections 3.1 and 4.1                             |
| Input Voltage Range for IN- in Pseudo-Differential Mode                                                                                                                                                                      | IN-          | $V_{SS} - 100$  | —                     | $V_{SS} + 100$     | mV             | See Sections 3.1 and 4.1                             |
| Leakage Current                                                                                                                                                                                                              |              | —               | .001                  | $\pm 1$            | $\mu A$        |                                                      |
| Switch Resistance                                                                                                                                                                                                            | $R_{SS}$     | —               | 1 k                   | —                  | $\Omega$       | See Figure 4-1                                       |
| Sample Capacitor                                                                                                                                                                                                             | $C_{SAMPLE}$ | —               | 20                    | —                  | pF             | See Figure 4-1                                       |
| <b>Digital Input/Output:</b>                                                                                                                                                                                                 |              |                 |                       |                    |                |                                                      |
| Data Coding Format                                                                                                                                                                                                           |              | Straight Binary |                       |                    |                |                                                      |
| High Level Input Voltage                                                                                                                                                                                                     | $V_{IH}$     | $0.7 V_{DD}$    | —                     | —                  | V              |                                                      |
| Low Level Input Voltage                                                                                                                                                                                                      | $V_{IL}$     | —               | —                     | $0.3 V_{DD}$       | V              |                                                      |

**Note 1:** This parameter is established by characterization and not 100% tested.

**Note 2:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See [Section 6.2 “Maintaining Minimum Clock Speed”](#) for more information.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at  $V_{DD} = 5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 100$  ksp/s and  $f_{CLK} = 18 \cdot f_{SAMPLE}$ .

| Parameter                               | Sym               | Min. | Typ. | Max.       | Units      | Conditions                                                     |
|-----------------------------------------|-------------------|------|------|------------|------------|----------------------------------------------------------------|
| High Level Output Voltage               | $V_{OH}$          | 4.1  | —    | —          | V          | $I_{OH} = -1$ mA, $V_{DD} = 4.5V$                              |
| Low Level Output Voltage                | $V_{OL}$          | —    | —    | 0.4        | V          | $I_{OL} = 1$ mA, $V_{DD} = 4.5V$                               |
| Input Leakage Current                   | $I_{LI}$          | -10  | —    | 10         | $\mu A$    | $V_{IN} = V_{SS}$ or $V_{DD}$                                  |
| Output Leakage Current                  | $I_{LO}$          | -10  | —    | 10         | $\mu A$    | $V_{OUT} = V_{SS}$ or $V_{DD}$                                 |
| Pin Capacitance<br>(All Inputs/Outputs) | $C_{IN}, C_{OUT}$ | —    | —    | 10         | pF         | $V_{DD} = 5.0V$ (Note 1)<br>$T_A = +25^{\circ}C$ , $f = 1$ MHz |
| <b>Timing Parameters:</b>               |                   |      |      |            |            |                                                                |
| Clock Frequency                         | $f_{CLK}$         | —    | —    | 1.8<br>0.9 | MHz<br>MHz | $V_{DD} = 5V$ (Note 2)<br>$V_{DD} = 2.7V$ (Note 2)             |
| Clock High Time                         | $t_{HI}$          | —    | —    | 2          | MHz        |                                                                |
| Clock Low Time                          | $t_{LO}$          | —    | —    | 2          | MHz        |                                                                |
| CS Fall To First Rising CLK Edge        | $t_{SUCS}$        | 100  | —    | —          | ns         |                                                                |
| Data Input Setup Time                   | $t_{SU}$          | 50   | —    | —          | ns         |                                                                |
| Data Input Hold Time                    | $t_{HD}$          | 50   | —    | —          | ns         |                                                                |
| CLK Fall To Output Data Valid           | $t_{DO}$          | —    | —    | 200        | ns         | See Test Circuits, Figure 1-2                                  |
| CLK Fall To Output Enable               | $t_{EN}$          | —    | —    | 200        | ns         | See Test Circuits, Figure 1-2                                  |
| CS Rise To Output Disable               | $t_{DIS}$         | —    | —    | 100        | ns         | See Test Circuits, Figure 1-2<br>Note 1                        |
| CS Disable Time                         | $t_{CSH}$         | 500  | —    | —          | ns         |                                                                |
| $D_{OUT}$ Rise Time                     | $t_R$             | —    | —    | 100        | ns         | See Test Circuits, Figure 1-2<br>Note 1                        |
| $D_{OUT}$ Fall Time                     | $t_F$             | —    | —    | 100        | ns         | See Test Circuits, Figure 1-2<br>Note 1                        |
| <b>Power Requirements:</b>              |                   |      |      |            |            |                                                                |
| Operating Voltage                       | $V_{DD}$          | 2.7  | —    | 5.5        | V          |                                                                |
| Operating Current                       | $I_{DD}$          | —    | 375  | 550        | $\mu A$    | $V_{DD} = 5.0V$ , $D_{OUT}$ unloaded                           |
| Standby Current                         | $I_{DDS}$         | —    | 0.5  | 5          | $\mu A$    | $CS = V_{DD} = 5.0V$                                           |

**Note 1:** This parameter is established by characterization and not 100% tested.

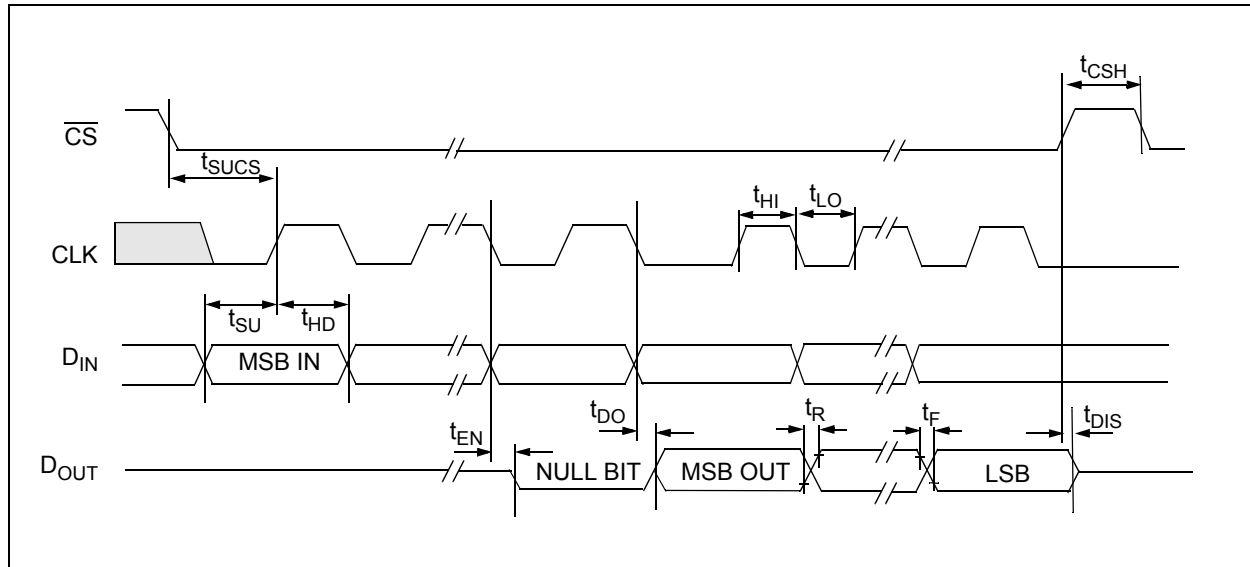
**Note 2:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See [Section 6.2 “Maintaining Minimum Clock Speed”](#) for more information.

**TEMPERATURE CHARACTERISTICS**

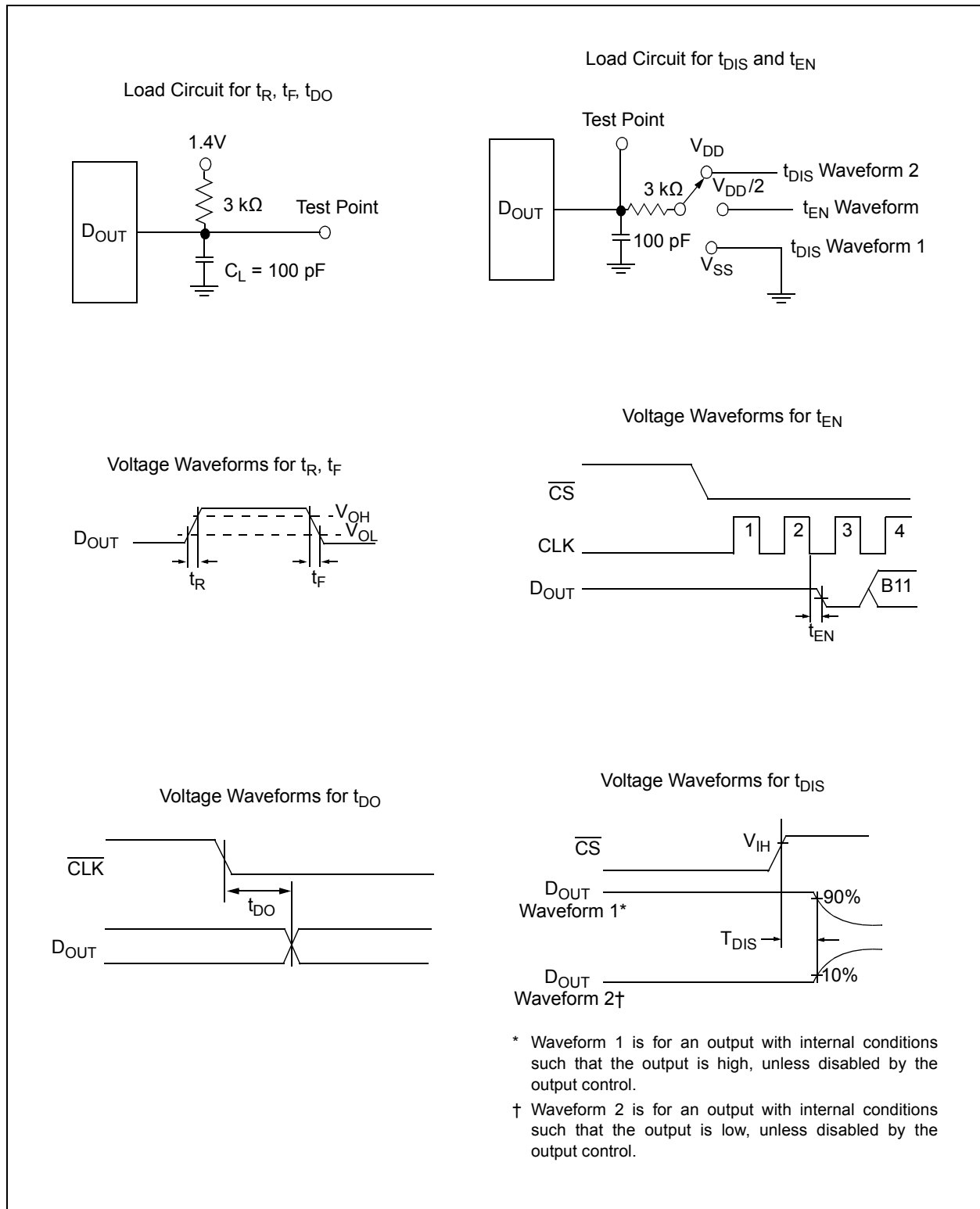
**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{SS} = GND$ .

| Parameters                         | Sym           | Min | Typ   | Max  | Units         | Conditions |
|------------------------------------|---------------|-----|-------|------|---------------|------------|
| <b>Temperature Ranges</b>          |               |     |       |      |               |            |
| Specified Temperature Range        | $T_A$         | -40 | —     | +85  | $^{\circ}C$   |            |
| Operating Temperature Range        | $T_A$         | -40 | —     | +85  | $^{\circ}C$   |            |
| Storage Temperature Range          | $T_A$         | -65 | —     | +150 | $^{\circ}C$   |            |
| <b>Thermal Package Resistances</b> |               |     |       |      |               |            |
| Thermal Resistance, 8L-MSOP        | $\theta_{JA}$ | —   | 211   | —    | $^{\circ}C/W$ |            |
| Thermal Resistance, 8L-PDIP        | $\theta_{JA}$ | —   | 89.5  | —    | $^{\circ}C/W$ |            |
| Thermal Resistance, 8L-SOIC        | $\theta_{JA}$ | —   | 149.5 | —    | $^{\circ}C/W$ |            |
| Thermal Resistance, 8L-TSSOP       | $\theta_{JA}$ | —   | 139   | —    | $^{\circ}C/W$ |            |

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**FIGURE 1-1:** Serial Timing.

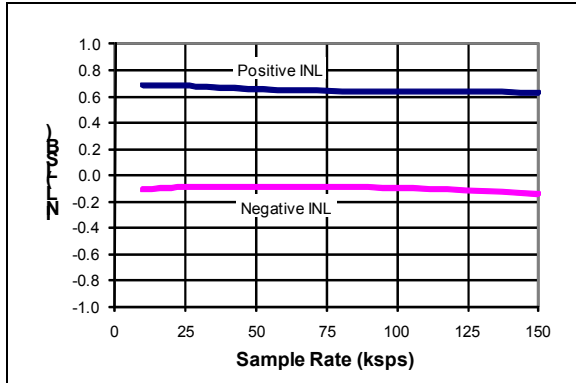


**FIGURE 1-2:** Test Circuits.

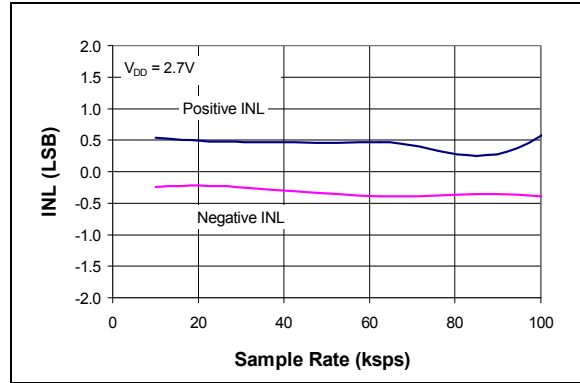
## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

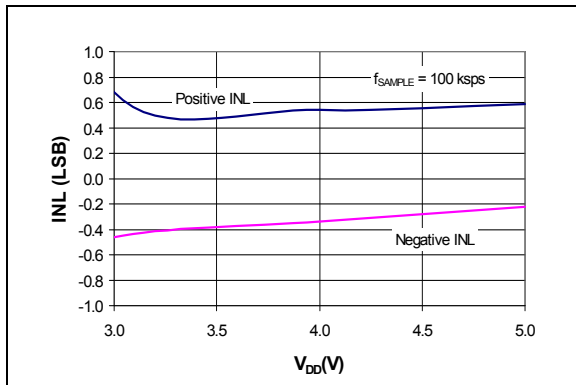
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kpsps,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



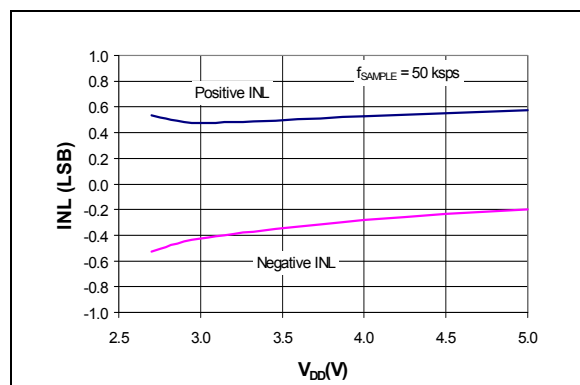
**FIGURE 2-1:** Integral Nonlinearity (INL) vs. Sample Rate.



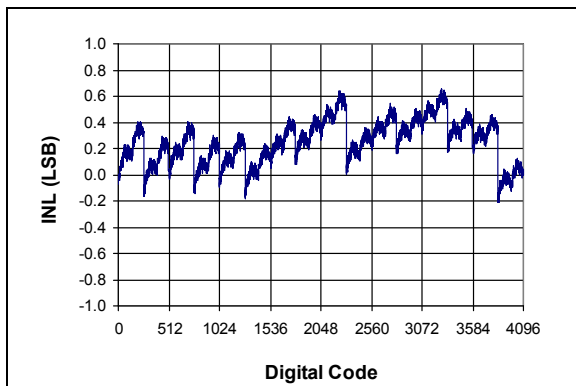
**FIGURE 2-4:** Integral Nonlinearity (INL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



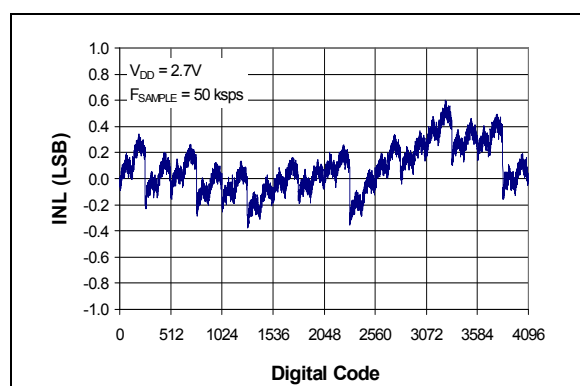
**FIGURE 2-2:** Integral Nonlinearity (INL) vs.  $V_{DD}$ .



**FIGURE 2-5:** Integral Nonlinearity (INL) vs.  $V_{DD}$ .

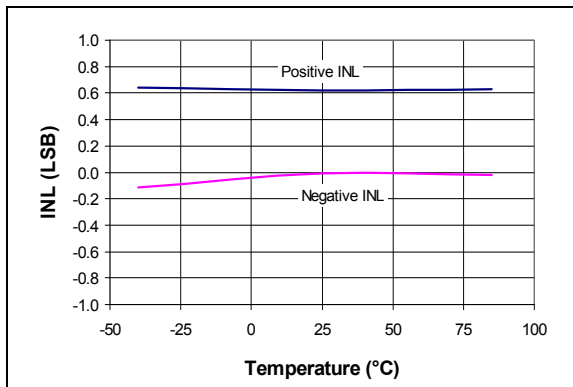


**FIGURE 2-3:** Integral Nonlinearity (INL) vs. Code (Representative Part).

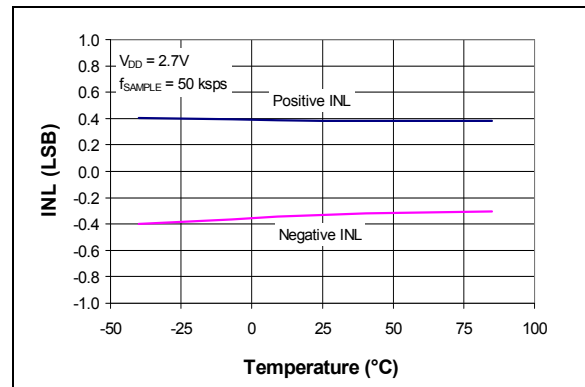


**FIGURE 2-6:** Integral Nonlinearity (INL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).

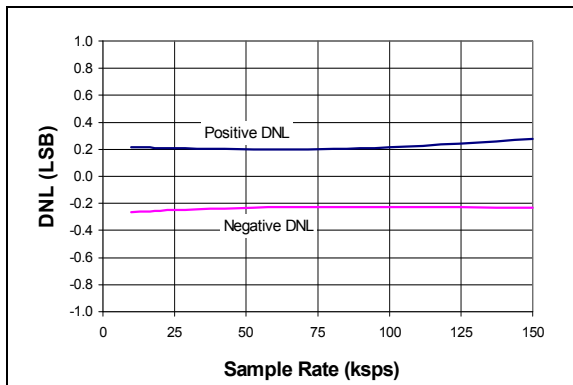
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kps,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



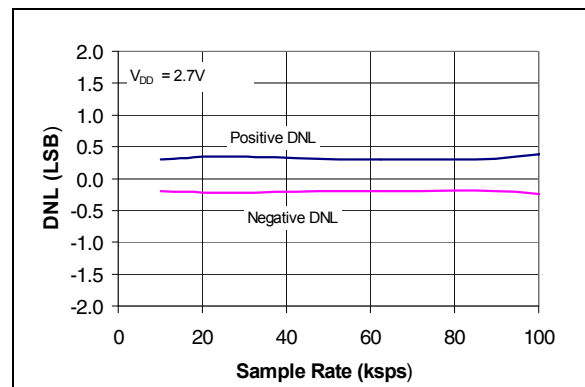
**FIGURE 2-7:** Integral Nonlinearity (INL) vs. Temperature.



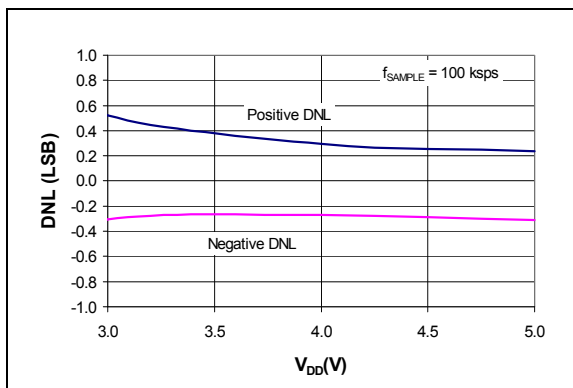
**FIGURE 2-10:** Integral Nonlinearity (INL) vs. Temperature ( $V_{DD} = 2.7V$ ).



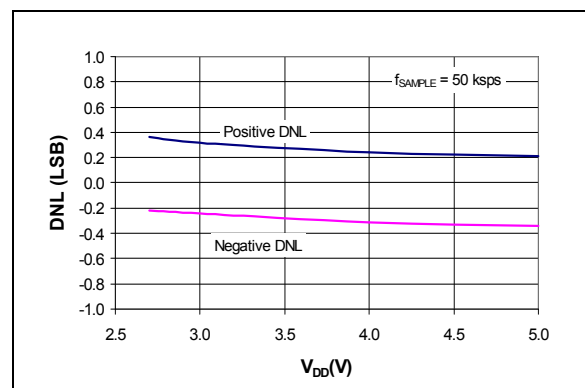
**FIGURE 2-8:** Differential Nonlinearity (DNL) vs. Sample Rate.



**FIGURE 2-11:** Differential Nonlinearity (DNL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



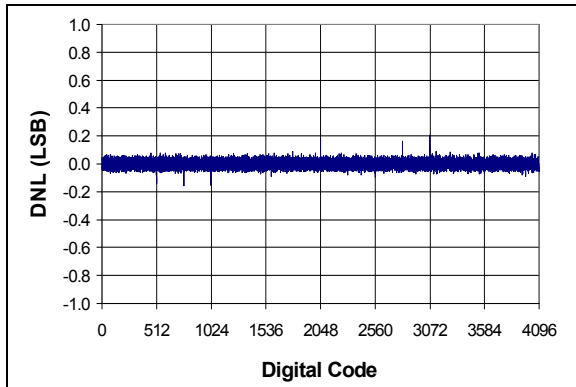
**FIGURE 2-9:** Differential Nonlinearity (DNL) vs.  $V_{DD}$ .



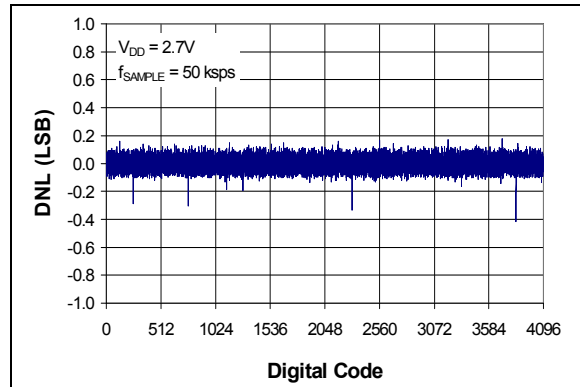
**FIGURE 2-12:** Differential Nonlinearity (DNL) vs.  $V_{DD}$ .

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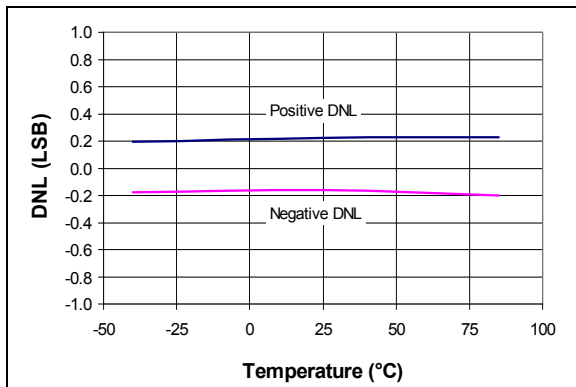
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kpsps,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



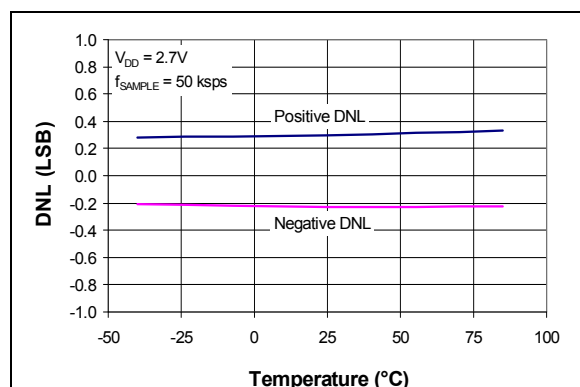
**FIGURE 2-13:** Differential Nonlinearity (DNL) vs. Code (Representative Part).



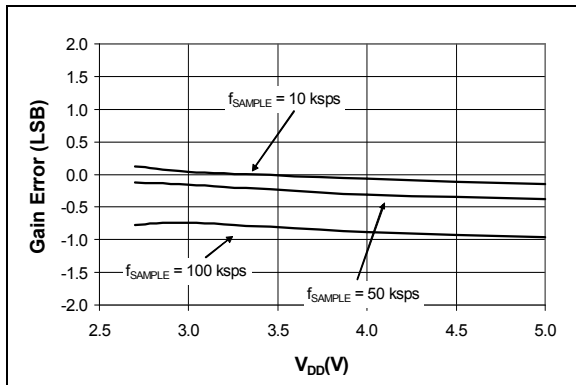
**FIGURE 2-16:** Differential Nonlinearity (DNL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).



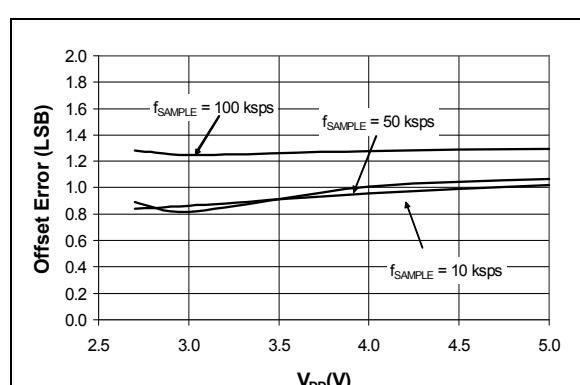
**FIGURE 2-14:** Differential Nonlinearity (DNL) vs. Temperature.



**FIGURE 2-17:** Differential Nonlinearity (DNL) vs. Temperature ( $V_{DD} = 2.7V$ ).

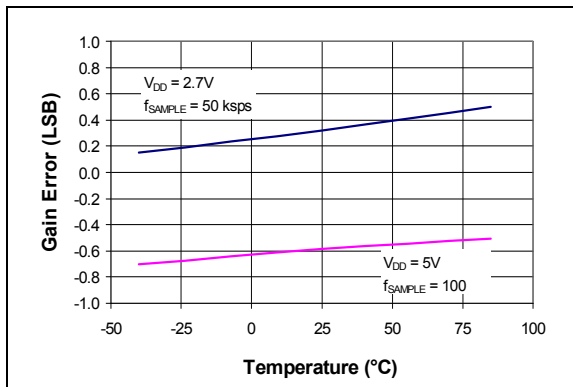


**FIGURE 2-15:** Gain Error vs.  $V_{DD}$ .

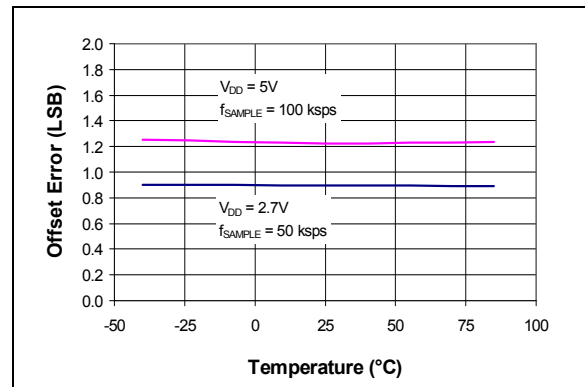


**FIGURE 2-18:** Offset Error vs.  $V_{DD}$ .

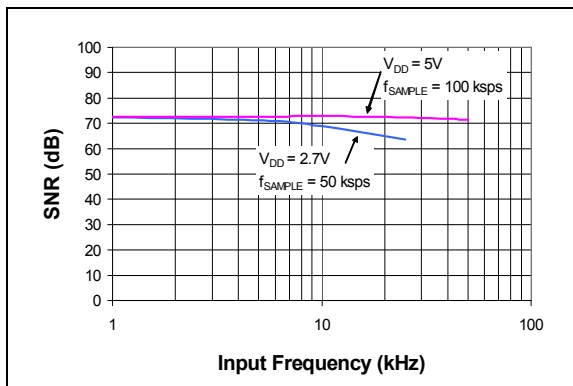
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kps,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



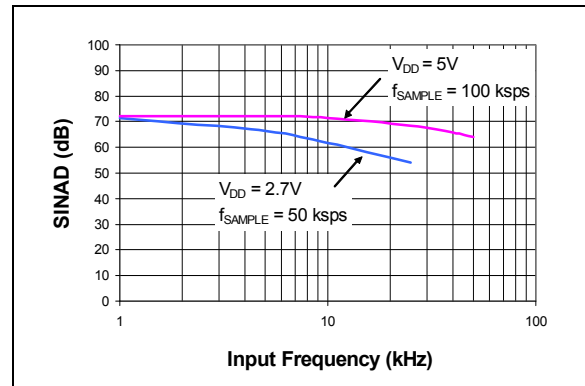
**FIGURE 2-19:** Gain Error vs. Temperature.



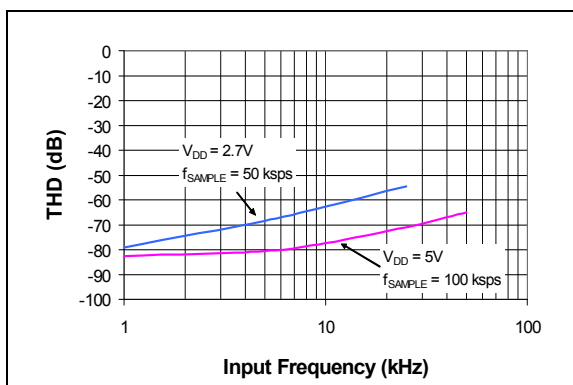
**FIGURE 2-22:** Offset Error vs. Temperature.



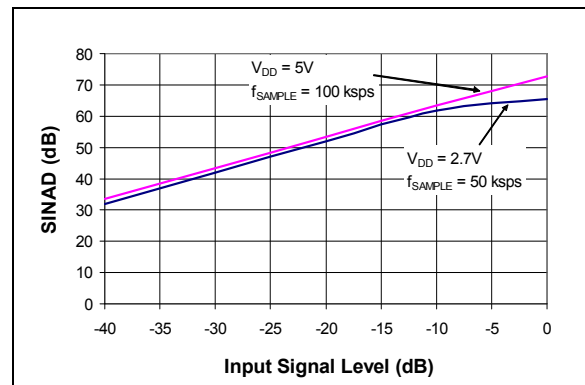
**FIGURE 2-20:** Signal-to-Noise Ratio (SNR) vs. Input Frequency.



**FIGURE 2-23:** Signal-to-Noise and Distortion (SINAD) vs. Input Frequency.



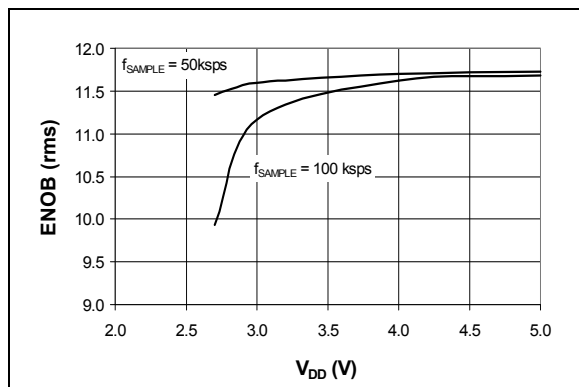
**FIGURE 2-21:** Total Harmonic Distortion (THD) vs. Input Frequency.



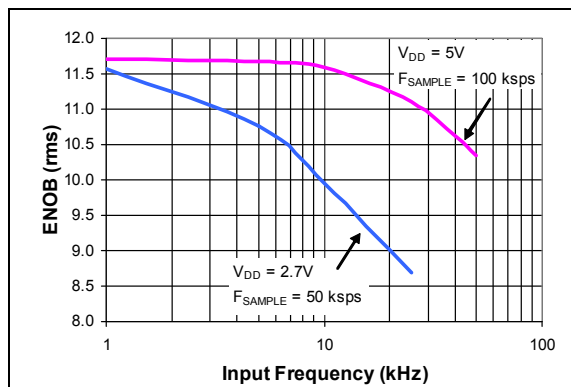
**FIGURE 2-24:** Signal-to-Noise and Distortion (SINAD) vs. Signal Level.

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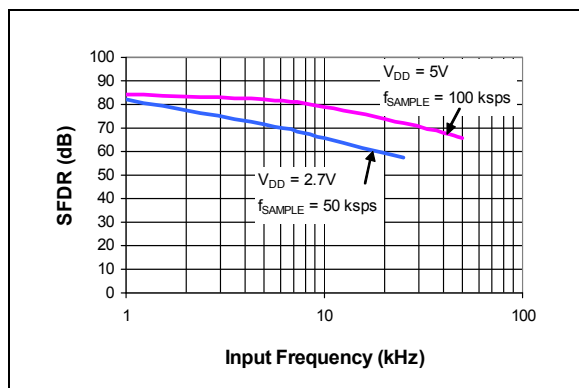
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100 \text{ kpsps}$ ,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ\text{C}$ .



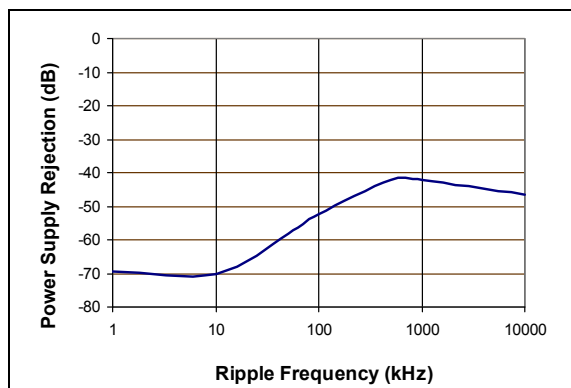
**FIGURE 2-25:** Effective Number of Bits (ENOB) vs.  $V_{DD}$ .



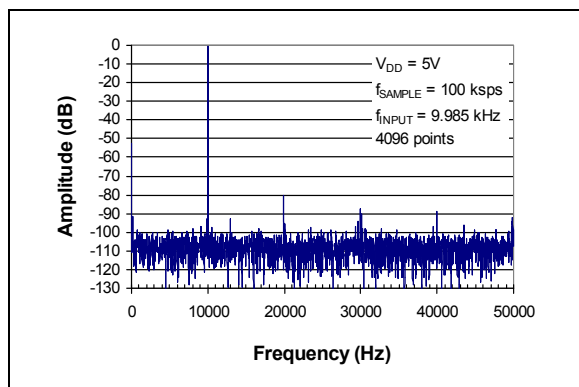
**FIGURE 2-28:** Effective Number of Bits (ENOB) vs. Input Frequency.



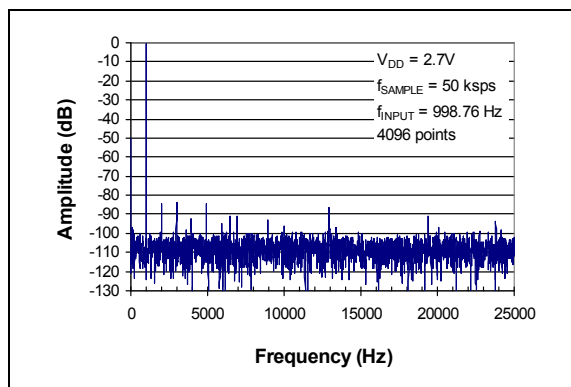
**FIGURE 2-26:** Spurious Free Dynamic Range (SFDR) vs. Input Frequency.



**FIGURE 2-29:** Power Supply Rejection (PSR) vs. Ripple Frequency.

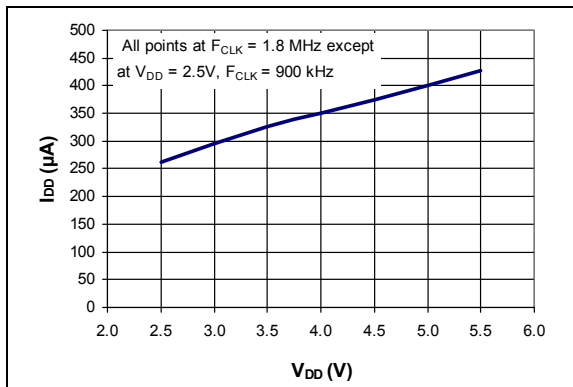


**FIGURE 2-27:** Frequency Spectrum of 10 kHz input (Representative Part).

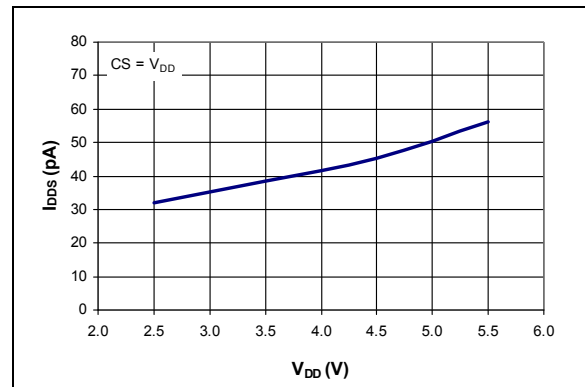


**FIGURE 2-30:** Frequency Spectrum of 1 kHz input (Representative Part,  $V_{DD} = 2.7V$ ).

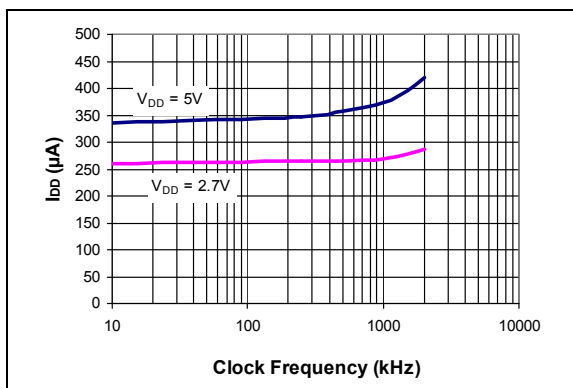
**Note:** Unless otherwise indicated,  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksps,  $f_{CLK} = 18 \cdot f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



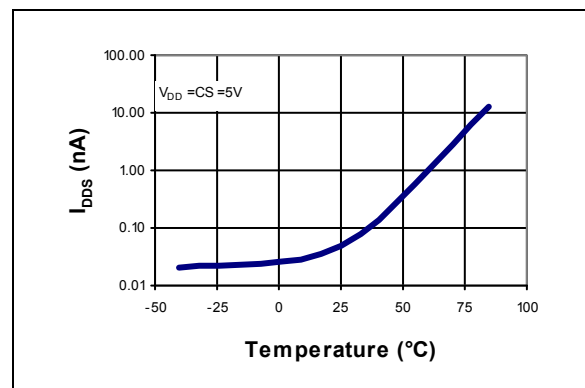
**FIGURE 2-31:**  $I_{DD}$  vs.  $V_{DD}$ .



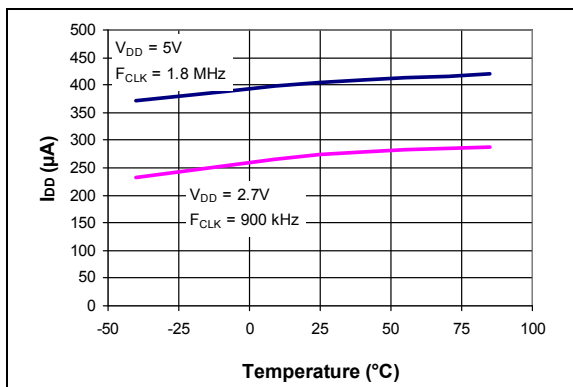
**FIGURE 2-34:**  $I_{DDS}$  vs.  $V_{DD}$ .



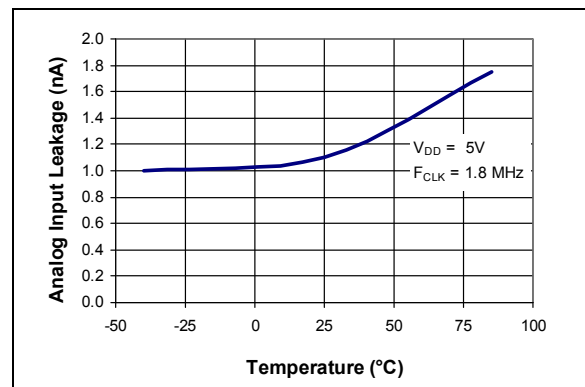
**FIGURE 2-32:**  $I_{DD}$  vs. Clock Frequency.



**FIGURE 2-35:**  $I_{DDS}$  vs. Temperature.



**FIGURE 2-33:**  $I_{DD}$  vs. Temperature.



**FIGURE 2-36:** Analog Input leakage current vs. Temperature.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3.1](#). Additional descriptions of the device pins follows.

**TABLE 3-1: PIN FUNCTION TABLE**

| MSOP, PDIP, SOIC, TSSOP | Name                               | Function                                               |
|-------------------------|------------------------------------|--------------------------------------------------------|
| 1                       | $\overline{\text{CS}}/\text{SHDN}$ | Chip Select/Shutdown Input                             |
| 2                       | CH0                                | Channel 0 Analog Input                                 |
| 3                       | CH1                                | Channel 1 Analog Input                                 |
| 4                       | V <sub>SS</sub>                    | Ground                                                 |
| 5                       | D <sub>IN</sub>                    | Serial Data In                                         |
| 6                       | D <sub>OUT</sub>                   | Serial Data Out                                        |
| 7                       | CLK                                | Serial Clock                                           |
| 8                       | V <sub>DD</sub> /V <sub>REF</sub>  | +2.7V to 5.5V Power Supply and Reference Voltage Input |

### 3.1 Analog Inputs (CH0/CH1)

Analog inputs for channels 0 and 1 respectively. These channels can be programmed to be used as two independent channels in Single-Ended mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See [Section 5.0 “Serial Communications”](#) for information on programming the channel configuration.

### 3.2 Chip Select/Shutdown ( $\overline{\text{CS}}/\text{SHDN}$ )

The  $\overline{\text{CS}}/\text{SHDN}$  pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The  $\overline{\text{CS}}/\text{SHDN}$  pin must be pulled high between conversions.

### 3.3 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See [Section 6.2 “Maintaining Minimum Clock Speed”](#) for constraints on clock speed.

### 3.4 Serial Data Input (D<sub>IN</sub>)

The SPI port serial data input pin is used to clock in input channel configuration data.

### 3.5 Serial Data Output (D<sub>OUT</sub>)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

## 4.0 DEVICE OPERATION

The MCP3202 A/D converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the second rising edge of the serial clock after the start bit has been received. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code.

Conversion rates of 100 ksp/s are possible on the MCP3202. See [Section 6.2 “Maintaining Minimum Clock Speed”](#) for information on minimum clock rates.

Communication with the device is done using a 3-wire SPI-compatible interface.

### 4.1 Analog Inputs

The MCP3202 device offers the choice of using the analog input channels configured as two single-ended inputs or a single pseudo-differential input. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, CH0 and CH1 are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to  $V_{REF}$  ( $V_{DD} + IN-$ ). The IN- input is limited to  $\pm 100$  mV from the  $V_{SS}$  rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D converter to meet specification, the charge holding capacitor ( $C_{SAMPLE}$ ) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in [Figure 4-1](#).

In this diagram, it is shown that the source impedance ( $R_S$ ) adds to the internal sampling switch ( $R_{SS}$ ) impedance, directly affecting the time that is required to charge the capacitor,  $C_{SAMPLE}$ . Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601 which has a closed loop output impedance of tens of ohms. The adverse effects of higher source impedances are shown in [Figure 4-2](#).

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than  $\{[V_{DD} + (IN-)] - 1 \text{ LSB}\}$ , then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below  $V_{SS}$ , then the voltage level at the IN+ input will have to go below  $V_{SS}$  to see the 000h output code. Conversely, if IN- is more than 1 LSB above  $V_{SS}$ , then the FFFh code will not be seen unless the IN+ input level goes above  $V_{DD}$  level.

## 4.2 Digital Output Code

The digital output code produced by an A/D converter is a function of the input signal and the reference voltage. For the MCP3202,  $V_{DD}$  is used as the reference voltage. As the  $V_{DD}$  level is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D converter is shown below.

### EQUATION 4-1:

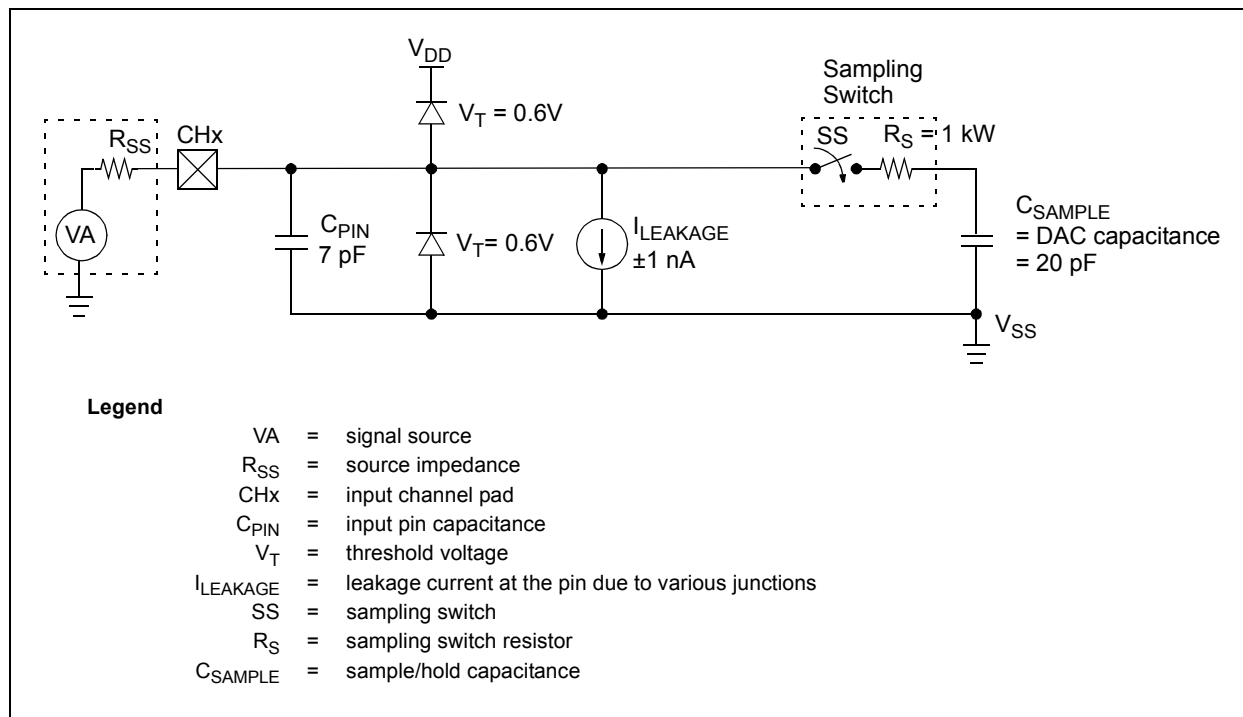
$$\text{Digital Output Code} = \frac{4096 \cdot V_{IN}}{V_{DD}}$$

where:

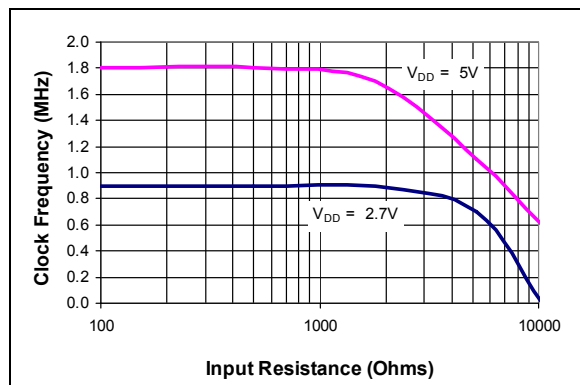
$V_{IN}$  = analog input voltage

$V_{DD}$  = supply voltage

# MCP3202



**FIGURE 4-1:** Analog Input Model.



**FIGURE 4-2:** Maximum Clock Frequency vs. Input Resistance ( $R_S$ ) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.

## 5.0 SERIAL COMMUNICATIONS

### 5.1 Overview

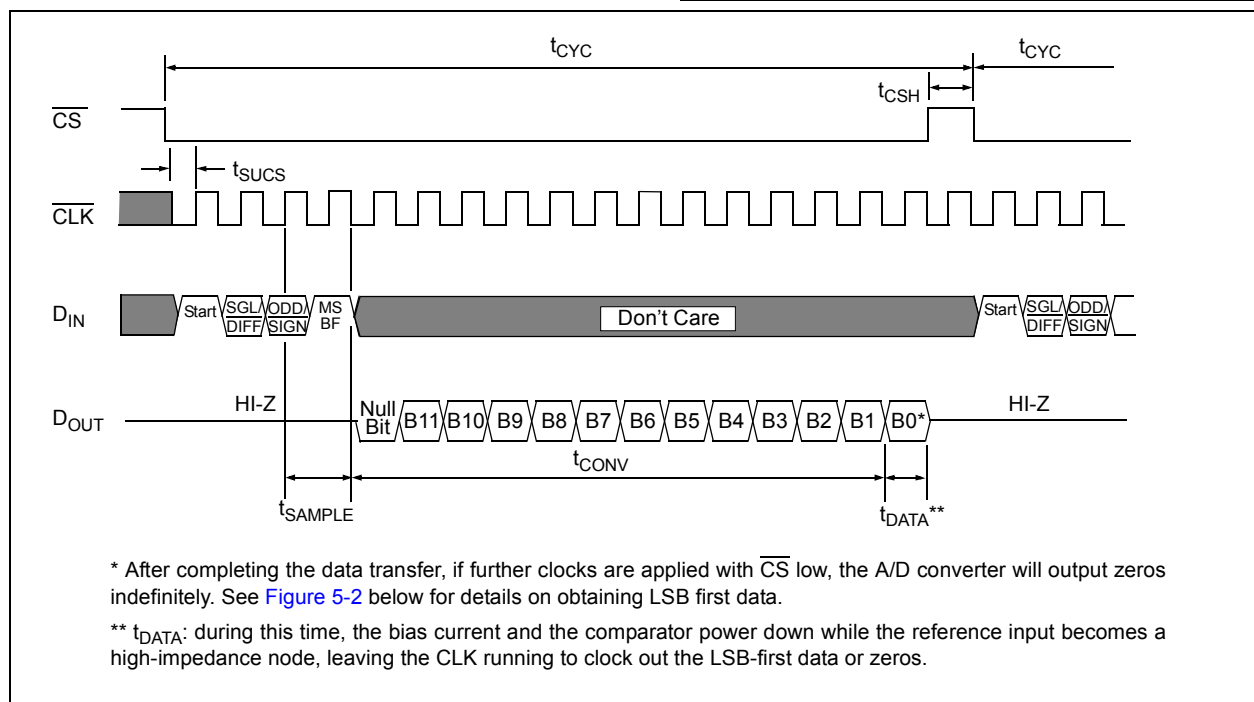
Communication with the MCP3202 is done using a standard SPI-compatible serial interface. Initiating communication with the device is done by bringing the  $\overline{\text{CS}}$  line low. See Figure 5-1. If the device was powered up with the  $\overline{\text{CS}}$  pin low, it must be brought high and back low to initiate communication. The first clock received with  $\overline{\text{CS}}$  low and  $\text{D}_{\text{IN}}$  high will constitute a start bit. The SGL/DIFF bit and the ODD/SIGN bit follow the start bit and are used to select the input channel configuration. The SGL/DIFF is used to select Single-Ended or Pseudo-Differential mode. The ODD/SIGN bit selects which channel is used in Single-Ended mode, and is used to determine polarity in Pseudo-Differential mode. Following the ODD/SIGN bit, the MSBF bit is transmitted to and is used to enable the LSB first format for the device. If the MSBF bit is high, then the data will come from the device in MSB first format and any further clocks with  $\overline{\text{CS}}$  low will cause the device to output zeros. If the MSBF bit is low, then the device will output the converted word LSB first after the word has been transmitted in the MSB first format. See Figure 5-2. Table 5-1 shows the configuration bits for the MCP3202. The device will begin to sample the analog input on the second rising edge of the clock, after the start bit has been received. The sample period will end on the falling edge of the third clock following the start bit.

On the falling edge of the clock for the MSBF bit, the device will output a low null bit. The next sequential 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the  $\overline{\text{CS}}$  is held low, (and MSBF = 1), the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while  $\overline{\text{CS}}$  is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring  $\overline{\text{CS}}$  low and clock in leading zeros on the  $\text{D}_{\text{IN}}$  line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 “Using the MCP3202 with Microcontroller (MCU) SPI Ports” for more details on using the MCP3202 devices with hardware SPI ports.

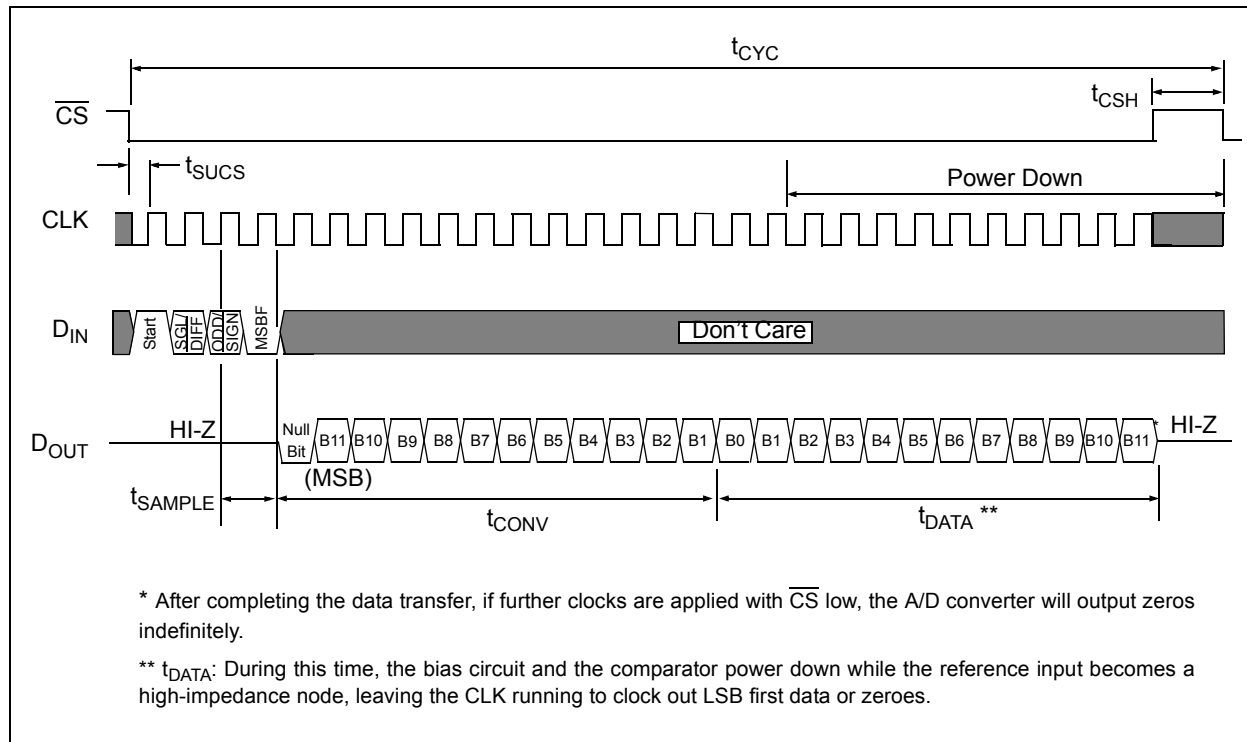
**TABLE 5-1: CONFIGURATION BITS FOR THE MCP3202**

|                          | Config Bits |          | Channel Selection |     | GND |
|--------------------------|-------------|----------|-------------------|-----|-----|
|                          | SGL/DIFF    | ODD/SIGN | 0                 | 1   |     |
| Single-Ended Mode        | 1           | 0        | +                 | —   | -   |
|                          | 1           | 1        | —                 | +   | -   |
| Pseudo-Differential Mode | 0           | 0        | IN+               | IN- |     |
|                          | 0           | 1        | IN-               | IN+ |     |



**FIGURE 5-1:** Communication with the MCP3202 using MSB first format only.

# MCP3202



**FIGURE 5-2:** Communication with MCP3202 using LSB first format.

## 6.0 APPLICATIONS INFORMATION

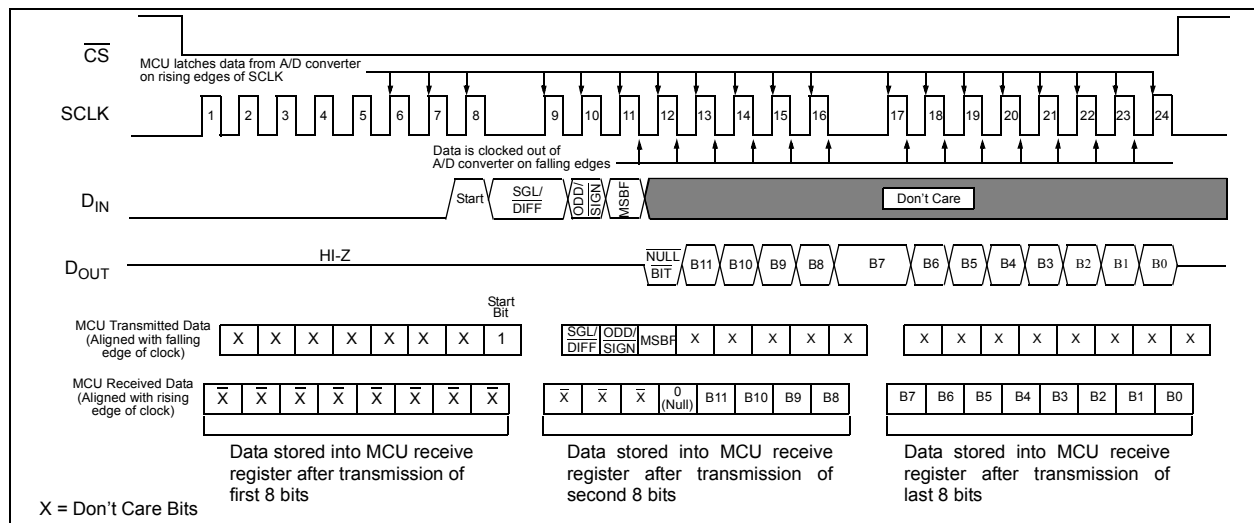
### 6.1 Using the MCP3202 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Depending on how communication routines are used, it is very possible that the number of clocks required for communication will not be a multiple of eight. Therefore, it may be necessary for the MCU to send more clocks than are actually required. This is usually done by sending 'leading zeros' before the start bit, which are ignored by the device.

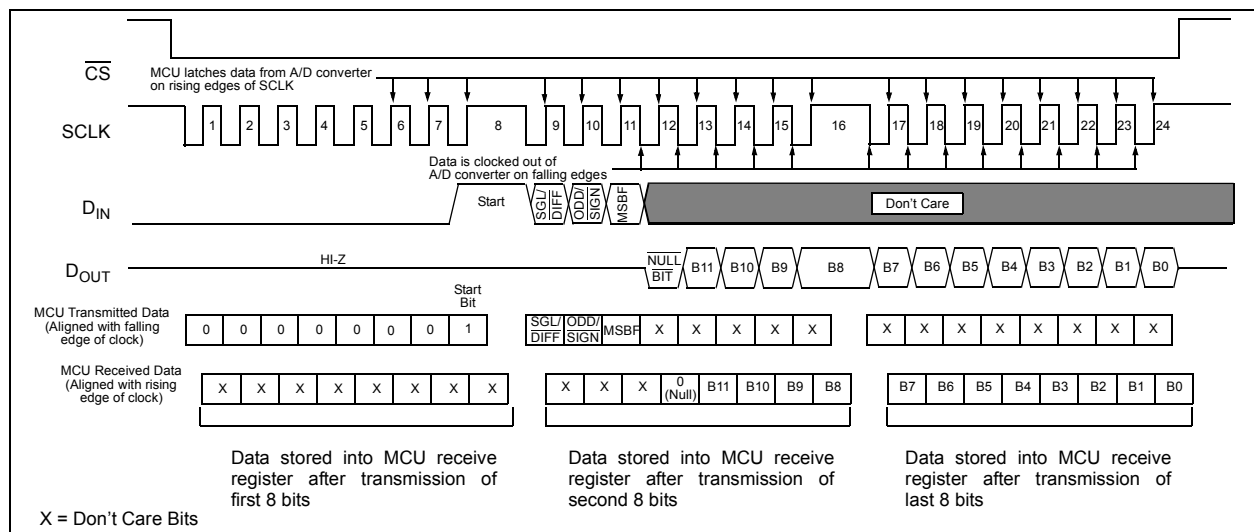
As an example, Figure 6-1 and Figure 6-2 show how the MCP3202 can be interfaced to a MCU with a hardware SPI port.

Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D converter contains seven leading zeros before the start bit. Arranging the leading zeros this way produces the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D converter on the falling edge of clock number 12. After the second eight clocks have been sent to the device, the MCU receive buffer will contain three unknown bits (the output is at high-impedance until the null bit is clocked out), the null bit and the highest order four bits of the conversion. After the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.



**FIGURE 6-1:** SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).



**FIGURE 6-2:** SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).

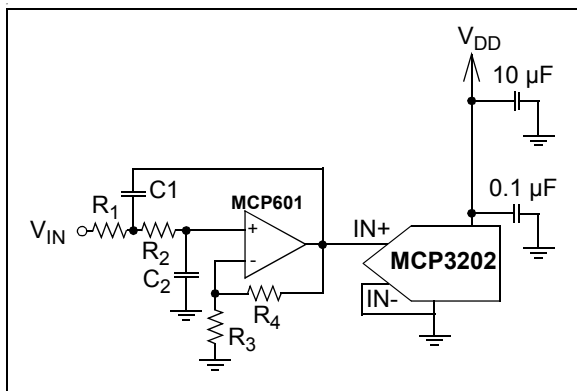
## 6.2 Maintaining Minimum Clock Speed

When the MCP3202 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

## 6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D converter is not a low-impedance source, it will have to be buffered or inaccurate conversion results may occur. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 below where an op amp is used to drive the analog input of the MCP3202. This amplifier provides a low-impedance output for the converter input and a low-pass filter, which eliminates unwanted high frequency noise.

Low-pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab® software. FilterLab will calculate capacitor and resistor values, as well as, determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 "Anti-Aliasing Analog Filters for Data Acquisition Systems".



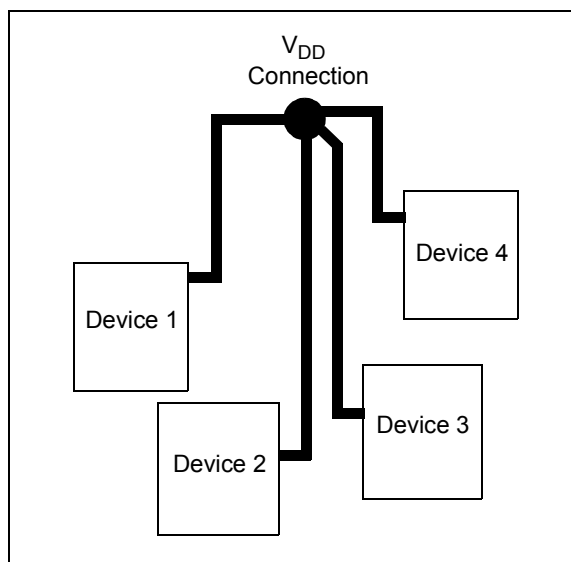
**FIGURE 6-3:** The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3202.

## 6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V<sub>DD</sub> connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D converters, refer to AN688 "Layout Tips for 12-Bit A/D Converter Applications" (DS00688).



**FIGURE 6-4:** V<sub>DD</sub> traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.

## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

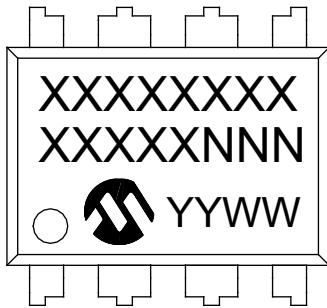
8-Lead MSOP (3x3 mm)



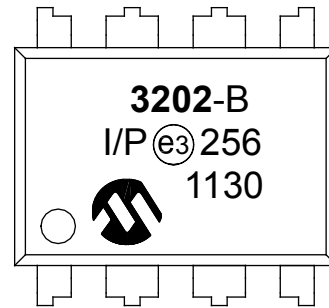
Example



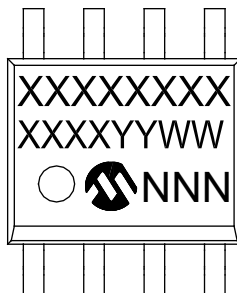
8-Lead PDIP (300 mil)



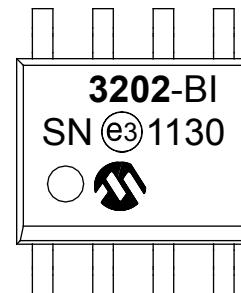
Example



8-Lead SOIC (3.90 mm)



Example



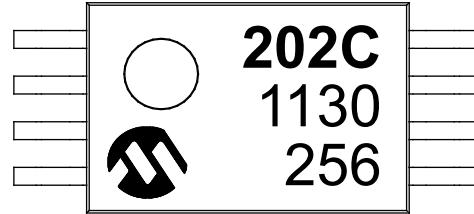
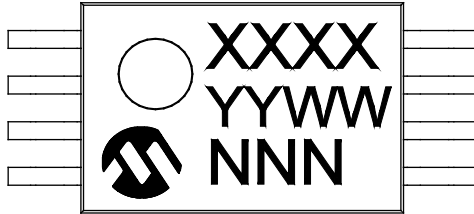
|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Customer-specific information                                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | ⓔ3     | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## Package Marking Information (Continued)

8-Lead TSSOP (4.4 mm)

Example

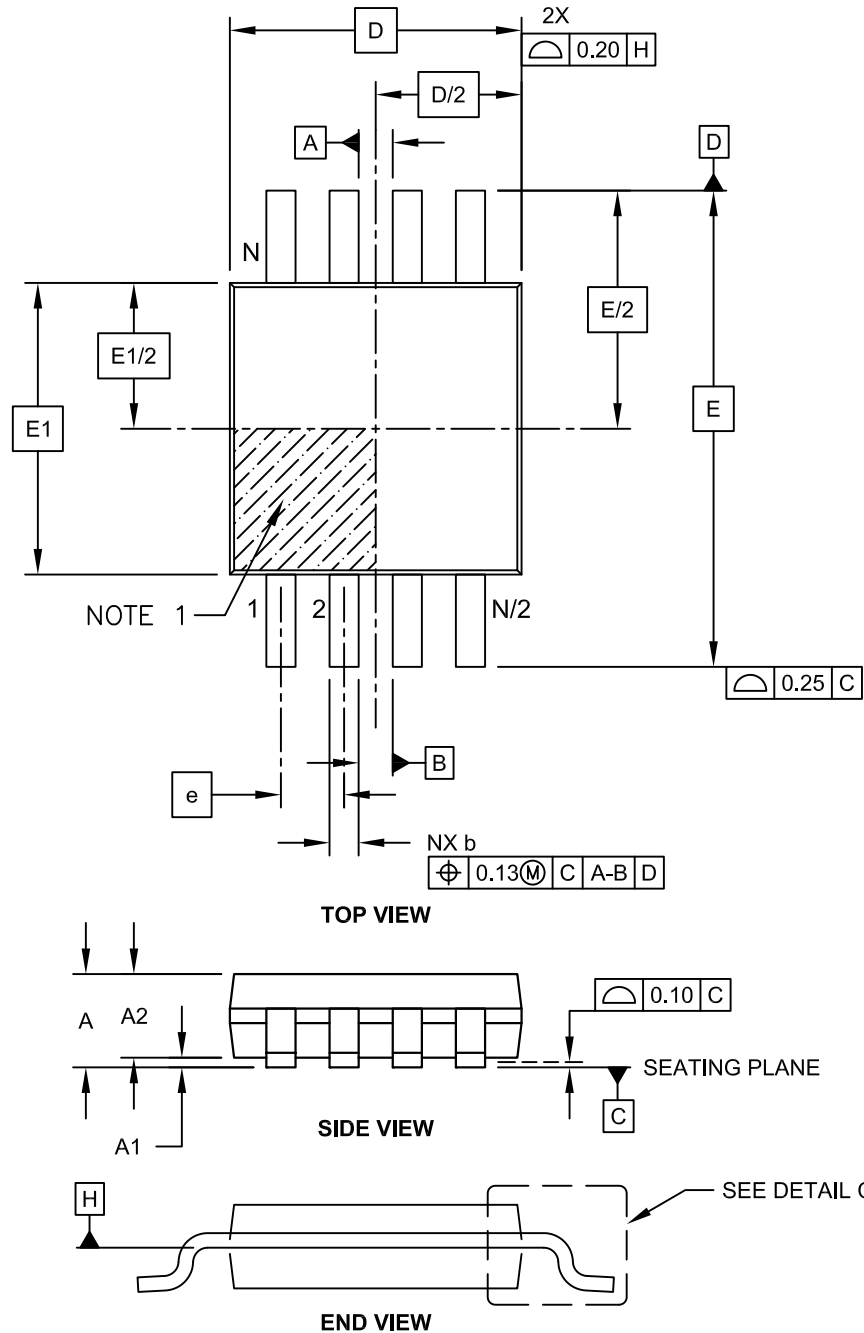


|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Customer-specific information                                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | (e3)   | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

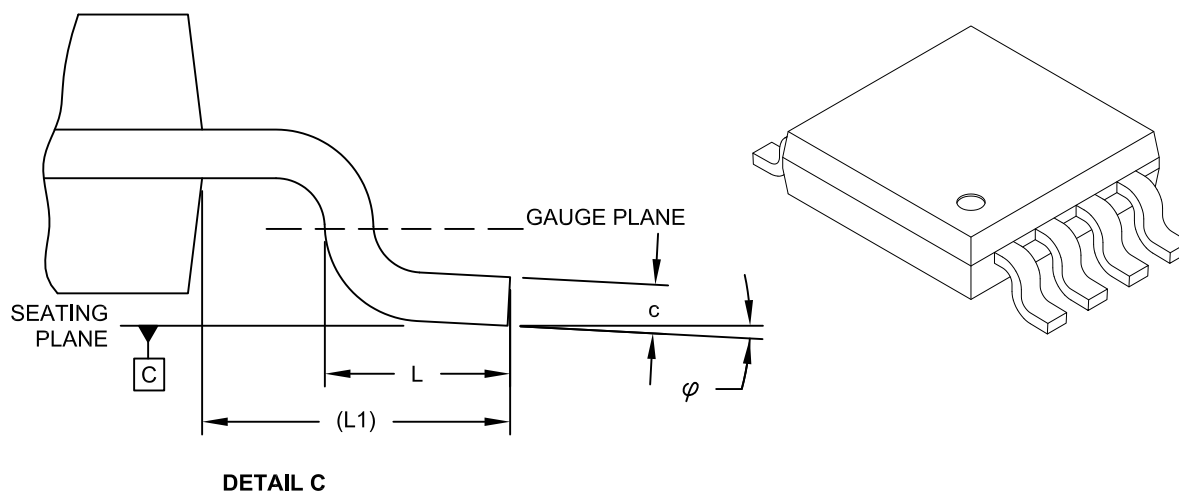


Microchip Technology Drawing C04-111C Sheet 1 of 2

# MCP3202

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |          |      |
|--------------------------|-------|-------------|----------|------|
|                          |       | MIN         | NOM      | MAX  |
| Number of Pins           | N     |             | 8        |      |
| Pitch                    | e     |             | 0.65 BSC |      |
| Overall Height           | A     | -           | -        | 1.10 |
| Molded Package Thickness | A2    | 0.75        | 0.85     | 0.95 |
| Standoff                 | A1    | 0.00        | -        | 0.15 |
| Overall Width            | E     |             | 4.90 BSC |      |
| Molded Package Width     | E1    |             | 3.00 BSC |      |
| Overall Length           | D     |             | 3.00 BSC |      |
| Foot Length              | L     | 0.40        | 0.60     | 0.80 |
| Footprint                | L1    |             | 0.95 REF |      |
| Foot Angle               | φ     | 0°          | -        | 8°   |
| Lead Thickness           | c     | 0.08        | -        | 0.23 |
| Lead Width               | b     | 0.22        | -        | 0.40 |

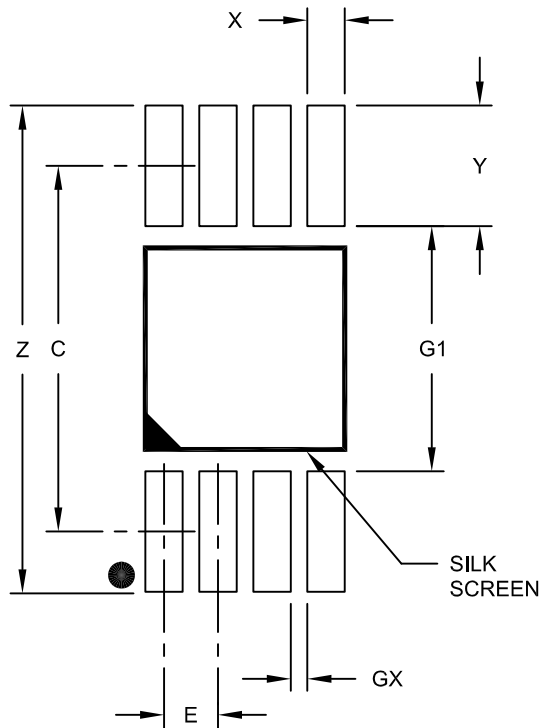
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits        | Units | MILLIMETERS |      |      |
|-------------------------|-------|-------------|------|------|
|                         |       | MIN         | NOM  | MAX  |
| Contact Pitch           | E     | 0.65 BSC    |      |      |
| Contact Pad Spacing     | C     |             | 4.40 |      |
| Overall Width           | Z     |             |      | 5.85 |
| Contact Pad Width (X8)  | X1    |             |      | 0.45 |
| Contact Pad Length (X8) | Y1    |             |      | 1.45 |
| Distance Between Pads   | G1    | 2.95        |      |      |
| Distance Between Pads   | GX    | 0.20        |      |      |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

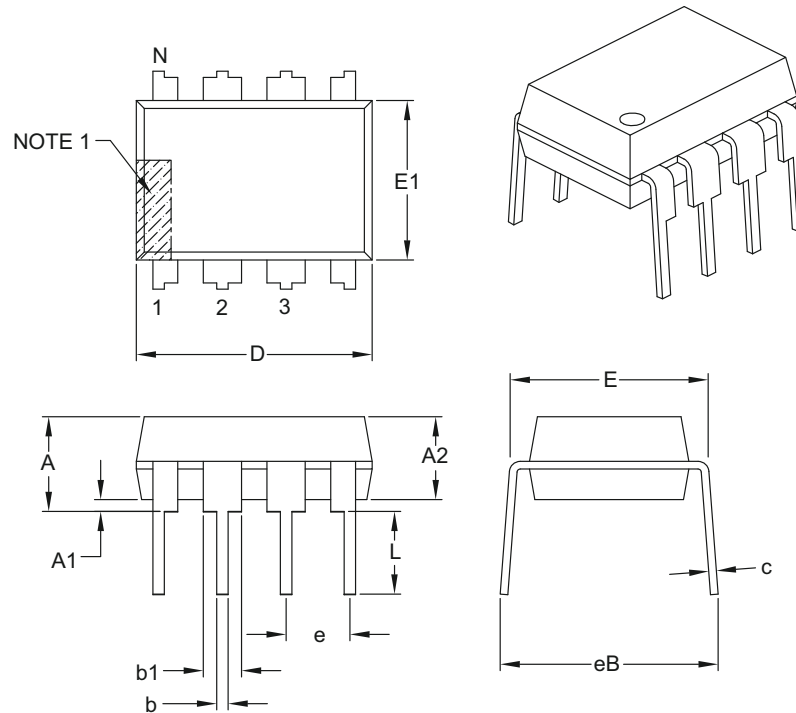
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

# MCP3202

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                      |    | INCHES   |      |      |
|----------------------------|----|----------|------|------|
| Dimension Limits           |    | MIN      | NOM  | MAX  |
| Number of Pins             | N  | 8        |      |      |
| Pitch                      | e  | .100 BSC |      |      |
| Top to Seating Plane       | A  | —        | —    | .210 |
| Molded Package Thickness   | A2 | .115     | .130 | .195 |
| Base to Seating Plane      | A1 | .015     | —    | —    |
| Shoulder to Shoulder Width | E  | .290     | .310 | .325 |
| Molded Package Width       | E1 | .240     | .250 | .280 |
| Overall Length             | D  | .348     | .365 | .400 |
| Tip to Seating Plane       | L  | .115     | .130 | .150 |
| Lead Thickness             | c  | .008     | .010 | .015 |
| Upper Lead Width           | b1 | .040     | .060 | .070 |
| Lower Lead Width           | b  | .014     | .018 | .022 |
| Overall Row Spacing §      | eB | —        | —    | .430 |

### Notes:

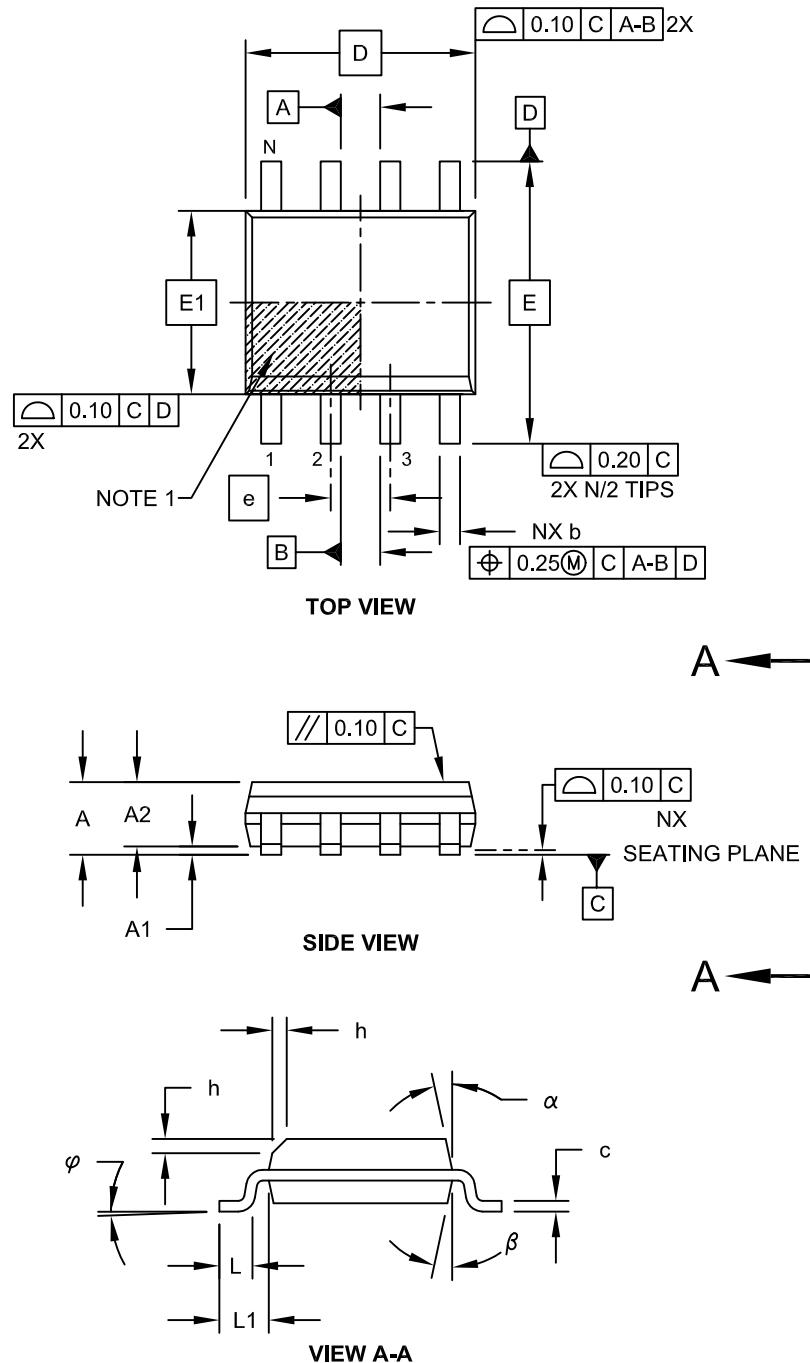
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

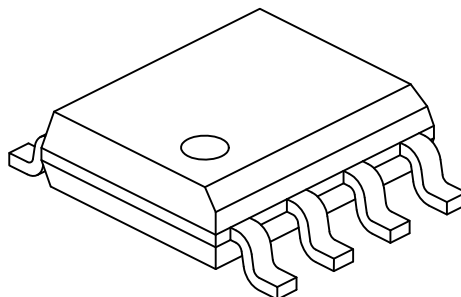


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

# MCP3202

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |    | MILLIMETERS |     |      |
|--------------------------|----|-------------|-----|------|
| Dimension Limits         |    | MIN         | NOM | MAX  |
| Number of Pins           | N  | 8           |     |      |
| Pitch                    | e  | 1.27 BSC    |     |      |
| Overall Height           | A  | -           | -   | 1.75 |
| Molded Package Thickness | A2 | 1.25        | -   | -    |
| Standoff §               | A1 | 0.10        | -   | 0.25 |
| Overall Width            | E  | 6.00 BSC    |     |      |
| Molded Package Width     | E1 | 3.90 BSC    |     |      |
| Overall Length           | D  | 4.90 BSC    |     |      |
| Chamfer (Optional)       | h  | 0.25        | -   | 0.50 |
| Foot Length              | L  | 0.40        | -   | 1.27 |
| Footprint                | L1 | 1.04 REF    |     |      |
| Foot Angle               | φ  | 0°          | -   | 8°   |
| Lead Thickness           | c  | 0.17        | -   | 0.25 |
| Lead Width               | b  | 0.31        | -   | 0.51 |
| Mold Draft Angle Top     | α  | 5°          | -   | 15°  |
| Mold Draft Angle Bottom  | β  | 5°          | -   | 15°  |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M

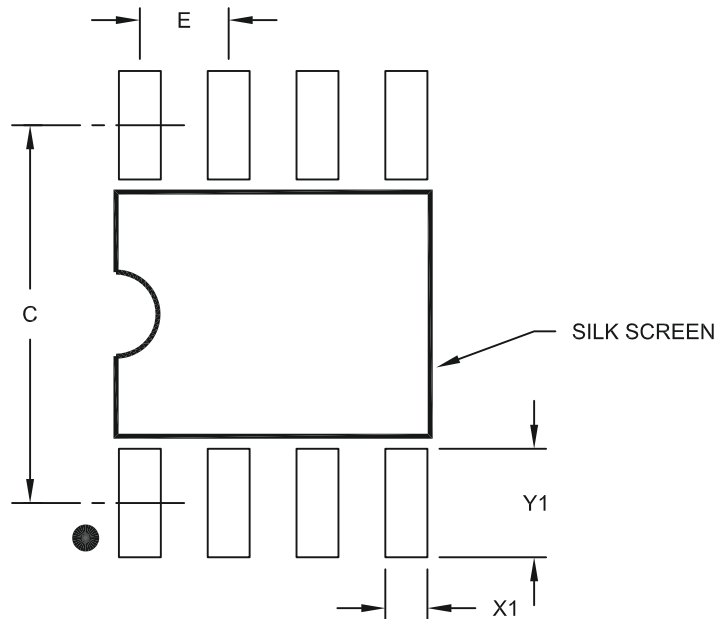
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units                   |    | MILLIMETERS |      |      |
|-------------------------|----|-------------|------|------|
| Dimension Limits        |    | MIN         | NOM  | MAX  |
| Contact Pitch           | E  | 1.27 BSC    |      |      |
| Contact Pad Spacing     | C  |             | 5.40 |      |
| Contact Pad Width (X8)  | X1 |             |      | 0.60 |
| Contact Pad Length (X8) | Y1 |             |      | 1.55 |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

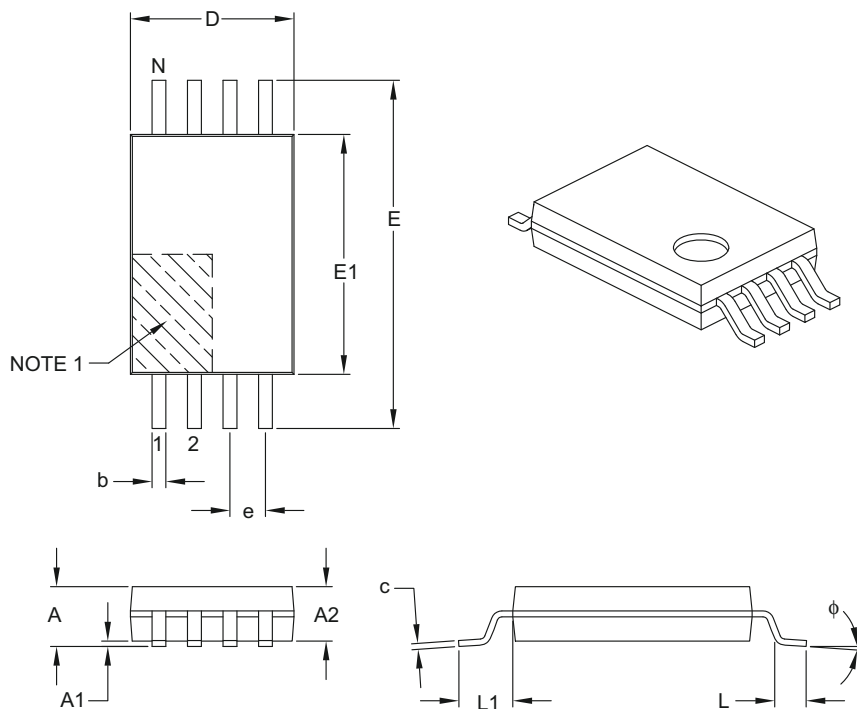
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

# MCP3202

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |      |      |
|--------------------------|-------|-------------|------|------|
|                          |       | MIN         | NOM  | MAX  |
| Number of Pins           | N     | 8           |      |      |
| Pitch                    | e     | 0.65 BSC    |      |      |
| Overall Height           | A     | –           | –    | 1.20 |
| Molded Package Thickness | A2    | 0.80        | 1.00 | 1.05 |
| Standoff                 | A1    | 0.05        | –    | 0.15 |
| Overall Width            | E     | 6.40 BSC    |      |      |
| Molded Package Width     | E1    | 4.30        | 4.40 | 4.50 |
| Molded Package Length    | D     | 2.90        | 3.00 | 3.10 |
| Foot Length              | L     | 0.45        | 0.60 | 0.75 |
| Footprint                | L1    | 1.00 REF    |      |      |
| Foot Angle               | φ     | 0°          | –    | 8°   |
| Lead Thickness           | c     | 0.09        | –    | 0.20 |
| Lead Width               | b     | 0.19        | –    | 0.30 |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

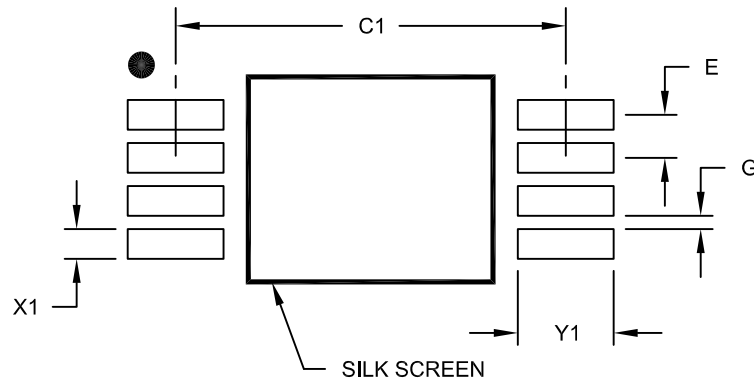
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension               | Units | MILLIMETERS |      |      |
|-------------------------|-------|-------------|------|------|
|                         |       | MIN         | NOM  | MAX  |
| Contact Pitch           | E     | 0.65 BSC    |      |      |
| Contact Pad Spacing     | C1    |             | 5.90 |      |
| Contact Pad Width (X8)  | X1    |             |      | 0.45 |
| Contact Pad Length (X8) | Y1    |             |      | 1.45 |
| Distance Between Pads   | G     | 0.20        |      |      |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

## APPENDIX A: REVISION HISTORY

### Revision F (November 2011)

Updated [Product Identification System](#)

Corrected MSOP package marking drawings.

Updated Package Specification Drawings with new additions.

### Revision E (December 2008)

Updates to packaging outline drawings.

### Revision D (December 2006)

Updates to packaging outline drawings.

### Revision C (August 2001)

Undocumented changes.

### Revision B (June 2000)

Undocumented changes.

### Revision A (August 1999)

Initial release of this document.



NOTES:

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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