Low Noise, Precision, Rail-to-Rail Output, JFET Single/Dual/Quad Op Amps

Data Sheet

ADA4610-1/ADA4610-2/ADA4610-4

FEATURES

- **Low offset voltage**
  - **B grade: 0.4 mV maximum (ADA4610-1/ADA4610-2 only)**
  - **A grade: 1 mV maximum**
- **Low offset voltage drift**
  - **B grade: 4 µV/°C maximum (ADA4610-1/ADA4610-2 only)**
  - **A grade: 8 µV/°C maximum**
- **Low input bias current: 5 pA typical**
- **Dual-supply operation: ±5 V to ±15 V**
- **Low voltage noise: 0.45 µV p-p at 0.1 Hz to 10 Hz**
- **Voltage noise density: 7.30 nV/√Hz at f = 1 kHz**
- **Low total harmonic distortion (THD) + noise: 0.00025%**
- **No phase reversal**
- **Rail-to-rail output**
- **Unity-gain stable**

APPLICATIONS

- **Instrumentation**
- **Medical instruments**
- **Multipole filters**
- **Precision current measurement**
- **Photodiode amplifiers**
- **Sensors**
- **Audio**

PIN CONFIGURATION

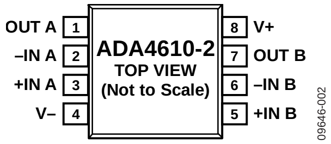

Figure 1. ADA4610-2 8-Lead SOIC_N (R Suffix); for Additional Packages and Models, See the Pin Configurations and Function Descriptions Section

GENERAL DESCRIPTION

The ADA4610-1/ADA4610-2/ADA4610-4 are precision JFET amplifiers that feature low input noise voltage, current noise, offset voltage, input bias current, and rail-to-rail output. The ADA4610-1 is a single amplifier, the ADA4610-2 is a dual amplifier, and the ADA4610-4 is a quad amplifier.

The combination of low offset, noise, and very low input bias current makes these amplifiers especially suitable for high impedance sensor amplification and precise current measurements using shunts. With excellent dc precision, low noise, and fast settling time, the ADA4610-1/ADA4610-2/ADA4610-4 provide superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the ADA4610-1/ADA4610-2/ADA4610-4 maintain fast settling performance with substantial capacitive loads. Unlike many older JFET amplifiers, the ADA4610-1/ADA4610-2/ ADA4610-4 do not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

The fast slew rate and great stability with capacitive loads make the ADA4610-1/ADA4610-2/ADA4610-4 perfect fits for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range for photodiode amplifier circuits. Low noise and distortion, high output current, and excellent speed make the ADA4610-1/ADA4610-2/ADA4610-4 great choices for audio applications.

The ADA4610-1/ADA4610-2/ADA4610-4 are specified over the −40°C to +125°C extended industrial temperature range.

The ADA4610-1 is available in an 8-lead SOIC_N package. The ADA4610-2 is available in 8-lead SOIC_N, 8-lead MSOP, and 8-lead LFCSP_VD packages. The ADA4610-4 is available in 14-lead SOIC_N and 16-lead LFCSP_WQ packages.

Table 1. Related Precision JFET Operational Amplifiers

Single	Dual	Quad
AD8510	AD8512	AD8513
AD8610	AD8620	Not applicable
AD820	AD822	AD824
ADA4627-1/ADA4637-1	Not applicable	Not applicable
Not applicable	ADA4001-2	Not applicable

Rev. E **Document Feedback**

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12/11—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
B Grade (ADA4610-1/ADA4610-2)				0.2	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
A Grade				0.4	1	mV
		−40°C < T_A < +125°C			1.8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
B Grade (ADA4610-1/ADA4610-2)[1]				0.5	4	µV/°C
A Grade[1]				1	8	µV/°C
Input Bias Current	I_B			5	25	pA
		−40°C < T_A < +125°C			1.5	nA
Input Offset Current	I_{OS}			2	20	pA
		−40°C < T_A < +125°C			0.25	nA
Input Voltage Range			−2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.5 V to +2.5 V	94	110		dB
		−40°C < T_A < +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −3.5 V to +3.5 V				
ADA4610-2			98	100		dB
		−40°C < T_A < +125°C	86			dB
ADA4610-1/ADA4610-4			96	98		dB
		−40°C < T_A < +125°C	84			dB
Input Capacitance		V_{CM} = 0 V				
Differential				3.1		pF
Common-Mode				4.8		pF
Input Resistance		V_{CM} = 0 V		$>10^{13}$		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.85	4.90		V
		−40°C < T_A < +125°C	4.60			V
		R_L = 600 Ω	4.60	4.89		V
		−40°C < T_A < +125°C	4.05			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−4.95	−4.90	V
		−40°C < T_A < +125°C			−4.75	V
		R_L = 600 Ω		−4.90	−4.80	V
		−40°C < T_A < +125°C			−4.40	V
Short-Circuit Current	I_{SC}			±63		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V				
ADA4610-2			106	125		dB
		−40°C < T_A < +125°C	103			dB
ADA4610-1/ADA4610-4			104	117		dB
		−40°C < T_A < +125°C	100			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		1.50	1.70	mA
		−40°C < T_A < +125°C			1.85	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L = 2 kΩ, A_V = +1				
Rising			15[1]	21		V/µs
Falling			15[1]	46		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = +100		15.4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = +1		9.3		MHz
Phase Margin	φ_M			61		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 5 mV p-p		10.6		MHz
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, A_V = +1, R_L = 2 kΩ, V_{IN} = 1 V rms		0.00025		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.45		µV p-p
Voltage Noise Density	e_n	f = 10 Hz		14		nV/√Hz
		f = 100 Hz		8.20		nV/√Hz
		f = 1 kHz		7.30		nV/√Hz
		f = 10 kHz		7.30		nV/√Hz

[1] Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
B Grade (ADA4610-1/ADA4610-2)				0.2	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
A Grade				0.4	1	mV
		−40°C < T_A < +125°C			1.8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
B Grade (ADA4610-1/ADA4610-2)[1]				0.5	4	µV/°C
A Grade[1]				1	8	µV/°C
Input Bias Current	I_B			5	25	pA
		−40°C < T_A < +125°C			1.50	nA
Input Offset Current	I_{OS}			2	20	pA
		−40°C < T_A < +125°C			0.25	nA
Input Voltage Range			−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	100	115		dB
		−40°C < T_A < +125°C	96			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = ±13.5 V				
ADA4610-2			104	107		dB
		−40°C < T_A < +125°C	91			dB
ADA4610-1/ADA4610-4			102	104		dB
		−40°C < T_A < +125°C	86			dB
Input Capacitance		V_{CM} = 0 V				
Differential				3.1		pF
Common-Mode				4.8		pF
Input Resistance		V_{CM} = 0 V		$>10^{13}$		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	14.80	14.90		V
		−40°C < T_A < +125°C	14.65			V
		R_L = 600 Ω	14.25	14.47		V
		−40°C < T_A < +125°C	13.35			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−14.90	−14.85	V
		−40°C < T_A < +125°C			−14.75	V
		R_L = 600 Ω		−14.68	−14.60	V
		−40°C < T_A < +125°C			−14.30	V
Short-Circuit Current	I_{SC}			±79		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V				
ADA4610-2			106	125		dB
		−40°C < T_A < +125°C	103			dB
ADA4610-1/ADA4610-4			104	117		dB
		−40°C < T_A < +125°C	100			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		1.60	1.85	mA
		−40°C < T_A < +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L = 2 kΩ, A_V = +1				
Rising			17[1]	25		V/µs
Falling			17[1]	61		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = +100		16.3		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = +1		9.3		MHz
Phase Margin	φ_M			66		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 5 mV p-p		9.5		MHz
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, A_V = +1, R_L = 2 kΩ, V_{IN} = 5 V rms		0.00025		%
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.45		µV p-p
Voltage Noise Density	e_n	f = 10 Hz		14		nV/√Hz
		f = 100 Hz		8.50		nV/√Hz
		f = 1 kHz		7.30		nV/√Hz
		f = 10 kHz		7.30		nV/√Hz

[1] Guaranteed by design and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_S$
Input Current[1]	±10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)[2]	2500 V
Field Induced Charge Device Model (FICDM)[3]	1250 V

[1] The input pins have clamp diodes connected to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

[2] ESDA/JEDEC JS-001-2011 applicable standard.

[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC_N	120	43	°C/W
8-Lead LFCSP_VD	57	12	°C/W
8-Lead MSOP	142	45	°C/W
14-Lead SOIC_N	115	36	°C/W
16-Lead LFCSP_WQ	65	3.2	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

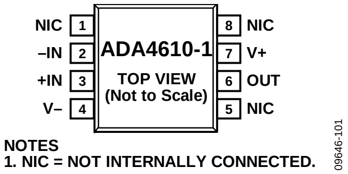


Figure 2. ADA4610-1 Pin Configuration, 8-Lead SOIC_N (R Suffix)

Table 6. ADA4610-1 Pin Function Descriptions, 8-Lead SOIC_N

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not Internally Connected
2	−IN	Inverting Input
3	+IN	Noninverting Input
4	V−	Negative Supply Voltage
6	OUT	Output
7	V+	Positive Supply Voltage

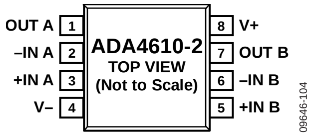


Figure 3. ADA4610-2 Pin Configuration, 8-Lead SOIC_N (R Suffix)

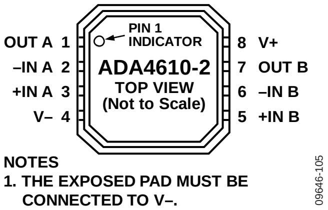


Figure 5. ADA4610-2 Pin Configuration, 8-Lead LFCSP_VD (CP Suffix)

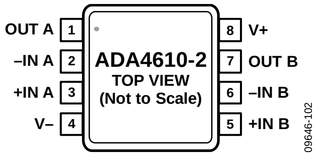


Figure 4. ADA4610-2 Pin Configuration, 8-Lead MSOP (RM Suffix)

Table 7. ADA4610-2 Pin Function Descriptions, 8-Lead SOIC_N, 8-Lead MSOP, and 8-Lead LFCSP_VD

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	–IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V–	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	–IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.
	EPAD	Exposed Pad for the 8-Lead LFCSP_VD (CP Suffix). The exposed pad must be connected to V–.

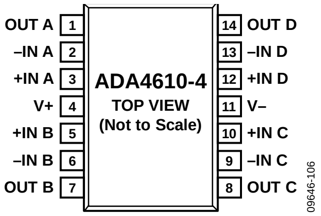


Figure 6. ADA4610-4 Pin Configuration, 14-Lead SOIC_N (R Suffix)

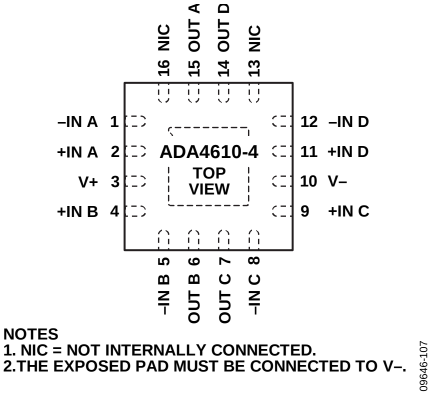


Figure 7. ADA4610-4 Pin Configuration, 16-Lead LFCSP_WQ (CP Suffix)

Table 8. ADA4610-4 Pin Function Descriptions, 14-Lead SOIC_N and 16-Lead LFCSP_WQ

Pin No.			
14-Lead SOIC_N	**16-Lead LFCSP_WQ**	**Mnemonic**	**Description**
1	15	OUT A	Output Channel A.
2	1	−IN A	Inverting Input Channel A.
3	2	+IN A	Noninverting Input Channel A.
4	3	V+	Positive Supply Voltage.
5	4	+IN B	Noninverting Input Channel B.
6	5	−IN B	Inverting Input Channel B.
7	6	OUT B	Output Channel B.
8	7	OUT C	Output Channel C.
9	8	−IN C	Inverting Input Channel C.
10	9	+IN C	Noninverting Input Channel C.
11	10	V−	Negative Supply Voltage.
12	11	+IN D	Noninverting Input Channel D.
13	12	−IN D	Inverting Input Channel D.
14	14	OUT D	Output Channel D.
Not applicable	13, 16	NIC	Not Internally Connected.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to V−.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

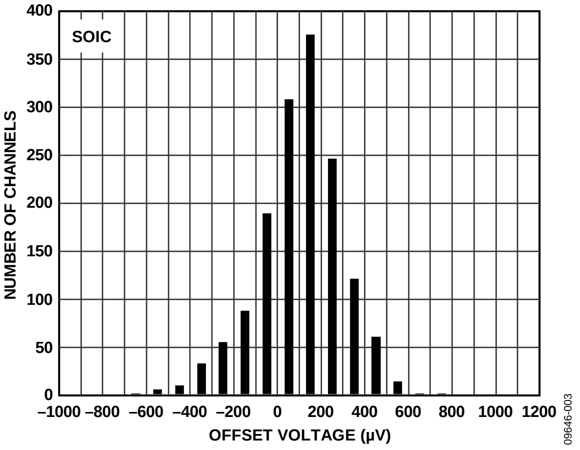


Figure 8. Input Offset Voltage Distribution, V_{SY} = ±5 V

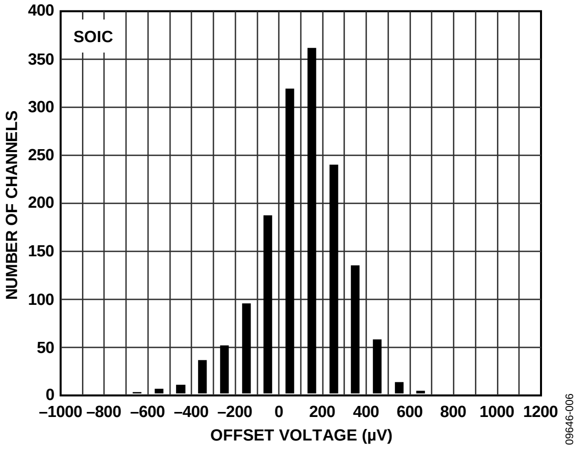


Figure 11. Input Offset Voltage Distribution, V_{SY} = ±15 V

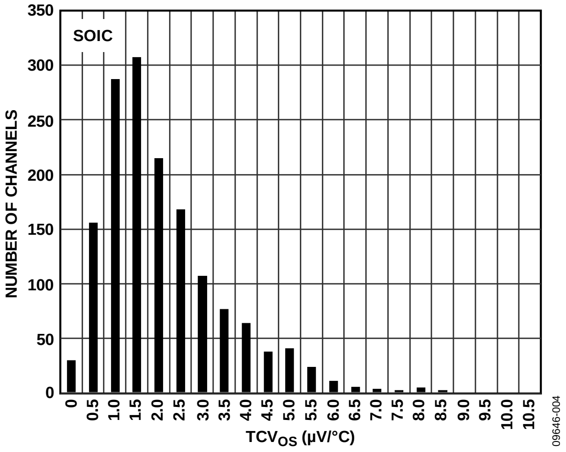


Figure 9. Input Offset Voltage Drift (TCV_{OS}) Distribution, V_{SY} = ±5 V

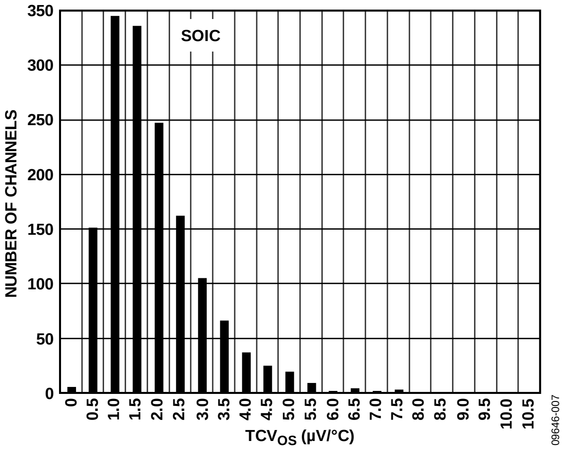


Figure 12. TCV_{OS} Distribution, V_{SY} = ±15 V

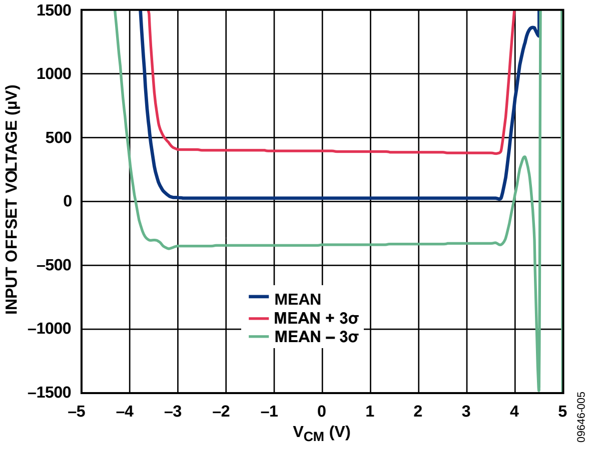


Figure 10. Input Offset Voltage vs. Common-Mode Input Voltage (V_{CM}), V_{SY} = ±5 V, $R_L = \infty$

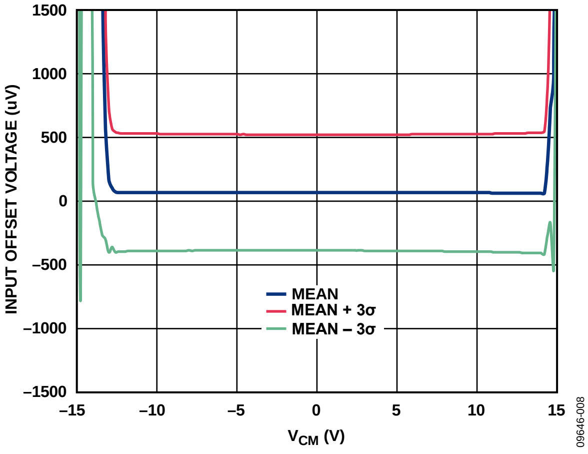


Figure 13. Input Offset Voltage vs. Input Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V, $R_L = \infty$

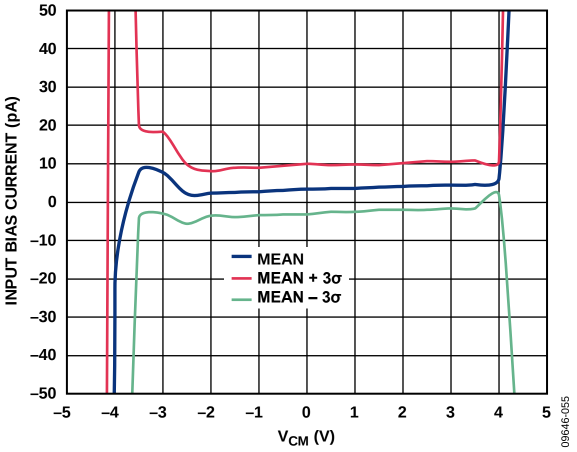


Figure 14. Input Bias Current vs. Common-Mode Input Voltage (V_{CM}), V_{SY} = ±5 V, $R_L = \infty$

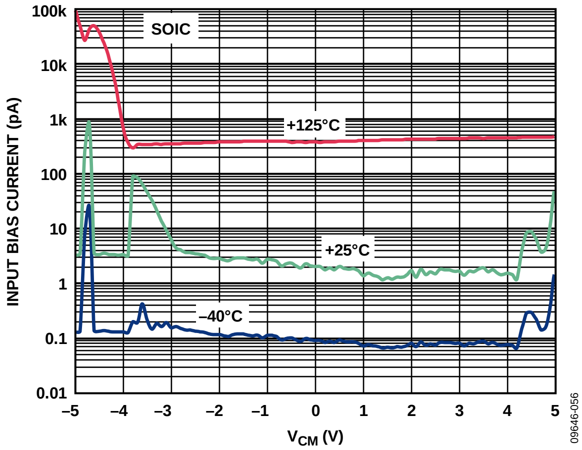


Figure 15. Input Bias Current vs. Common-Mode Input Voltage (V_{CM}), V_{SY} = ±5 V, $R_L = \infty$

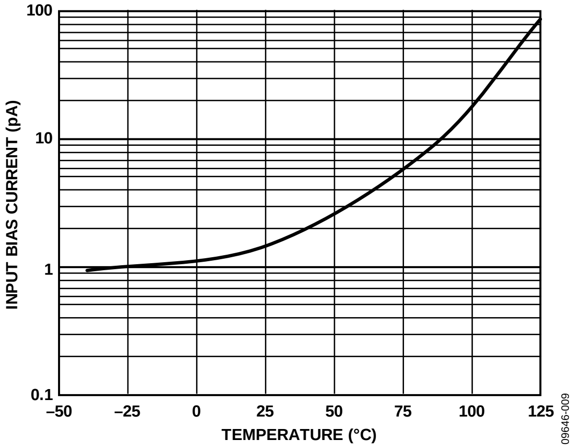


Figure 16. Input Bias Current vs. Temperature, V_{SY} = ±5 V

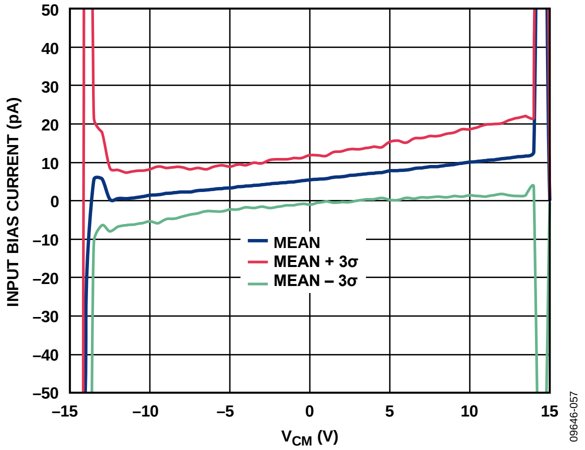


Figure 17. Input Bias Current vs. Common-Mode Input Voltage (V_{CM}), V_{SY} = ±15 V, $R_L = \infty$

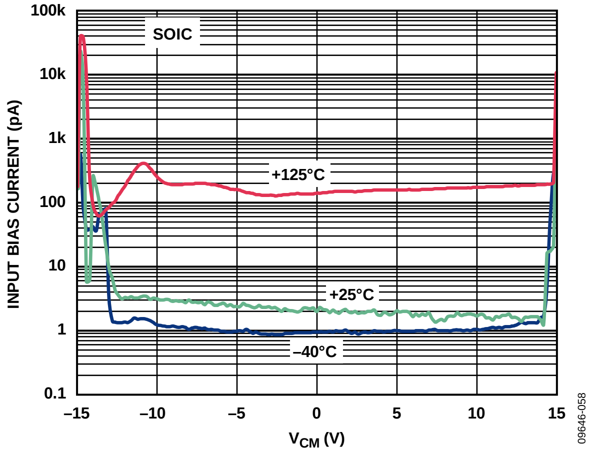


Figure 18. Input Bias Current vs. Common-Mode Input Voltage (V_{CM}), V_{SY} = ±15 V, $R_L = \infty$

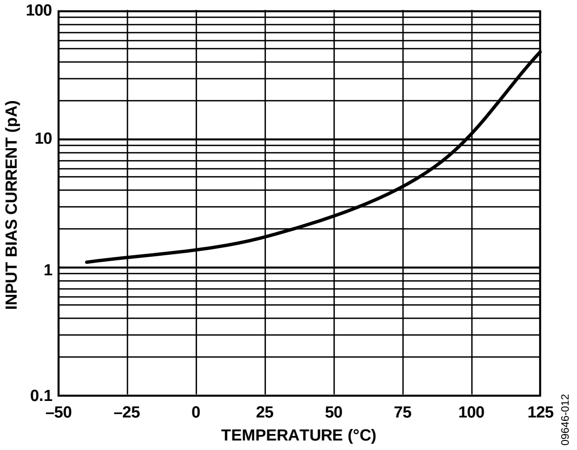


Figure19. Input Bias Current vs. Temperature, V_{SY} = ±15 V

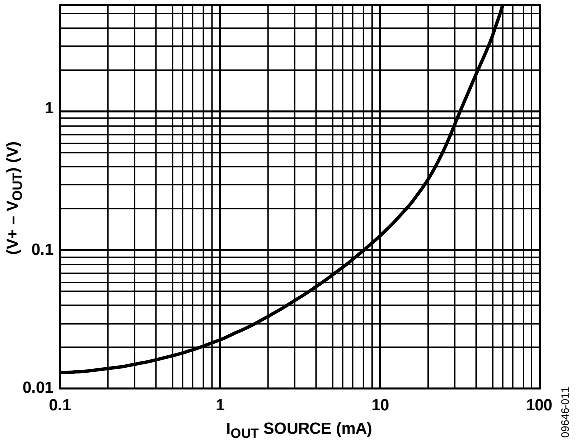


Figure 20. Dropout Voltage (V+ – V_{OUT}) vs. I_{OUT} Source, V_{SY} = ±5 V

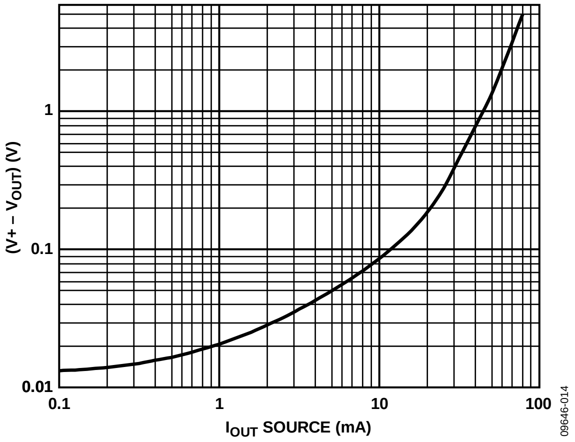


Figure 23. Dropout Voltage (V+ – V_{OUT}) vs. I_{OUT} Source, V_{SY} = ±15 V

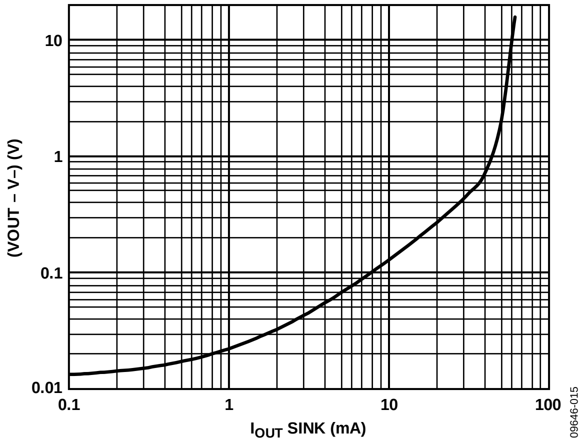


Figure 21. Dropout Voltage (V_{OUT} – V–) vs. I_{OUT} Sink, V_{SY} = ±5 V

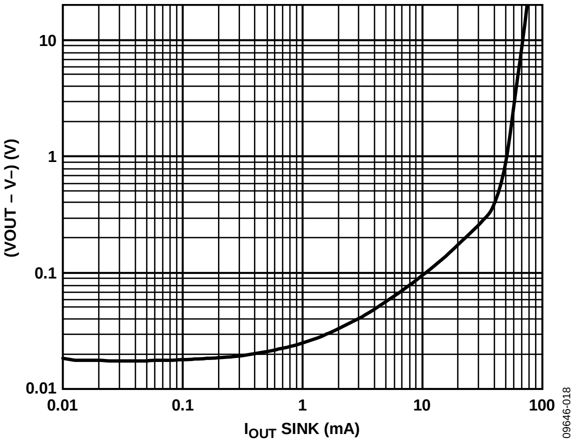


Figure 24. Dropout Voltage (V_{OUT} – V–) vs. I_{OUT} Sink, V_{SY} = ±15 V

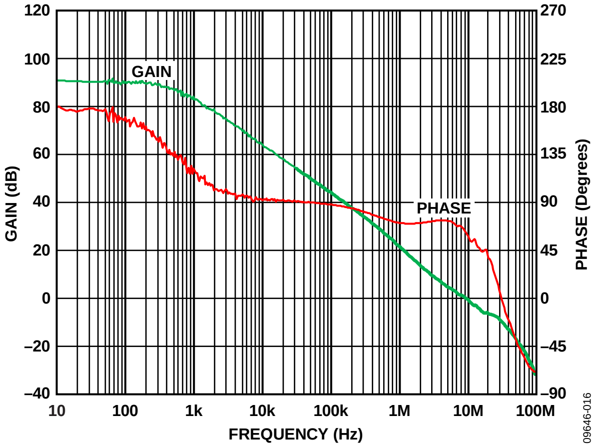


Figure 22. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V, R_L = 2 kΩ, V_{IN} = 5 mV

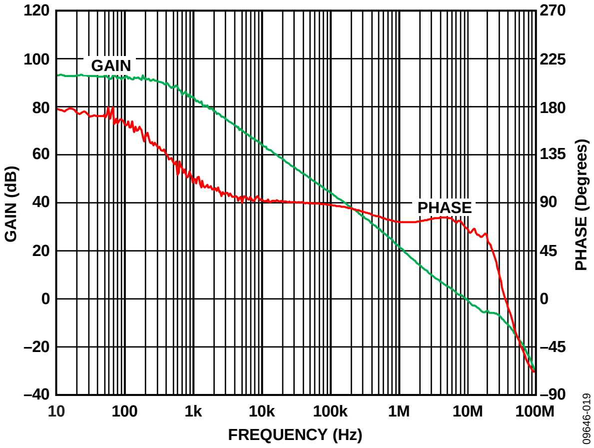


Figure 25. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±15 V, R_L = 2 kΩ, V_{IN} = 5 mV

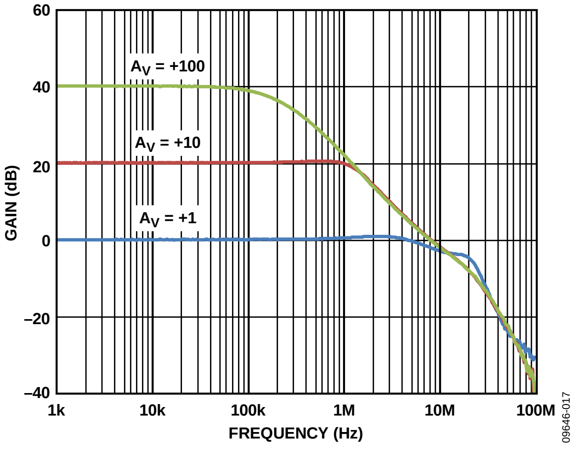


Figure 26. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

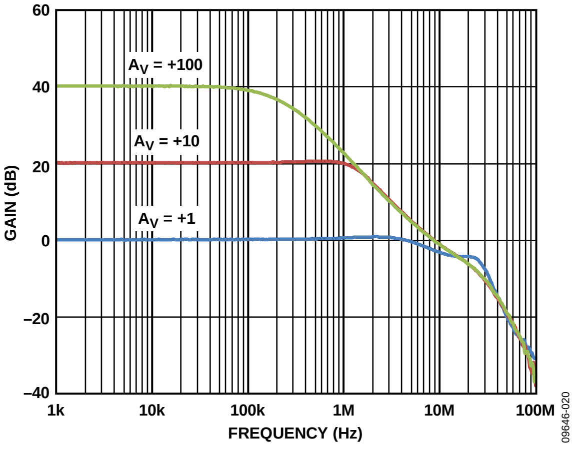


Figure 29. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

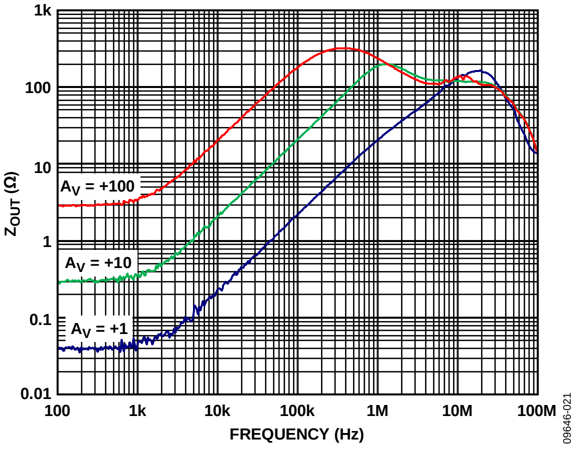


Figure 27. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

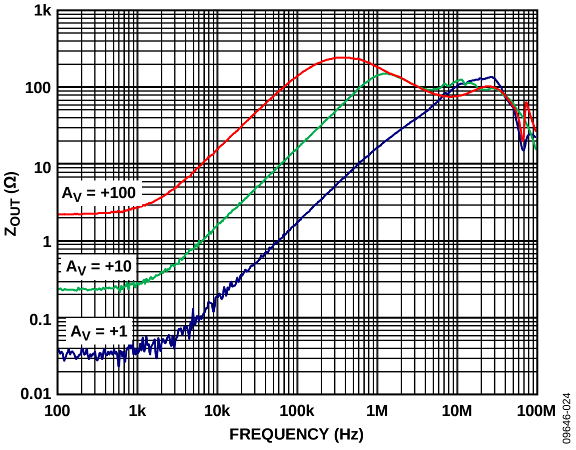


Figure 30. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

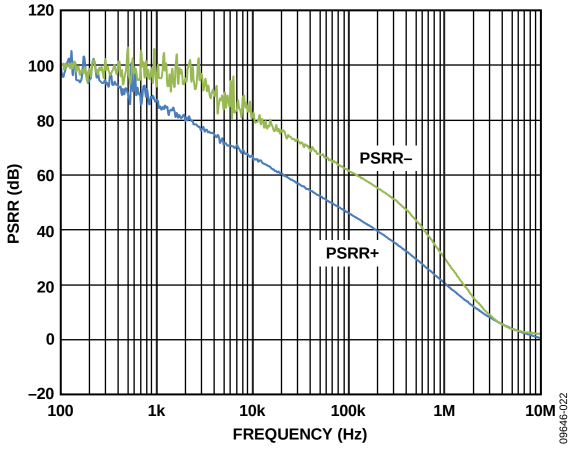


Figure 28. PSRR vs. Frequency, V_{SY} = ±5 V

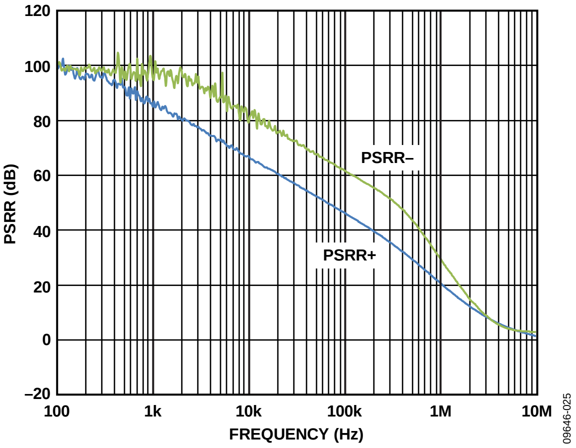


Figure 31. PSRR vs. Frequency, V_{SY} = ±15 V

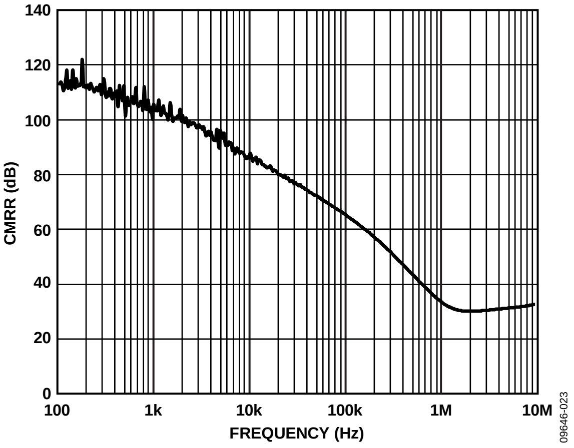


Figure 32. CMRR vs. Frequency, V_{SY} = ±5 V

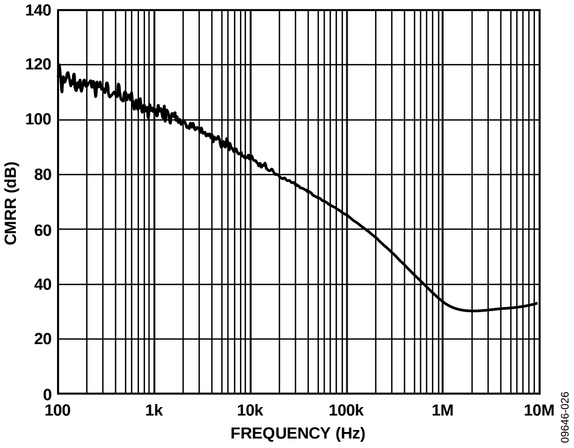


Figure 35. CMRR vs. Frequency, V_{SY} = ±15 V

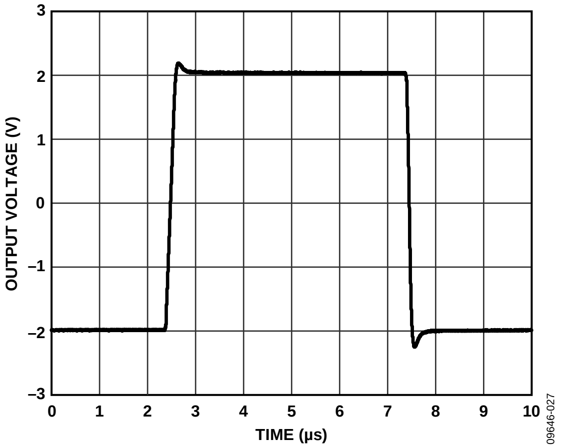


Figure 33. Large Signal Transient Response, V_{SY} = ±5 V, A_V = +1, R_L = 2 kΩ, C_L = 100 pF

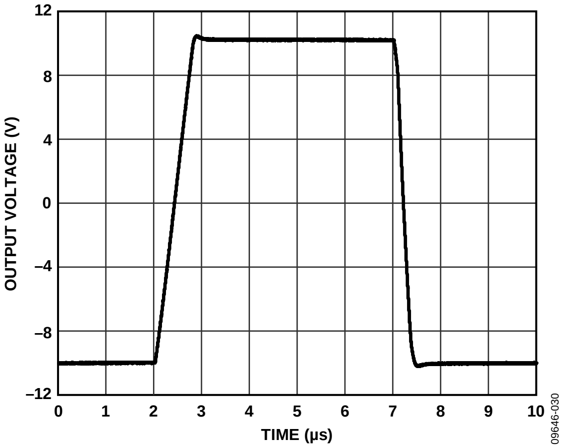


Figure 36. Large Signal Transient Response, V_{SY} = ±15 V, A_V = +1, R_L = 2 kΩ, C_L = 100 pF

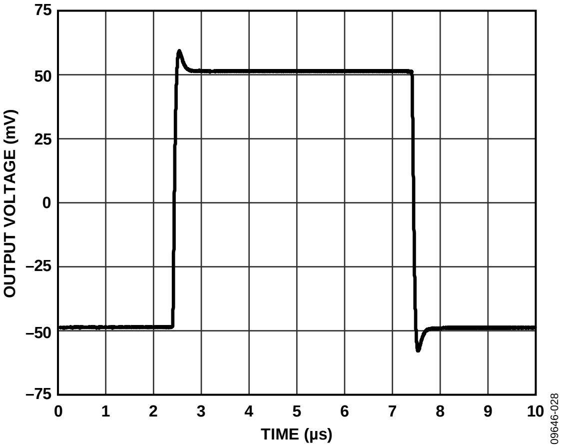


Figure 34. Small Signal Transient Response, V_{SY} = ±5 V, A_V = +1, R_L = 2 kΩ, C_L = 100 pF

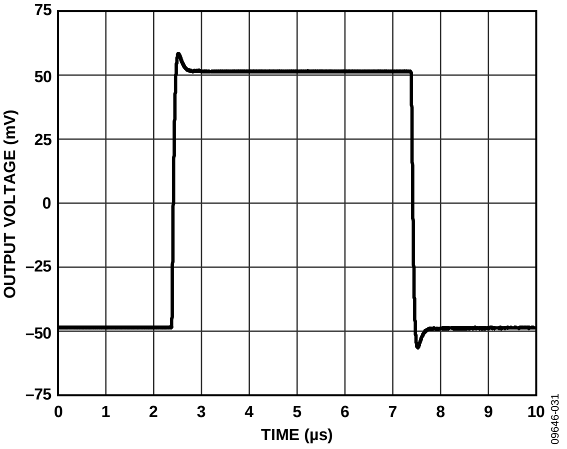


Figure 37. Small Signal Transient Response, V_{SY} = ±15 V, A_V = +1, R_L = 2 kΩ, C_L = 100 pF

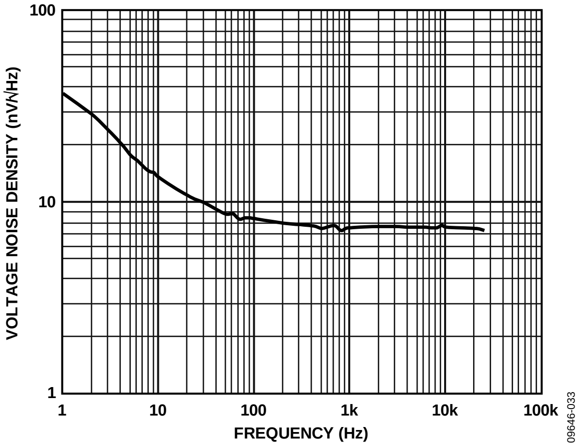


Figure 38. Voltage Noise Density vs. Frequency, V_{SY} = ±5 V

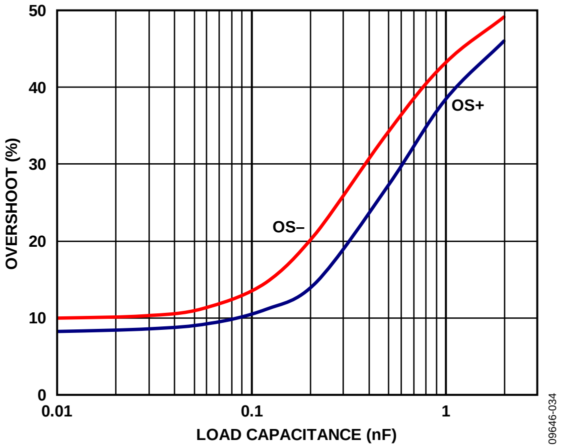


Figure 39. Overshoot vs. Load Capacitance, V_{SY} = ±5 V, A_V = +1, R_L = 2 kΩ, V_{IN} = 100 mV p-p

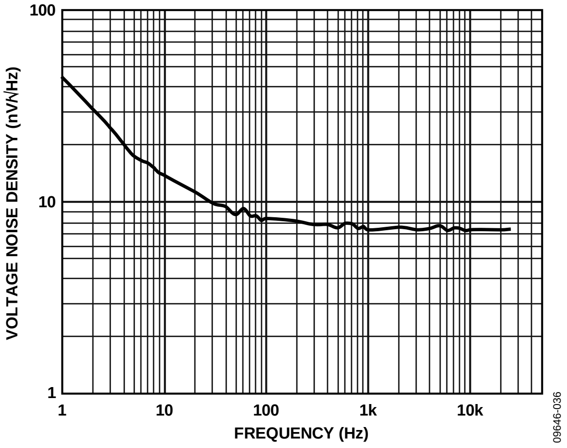


Figure 40. Voltage Noise Density vs. Frequency, V_{SY} = ±15 V

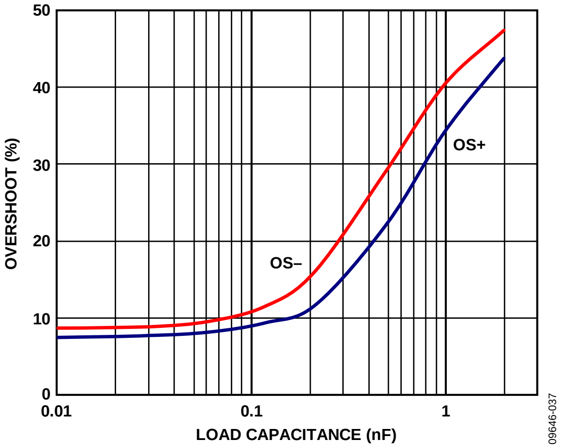


Figure 41. Overshoot vs. Load Capacitance, V_{SY} = ±15 V, A_V = +1, R_L = 2 kΩ, V_{IN} = 100 mV p-p

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

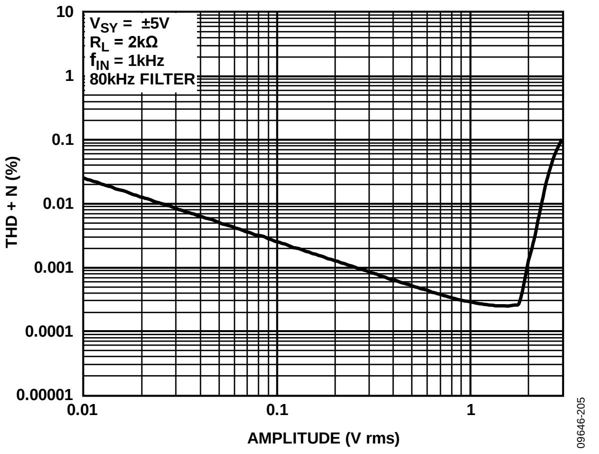


Figure 42. THD + N vs. Amplitude, V_{SY} = ±5 V

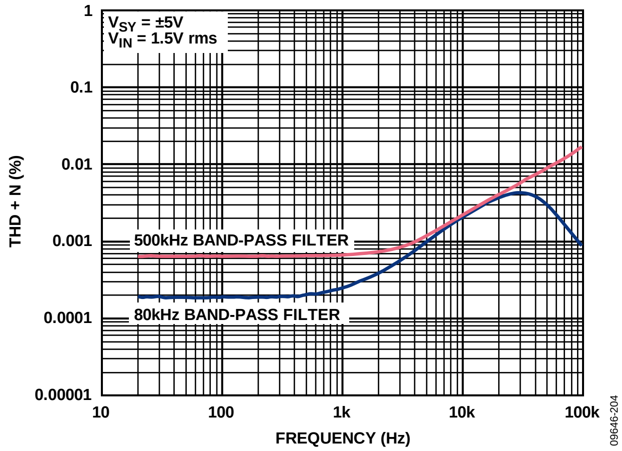


Figure 43. THD + N vs. Frequency, V_{SY} = ±5 V

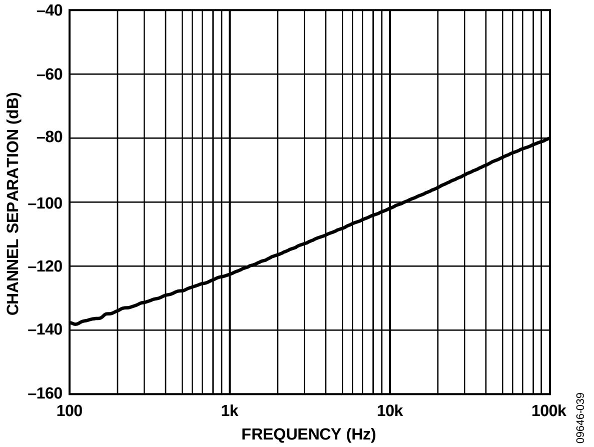


Figure 44. Channel Separation vs. Frequency

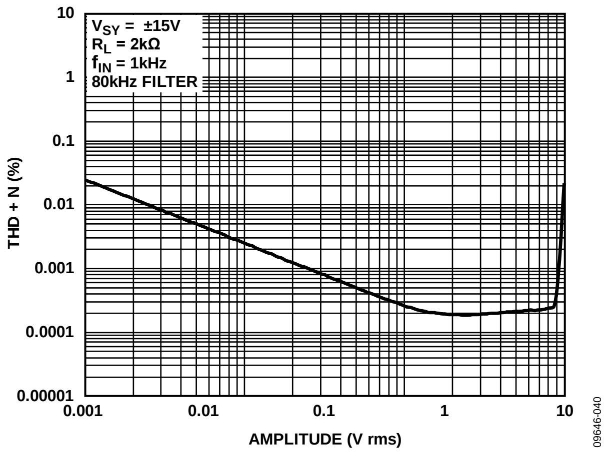


Figure 45. THD + N vs. Amplitude, V_{SY} = ±15 V

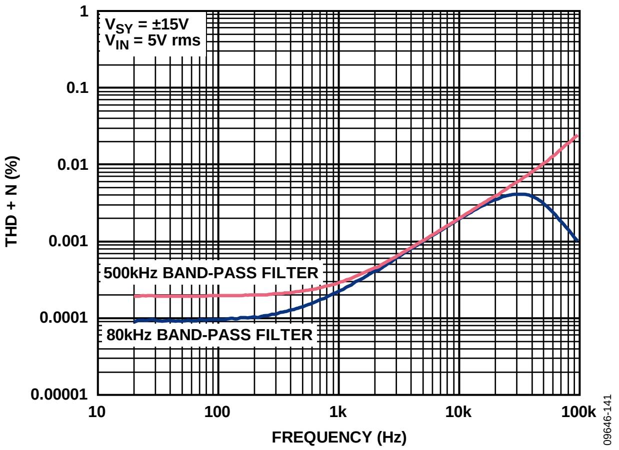


Figure 46. THD + N vs. Frequency, V_{SY} = ±15 V

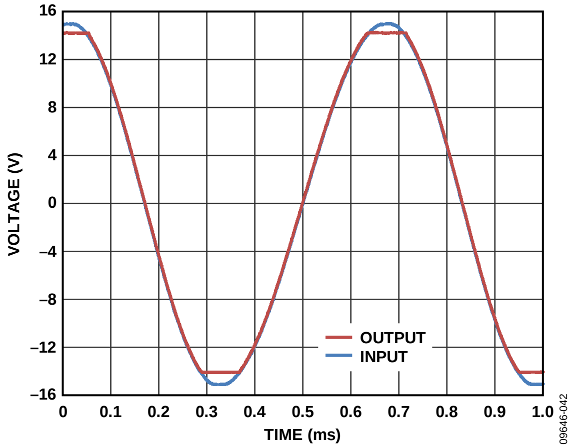


Figure 47. No Phase Reversal, V_{SY} = ±15 V, A_V = +1, R_L = 2 kΩ, C_L = 100 pF

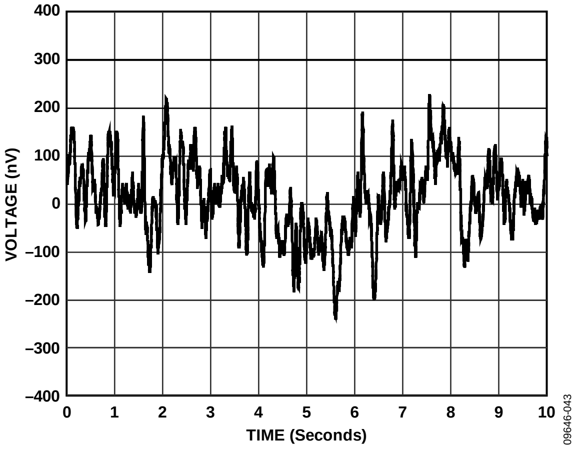


Figure 48. Voltage Noise, 0.1 Hz to 10 Hz

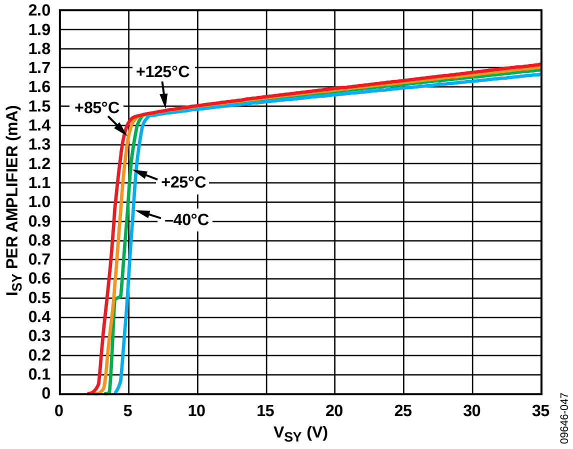


Figure 51. Supply Current (I_{SY}) per Amplifier vs. Supply Voltage (V_{SY}) at Various Temperatures

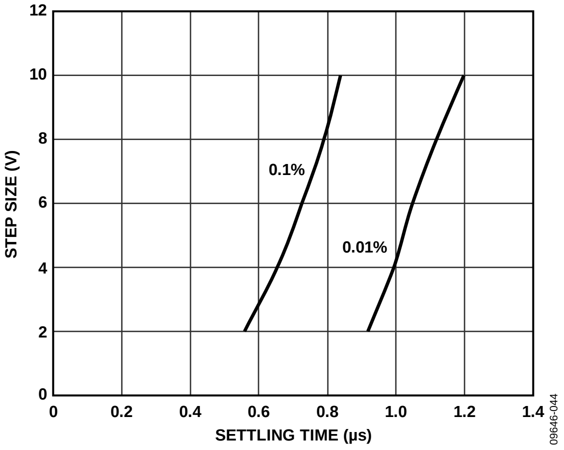


Figure 49. Positive Step Settling Time

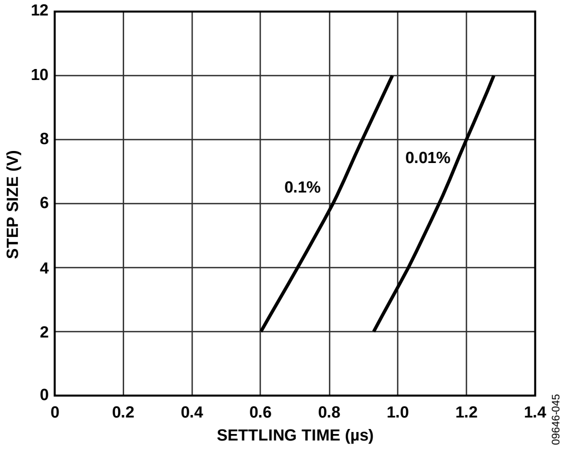


Figure 52. Negative Step Settling Time

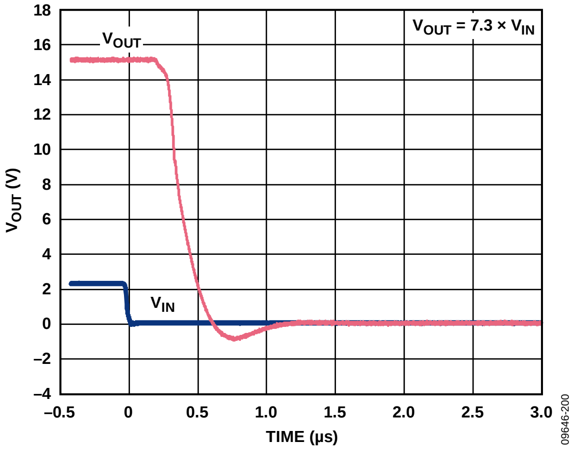


Figure 50. Positive Overload Recovery

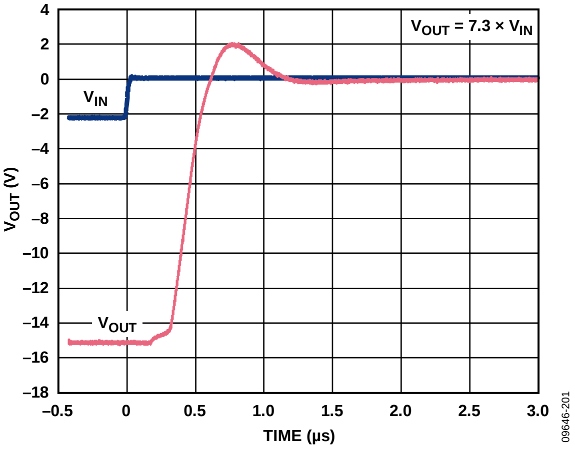


Figure 53. Negative Overload Recovery

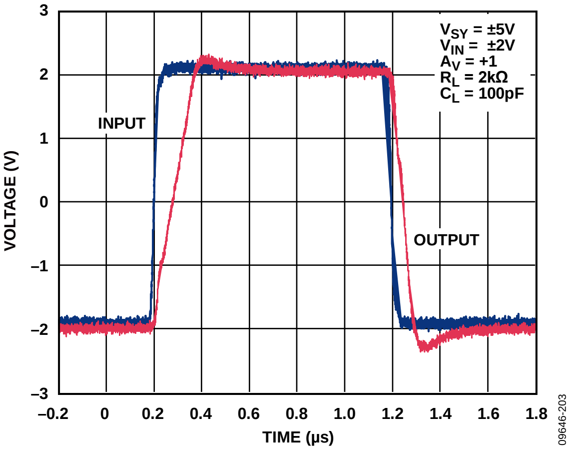


Figure 54. Positive and Negative Slew Rate (V_{SY} = ±5 V, A_V = +1, R_L = 2 kΩ)

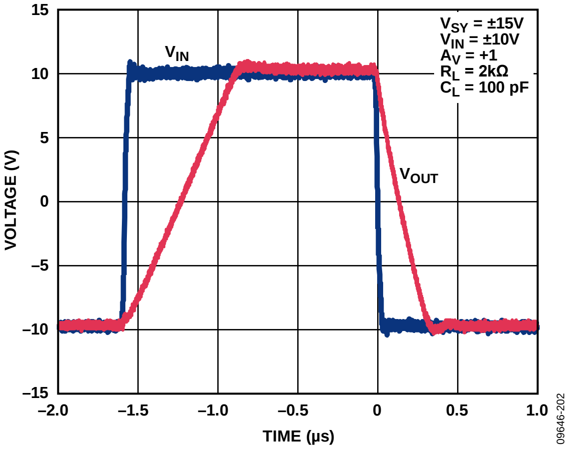


Figure 55. Positive and Negative Slew Rate (V_{SY} = ±15 V, A_V = +1, R_L = 2 kΩ)

FUNCTIONAL DESCRIPTION

The ADA4610-1/ADA4610-2/ADA4610-4 are manufactured using the Analog Devices, Inc. *i*Polar® process, a 36 V dielectrically isolated (DI) process with P-channel JFET technology. The unique architecture of the ADA4610-1/ADA4610-2/ADA4610-4 makes it possible to combine high precision and high speed characteristics into a high voltage, low power op amp. A simplified schematic for the ADA4610-1/ADA4610-2/ADA4610-4 is shown in Figure 56. The JFET input stage architecture offers advantages of low input bias current, high bandwidth, high gain, low noise, and no phase reversal when the applied input signal exceeds the common-mode voltage range. The output stage is rail to rail with high drive characteristics and low dropout voltage for both sinking and sourcing currents.

The ADA4610-1/ADA4610-2/ADA4610-4 are unconditionally stable for all gain configurations, even with capacitive loads well in excess of 1 nF. The devices have internal protective circuitry that allows voltages as high as 0.3 V beyond the supplies to be applied at the input of either terminal without causing damage (for higher input voltages, refer to the Input Overvoltage Protection section). The ADA4610-1/ADA4610-2 B grades achieve less than 0.4 mV of offset and 4 µV/°C of offset drift; these characteristics are usually associated with very high precision bipolar input amplifiers. The gate current of a typical JFET doubles every 10°C, resulting in a similar increase in input bias current over temperature. The low power consumption characteristic of the ADA4610-1/ADA4610-2/ADA4610-4 minimizes the die temperature, which warrants low input bias currents even at elevated ambient temperatures, making the amplifiers ideal for applications that require low leakage specifications without active cooling. Give special care to the printed circuit board (PCB) layout to minimize leakage currents between PCB traces. Improper layout and board handling may generate leakage currents exceeding the bias currents of the operational amplifier.

The ADA4610-1/ADA4610-2/ADA4610-4 are fully specified with supply voltages from ±5 V to ±15 V over the extended industrial temperature range of −40°C to +125°C. The ADA4610-1 is available in an 8-lead SOIC_N. The ADA4610-2 is available in an 8-lead MSOP, an 8-lead SOIC_N, and an 8-lead LFCSP_VD. The ADA4610-4 is available in a 14-lead SOIC_N and a 16-lead LFCSP_WQ. All these packages are surface-mount type.

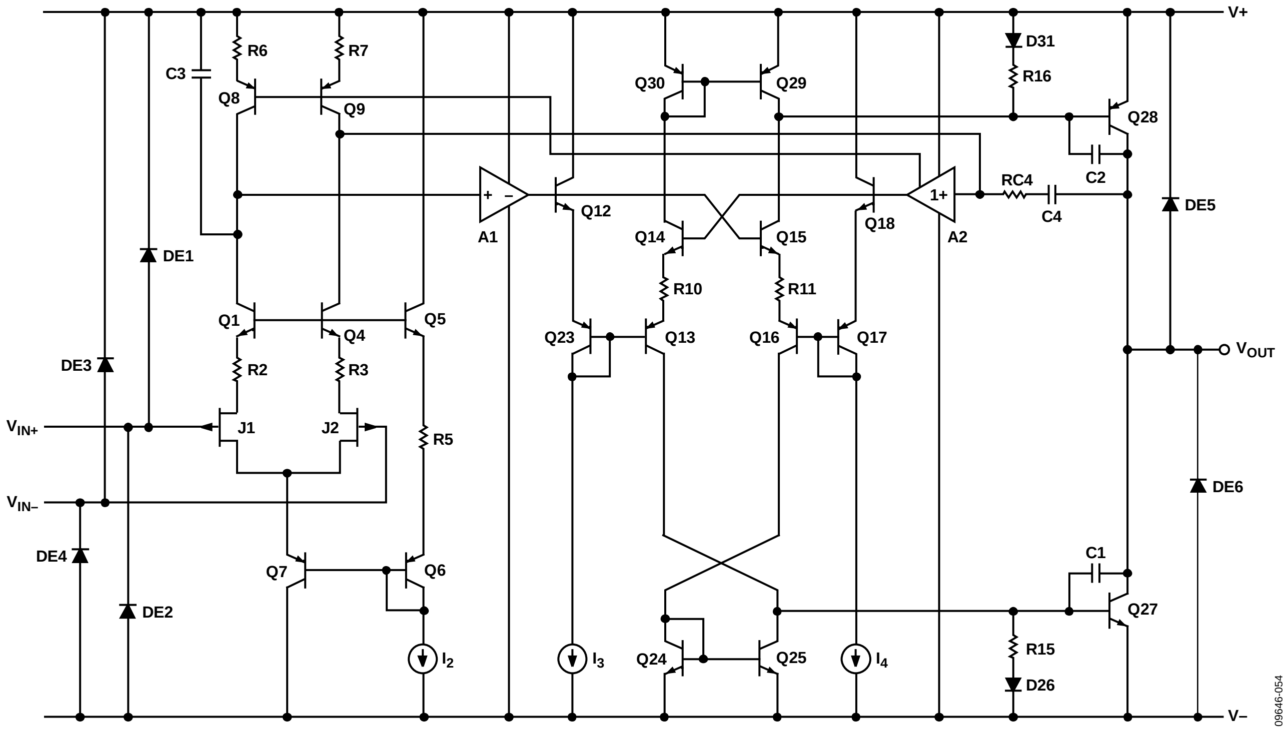


Figure 56. Simplified Schematic

APPLICATIONS INFORMATION

INPUT OVERVOLTAGE PROTECTION

The ADA4610-1/ADA4610-2/ADA4610-4 have internal protective circuitry that allows voltages as high as 0.3 V beyond the supplies to be applied at the input of either terminal without causing damage. For higher input voltages, a series resistor is necessary to limit the input current. Determine the resistor value by

$$\frac{V_{IN} - V_S}{R_S} \leq 10 \text{ mA}$$

where:
V_{IN} is the input voltage.
V_S is the voltage of either V+ or V−.
R_S is the series resistor.

With a very low bias current of <1.5 nA up to 125°C, higher resistor values can be used in series with the inputs. A 5 kΩ resistor protects the inputs from voltages as high as 25 V beyond the supplies and adds less than 10 µV to the offset.

PEAK DETECTOR

The function of a peak detector is to capture the peak value of a signal and produce an output equal to it. By taking advantage of the dc precision and super low input bias current of the JFET input amplifiers, such as the ADA4610-1/ADA4610-2/ADA4610-4, a highly accurate peak detector can be built, as shown in Figure 57.

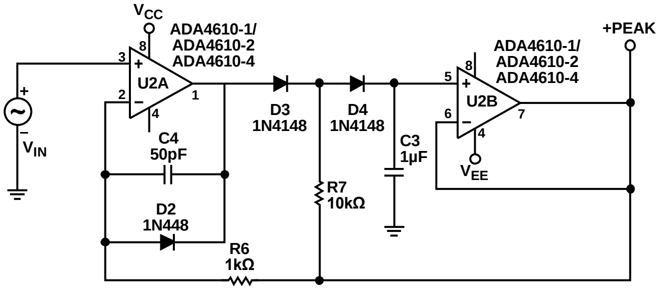


Figure 57. Positive Peak Detector

In this application, Diode D3 and Diode D4 act as unidirectional current switches that open up when the output is kept constant (in hold mode). To detect a positive peak, U2A drives C3 through D3, and D4 until C3 is charged to a voltage equal to the input peak value. Feedback from the output of the U2B (+ peak) through R6 limits the output voltage of U2A. After detecting the peak, the output of U2A swings low but is clamped by D2. Diode D3 reverses bias and the common node of D3, D4, and R7 is held to a voltage equal to + peak by R7. The voltage across D4 is 0 V; therefore, its leakage is small. The bias current of U2B is also small. With almost no leakage, C3 has a long hold time.

The ADA4610-1/ADA4610-2/ADA4610-4, shown in Figure 57, are a perfect fit for building a peak detector because U2A requires dc precision and high output current during fast peaks, and U2B requires low input bias current (I_B) to minimize capacitance discharge between peaks. A low leakage and low dielectric absorption capacitor, such as polystyrene or polypropylene, is required for C3. Reversing the diode directions causes the circuit to detect negative peaks.

CURRENT TO VOLTAGE (I TO V) CONVERSION APPLICATIONS

Photodiode Circuits

Common applications for I to V conversion include photodiode circuits where the amplifier converts a current emitted by a diode placed at the negative input terminal into an output voltage.

The low input bias current, wide bandwidth, and low noise of the ADA4610-1/ADA4610-2/ADA4610-4 make them excellent choices for various photodiode applications, including fax machines, fiber optic controls, motion sensors, and barcode readers.

The circuit shown in Figure 58 uses a silicon diode with zero bias voltage. This setup is a photovoltaic mode, which uses many large photodiodes. This configuration limits the overall noise and is suitable for instrumentation applications.

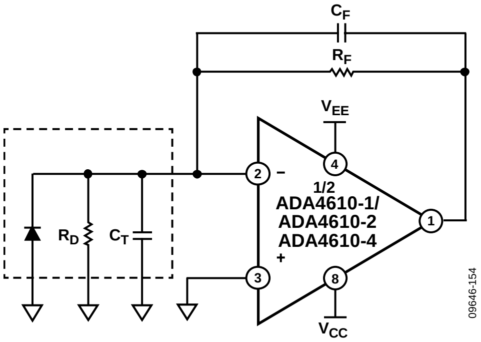


Figure 58. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance (C_T) consists of the sum of the diode capacitance (typically 30 pF to 40 pF) and the amplifier input capacitance (<10 pF), which includes external parasitic capacitance. C_T creates a zero in the frequency response that can lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, place a capacitor in the feedback loop of the circuit shown in Figure 58. The capacitor creates a pole and yields a bandwidth with a corner frequency of

$$1/(2\pi(R_F C_F))$$

where:
R_F is the feedback resistor.
C_F is the feedback capacitor.

Determine the R_F value by the following ratio:

$$V/I_D$$

where:
V is the desired output voltage of the op amp.
I_D is the diode current.

For example, if I_D is 100 µA and a 10 V output voltage is needed, R_F must be 100 kΩ. The resistance of the photodiode (R_D) is a junction resistance (see Figure 58).

A typical value for R_D is 1000 MΩ. Because $R_D >> R_F$, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

$$f_{MAX} = \sqrt{\frac{ft}{2\pi R_F C_T}}$$

where *ft* is the unity-gain frequency of the op amp.

Calculate C_F by

$$C_F = \sqrt{\frac{C_T}{2\pi R_F ft}}$$

where *ft* is the unity-gain frequency of the op amp, and it achieves a phase margin, φ_M, of approximately 45°.

Increase the C_F value to obtain a higher phase margin. Setting C_F to twice the previous value yields approximately $\varphi_M = 65°$ and a maximal flat frequency response, but it reduces the maximum signal bandwidth by 50%.

Using the previous parameters with a $C_F \approx 7$ pF, the signal bandwidth is approximately 250 kHz.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp can be used as a comparator; however, this is not recommended for rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the device operating in open-loop mode, the second stage increases the current drive to the ratioed mirror to close the loop. However, the second stage cannot close the loop, which results in an increase in supply current. With the ADA4610-1/ADA4610-2/ADA4610-4 op amps configured as comparators, the supply current can be significantly higher (see Figure 59 for the supply current vs. the supply voltage for the ADA4610-4). Configuring an unused section as a voltage follower with the noninverting input connected to a voltage within the input voltage range is recommended. The ADA4610-1/ADA4610-2/ADA4610-4 have a unique output stage design that reduces the excess supply current but does not entirely eliminate this effect when the op amp is operating in open-loop mode.

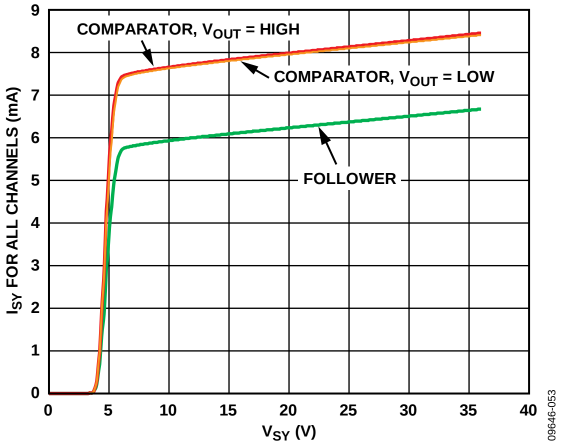
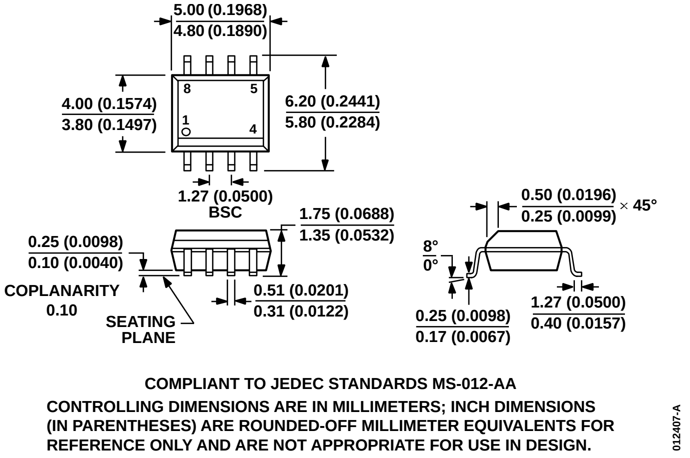


Figure 59. Supply Current (I_{SY}) vs. Supply Voltage (V_{SY}) for the ADA4610-4 Only

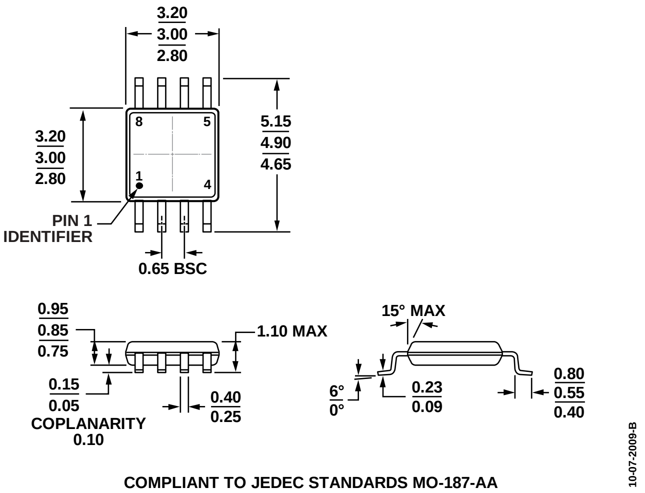
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

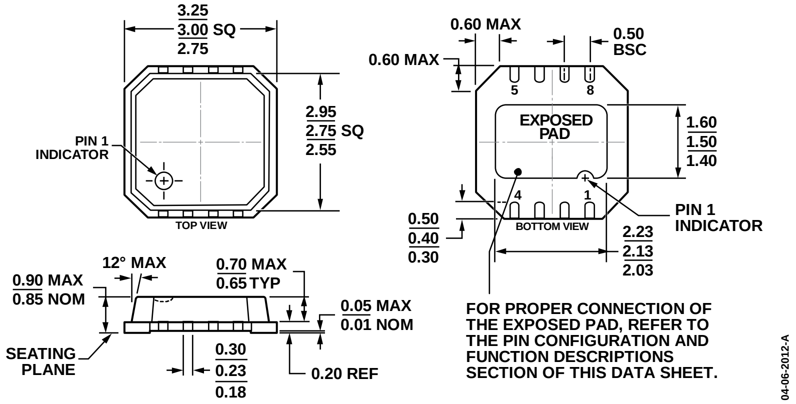
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 60. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



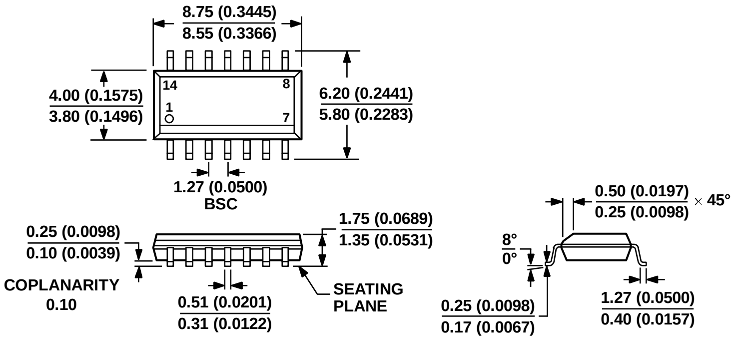
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 61. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

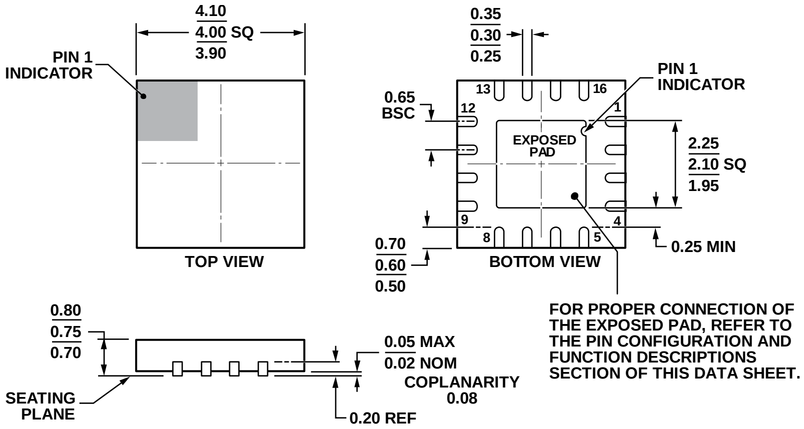
Figure 62. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 63. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 64. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4610-1ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-1ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-1ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-1BRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-1BRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-1BRZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-9	A2U
ADA4610-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-9	A2U
ADA4610-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2U
ADA4610-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2U
ADA4610-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2U
ADA4610-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2BRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2BRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-2BRZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4610-4ARZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4610-4ARZ-R7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4610-4ARZ-RL	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADA4610-4ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	
ADA4610-4ACPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	

[1] Z = RoHS-Compliant Part.

D09646-0-4/15(E)

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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http://moschip.ru/get-element

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