Version 1.2 2005

PEX 8311

PCI Express to Generic Local Bus Bridge

Features

- **PEX 8311 Key Features**
  - PCI Express to Generic Local Bus Bridge
  - Root Complex and EndPoint Modes of Operation
  - Local Bus modes:
    - 32-bit address & 32-bit data C Mode
    - Multiplexed 32-bit address/data J Mode
  - Local Bus Clock rates to 66MHz
  - Zero wait state bursts to 264 MB/sec
  - 1 Lane PCI Express Port
  - 2 DMA Channels
  - Integrated SerDes
  - 21mmx21mm, 337 pin PBGA package
  - 3.3V I/O and 5V tolerant Local Bus
  - Power: 1.0 Watt
- **PEX 8311 Additional Features**
  - Integrated PCI Express Interface
    - Compliant to PCIe Specification, r1.0a
    - x1 Link, dual-simplex, 2.5 Gbps/direction
    - Auto Polarity reversal
    - 128 Byte payload maximum
    - Link CRC support
    - Link/Device power management
    - Flow control buffering
    - PCIe transaction queues for eight outstanding TLPs
  - VGA/ISA Enable Registers
  - On-the-fly Endian conversion
  - Multiple DMA operational modes
    - Block and scatter/gather transfers
    - DMA descriptor ring management
    - Demand mode & EOT H/W controls
  - Direct Master data transfers
    - Read ahead and programmable read pre-fetch counter
    - Generate any PCIe transaction
  - Direct Slave data transfers
    - 8-,16-, and 32-bit local bus access
    - Writes, read ahead, posted writes, programmable read pre-fetch counter
  - Control
    - Eight mailbox and two doorbell registers
    - Root Complex or EndPoint mode reset/interrupt
    - Serial EEPROM Interface
    - DC JTAG Boundary Scan
    - Four GPIO Pins, 1 GPO, 1 GPI
    - I2O Messaging Unit

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

Multi-purpose and Feature-Rich PCI Express Bridge

The bridge offers PCI Express™ (PCIe) bridging capability from a Generic Local Bus to PCIe enabling users to add scalable high bandwidth interconnection to a wide variety of applications including communication line cards, surveillance systems, video capture cards, industrial control, office automation, IP Media Servers, RAID systems and medical imaging. Many embedded system designs utilizing PCI today can easily migrate to PCIe. The ExpressLane™ PEX 8311 bridge can be used in Root Complex mode with the device directly interfacing multiple local bus devices including processors and FPGAs to a downstream PCIe port. The bridge can also function in an EndPoint type application connecting multiple local bus components to an upstream PCIe port.

Highly Flexible, Generic Local Bus

The PEX 8311 offers a highly flexible yet low overhead generic Local Bus which provides a direct connection to two generic industry-standard interconnect buses. The bus protocol can be set to the non-multiplexed address and data mode with up to 32-bit transfers "C-Mode" or multiplexed address/data with up to 32-bit transfers "J-Mode". This bus can be directly connected to many processors with minimal or no glue logic. Memory, FPGAs, FIFOs and other devices can be simultaneously placed on this bus.

Dual Independent DMA Channels

The PEX 8311 provides two data transfer channels each with internal independent programmable FIFOs. These channels provide independent data transfers with the bridge initiating both the PCIe and local bus. With dual channels, data from two different sources or bidirectional traffic can be transferred simultaneously without the need to finish one transfer before starting the second. Each DMA channel can use independent scatter-gather descriptor lists for increased flexibility. The use of DMA descriptors allows the two channels to look like multiple virtual DMA channels.

Complete Conversion from PCI Express Signaling

The PEX 8311 provides a complete local bus to PCIe translation. The bridge is equipped with a standard PCIe port that operates as a single x1 link with a maximum of 250 Megabytes per second of throughput per transmit and receive directions. The single 2.5 Gbps integrated SerDes delivers the highest bandwidth with the lowest possible pin-count. The device supports internal queues with flow control features to optimize throughput and traffic flow.

Root Complex and EndPoint Modes

The PEX 8311 bridge supports both Root Complex and EndPoint modes of operation. This flexibility allows a Root Complex system designer to utilize the part as a type of "north bridge" whereby multiple Local Bus components present including a processor, FPGAs, memory, DSP, etc., can communicate with each other as well with downstream PCIe devices. In this case, the bridge's configuration and system hierarchy comes through the Local Bus. In EndPoint mode, the bridge is configured through the PCIe port.

Direct Master or Direct Slave Operation

The PEX 8311 bridge provides master (Upstream traffic generation) and slave (Downstream traffic acceptance) capability. These transfers can occur simultaneously with the DMA transfers and are given priority. For master mode requests, the bridge services local bus masters by generating Upstream traffic on the PCIe side. There are two local bus address space maps to PCIe (Direct Master mode): one to memory and one to I/O with the bridge generating PCIe memory and I/O transaction types. The bridge has independent large depth Read and Write FIFOs. Read ahead and programmable read pre-fetch counters enhance performance. Register configuration is through the PCIe port, Local Bus or through an optional EEPROM.

The PEX 8311 also supports direct slave requests where the bridge services PCIe side Downstream traffic initiators by mastering the Local Bus side. The bridge has two general purpose address spaces and one Expansion ROM space that could be used as a general purpose direct slave space map to the Local Bus. Each address space may be configured for 8-, 16-, or 32-bit Local Bus data widths for flexible connectivity to Local Bus devices. Independent Read and Write FIFOs of large depth provide buffering. Performance is enhanced through deferred writes, posted writes, read ahead, and programmable read pre-fetch counters.

Hardware DMA Controls-EOT /Demand Mode

To optimize data transfers in many applications, particularly communications, the PEX 8311 supports hardware based control signals. When End of Transfer (EOT#) is asserted, the bridge immediately terminates the current transfer and indicates the number of bytes transferred. Along with unlimited bursting capability, EOT is useful in applications where the lengths of the read packets are not known until the packets are read. Additional hardware signaling control based DMA transfers are available.

With Demand Mode each DMA channel has a pair of hardware signals that are used to pause and resume the current transfer. This allows a peripheral device such as a line card with its own FIFO to control DMA transfers. This mode can be used on many non-FIFO transfers as well in a variety of end applications.

Advanced Performance Features

The PEX 8311 has a variety of added capabilities which enhance throughput and flexibility for all transfer types: DMA, Direct Master and Direct Slave. These include zero wait state local bus bursts to 264 MB/s with programmable burst lengths including unlimited bursting, deep FIFO for maximum PCIe packet generation, unaligned Local Bus transfers of any byte length, on-the-fly Local Bus Endian conversion, programmable Local Bus wait states, and Local Bus parity checking. General purpose messaging for proprietary message schemes include: eight 32-bit registers for polled topologies and two 32-bit doorbell registers for interrupt driven environments.

Fully Compliant Power Management

For applications that require power management, the PEX 8311 device supports both link (L0, L0s, L1, L2/L3 Ready, and L3) and device (D0, D1, D2 and D3) power management states, in compliance with the PCIe power management specification. Full power management event packets are generated and received and translated to local bus signaling.

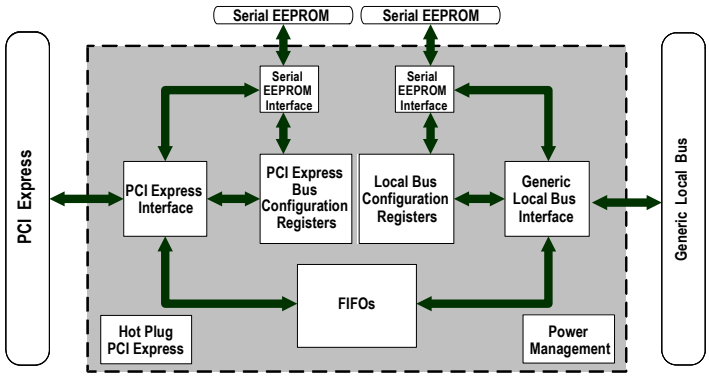
PLX I/O Accelerator Compatibility

The PEX 8311 is Register compatible with existing PLX's bus mastering Local Bus to PCI bridging solutions (PLX PCI 9000 series). For many designs migrating from PCI to PCIe, existing code utilizing these I/O Accelerators can be used. As PCIe and PCI are compatible, designs can quickly be extended to take advantage of PCI Express' bandwidth, system control, and data integrity.

Internal Block Diagram

Figure 1 below shows an overview of the PEX 8311 Bridge. The device provides for full FIFO memory buffers for each DMA channel and for Direct Master and Direct Slave operation. A complete three layer PCIe protocol interface with integrated SerDes provides conversion from local bus data to/from PCI Express port transfers. Modules for Hot Plug and power management are included. Two serial EEPROM interfaces allow an additional configuration option.

Figure 1. High-Speed Data Transfers



Applications

Suitable for Root Complex-centric as well as EndPoint I/O applications, the PEX 8311 can be configured for a wide variety of form factors and applications.

System Controller Card

The PEX 8311 bridge, with its Root Complex mode support, simplified generic local bus interface, PCIe protocol packet conversion, and multiple DMA controllers allows users to use the device as a "north bridge" type application in embedded systems. Such controllers often manage "control path" data. The local bus has the capability to support numerous simultaneous local bus devices. Figure 2 shows the bridge interfacing a local processor, FPGA, and memory to a downstream PCIe port. The PCIe port connects to a switching fabric or I/O card.

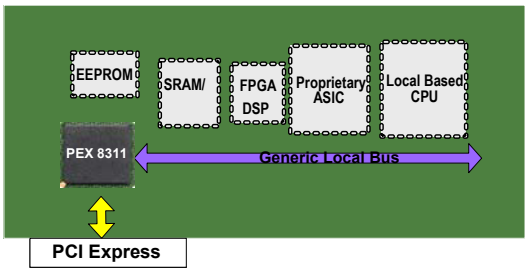


Figure 2. "Northbridge" Host Bridge

Line Card Application

The number and variety of PCI Express native-mode devices is growing quickly. As these devices become mainstream, it will be necessary to create multifunction and multi-port adapter cards with PCI Express capability.

The PEX 8311 can be used to create a communications line card that bridges a local processing device and memory to an upstream PCIe port. The bridge allows a line card to be a backplane or a motherboard. Figure 3 shows the PEX 8311 in this application. In this mode, the bridge acts in an "EndPoint mode". Configuration to the bridge comes from the PCIe. Use of DMA for data path and higher priority simultaneous Direct Master/Slave for control path data is invaluable.

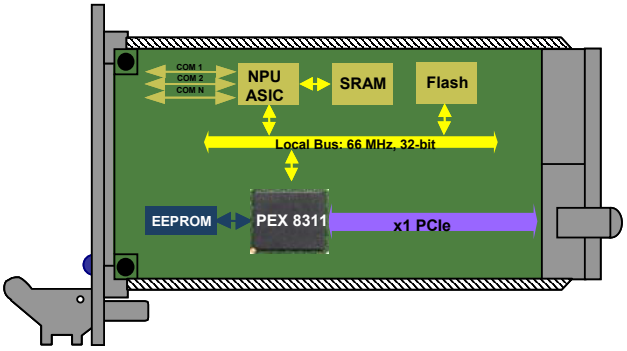


Figure 3. Communications Line Card

Industrial Control Systems

The PEX 8311 is an excellent choice to bridge programmable logic, local processors, and other devices to a PCIe switch. The bridge is fully interoperable with PCIe switches from a variety of PCIe products including multiple switches from PLX Technology with lane counts from 8 to 32. Figure 4 illustrates PEX 8311 bridging programmable logic devices to the PEX 8524 switch. One of the many applications for the bridge is to interface inputs via an FPGA from industrial signals from the manufacturing floor to a PCIe switch where the data is sent to a local processor and then to a central host for system control applications. This use can be generalized to many similar bridging operations such as in instrumentation or medical imaging.

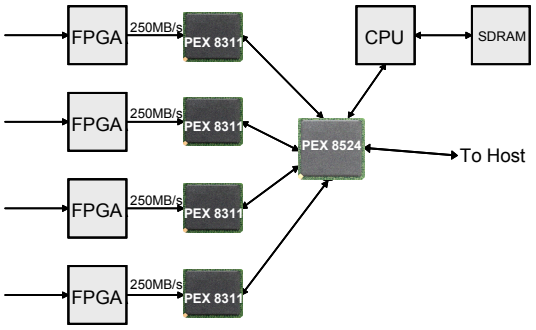


Figure 4. Industrial Control

In this type application, the bridge's x1 lane PCIe 2.5 Gbps bandwidth in combination with its large local bus capacitive loading can support up to five simultaneous input sources on each PEX 8311. With a Local Bus of up to 66 MHz and 32-bit data, complete bandwidth matching with the PCIe port can be achieved in unidirectional designs.

Video Surveillance System

The PEX 8311 is a very economical bridge and can support many "mass market" applications. These applications include PC television capture cards, data acquisition boards, video editing, and surveillance systems. The later is shown in Figure 5 below. This design allows multiple camera sources to feed their inputs through a series of compression, buffering stages and local processing and be bridged to a PCIe switch or directly to a PCIe slot on a motherboard. The PC then allows security personnel to monitor multiple feeds and switch interactively among the various feeds. Video editing by consumers could use a similar design topology as well.

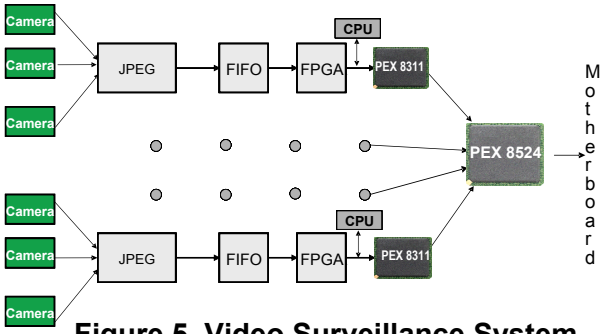


Figure 5. Video Surveillance System

Software Usage Model

From a system model viewpoint, the PEX 8311 has its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI to PCI Bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

Interrupt Sources/Events

The PEX 8311 switch supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX 8311 for hot plug events, and baseline error reporting.

Development Tools

PLX is offering hardware and software tools to enable rapid customer design activity. These tools include the hardware Rapid Development Kit (PEX 8311 RDK) shown in Figure 6 and the Software Development Kit (SDK).

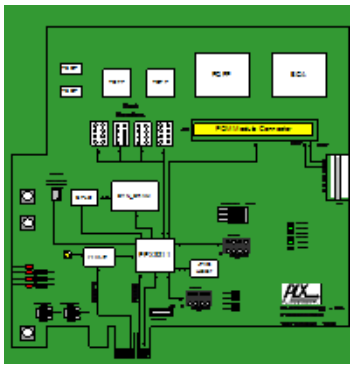


Figure 6. PEX 8311RDK

The RDK hardware module includes the PEX 8311 with a x1 port connected to a male-edge connector, and a Generic Local Bus port with support for non-multiplexed "C" and multiplexed "J" modes. SBSRAM, CPLD components are included with a Prototyping area. The board includes a mid-bus PCIe probe interface and a reset for PCIe. Support for all DMA methods including block mode, scatter-gather, and ring management along with Direct Slave is supported. JTAG provides down-loading of code to the CPLD. An external 100 MHz differential reference clock can be provided at the card edge connector or from the slot.

The PEX 8311RDK can be installed in a motherboard, used as a riser card, or configured as a bench-top board.

The PEX 8311RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for the PEX 8311 features and benefits.

SDK

The SDK tool set includes:

- Linux & Windows NT/98/2000/Me/XP/2003 server drivers
- C/C++ Source code, Objects, and libraries
- User's Guides, Application examples, and Tutorial

Product Ordering Information

Part Number	Description
PEX 8311-AA66BC F	PCI Express to Generic Local Bus Bridge; Lead-free Package
PEX 8311RDK	Rapid Development Kit for PEX 8311
SDK	Windows Host-side and Local side software development kit

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for sampling.

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