

IS61WV6416DALL/DALS

IS61WV6416DBLL/DBLS

IS64WV6416DBLL/DBLS



64K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM

JANUARY 2011

FEATURES

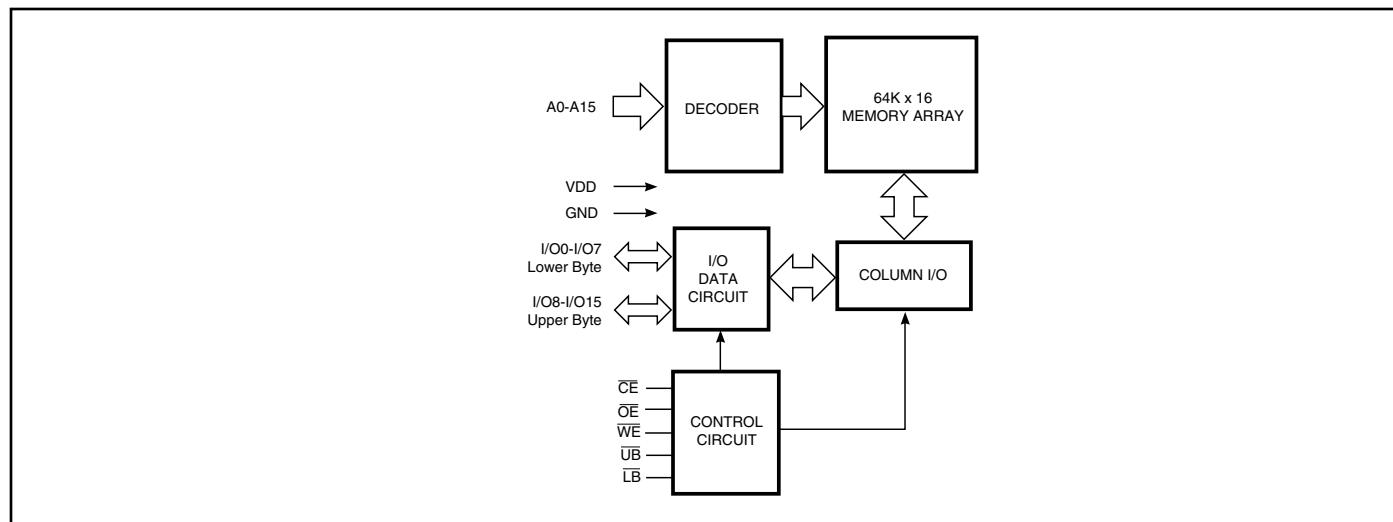
HIGH SPEED: (IS61/64WV6416DALL/DBLL)

- High-speed access time: 8, 10, 12, 20 ns
- Low Active Power: 135 mW (typical)
- Low Standby Power: 12 μ W (typical)
CMOS standby

LOW POWER: (IS61/64WV6416DALS/DBLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 55 mW (typical)
- Low Standby Power: 12 μ W (typical)
CMOS standby
- Single power supply
 - V_{DD} 1.65V to 2.2V (IS61WV6416DAxx)
 - V_{DD} 2.4V to 3.6V (IS61/64WV6416DBxx)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



Copyright © 2010 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

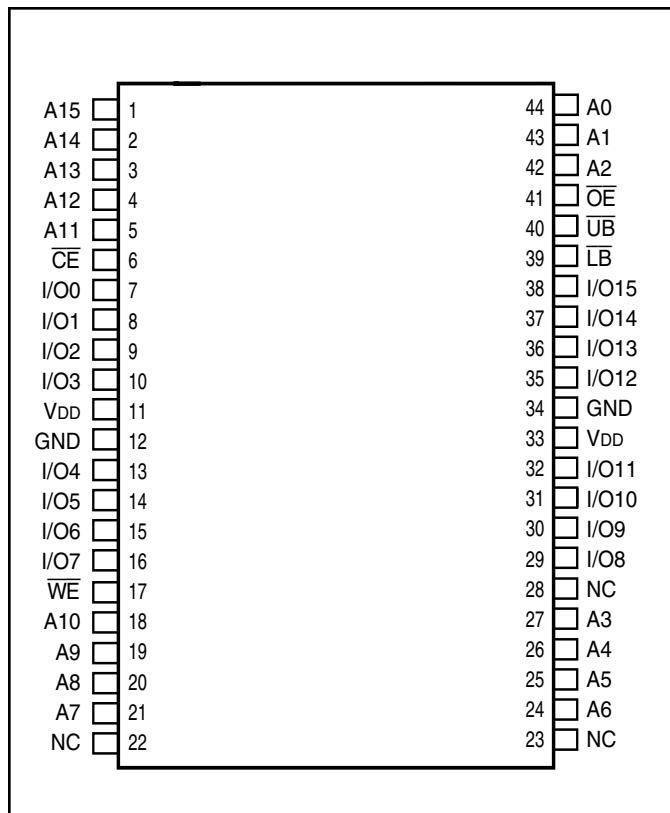
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

TRUTH TABLE

Mode	\overline{WE}	\overline{CE}	\overline{OE}	\overline{LB}	\overline{UB}	I/O PIN		
						I/O0-I/O7	I/O8-I/O15	V _{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I _{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D _{OUT}	High-Z	I _{CC}
	H	L	L	H	L	High-Z	D _{OUT}	
	H	L	L	L	L	D _{OUT}	D _{OUT}	
Write	L	L	X	L	H	D _{IN}	High-Z	I _{CC}
	L	L	X	H	L	High-Z	D _{IN}	
	L	L	X	L	L	D _{IN}	D _{IN}	

PIN CONFIGURATIONS

44-Pin TSOP-II

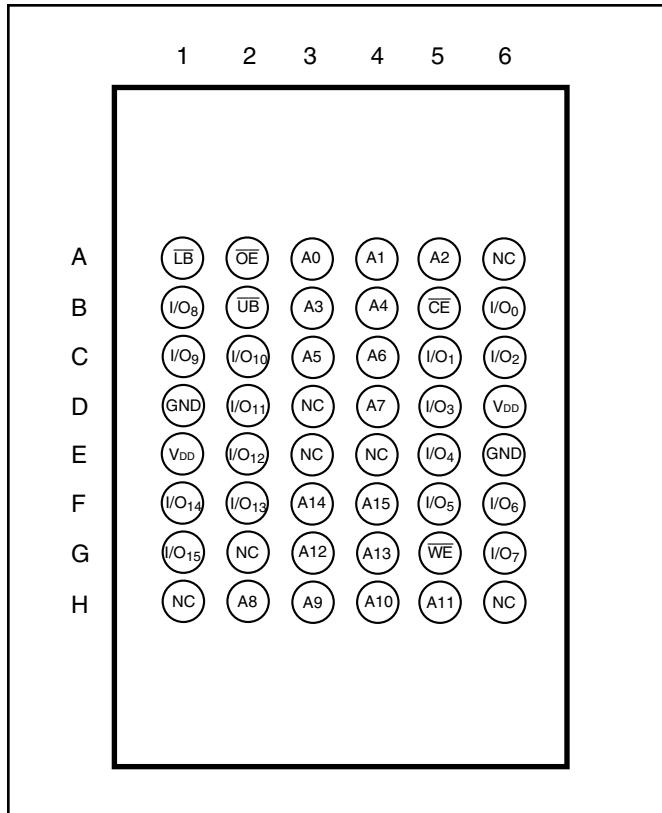


PIN DESCRIPTIONS

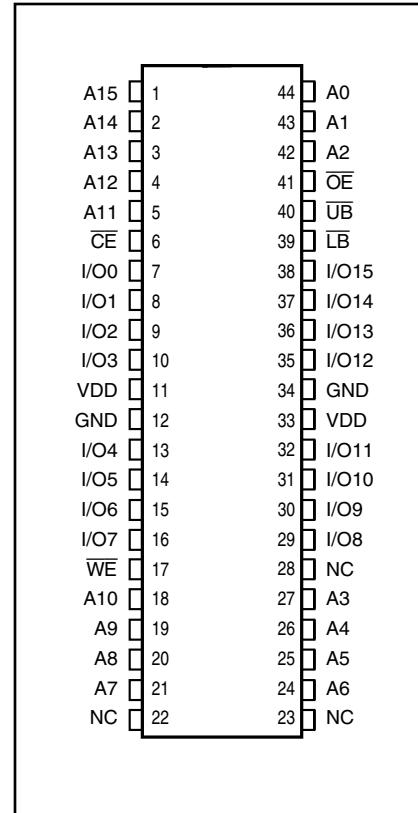
A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
\overline{LB}	Lower-byte Control (I/O0-I/O7)
\overline{UB}	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V _{DD}	Power
GND	Ground

PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)



44-Pin SOJ (K)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
\overline{LB}	Lower-byte Control (I/O0-I/O7)
\overline{UB}	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V _{DD}	Power
GND	Ground

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2	V _{DD} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	-1	1	µA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	-1	1	µA

Note:

1. V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -1.0 mA	1.8	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 1.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{DD} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	-1	1	µA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	-1	1	µA

Note:

1. V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V _{DD}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V _{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V _{DD} + 0.2	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	-1	1	µA	
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	-1	1	µA	

Note:

1. V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V _{DD} - 0.3V	0.4V to V _{DD} - 0.3V	0.4V to V _{DD} - 0.3V
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level (V _{Ref})	V _{DD} /2	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 (Ω)	1909	317	13500
R2 (Ω)	1105	351	10800
V _{TM} (V)	3.0V	3.3V	1.8V

AC TEST LOADS

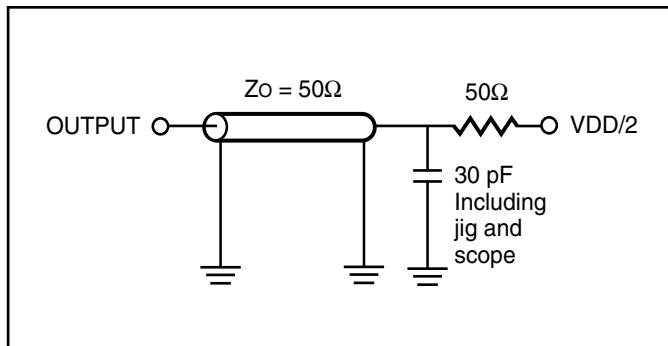


Figure 1.

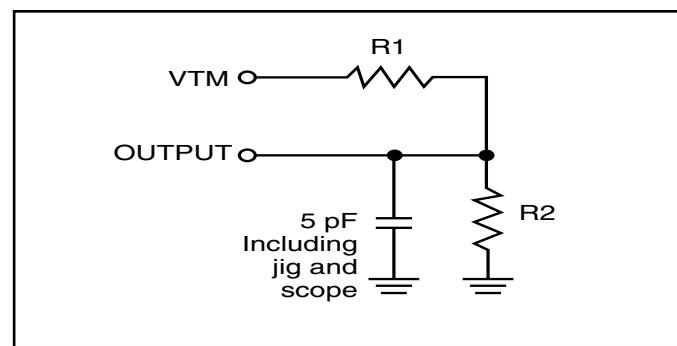


Figure 2.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V
V_{DD}	V_{DD} Relates to GND	-0.3 to 4.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{OUT} = 0V$	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25^\circ C$, $f = 1$ MHz, $V_{DD} = 3.3V$.

HIGH SPEED (IS61WV6416DALL/DBLL)

OPERATING RANGE (V_{DD}) (IS61WV6416DALL)

Range	Ambient Temperature	V_{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	-40°C to +85°C	1.65V-2.2V	20ns
Automotive	-40°C to +125°C	1.65V-2.2V	20ns

OPERATING RANGE (V_{DD}) (IS61WV6416DBLL)⁽¹⁾

Range	Ambient Temperature	V_{DD} (8 ns) ¹	V_{DD} (10 ns) ¹
Commercial	0°C to +70°C	3.3V \pm 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V \pm 5%	2.4V-3.6V

Note:

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V \pm 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV6416DBLL)

Range	Ambient Temperature	V_{DD} (10 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-8		-10		-12		-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Icc	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	65	—	50	—	45	—	40 mA
		CE = V _{IL}	Ind.	—	70	—	55	—	50	—	45
		V _{IN} \geq V _{DD} - 0.3V, or V _{IN} \leq 0.4V	Auto. ⁽³⁾	—	—	—	65	—	55	—	50
		typ. ⁽²⁾		45		45		45			
Isb2	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., CE \geq V _{DD} - 0.2V, V _{IN} \geq V _{DD} - 0.2V, or V _{IN} \leq 0.2V, f = 0	Com.	—	40	—	40	—	40	—	40 μ A
		Ind.	—	55	—	55	—	55	—	55	—
		Auto.	—	—	—	90	—	90	—	90	—
		typ. ⁽²⁾		4		4		4			

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.
- For Automotive grade at 15ns, typ. Icc = 38mA, not 100% tested.

LOW POWER (IS61WV6416DALS/DBLS)

OPERATING RANGE (V_{DD}) (IS61WV6416DALS)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	45ns
Automotive	-40°C to +125°C	1.65V-2.2V	55ns

OPERATING RANGE (V_{DD}) (IS61WV6416DBLS)

Range	Ambient Temperature	V _{DD} (35 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	-40°C to +85°C	2.4V-3.6V

OPERATING RANGE (V_{DD}) (IS64WV6416DBLS)

Range	Ambient Temperature	V _{DD} (35 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-25		-35		-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} , C _E = V _{IL} , V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	Com. Ind. Auto. typ. ⁽²⁾	— — — 18	20 25 40	— — — 35	20 25 35	— — — 30	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., C _E ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind. Auto. typ. ⁽²⁾	— — — 4	40 50 75	— — — 75	40 50 75	— — — 75	μA

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	ns
t _{OH} A	Output Hold Time	2.0	—	2.0	—	3	—	ns
t _{ACE}	CE Access Time	—	8	—	10	—	12	ns
t _{DOE}	OE Access Time	—	5.5	—	6.5	—	6.5	ns
t _{HZOE} ⁽²⁾	OE to High-Z Output	—	3	—	4	—	6	ns
t _{LZOE} ⁽²⁾	OE to Low-Z Output	0	—	0	—	0	—	ns
t _{HZCE} ⁽²⁾	CE to High-Z Output	0	3	0	4	0	6	ns
t _{LZCE} ⁽²⁾	CE to Low-Z Output	3	—	3	—	3	—	ns
t _{BA}	LB, UB Access Time	—	5.5	—	6.5	—	6.5	ns
t _{HZB} ⁽²⁾	LB, UB to High-Z Output	0	5.5	0	6.5	0	6.5	ns
t _{LZB} ⁽²⁾	LB, UB to Low-Z Output	0	—	0	—	0	—	ns
t _{PU}	Power Up Time	0	—	0	—	0	—	ns
t _{PD}	Power Down Time	—	8	—	10	—	10	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

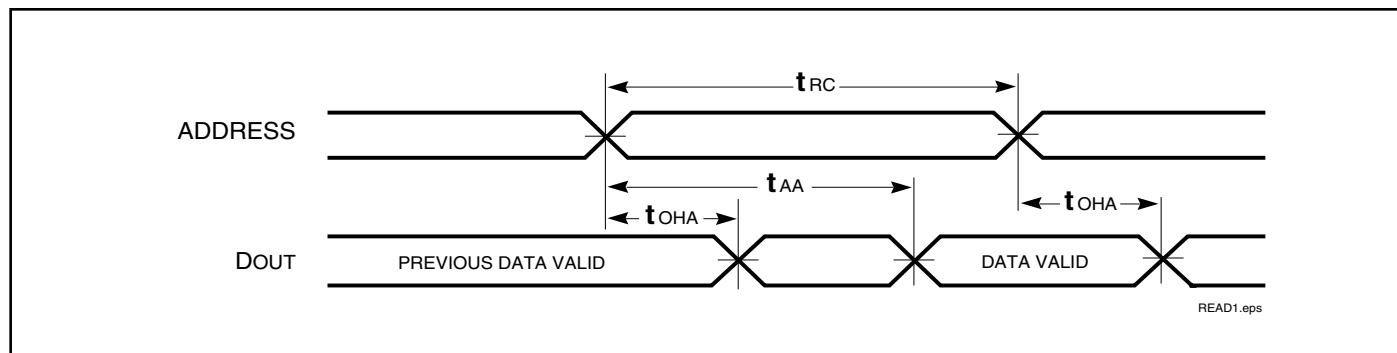
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t _{OH}	Output Hold Time	2.5	—	6	—	8	—	10	—	ns
t _{ACE}	CE Access Time	—	20	—	25	—	35	—	45	ns
t _{DOE}	OE Access Time	—	8	—	12	—	15	—	20	ns
t _{HZOE} ⁽²⁾	OE to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZOE} ⁽²⁾	OE to Low-Z Output	0	—	0	—	0	—	0	—	ns
t _{HZCE} ⁽²⁾	CE to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZCE} ⁽²⁾	CE to Low-Z Output	3	—	10	—	10	—	10	—	ns
t _{BA}	LB, UB Access Time	—	8	—	25	—	35	—	45	ns
t _{HZB}	LB, UB to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZB}	LB, UB to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:

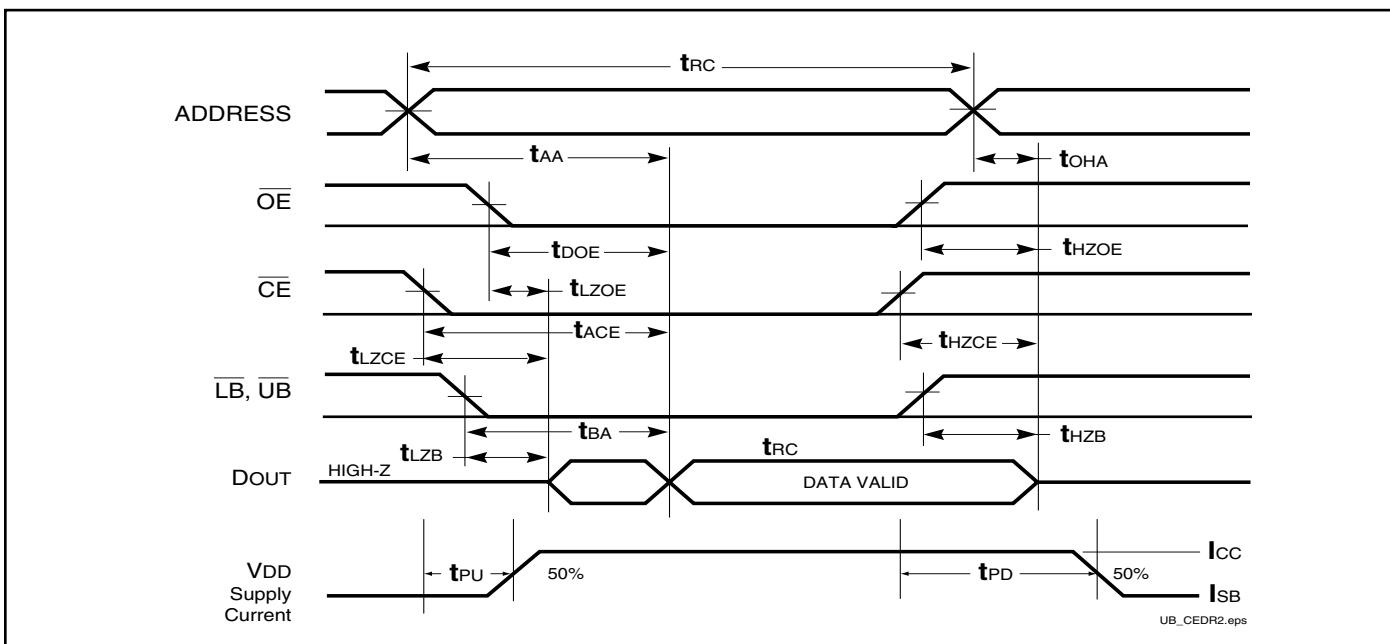
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} and/or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} and/or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{SCE}	\overline{CE} to Write End	6.5	—	8	—	9	—	ns
t _{AW}	Address Setup Time to Write End	6.5	—	8	—	9	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWB}	\overline{LB} , \overline{UB} Valid to End of Write	6.5	—	8	—	9	—	ns
t _{PWE1}	\overline{WE} Pulse Width	6.5	—	8	—	9	—	ns
t _{PWE2}	\overline{WE} Pulse Width ($\overline{OE} = \text{LOW}$)	8.0	—	10	—	11	—	ns
t _{SD}	Data Setup to Write End	5	—	6	—	9	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE⁽²⁾}	\overline{WE} LOW to High-Z Output	—	3.5	—	5	—	6	ns
t _{LZWE⁽²⁾}	\overline{WE} HIGH to Low-Z Output	2	—	2	—	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

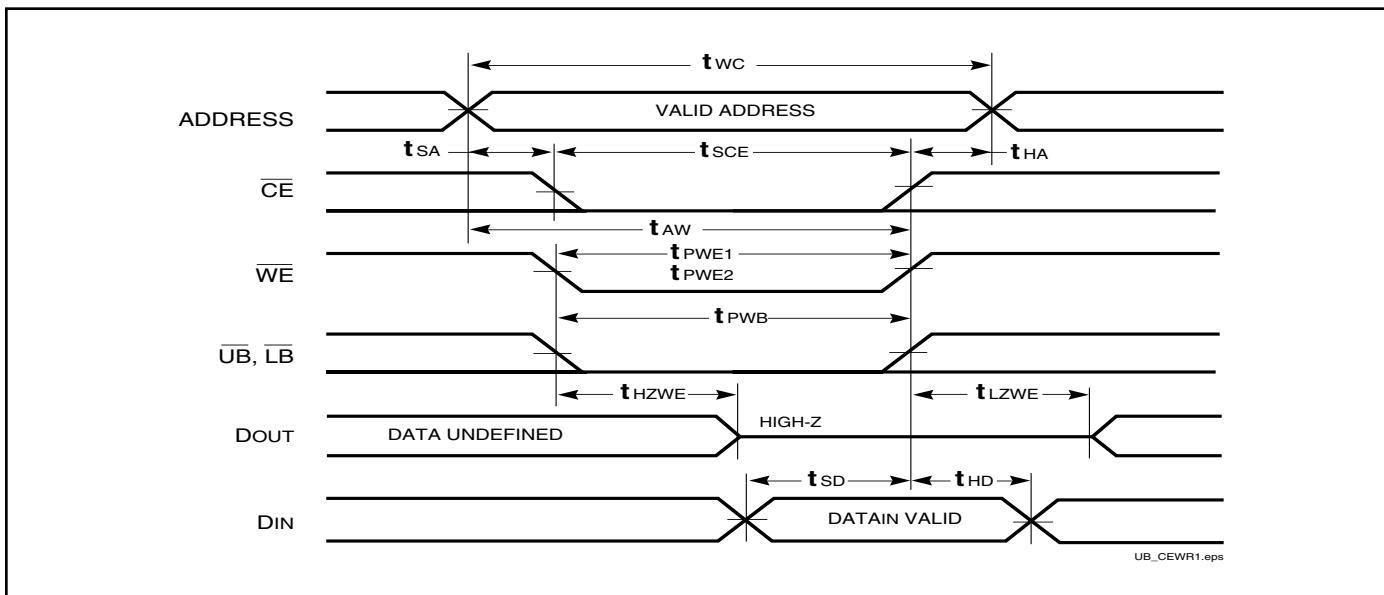
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t _{SCE}	\overline{CE} to Write End	12	—	18	—	25	—	35	—	ns
t _{AW}	Address Setup Time to Write End	12	—	15	—	25	—	35	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWB}	\overline{LB} , \overline{UB} Valid to End of Write	12	—	18	—	30	—	35	—	ns
t _{PWE1}	\overline{WE} Pulse Width ($\overline{OE} = \text{HIGH}$)	12	—	18	—	30	—	35	—	ns
t _{PWE2}	\overline{WE} Pulse Width ($\overline{OE} = \text{LOW}$)	17	—	20	—	30	—	35	—	ns
t _{SD}	Data Setup to Write End	9	—	12	—	15	—	20	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE⁽³⁾}	\overline{WE} LOW to High-Z Output	—	9	—	12	—	20	—	20	ns
t _{LZWE⁽³⁾}	\overline{WE} HIGH to Low-Z Output	3	—	5	—	5	—	5	—	ns

Notes:

1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

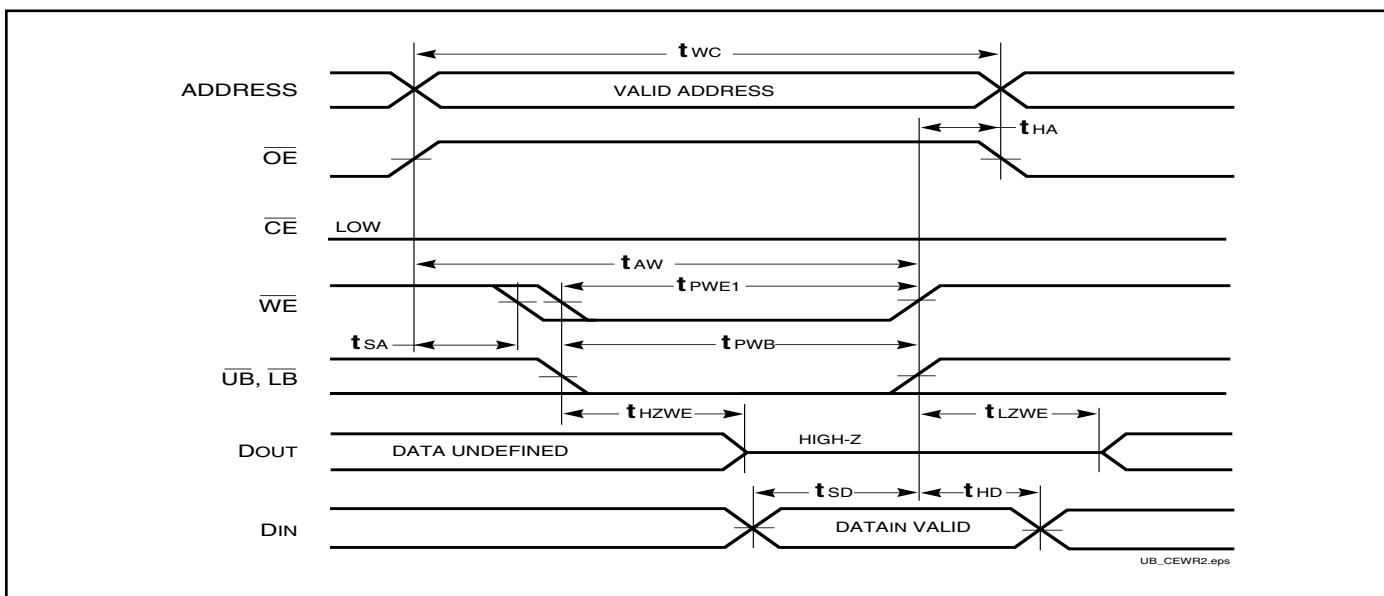
WRITE CYCLE NO. 1 (\overline{CE} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾



Notes:

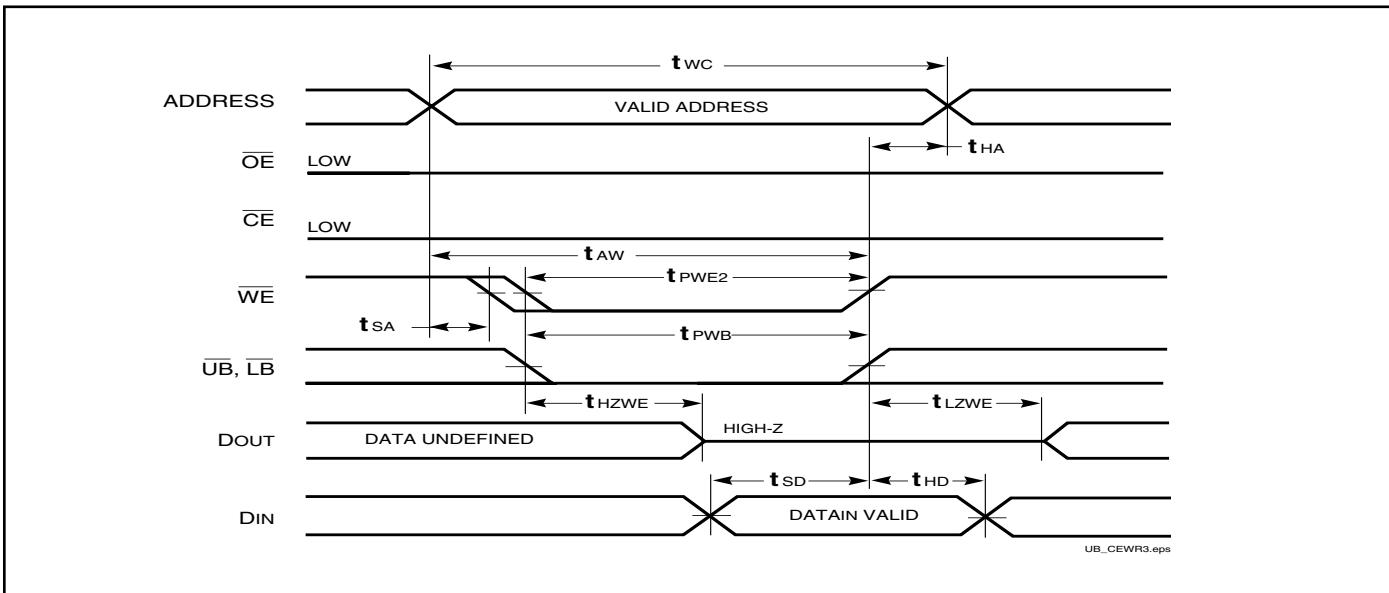
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the LB and UB inputs being in the LOW state.
2. $WRITE = (\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE})$.

WRITE CYCLE NO. 2 (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle) ^(1,2)

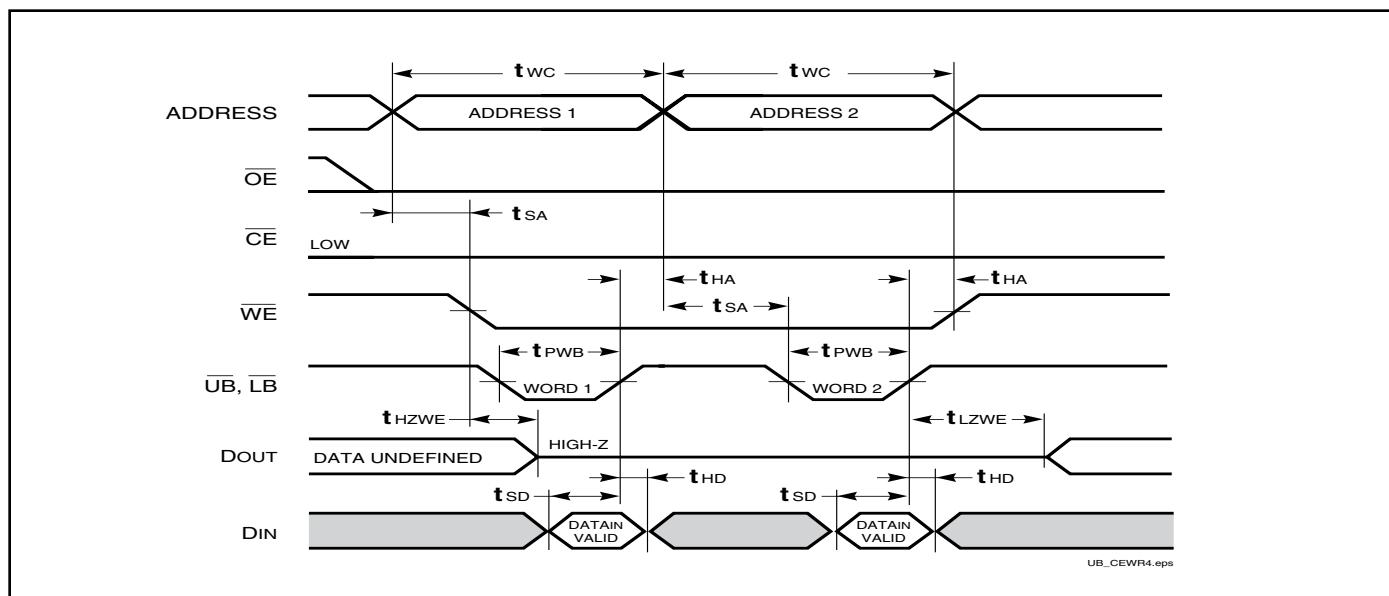


AC WAVEFORMS

WRITE CYCLE NO. 3 (\overline{WE} Controlled. \overline{OE} is LOW During Write Cycle) ⁽¹⁾



WRITE CYCLE NO. 4 (\overline{LB} , \overline{UB} Controlled, Back-to-Back Write) ^(1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{CE} = \text{LOW}$, \overline{UB} and/or $\overline{LB} = \text{LOW}$, and $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with \overline{OE} HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. \overline{WE} may be held LOW across many address cycles and the \overline{LB} , \overline{UB} pins can be used to control the Write function.

HIGH SPEED (IS61WV6416DALL/DBLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	55	
			Auto.			90	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

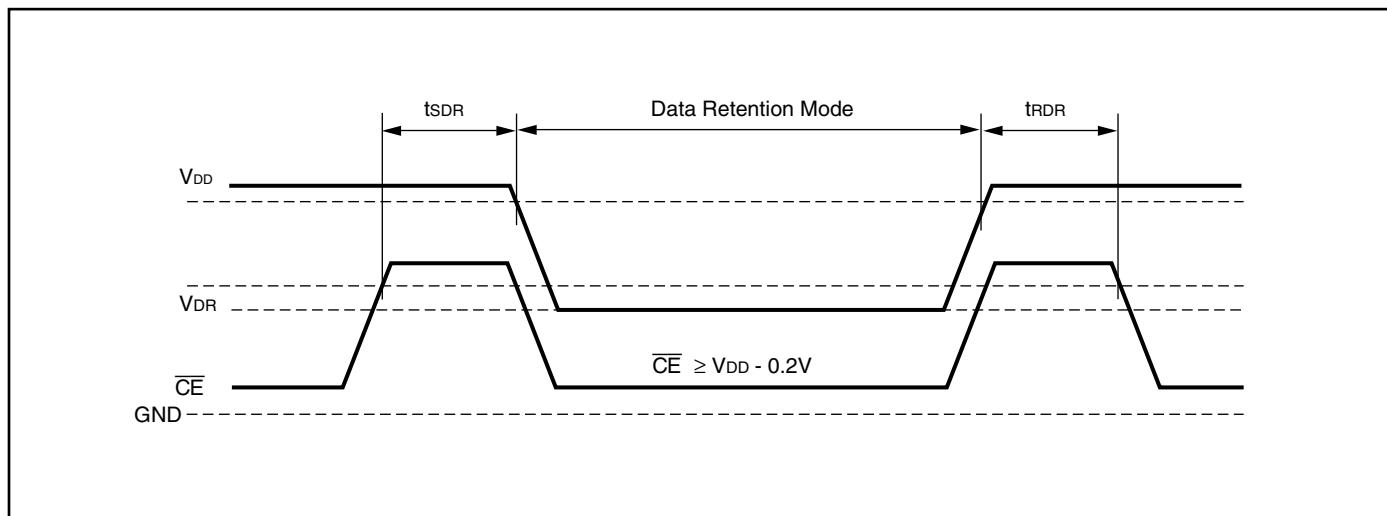
Note 1: Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	55	
			Auto.	—	—	90	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 1.8V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



LOW POWER (IS61WV6416DALS/DBLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	Vdd for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	50	
			Auto.		—	75	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

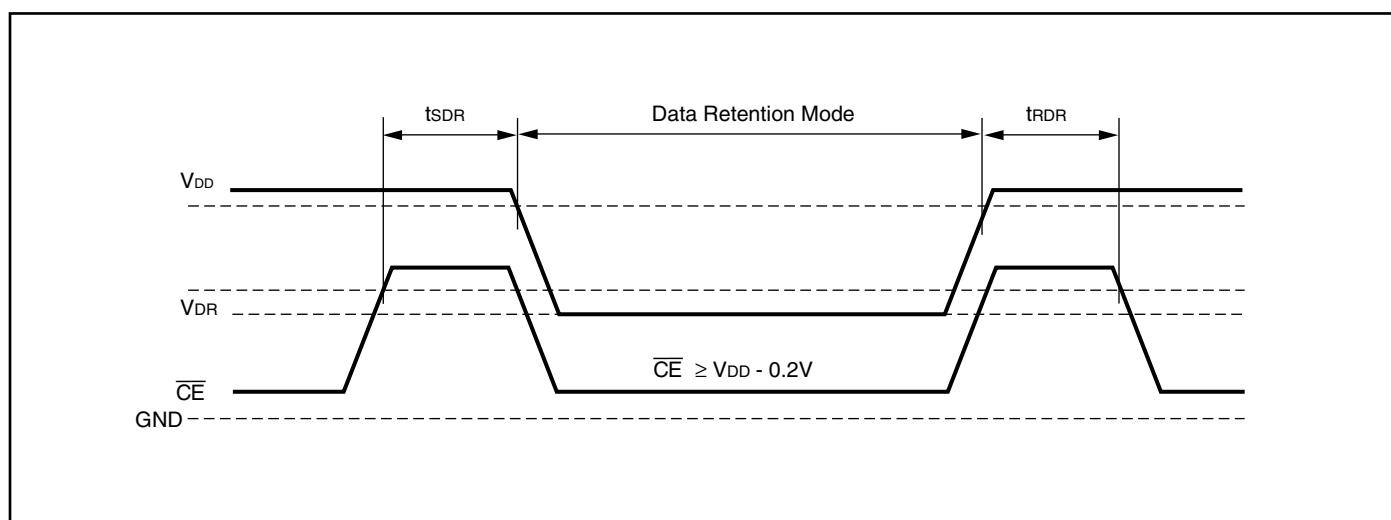
Note 1: Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	Vdd for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	4	40	μA
			Ind.	—	—	50	
			Auto.	—	—	75	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 1.8V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION (HIGH SPEED)

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
8	IS61WV6416DBLL-8BI	48 mini BGA (6mm x 8mm)
	IS61WV6416DBLL-8BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV6416DBLL-8TI	TSOP (Type II)
	IS61WV6416DBLL-8TLI	TSOP (Type II), Lead-free
	IS61WV6416DBLL-8KI	400-mil Plastic SOJ
	IS61WV6416DBLL-8KLI	400-mil Plastic SOJ, Lead-free
10	IS61WV6416DBLL-10BI	48 mini BGA (6mm x 8mm)
	IS61WV6416DBLL-10BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV6416DBLL-10TI	TSOP (Type II)
	IS61WV6416DBLL-10TLI	TSOP (Type II), Lead-free
	IS61WV6416DBLL-10KI	400-mil Plastic SOJ
	IS61WV6416DBLL-10KLI	400-mil Plastic SOJ, Lead-free

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV6416DALL-20BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV6416DALL-20TLI	TSOP (Type II), Lead-free

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

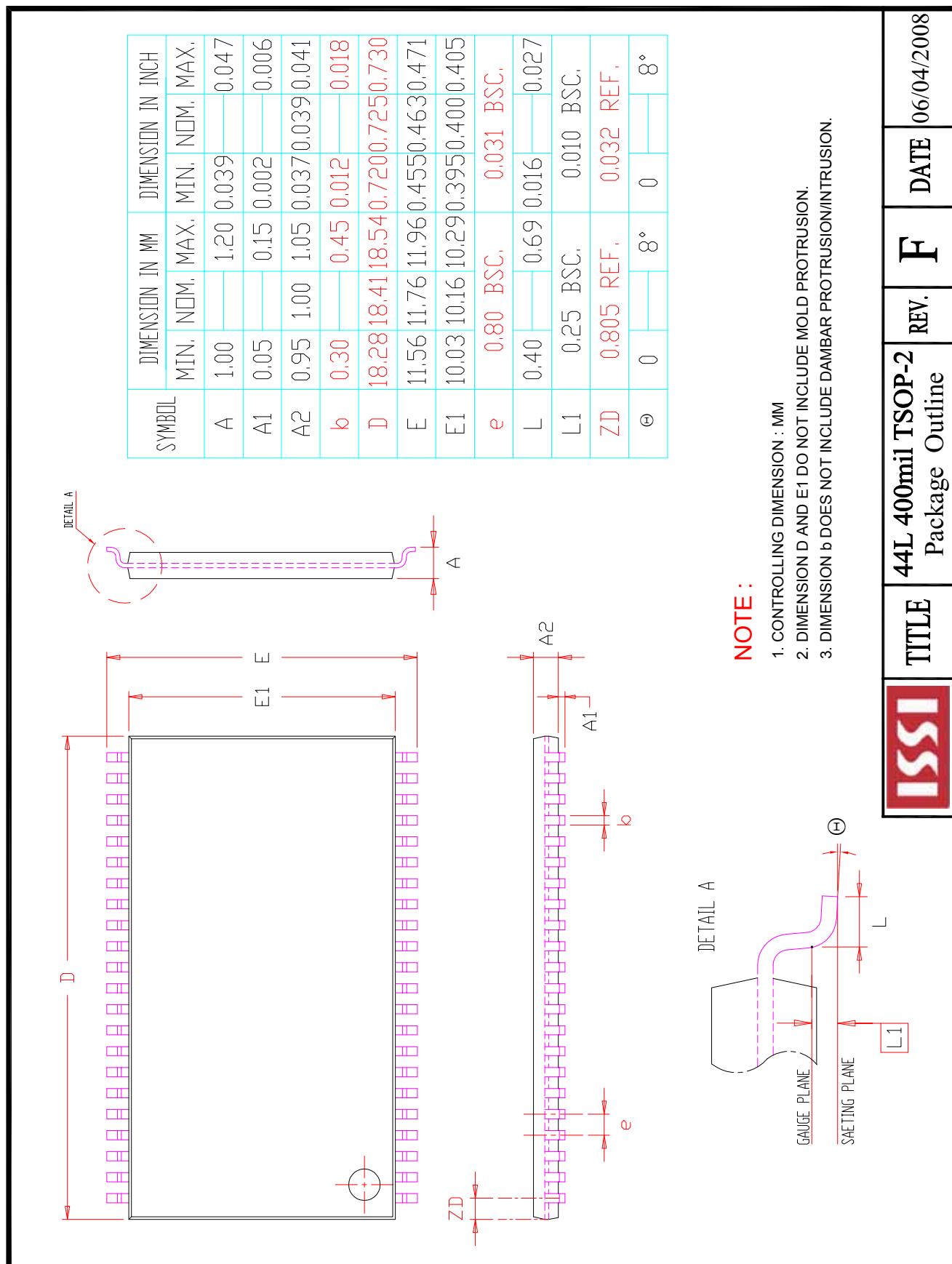
Speed (ns)	Order Part No.	Package
10	IS64WV6416DBLL-10BA3	48 mini BGA (6mm x 8mm)
	IS64WV6416DBLL-10BLA3	48 mini BGA (6mm x 8mm), Lead-free
	IS64WV6416DBLL-10CTA3	TSOP (Type II), Copper Leadframe
	IS64WV6416DBLL-10CTLA3	TSOP (Type II), Lead-free, Copper Leadframe

ORDERING INFORMATION (LOW POWER - IN EVALUATION)

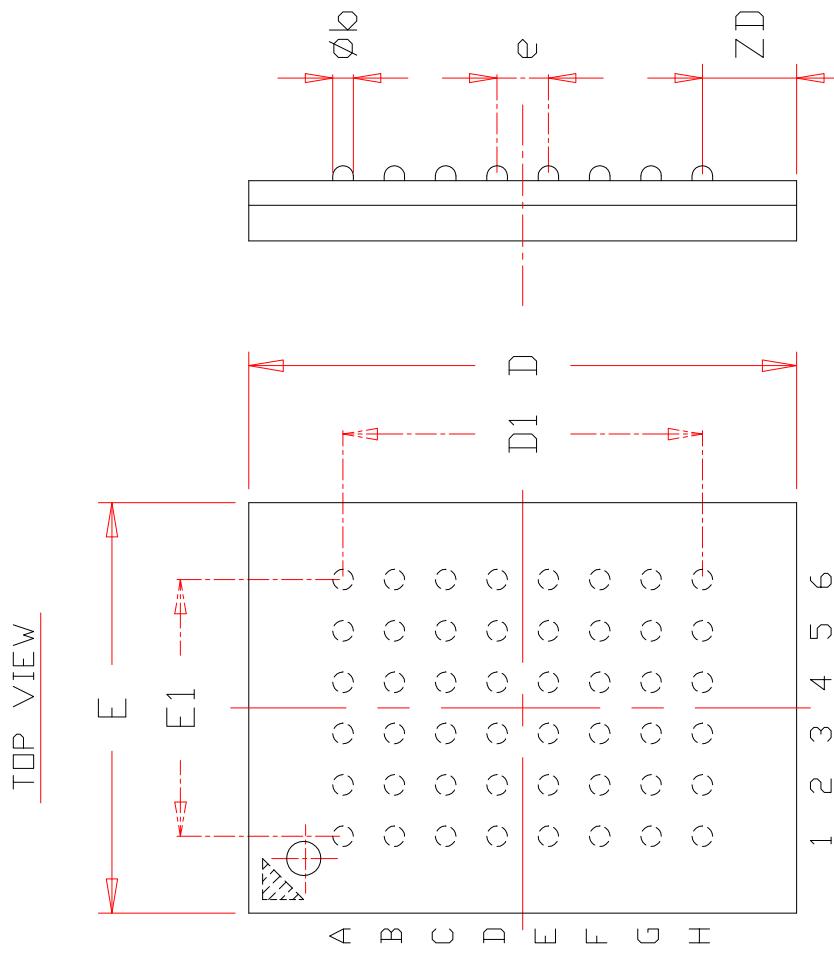
Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
35	IS61WV6416DBLS-35TLI	TSOP (Type II), Lead-free

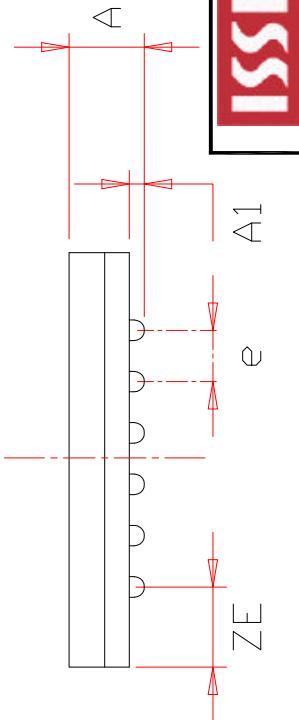


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A		1.20			0.047	
A1	0.20	0.30	0.008		0.012	
ϕb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25	BSC	0.207	BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75	BSC	0.148	BSC		
e	0.75	BSC,	0.030	BSC,		
ZD	1.375	REF.	0.054	REF.		
ZE	1.125	REF.	0.044	REF.		



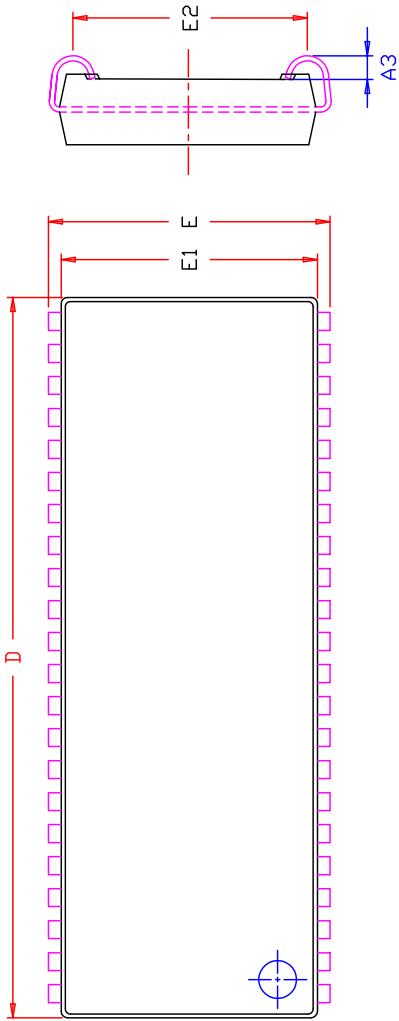
NOTE :

1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207



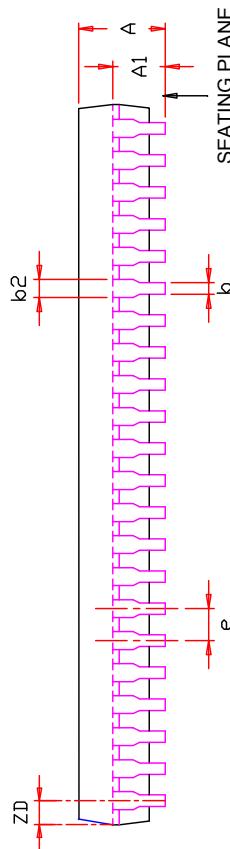
ISSI	TITLE	48L 6x8mm TF-BGA Package Outline	REV.	C	DATE	08/12/2008
	A1					

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	3.25	3.76	0.128	0.148
A1	2.08		0.082	
A3	0.635		0.025	
b	0.38		0.51	0.015
b2	0.66	0.71	0.81	0.0260
D	28.45	28.58	28.70	1.120
E	11.05	11.18	11.30	0.4350
E1	10.03	10.16	10.29	0.3950
E2	9.40	BSC.	0.370	BSC.
e	1.27	BSC.	0.050	BSC.
ZD	0.95	REF.	0.037	REF.



NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusions.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.



ISSI	TITLE	44L 400mil SOJ Package Outline	REV.	E	DATE	12/21/2007
------	-------	-----------------------------------	------	---	------	------------

Данный компонент на территории Российской Федерации**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибуторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru
moschip.ru_4

moschip.ru_6
moschip.ru_9