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# **Si4542DY**

# 30V Complementary PowerTrench®MOSFET

## **General Description**

This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

#### **Applications**

- DC/DC converter
- Power management

#### **Features**

Q1: N-Channel

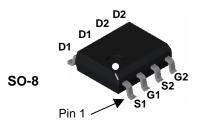
6 A, 30 V  $R_{DS(on)} = 28 \text{ m}\Omega @ V_{GS} = 10 \text{V}$ 

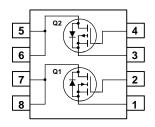
 $R_{DS(on)} = 35 \text{ m}\Omega @ V_{GS} = 4.5V$ 

• Q2: P-Channel

-6 A, -30 V  $R_{DS(on)} = 32 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$ 

 $R_{DS(on)} = 45 \text{ m}\Omega$  @  $V_{GS} = -4.5V$ 





# Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	-30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	6	-6	Α
	- Pulsed		20	-20	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	2	W
	Power Dissipation for Single Operation	(Note 1a)	1	.6	
		(Note 1b)	1	.2	
		(Note 1c)	,	1	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	ure Range	–55 to	+175	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

**Package Marking and Ordering Information** 

Device Marking Device		Reel Size	Tape width	Quantity
4542	Si4542DY	13"	12mm	2500 units

<b>Symbol</b>	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Cha	racteristics		•	•			•
BV <sub>DSS</sub>	Drain-Source Breakdown	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	Q1	30			V
	Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	Q2	-30			
$\Delta BV_{DSS}$	Breakdown Voltage	$I_D = 250 \mu A$ , Referenced to $25^{\circ}C$	Q1		23		mV/°C
$\Delta T_{J}$	Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to 25°C	Q2		-21		
I <sub>DSS</sub>	Zero Gate Voltage Drain	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1			1	μΑ
	Current	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	Q2			-1	·
I <sub>GSS</sub>	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1			<u>+</u> 100	nA
		$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q2			<u>+</u> 100	
On Cha	racteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	Q1	1	1.5	3	V
- 00(11)		$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	Q2	-1	-1.7	-3	
$\Delta V_{GS(th)}$	Gate Threshold Voltage	I <sub>D</sub> = 250 μA, Referenced to 25°C	Q1		-4		mV/°0
$\Delta T_{J}$	Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to 25°C	Q2		4		
R <sub>DS(on)</sub>	Static Drain-Source	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A	Q1		19	28	mΩ
-(- /	On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}, T_J = 125^{\circ}\text{C}$			32	48	
		$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$			25	35	
		$V_{GS} = -10 \text{ V}, I_D = -6 \text{ A}$	Q2		21	32	
		$V_{GS} = -10 \text{ V}, I_D = -6 \text{ A}, T_J = 125^{\circ}\text{C}$			29	51	
		$V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$			30	45	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	Q1	20			Α
(- )		$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	Q2	-20			
<b>g</b> FS	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 6 \text{ A}$	Q1		18		S
		$V_{DS} = -10 \text{ V}, I_{D} = -6 \text{ A}$	Q2		16		
Dynami	c Characteristics						
C <sub>iss</sub>	Input Capacitance	Q1	Q1		830		pF
		$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$	Q2		1540		
$C_{oss}$	Output Capacitance	f = 1.0 MHz	Q1		185		pF
		Q2	Q2		400		
C <sub>rss</sub>	Reverse Transfer	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$	Q1		80		pF
	Capacitance	f = 1.0 MHz	Q2		170		

Electri	Electrical Characteristics (continued) T <sub>A</sub> = 25°C unless otherwise noted						
Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Switchir	ng Characteristics (Note	2)					
t <sub>d(on)</sub>	Turn-On Delay Time	Q1 V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 A,	Q1 Q2		6 13	12 24	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10V, R_{GEN} = 6 \Omega$	Q1 Q2		10	18 35	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2 V <sub>DS</sub> = -15 V. I <sub>D</sub> = -1 A.	Q1 Q2		18 47	29 75	ns
t <sub>f</sub>	Turn-Off Fall Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		5 18	12 30	ns
Qg	Total Gate Charge	Q1 Vps = 15 V. lp = 7.5 A. Vgs = 5 V	Q1 Q2		9	13 20	nC
$Q_{gs}$	Gate-Source Charge	Q2	Q1 Q2		2.8		nC
Q <sub>gd</sub>	Gate-Drain Charge	$V_{DS} = -10 \text{ V}, I_{D} = -6 \text{ A}, V_{GS} = -5 \text{V}$	Q1 Q2		3.1 5		nC

Drain-Source Diode Characteristics and Maximum Ratings							
Is	Maximum Continuous Drain-Source Diode Forward Current	Q1 Q2		1.3 -1.3	Α		
$V_{SD}$	Drain-Source Diode Forward $V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A} \text{ (Note 2)}$ Voltage $V_{GS} = 0 \text{ V}, I_S = -1.3 \text{ A} \text{ (Note 2)}$	Q1 Q2	0.7	1.2	V		

#### Notes:

 R<sub>8JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>8JC</sub> is guaranteed by design while R<sub>8CA</sub> is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°C/W when mounted on a .02 in<sup>2</sup> pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width <  $300\mu$ s, Duty Cycle < 2.0%

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