

Microcontrollers



Never stop thinking.

Edition 2000-12

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C165

16-Bit Single-Chip Microcontroller

Microcontrollers



C165

Revision F	listory:	2000-12	V2.0
Previous V	ersion:	1998-12 01.96 07.95 09.94	Update 0.5µ technology 3 Volt Addendum 25 MHz Addendum Data Sheet
Page	Subjects (r	najor change	es since last revision)
All	Converted t	o Infineon lay	rout
2	ROM deriva	atives remove	d, 25-MHz derivatives and 3 V derivatives
6ff	Pin number	s for TQFP a	dded
14	Address wir	ndow arbitration	on and master/slave mode introduced
32	New standa	ard layout for	section "Absolute Maximum Ratings"
33	Section "Op	erating Cond	itions" added
34 f	Parameter '	'RSTIN pullup	o" replaced by "RSTIN current"
36 f	DC Charact	teristics for re	duced supply voltage added
38 f	Separate sp	ecification for	power consumption with greatly improved values
40 ff	Description	of clock gene	eration improved
45 , 55 , 65	Timing adap	oted to 25 MH	łz
48 , 58 , 66	Timing for r	educed suppl	y voltage added

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16-Bit Single-Chip Microcontroller C166 Family

C165

C165

- High Performance 16-bit CPU with 4-Stage Pipeline
 - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
 - -400 ns Multiplication (16 \times 16 bit), 800 ns Division (32 / 16 bit)
 - Enhanced Boolean Bit Manipulation Facilities
 - Additional Instructions to Support HLL and Operating Systems
 - Register-Based Design with Multiple Variable Register Banks
 - Single-Cycle Context Switching Support
 - 16 MBytes Total Linear Address Space for Code and Data
 - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 28 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via prescaler or via direct clock input
- On-Chip Memory Modules
 - 2 KBytes On-Chip Internal RAM (IRAM)
- On-Chip Peripheral Modules
 - Two Multi-Functional General Purpose Timer Units with 5 Timers
 - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Up to 16 MBytes External Address Space for Code and Data
 - Programmable External Bus Characteristics for Different Address Ranges
 - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit
 Data Bus Width
 - Five Programmable Chip-Select Signals
 - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer
- Up to 77 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Power Supply: the C165 can operate from a 5 V or a 3 V power supply
- Supported by a Large Range of Development Tools like C-Compilers,
 Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers,
 Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin MQFP Package (0.65 mm pitch)
- 100-Pin TQFP Package (0.5 mm pitch)

Data Sheet 1 V2.0, 2000-12



This document describes several derivatives of the C165 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C165 Derivative Synopsis

Derivative ¹⁾	Max. Operating Frequency	Operating Voltage	Package
SAF-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAB-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAF-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100
SAB-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100

¹⁾ This Data Sheet is valid for devices starting with and including design step HA.

For simplicity all versions are referred to by the term **C165** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C165 please refer to the "**Product Catalog Microcontrollers**", which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.



Introduction

The C165 is a derivative of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with peripheral functionality and enhanced IO-capabilities. The C165 is especially suited for cost sensitive applications.

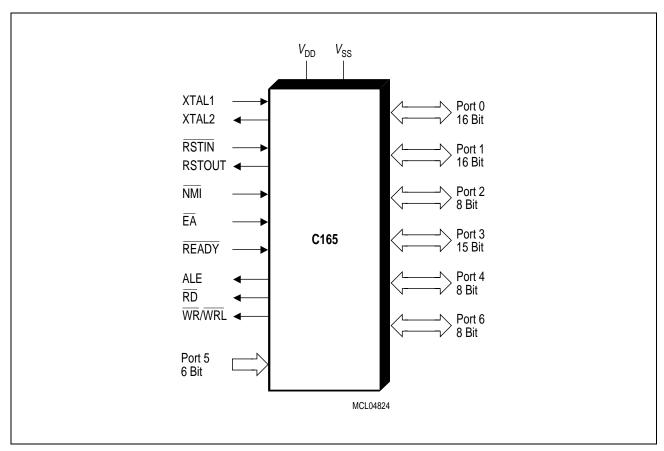


Figure 1 Logic Symbol



Pin Configuration TQFP Package

(top view)

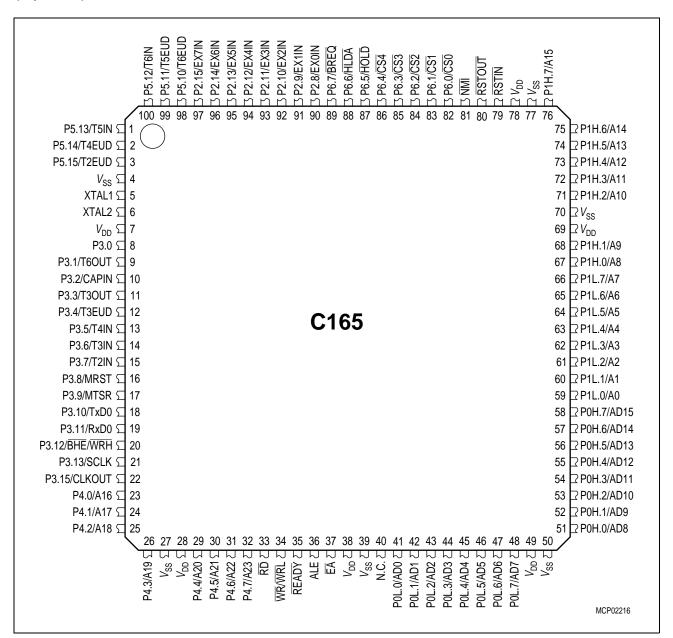


Figure 2



Pin Configuration MQFP Package

(top view)

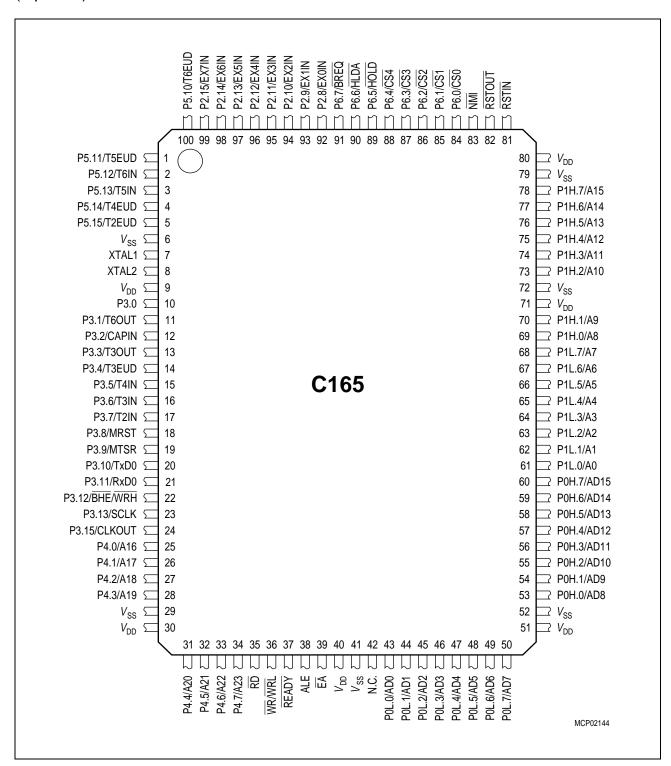


Figure 3



Table 2 Pin Definitions and Functions

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function	
XTAL1	5	7	I	XTAL1:	Input to the oscillator amplifier and input to the internal clock generator
XTAL2	6	8	0	XTAL1, wh Minimum a	Output of the oscillator amplifier circuit. le device from an external source, drive lile leaving XTAL2 unconnected. and maximum high/low and rise/fall times in the AC Characteristics must be
P3			IO	programma For a pin co into high-in configured	15-bit bidirectional I/O port. It is bit-wise able for input or output via direction bits. Onfigured as input, the output driver is put appedance state. Port 3 outputs can be as push/pull or open drain drivers. The serve for following alternate functions:
P3.0	8	10			•
P3.1	9	11	0	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	10	12		CAPIN	GPT2 Register CAPREL Capture Input
P3.3	11	13	0	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	12	14		T3EUD	GPT1 Timer T3 Ext. Up/Down Ctrl Input
P3.5	13	15	1	T4IN	GPT1 Timer T4
					Count/Gate/Reload/Capture Input
P3.6	14	16	1	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	15	17		T2IN	GPT1 Timer T2
					Count/Gate/Reload/Capture Input
P3.8	16	18	I/O	MRST	SSC Master-Receive/Slave-Transmit Input/Output
P3.9	17	19	I/O	MTSR	SSC Master-Transmit/Slave-Receive Output/Input
P3.10	18	20	0	TxD0	ASC0 Clock/Data Output (Asyn./Sync.)
P3.11	19	21	1/0	RxD0	ASC0 Data Inp. (Asyn.) or In/Out (Sync)
P3.12	20	22	0	BHE	Ext. Memory High Byte Enable Signal,
1 3.12	20		0	WRH	Ext. Memory High Byte Write Strobe
P3.13	21	23	1/0	SCLK	SSC Master Cl. Output / Slave Cl. Input
P3.15			0	CLKOUT	•
rs.15	22	24		CLROUI	System Clock Output (= CPU Clock)



Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P4			Ю	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	23	25	0	A16 Least Significant Segment Address Line
P4.1	24	26	0	A17 Segment Address Line
P4.2	25	27	0	A18 Segment Address Line
P4.3	26	28	0	A19 Segment Address Line
P4.4	29	31	0	A20 Segment Address Line
P4.5	30	32	0	A21 Segment Address Line
P4.6	31	33	0	A22 Segment Address Line
P4.7	32	34	0	A23 Most Significant Segment Address Line
RD	33	35	0	External Memory Read Strobe. RD is activated for every external instruction or data read access.
WR/ WRL	34	36	0	External Memory Write Strobe. In WR-mode this pin is activated for every external data write access. In WRL-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
READY	35	37	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle waitstates until the pin returns to a low level. An internal pullup device holds this pin high when nothing is driving it.
ALE	36	38	0	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
ĒĀ	37	39	I	External Access Enable pin. A low level at this pin during and after Reset forces the C165 to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.



Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function		
NC	40	42	_	This pin is not connection to the		
PORTO POL.0-7	41-48	43-50	Ю	PORT0 consists of ports P0L and P0H. input or output via di	It is bit-wise p	rogrammable for
P0H.0-7	51-58	53-60		as input, the output of state. In case of an PORT0 serves as the (AD) bus in multiple (D) bus in demultiple Demultiplexed bus Data Path Width: P0L.0 – P0L.7: P0H.0 – P0H.7: Multiplexed bus m Data Path Width: P0L.0 – P0L.7: P0H.0 – P0L.7: P0H.0 – P0H.7:	driver is put into external bus contended bus modes exed bus modes around a second bus modes around bus around bu	high-impedance onfiguration, and address/data is and as the data es. 16-bit D0 - D7 D8 - D15
PORT1 P1L.0-7 P1H.0-7		61-68 69-70, 73-78	IO	PORT1 consists of ports P1L and P1H. input or output via di as input, the output of state. PORT1 is use in demultiplexed bus from a demultiplexed mode.	It is bit-wise parection bits. For driver is put into ed as the 16-bits modes and also	rogrammable for r a pin configured high-impedance address bus (A) so after switching



Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
RSTIN	79	81	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C165. An internal pullup resistor permits power-on reset using only a capacitor connected to $V_{\rm SS}$. A spike filter suppresses input pulses < 10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\rm RSTIN}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table.
				Note: To let the reset configuration of PORT0 settle a reset duration of ca. 1 ms is recommended.
RST OUT	80	82	0	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. RSTOUT remains low until the EINIT (end of initialization) instruction is executed.
NMI	81	83	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the C165 to go into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.



Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P6			Ю	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	82	84	0	CS0 Chip Select 0 Output
P6.1	83	85	Ö	CS1 Chip Select 1 Output
P6.2	84	86	Ö	CS2 Chip Select 2 Output
P6.3	85	87	Ö	CS3 Chip Select 3 Output
P6.4	86	88	Ö	CS4 Chip Select 4 Output
P6.5	87	89	ľ	HOLD External Master Hold Request Input
P6.6	88	90	1/0	HLDA Hold Acknowledge Outp.(master mode)
. 0.0			"	or Input (slave mode)
P6.7	89	91	0	BREQ Bus Request Output
P2.8 P2.9 P2.10 P2.11 P2.12 P2.13 P2.14 P2.15	90 91 92 93 94 95 96 97	92 93 94 95 96 97 98 99	IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins serve for alternate functions: EX0IN Fast External Interrupt 0 Input EX1IN Fast External Interrupt 1 Input EX2IN Fast External Interrupt 2 Input EX3IN Fast External Interrupt 3 Input EX4IN Fast External Interrupt 4 Input EX5IN Fast External Interrupt 5 Input EX5IN Fast External Interrupt 5 Input EX6IN Fast External Interrupt 6 Input EX7IN Fast External Interrupt 7 Input
P5.10 P5.11 P5.12 P5.13 P5.14	98 99 100 1	100 1 2 3 4		Port 5 is a 6-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as timer inputs: T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl Input T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl Input T6IN GPT2 Timer T6 Count Input T5IN GPT2 Timer T5 Count Input T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl Input
P5.15	3	5	1	T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl Input



Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
V_{DD}	7, 28, 38, 49, 69, 78	9, 30, 40, 51, 71, 80	_	Digital Supply Voltage: + 5 V or + 3 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
$\overline{V_{SS}}$	4, 27, 39, 50, 70, 77	6, 29, 41, 52, 72, 79	_	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin RSTIN may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.



Functional Description

The architecture of the C165 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C165.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

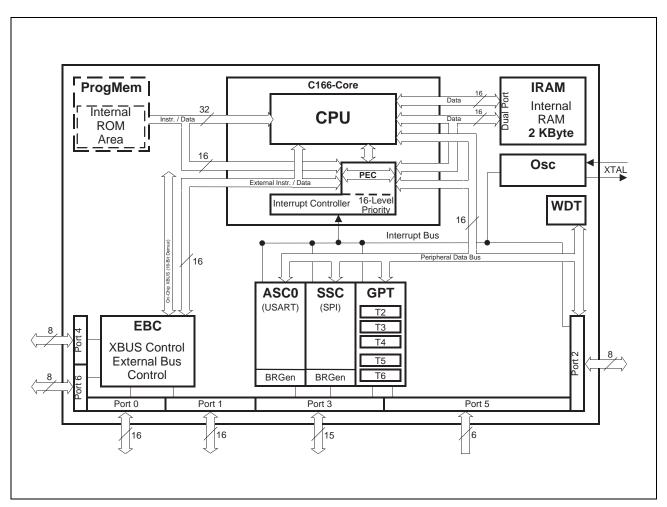


Figure 4 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see **Figure 4**).



Memory Organization

The memory space of the C165 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C165 is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.



External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{\text{CS}}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{\text{CS}}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{\text{CS}}$ signals are directly generated from the address. The unlatched $\overline{\text{CS}}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular 'Ready' function.

A HOLD/HLDA protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 ... P6.5 (BREQ, HLDA, HOLD) are automatically controlled by the EBC. In Master Mode (default after reset) the HLDA pin is an output. By setting bit DP6.7 to '1' the Slave Mode is selected where pin HLDA is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

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Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C165's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

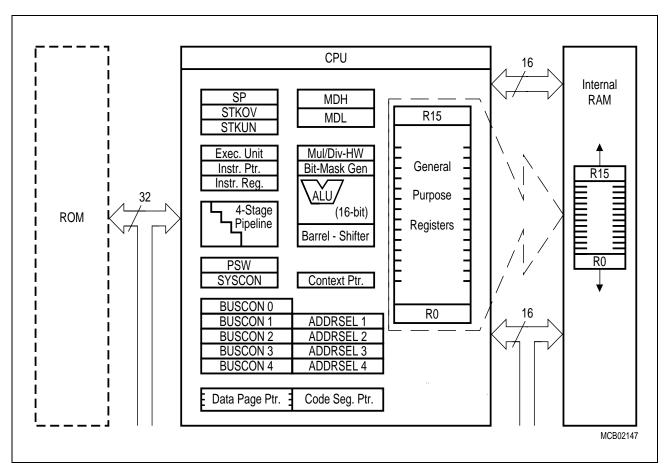


Figure 5 CPU Block Diagram



The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C165 instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.



Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).



Table 3 C165 Interrupt Nodes

External Interrupt 0 CC8IR CC8IE CC8INT 00'0060 _H 18 _H External Interrupt 1 CC9IR CC9IE CC9INT 00'0064 _H 19 _H External Interrupt 2 CC10IR CC10IE CC10INT 00'0068 _H 1A _H External Interrupt 3 CC11IR CC11IE CC11INT 00'006C _H 1B _H External Interrupt 4 CC12IR CC12IE CC12INT 00'0070 _H 1C _H External Interrupt 5 CC13IR CC13IE CC13INT 00'0070 _H 1D _H External Interrupt 6 CC14IR CC14IE CC14INT 00'0078 _H 1E _H External Interrupt 7 CC15IR CC15IE CC15INT 00'0076 _H 1F _H External Interrupt 7 CC15IR CC15IE CC15INT 00'0076 _H 1F _H External Interrupt 7 CC15IR CC15IE CC15INT 00'0076 _H 1F _H External Interrupt 6 T3IR T3IE T3INT 00'0086 _H 22 _H GPT1 Timer 3 T3IR	1 1 1 1 1
External Interrupt 2 CC10IR CC10IE CC10INT 00'0068 _H 1A _H External Interrupt 3 CC11IR CC11IE CC11INT 00'006C _H 1B _H External Interrupt 4 CC12IR CC12IE CC12INT 00'0070 _H 1C _H External Interrupt 5 CC13IR CC13IE CC13INT 00'0074 _H 1D _H External Interrupt 6 CC14IR CC14IE CC14INT 00'0078 _H 1E _H External Interrupt 7 CC15IR CC15IE CC15INT 00'007C _H 1F _H GPT1 Timer 2 T2IR T2IE T2INT 00'0088 _H 22 _H GPT1 Timer 3 T3IR T3IE T3INT 00'008C _H 23 _H GPT2 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'0098 _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT <	1 1 1 1
External Interrupt 3 CC11IR CC11IE CC11INT 00'006C _H 1B _H External Interrupt 4 CC12IR CC12IE CC12INT 00'0070 _H 1C _H External Interrupt 5 CC13IR CC13IE CC13INT 00'0074 _H 1D _H External Interrupt 6 CC14IR CC14IE CC14INT 00'0078 _H 1E _H External Interrupt 7 CC15IR CC15IE CC15INT 00'007C _H 1F _H GPT1 Timer 2 T2IR T2IE T2INT 00'0088 _H 22 _H GPT1 Timer 3 T3IR T3IE T3INT 00'008C _H 23 _H GPT1 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'0096 _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	1 1 1
External Interrupt 4 CC12IR CC12IE CC12INT 00'0070 _H 1C _H External Interrupt 5 CC13IR CC13IE CC13INT 00'0074 _H 1D _H External Interrupt 6 CC14IR CC14IE CC14INT 00'0078 _H 1E _H External Interrupt 7 CC15IR CC15IE CC15INT 00'007C _H 1F _H GPT1 Timer 2 T2IR T2IE T2INT 00'0088 _H 22 _H GPT1 Timer 3 T3IR T3IE T3INT 00'008C _H 23 _H GPT1 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'0098 _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	1 1
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External Interrupt 6 CC14IR CC14IE CC14INT 00'0078 _H 1E _H External Interrupt 7 CC15IR CC15IE CC15INT 00'007C _H 1F _H GPT1 Timer 2 T2IR T2IE T2INT 00'0088 _H 22 _H GPT1 Timer 3 T3IR T3IE T3INT 00'008C _H 23 _H GPT1 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	1
External Interrupt 7 CC15IR CC15IE CC15INT 00'007C _H 1F _H GPT1 Timer 2 T2IR T2IE T2INT 00'0088 _H 22 _H GPT1 Timer 3 T3IR T3IE T3INT 00'008C _H 23 _H GPT1 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	
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GPT1 Timer 4 T4IR T4IE T4INT 00'0090 _H 24 _H GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	1
GPT2 Timer 5 T5IR T5IE T5INT 00'0094 _H 25 _H GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	1
GPT2 Timer 6 T6IR T6IE T6INT 00'0098 _H 26 _H GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	
GPT2 CAPREL Reg. CRIR CRIE CRINT 00'009C _H 27 _H ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	l
ASC0 Transmit S0TIR S0TIE S0TINT 00'00A8 _H 2A _H	l
	1
ASC0 Transmit Buffer S0TBIR S0TBIE S0TBINT 00'011C _H 47 _H	1
	l
ASC0 Receive SORIR SORIE SORINT 00'00AC _H 2B _H	1
ASC0 Error S0EIR S0EIE S0EINT 00'00B0 _H 2C _F	1
SSC Transmit SCTIR SCTIE SCTINT 00'00B4 _H 2D _F	1
SSC Receive SCRIR SCRIE SCRINT 00'00B8 _H 2E _H	1
SSC Error SCEIR SCEIE SCEINT 00'00BC _H 2F _H	1
Unassigned node XP0IR XP0IE XP0INT 00'0100 _H 40 _H	l
Unassigned node XP1IR XP1IE XP1INT 00'0104 _H 41 _H	1
Unassigned node XP2IR XP2IE XP2INT 00'0108 _H 42 _H	
Unassigned node XP3IR XP3IE XP3INT 00'010C _H 43 _H	l
Unassigned node CC29IR CC29IE CC29INT 00'0110 _H 44 _H	
Unassigned node CC30IR CC30IE CC30INT 00'0114 _H 45 _H	
Unassigned node CC31IR CC31IE CC31INT 00'0118 _H 46 _H	1



The C165 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during runtime:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: - Hardware Reset - Software Reset - W-dog Timer Overflow	-	RESET RESET RESET	00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	
Class A Hardware Traps: - Non-Maskable Interrupt - Stack Overflow - Stack Underflow	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	
Class B Hardware Traps: - Undefined Opcode - Protected Instruction Fault	UNDOPC PRTFLT	BTRAP BTRAP	00'0028 _H 00'0028 _H	0A _H 0A _H	I
 Illegal Word Operand Access 	ILLOPA	BTRAP	00'0028 _H	0A _H	1
Illegal Instruction Access	ILLINA	BTRAP	00'0028 _H	0A _H	1
Illegal External Bus Access	ILLBUS	BTRAP	00'0028 _H	0A _H	I
Reserved	_	_	[2C _H – 3C _H]	[0B _H – 0F _H]	_
Software Traps – TRAP Instruction	_	_	Any [00'0000 _H - 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority



General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.



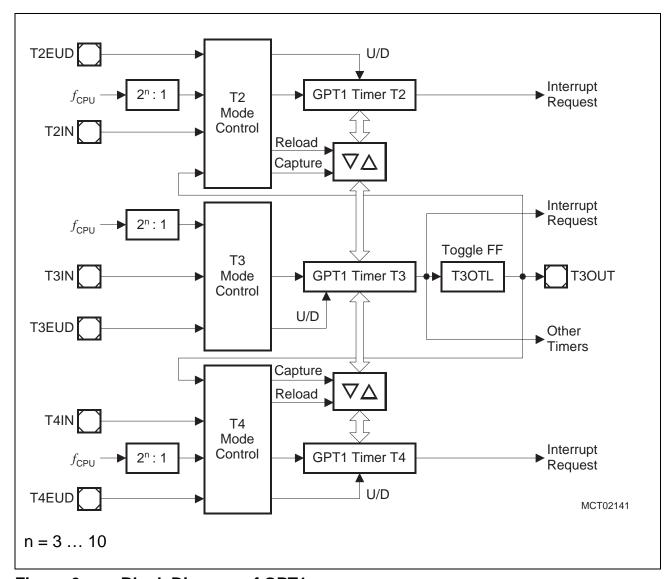


Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5 and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C165 to measure absolute time differences or to perform pulse multiplication without software overhead.



The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

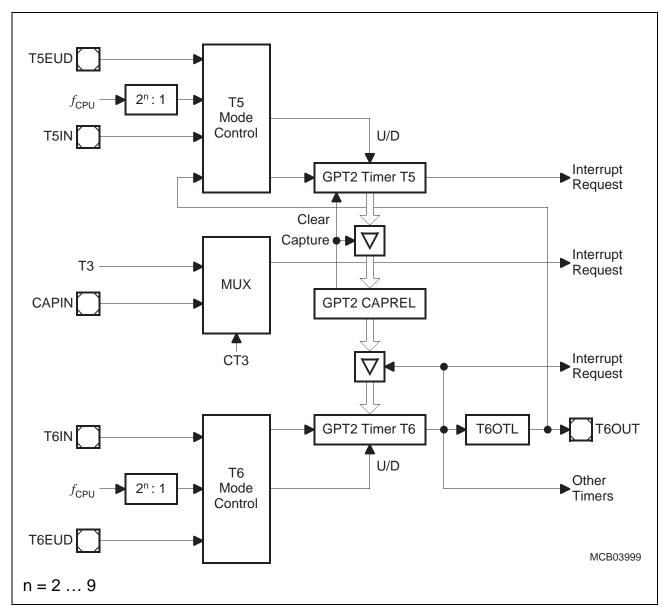


Figure 7 Block Diagram of GPT2



Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 KBaud and half-duplex synchronous communication at up to 3.1 MBaud (@ 25 MHz CPU clock).

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25 MBaud (@ 25 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception, and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

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Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the RSTOUT pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between $20 \, \mu s$ and $336 \, ms$ can be monitored (@ $25 \, MHz$).

The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C165 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 ... A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal BHE/WRH, and the system clock output CLKOUT.

Port 5 is used for timer control signals.

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Instruction Set Summary

Table 5 lists the instructions of the C165 in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "C166 Family Instruction Set Manual".

This document also provides a detailed description of each instruction.

Table 5 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with Carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with Carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2/4
OR(B)	Bitwise OR, (word/byte operands)	2/4
XOR(B)	Bitwise XOR, (word/byte operands)	2/4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2



Table 5 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2/4
MOVBS	Move byte operand to word operand with sign extension	2/4
MOVBZ	Move byte operand to word operand. with zero extension	2/4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack und update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
DLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes NMI-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2/4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2/4
NOP	Null operation	2



Special Function Registers Overview

The following table lists all SFRs which are implemented in the C165 in alphabetical order.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 6 C165 Registers, Ordered by Name

Name		Physical Address	8-Bit Addr.	Description	Reset Value
ADDRSEL1		FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2	2	FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3	3	FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4	ļ	FE1E _H	0F _H	Address Select Register 4	0000 _H
BUSCON0	b	FF0C _H	86 _H	Bus Configuration Register 0	0XX0 _H
BUSCON1	b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2	b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3	b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4	b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
CAPREL	APREL FE4A _H		25 _H	GPT2 Capture/Reload Register	0000 _H
CC10IC	b	FF8C _H	C6 _H	EX2IN Interrupt Control Register	0000 _H
CC11IC	b	FF8E _H	C7 _H	EX3IN Interrupt Control Register	0000 _H
CC12IC	b	FF90 _H	C8 _H	EX4IN Interrupt Control Register	0000 _H
CC13IC	b	FF92 _H	C9 _H	EX5IN Interrupt Control Register	0000 _H
CC14IC	b	FF94 _H	CA _H	EX6IN Interrupt Control Register	0000 _H
CC15IC	b	FF96 _H	CB _H	EX7IN Interrupt Control Register	0000 _H
CC29IC	b	F184 _H E	C2 _H	Software Interrupt Control Register	0000 _H
CC30IC	b	F18C _H E	C6 _H	Software Interrupt Control Register	0000 _H
CC31IC	b	F194 _H E	CA _H	Software Interrupt Control Register	0000 _H
CC8IC	b	FF88 _H	C4 _H	EX0IN Interrupt Control Register	0000 _H
CC9IC b FF8A _H		C5 _H	EX1IN Interrupt Control Register	0000 _H	



Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physica Address		8-Bit Addr.	Description	Reset Value	
СР		FE10 _H		08 _H	CPU Context Pointer Register	FC00 _H	
CRIC	b	FF6A _H		B5 _H	GPT2 CAPREL Interrupt Ctrl. Reg.	0000 _H	
CSP		FE08 _H		04 _H	CPU Code Seg. Pointer Reg. (read only)	0000 _H	
DP0H	b	F102 _H	Ε	81 _H	P0H Direction Control Register	00 _H	
DP0L	b	F100 _H	Ε	80 _H	P0L Direction Control Register	00 _H	
DP1H	b	F106 _H	Ε	83 _H	P1H Direction Control Register	00 _H	
DP1L	b	F104 _H	Ε	82 _H	P1L Direction Control Register	00 _H	
DP2	b	FFC2 _H		E1 _H	Port 2 Direction Control Register	0000 _H	
DP3	b	FFC6 _H		E3 _H	Port 3 Direction Control Register	0000 _H	
DP4	b	FFCA _H		E5 _H	Port 4 Direction Control Register	00 _H	
DP6	b	FFCE _H		E7 _H	Port 6 Direction Control Register	00 _H	
DPP0		FE00 _H		00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H	
DPP1		FE02 _H		01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H	
DPP2		FE04 _H		02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H	
DPP3		FE06 _H		03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H	
EXICON	b	F1C0 _H	Ε	E0 _H	External Interrupt Control Register	0000 _H	
IDCHIP		F07C _H	Ε	3E _H	H Identifier		
IDMANUF		F07E _H	Ε	3F _H	Identifier	1820 _H	
IDMEM		F07A _H	Ε	3D _H	Identifier	0000 _H	
IDMEM2		F076 _H	Ε	3B _H	Identifier	0000 _H	
IDPROG		F078 _H	Ε	3C _H	Identifier	0000 _H	
MDC	b	FF0E _H		87 _H	CPU Multiply Divide Control Register	0000 _H	
MDH		FE0C _H		06 _H	CPU Multiply Divide Reg. – High Word	0000 _H	
MDL		FE0E _H		07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H	
ODP2	b	F1C2 _H	Ε	E1 _H	Port 2 Open Drain Control Register	0000 _H	
ODP3	b	F1C6 _H	Ε	E3 _H	Port 3 Open Drain Control Register	0000 _H	
ODP6	b	F1CE _H	Ε	E7 _H	Port 6 Open Drain Control Register	00 _H	
ONES	b	FF1E _H 8F _H Constant Value 1's Register (read		Constant Value 1's Register (read only)	FFFF _H		
РОН	b	FF02 _H		81 _H	Port 0 High Reg. (Upper half of PORT0)	00 _H	
P0L	b	FF00 _H		80 _H	Port 0 Low Reg. (Lower half of PORT0)	00 _H	



Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
P1H	b	FF06 _H	83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b	FF04 _H	82 _H	Port 1 Low Reg.(Lower half of PORT1)	00 _H
P2	b	FFC0 _H	E0 _H	Port 2 Register	0000 _H
P3	b	FFC4 _H	E2 _H	Port 3 Register	0000 _H
P4	b	FFC8 _H	E4 _H	Port 4 Register (8 bits)	00 _H
P5	b	FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P6	b	FFCC _H	E6 _H	Port 6 Register (8 bits)	00 _H
PECC0		FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1		FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2		FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3		FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4		FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5		FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6		FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7		FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PSW	b	FF10 _H	88 _H	CPU Program Status Word	0000 _H
RP0H	b	F108 _H E	84 _H	System Startup Config. Reg. (Rd. only)	XX _H
S0BG		FEB4 _H	5A _H	Serial Channel 0 Baud Rate Generator Reload Register	0000 _H
S0CON	b	FFB0 _H	D8 _H	Serial Channel 0 Control Register	0000 _H
S0EIC	b	FF70 _H	B8 _H	Serial Channel 0 Error Interrupt Ctrl. Reg	0000 _H
S0RBUF		FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	XX _H
SORIC	b	FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC	b	F19C _H E	CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF		FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Register (write only)	00 _H
SOTIC	b	FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H



Table 6 C165 Registers, Ordered by Name (cont'd)

Name Physical Address		8-Bit Addr.	Description	Reset Value	
SP FE12 _H		09 _H	CPU System Stack Pointer Register	FC00 _H	
SSCBR		F0B4 _H E	4 _H E 5A _H SSC Baudrate Register		0000 _H
SSCCON	b	FFB2 _H	D9 _H	SSC Control Register	0000 _H
SSCEIC	b	FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB		F0B2 _H E	59 _H	SSC Receive Buffer	XXXX _H
SSCRIC	b	FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB		F0B0 _H E	58 _H	SSC Transmit Buffer	0000 _H
SSCTIC	b	FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV		FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN		FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b	FF12 _H	89 _H	CPU System Configuration Register	¹⁾ 0XX0 _H
T2		FE40 _H	FE40 _H 20 _H GPT1 Timer 2 Register		0000 _H
T2CON	b	FF40 _H A0 _H GPT1 Timer 2 Control Register		0000 _H	
T2IC	b	FF60 _H	B0 _H	GPT1 Timer 2 Interrupt Control Register	0000 _H
T3		FE42 _H	FE42 _H 21 _H GPT1 Timer 3 Register		0000 _H
T3CON	b	FF42 _H A1 _H GPT1 Timer 3		GPT1 Timer 3 Control Register	0000 _H
T3IC	b	FF62 _H B1 _H GPT1		GPT1 Timer 3 Interrupt Control Register	0000 _H
T4		FE44 _H	22 _H	GPT1 Timer 4 Register	0000 _H
T4CON	b	FF44 _H	A2 _H	GPT1 Timer 4 Control Register	0000 _H
T4IC	b	FF64 _H	B2 _H	GPT1 Timer 4 Interrupt Control Register	0000 _H
T5		FE46 _H	23 _H	GPT2 Timer 5 Register	0000 _H
T5CON	b	FF46 _H	A3 _H	GPT2 Timer 5 Control Register	0000 _H
T5IC	b	FF66 _H	B3 _H	GPT2 Timer 5 Interrupt Control Register	0000 _H
T6		FE48 _H	24 _H	GPT2 Timer 6 Register	0000 _H
T6CON	b	FF48 _H	A4 _H	GPT2 Timer 6 Control Register	0000 _H
T6IC	b	FF68 _H	B4 _H	GPT2 Timer 6 Interrupt Control Register	0000 _H
TFR	b	FFAC _H	D6 _H	Trap Flag Register	0000 _H
WDT		FEAE _H	57 _H	Watchdog Timer Register (read only)	0000 _H
WDTCON	b	FFAE _H	D7 _H	Watchdog Timer Control Register	²⁾ 00XX _H
XP0IC	b	F186 _H E	C3 _H	Software Interrupt Control Register	0000 _H



Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physica Address		8-Bit Addr.	Description	Reset Value
XP1IC	b	F18E _H	Ε	C7 _H	Software Interrupt Control Register	0000 _H
XP2IC	b	F196 _H	Е	CB _H	Software Interrupt Control Register	0000 _H
XP3IC	b	F19E _H	Е	CF _H	Software Interrupt Control Register	0000 _H
ZEROS	b	FF1C _H		8E _H	Constant Value 0's Register (read only)	0000 _H

¹⁾ The system configuration is selected during reset.

 $^{^{2)}\,\,}$ The reset value depends on the indicated reset source.



Absolute Maximum Ratings

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes	
		min.	max.			
Storage temperature	T_{ST}	- 65	150	°C	_	
Junction temperature	T_{J}	- 40	150	°C	under bias	
Voltage on $V_{\rm DD}$ pins with respect to ground ($V_{\rm SS}$)	V_{DD}	- 0.5	6.5	V	_	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	- 0.5	V _{DD} + 0.5	V	_	
Input current on any pin during overload condition	_	- 10	10	mA	_	
Absolute sum of all input currents during overload condition	_	-	100	mA	_	
Power dissipation	P_{DISS}	_	1.5	W	_	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions $(V_{IN} > V_{DD})$ or $V_{IN} < V_{SS}$ the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.



Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C165. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 8 Operating Condition Parameters

Parameter	Symbol	Limit '	Values	Unit	Notes
		min.	max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, $f_{\text{CPUmax}} = 25 \text{ MHz}$
(5 V versions)		2.5 ¹⁾	5.5	V	PowerDown mode
Reduced digital supply voltage	V_{DD}	3.0	3.6	V	Active mode, $f_{\text{CPUmax}} = 20 \text{ MHz}$
(3 V versions)		2.5 ¹⁾	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	_	± 5	mA	Per pin ²⁾³⁾
Absolute sum of overload currents	$\Sigma I_{OV} $	_	50	mA	3)
External Load Capacitance	C_{L}	_	100	pF	_
Ambient temperature	T_{A}	0	70	°C	SAB-C165
		- 40	85	°C	SAF-C165
		- 40	125	°C	SAK-C165

¹⁾ Output voltages and output currents will be reduced when $V_{
m DD}$ leaves the range defined for active mode.

Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{\rm OV} > V_{\rm DD} + 0.5$ V or $V_{\rm OV} < V_{\rm SS} - 0.5$ V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{\rm RD}$, $\overline{\rm WR}$, etc.

³⁾ Not 100% tested, guaranteed by design and characterization.



Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C165 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

CC (Controller Characteristics):

The logic of the C165 will provide signals with the respective timing characteristics.

SR (**S**ystem Requirement):

The external system must provide signals with the respective timing characteristics to the C165.

DC Characteristics (Standard Supply Voltage Range)

(Operating Conditions apply)¹⁾

Parameter	Symbol	Limit '	Values	Unit	Test Condition
		min.	max.		
Input low voltage (TTL, all except XTAL1)	V _{IL} SR	- 0.5	0.2 V _{DD} - 0.1	V	_
Input low voltage XTAL1	V_{IL2} SR	- 0.5	0.3 V _{DD}	V	_
Input high voltage (TTL, all except RSTIN and XTAL1)	V _{IH} SR	0.2 V _{DD} + 0.9	V _{DD} + 0.5	V	_
Input high voltage RSTIN (when operated as input)	V _{IH1} SR	0.6 V _{DD}	V _{DD} + 0.5	V	_
Input high voltage XTAL1	V _{IH2} SR	0.7 V _{DD}	V _{DD} + 0.5	V	_
Output low voltage (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, RSTOUT, RSTIN ²⁾)	V _{OL} CC	_	0.45	V	I _{OL} = 2.4 mA
Output low voltage (all other outputs)	V _{OL1} CC	_	0.45	V	I _{OL} = 1.6 mA
Output high voltage ³⁾	V_{OH} CC	2.4	_	V	I_{OH} = - 2.4 mA
(PORT0, PORT1, Port 4, ALE, RD, WR, BHE, RSTOUT)		0.9 V _{DD}	_	V	I _{OH} = - 0.5 mA
Output high voltage ³⁾	$V_{OH1}CC$	2.4	_	V	I_{OH} = - 1.6 mA
(all other outputs)		0.9 V _{DD}	_	V	I_{OH} = - 0.5 mA
Input leakage current (Port 5)	I _{OZ1} CC	_	± 200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)	I _{OZ2} CC	_	± 500	nA	$0.45 \text{ V} < V_{\text{IN}} < V_{\text{DD}}$
RSTIN inactive current ⁴⁾	I _{RSTH} 5)	_	- 10	μΑ	$V_{IN} = V_{IH1}$



DC Characteristics (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
RSTIN active current ⁴⁾	I _{RSTL} ⁶⁾	- 100	_	μΑ	$V_{IN} = V_{IL}$
READY/RD/WR inact. current ⁷⁾	$I_{\text{RWH}}^{5)}$	_	- 40	μΑ	V_{OUT} = 2.4 V
READY/RD/WR active current ⁷⁾	$I_{\text{RWL}}^{6)}$	- 500	_	μΑ	$V_{OUT} = V_{OLmax}$
ALE inactive current ⁷⁾	$I_{ALEL}^{5)}$	_	40	μΑ	$V_{OUT} = V_{OLmax}$
ALE active current ⁷⁾	$I_{ALEH}^{(6)}$	500	_	μΑ	V_{OUT} = 2.4 V
Port 6 inactive current ⁷⁾	I _{P6H} ⁵⁾	_	- 40	μΑ	V _{OUT} = 2.4 V
Port 6 active current ⁷⁾	I _{P6L} ⁶⁾	- 500	_	μΑ	$V_{OUT} = V_{OL1max}$
PORT0 configuration current ⁸⁾	$I_{P0H}^{5)}$	_	- 10	μΑ	$V_{IN} = V_{IHmin}$
	$I_{P0L}^{6)}$	- 100	_	μΑ	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	_	± 20	μΑ	0 V < V_{IN} < V_{DD}
Pin capacitance ⁹⁾ (digital inputs/outputs)	C _{IO} CC	_	10	pF	f = 1 MHz $T_{\rm A}$ = 25 °C

Neeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .

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²⁾ Valid in bidirectional reset mode only.

³⁾ This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

These parameters describe the \overline{RSTIN} pullup, which equals a resistance of ca. 50 to 250 k Ω .

⁵⁾ The maximum current may be drawn while the respective signal line remains inactive.

⁶⁾ The minimum current must be drawn in order to drive the respective signal line active.

⁷⁾ This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$ -pullup is always active, except for Powerdown mode.

⁸⁾ This specification is valid during Reset and during Adapt-mode.

⁹⁾ Not 100% tested, guaranteed by design and characterization.



DC Characteristics (Reduced Supply Voltage Range) (Operating Conditions apply)¹⁾

Parameter	Symbol	Limit '	Values	Unit	Test Condition	
		min.	max.			
Input low voltage (TTL, all except XTAL1)	V_{IL} SR	- 0.5	0.8	V	_	
Input low voltage XTAL1	V_{IL2} SR	- 0.5	0.3 V _{DD}	V	_	
Input high voltage (TTL, all except RSTIN and XTAL1)	V _{IH} SR	1.8	V _{DD} + 0.5	V	_	
Input high voltage RSTIN (when operated as input)	V_{IH1} SR	0.6 V _{DD}	V _{DD} + 0.5	V	_	
Input high voltage XTAL1	V_{IH2} SR	0.7 V _{DD}	V _{DD} + 0.5	V	_	
Output low voltage (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, RSTOUT, RSTIN ²⁾)	V _{OL} CC	_	0.45	V	I _{OL} = 1.6 mA	
Output low voltage (all other outputs)	V _{OL1} CC	-	0.45	V	$I_{\rm OL}$ = 1.0 mA	
Output high voltage ³⁾ (PORT0, PORT1, Port 4, ALE, RD, WR, BHE, RSTOUT)	V _{OH} CC	0.9 V _{DD}	_	V	I _{OH} = - 0.5 mA	
Output high voltage ³⁾ (all other outputs)	V _{OH1} CC	0.9 V _{DD}	_	V	$I_{\rm OH}$ = - 0.25 mA	
Input leakage current (Port 5)	I _{OZ1} CC	_	± 200	nA	$0 \ V < V_{IN} < V_{DD}$	
Input leakage current (all other)	I _{OZ2} CC	_	± 500	nA	$0.45 \ V < V_{IN} < V_{DD}$	
RSTIN inactive current ⁴⁾	$I_{RSTH}^{5)}$	_	- 10	μΑ	$V_{IN} = V_{IH1}$	
RSTIN active current ⁴⁾	$I_{\rm RSTL}^{6)}$	- 100	_	μΑ	$V_{IN} = V_{IL}$	
READY/RD/WR inact. current ⁷⁾	$I_{\text{RWH}}^{5)}$	_	- 10	μΑ	V_{OUT} = 2.4 V	
READY/RD/WR active current ⁷⁾	$I_{\rm RWL}^{6)}$	- 500	_	μΑ	$V_{OUT} = V_{OLmax}$	
ALE inactive current ⁷⁾	$I_{ALEL}^{5)}$	_	20	μΑ	$V_{OUT} = V_{OLmax}$	
ALE active current ⁷⁾	$I_{ALEH}^{6)}$	500	_	μΑ	V_{OUT} = 2.4 V	
Port 6 inactive current ⁷⁾	$I_{{ m P6H}}^{5)}$	_	- 10	μΑ	V_{OUT} = 2.4 V	
Port 6 active current ⁷⁾	$I_{P6L}^{6)}$	- 500	_	μΑ	$V_{\text{OUT}} = V_{\text{OL1max}}$	



DC Characteristics (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
PORT0 configuration current ⁸⁾	$I_{P0H}^{5)}$	_	- 5	μΑ	$V_{IN} = V_{IHmin}$
	$I_{POL}^{(6)}$	- 100	_	μΑ	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	_	± 20	μΑ	$0 \ V < V_{IN} < V_{DD}$
Pin capacitance ⁹⁾ (digital inputs/outputs)	C_{IO} CC	_	10	pF	f = 1 MHz T_{A} = 25 °C

Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .

²⁾ Valid in bidirectional reset mode only.

³⁾ This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

⁴⁾ These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 k Ω .

⁵⁾ The maximum current may be drawn while the respective signal line remains inactive.

⁶⁾ The minimum current must be drawn in order to drive the respective signal line active.

⁷⁾ This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$ -pullup is always active, except for Powerdown mode.

⁸⁾ This specification is valid during Reset and during Adapt-mode.

⁹⁾ Not 100% tested, guaranteed by design and characterization.



Power Consumption C165 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Lim	Limit Values		Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD5}	_	15 + 1.8 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IL}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Idle mode supply current with all peripherals active	I_{IDX5}	_	2 + 0.4 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ f_{CPU} in [MHz] ¹⁾
Power-down mode supply current	I_{PDO5}	_	50	μΑ	$V_{\rm DD} = V_{\rm DDmax}^{2)}$

The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at $V_{\rm DDmax}$ and maximum CPU clock with all outputs disconnected and all inputs at $V_{\rm IL}$ or $V_{\rm IH}$.

Power Consumption C165 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Lim	Limit Values		Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD3}	_	3 + 1.3 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IL}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Idle mode supply current with all peripherals active	I_{IDX3}	_	1 + 0.4 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Power-down mode supply current	I_{PDO3}	_	30	μΑ	$V_{\rm DD} = V_{\rm DDmax}^{2}$

The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at $V_{\rm DDmax}$ and maximum CPU clock with all outputs disconnected and all inputs at $V_{\rm IL}$ or $V_{\rm IH}$.

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This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{\rm DD}$ – 0.1 V to $V_{\rm DD}$, all outputs (including pins configured as outputs) disconnected.

This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{\rm DD}$ – 0.1 V to $V_{\rm DD}$, all outputs (including pins configured as outputs) disconnected.



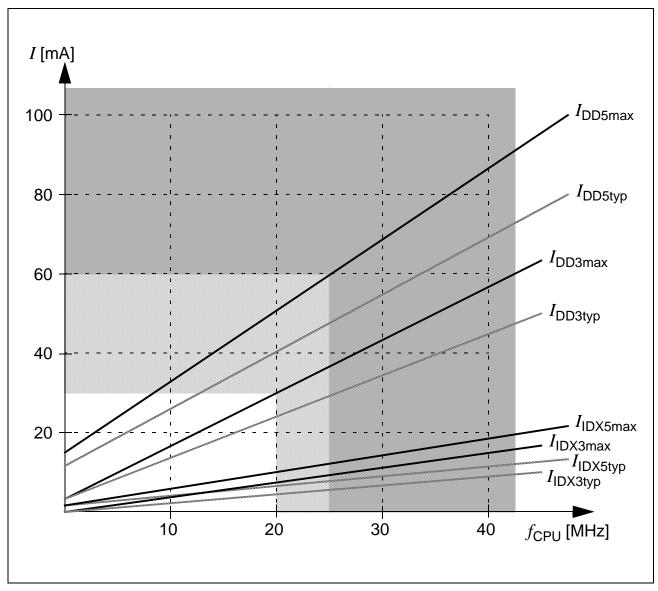


Figure 8 Supply/Idle Current as a Function of Operating Frequency



AC Characteristics Definition of Internal Timing

The internal operation of the C165 is controlled by the internal CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see Figure 9).

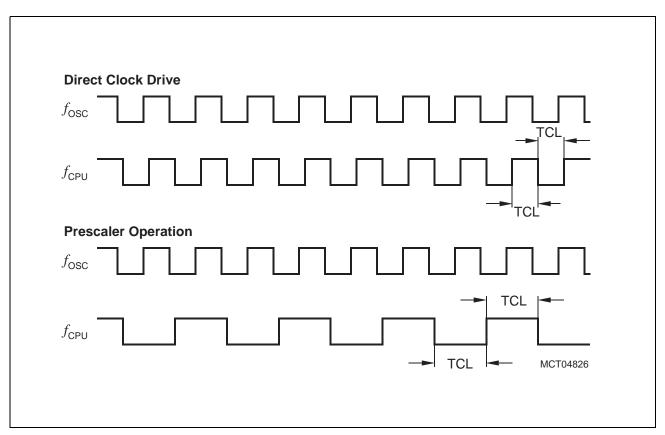


Figure 9 Generation Mechanisms for the CPU Clock

The CPU clock signal $f_{\rm CPU}$ can be generated from the oscillator clock signal $f_{\rm OSC}$ via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate $f_{\rm CPU}$. This influence must be regarded when calculating the timings for the C165.

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5. Upon a long hardware reset register RP0H is loaded with the logic levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins P0.15-13 (P0H.7-5).

Table 9 associates the combinations of these three bits with the respective clock generation mode.



Table 9 C165 C	Clock	Generation	Modes
----------------	-------	------------	-------

	CPU Frequency $f_{\text{CPU}} = f_{\text{OSC}} \times \text{F}$		Notes		
0 X X	$f_{\rm OSC} \times 1$	1 to 25 MHz	Direct drive ²⁾		
1 X X	f _{OSC} / 2	2 to 50 MHz	CPU clock via prescaler		

¹⁾ The external clock input range refers to a CPU clock range of 10 ... 25 MHz (PLL operation).

Prescaler Operation

When prescaler operation is configured (CLKCFG = $1XX_B$) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of $f_{\rm OSC}$ for any TCL.

Direct Drive

When direct drive is configured (CLKCFG = $0XX_B$) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

The frequency of $f_{\rm CPU}$ directly follows the frequency of $f_{\rm OSC}$ so the high and low time of $f_{\rm CPU}$ (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock $f_{\rm OSC}$.

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min}$$
 (DC = duty cycle)

For two consecutive TCLs the deviation caused by the duty cycle of $f_{\rm OSC}$ is compensated so the duration of 2TCL is always $1/f_{\rm OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, ...). Timings that require an even number of TCLs (2, 4, ...) may use the formula 2TCL = $1/f_{\rm OSC}$.

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²⁾ The maximum frequency depends on the duty cycle of the external clock signal.



Table 10 External Clock Drive XTAL1 (Standard Supply Voltage Range)
(Operating Conditions apply)

Parameter	Syml	•		t Drive 1:1			Unit
			min.	max.	min.	max.	
Oscillator period	tosc	SR	40	_	20	_	ns
High time ¹⁾	t_1		20 ²⁾	_	6	_	ns
Low time ¹⁾	t_2	SR	20 ²⁾	_	6	_	ns
Rise time ¹⁾	t_3	SR	_	10	_	6	ns
Fall time ¹⁾	<i>t</i> ₄	SR	_	10	_	6	ns

¹⁾ The clock input signal must reach the defined levels $V_{\rm IL2}$ and $V_{\rm IH2}$.

Table 11 External Clock Drive XTAL1 (Reduced Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol Dir			t Drive :1	Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	_	25	_	ns
High time ¹⁾	<i>t</i> ₁	SR	25 ²⁾	_	8	_	ns
Low time ¹⁾	t_2	SR	25 ²⁾	_	8	_	ns
Rise time ¹⁾	t_3	SR	_	10	_	6	ns
Fall time ¹⁾	<i>t</i> ₄	SR	_	10	_	6	ns

 $^{^{\}rm 1)}~$ The clock input signal must reach the defined levels $V_{\rm IL2}$ and $V_{\rm IH2}.$

The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.



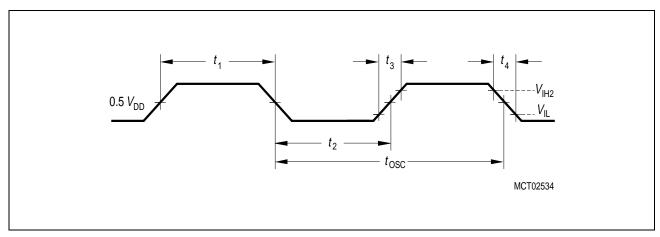


Figure 10 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).



Testing Waveforms

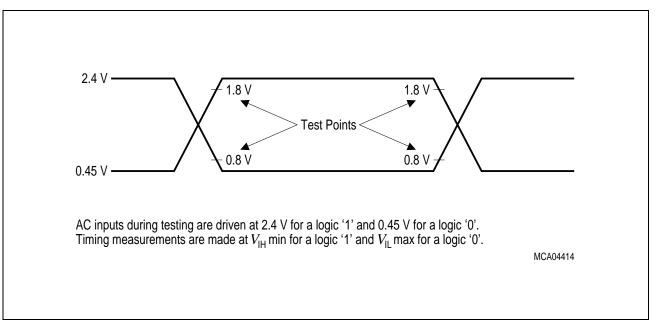


Figure 11 Input Output Waveforms

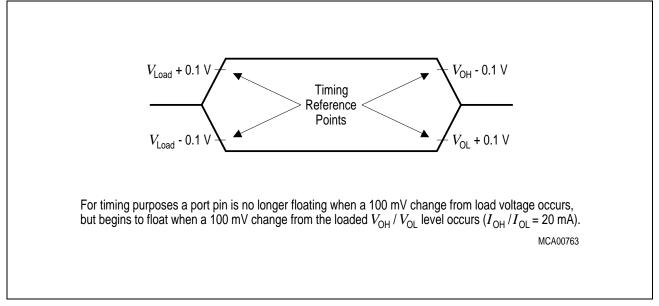


Figure 12 Float Waveforms



Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 12 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_{A}	TCL × <alectl></alectl>
Memory Cycle Time Waitstates	t_{C}	2TCL × (15 - <mctc>)</mctc>
Memory Tristate Time	t_{F}	2TCL × (1 - <mttc>)</mttc>

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Syr	nbol		U Clock MHz	Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
ALE high time	<i>t</i> ₅	CC	10 + t _A	_	TCL - 10 + t _A	_	ns
Address setup to ALE	<i>t</i> ₆	CC	$4 + t_A$	_	TCL - 16 + t _A	_	ns
Address hold after ALE	<i>t</i> ₇	CC	10 + t _A	_	TCL - 10 + t _A	_	ns
ALE falling edge to RD, WR (with RW-delay)	<i>t</i> ₈	CC	10 + t _A	_	TCL - 10 + t _A	_	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	<i>t</i> ₉	CC	- 10 + t _A	_	- 10 + t _A	_	ns
Address float after RD, WR (with RW-delay)	<i>t</i> ₁₀	CC	_	6	_	6	ns
Address float after RD, WR (no RW-delay)	<i>t</i> ₁₁	CC	_	26	_	TCL + 6	ns
RD, WR low time (with RW-delay)	<i>t</i> ₁₂	CC	30 + t _C	_	2TCL - 10 + t _C	_	ns



Multiplexed Bus (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Syr	nbol		U Clock MHz	Variable (Unit	
			min.	max.	min.	max.	
RD, WR low time (no RW-delay)	<i>t</i> ₁₃	CC	50 + t _C	_	3TCL - 10 + t _C	_	ns
RD to valid data in (with RW-delay)	<i>t</i> ₁₄	SR	_	20 + t _C	_	2TCL - 20 + t _C	ns
RD to valid data in (no RW-delay)	<i>t</i> ₁₅	SR	_	40 + t _C	_	3TCL - 20 + t _C	ns
ALE low to valid data in	<i>t</i> ₁₆	SR	_	$40 + t_{A} + t_{C}$	_	3TCL - 20 + t _A + t _C	ns
Address to valid data in	<i>t</i> ₁₇	SR	_	50 + 2t _A + t _C	_	4TCL - 30 + 2t _A + t _C	ns
Data hold after RD rising edge	<i>t</i> ₁₈	SR	0	_	0	_	ns
Data float after RD	<i>t</i> ₁₉	SR	_	26 + t _F	_	2TCL - 14 + t _F	ns
Data valid to WR	t ₂₂	CC	20 + t _C	_	2TCL - 20 + t _C	_	ns
Data hold after WR	t ₂₃	CC	26 + t _F	_	2TCL - 14 + t _F	_	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t ₂₅	CC	26 + t _F	_	2TCL - 14 + t _F	_	ns
Address hold after RD, WR	t ₂₇	CC	26 + t _F	_	2TCL - 14 + <i>t</i> _F	_	ns
ALE falling edge to $\overline{\text{CS}}^{1)}$	t ₃₈	CC	- 4 - t _A	10 - t _A	- 4 - t _A	10 - t _A	ns
CS low to Valid Data In ¹⁾	t ₃₉	SR	_	40 + t _C +2t _A	_	3TCL - 20 + t _C + 2t _A	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{1)}$	t ₄₀	CC	46 + t _F	_	3TCL - 14 + t _F	_	ns
ALE fall. edge to RdCS, WrCS (with RW delay)	t ₄₂	CC	16 + t _A	_	TCL - 4 + t _A	_	ns
ALE fall. edge to RdCS, WrCS (no RW delay)	t ₄₃	CC	- 4 + t _A	_	- 4 + t _A	_	ns



Multiplexed Bus (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		PU Clock MHz		CPU Clock 1 to 25 MHz	Unit
		min.	max.	min.	max.	
Address float after RdCS, WrCS (with RW delay)	t ₄₄ CC	_	0	_	0	ns
Address float after RdCS, WrCS (no RW delay)	<i>t</i> ₄₅ CC	_	20	_	TCL	ns
RdCS to Valid Data In (with RW delay)	<i>t</i> ₄₆ SR	-	16 + t _C	_	2TCL - 24 + t _C	ns
RdCS to Valid Data In (no RW delay)	<i>t</i> ₄₇ SR	_	36 + t _C	_	3TCL - 24 + t _C	ns
RdCS, WrCS Low Time (with RW delay)	t ₄₈ CC	30 + t _C	_	2TCL - 10 + t _C	_	ns
RdCS, WrCS Low Time (no RW delay)	t ₄₉ CC	50 + t _C	_	3TCL - 10 + t _C	_	ns
Data valid to WrCS	<i>t</i> ₅₀ CC	26 + t _C	_	2TCL - 14 + t _C	_	ns
Data hold after RdCS	<i>t</i> ₅₁ SR	0	_	0	_	ns
Data float after RdCS	<i>t</i> ₅₂ SR	_	20 + t _F	_	2TCL - 20 + t _F	ns
Address hold after RdCS, WrCS	t ₅₄ CC	20 + t _F	_	2TCL - 20 + t _F	_	ns
Data hold after WrCS	t ₅₆ CC	20 + t _F	_	2TCL - 20 + t _F	-	ns

¹⁾ These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).



Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Parameter Symbol			Max. CPU Clock = 20 MHz		CPU Clock 1 to 20 MHz	Unit
			min.	max.	min.	max.	
ALE high time	<i>t</i> ₅	CC	11 + t _A	_	TCL - 14 + t _A	_	ns
Address setup to ALE	<i>t</i> ₆	CC	$5 + t_A$	_	TCL - 20 + t _A	_	ns
Address hold after ALE	<i>t</i> ₇	CC	15 + t _A	_	TCL - 10 + t _A	_	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay)	<i>t</i> ₈	CC	15 + t _A	_	TCL - 10 + t _A	_	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	t ₉	CC	- 10 + t _A	_	-10 + t _A	_	ns
Address float after RD, WR (with RW-delay)	<i>t</i> ₁₀	CC	_	6	_	6	ns
Address float after RD, WR (no RW-delay)	t ₁₁	CC	_	31	_	TCL + 6	ns
RD, WR low time (with RW-delay)	t ₁₂	CC	34 + t _C	_	2TCL - 16 + t _C	_	ns
RD, WR low time (no RW-delay)	t ₁₃	CC	59 + t _C	_	3TCL - 16 +t _C	_	ns
RD to valid data in (with RW-delay)	t ₁₄	SR	_	22 + t _C	_	2TCL - 28 + t _C	ns
RD to valid data in (no RW-delay)	t ₁₅	SR	_	47 + t _C	_	3TCL - 28 + t _C	ns
ALE low to valid data in	<i>t</i> ₁₆	SR	_	45 + t _A + t _C	_	3TCL - 30 + t _A + t _C	ns
Address to valid data in	t ₁₇	SR	_	57 + 2 <i>t</i> _A + <i>t</i> _C	_	4TCL - 43 + 2t _A + t _C	ns
Data hold after RD rising edge	t ₁₈	SR	0	_	0	_	ns



Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		ymbol Max. CPU Clock = 20 MHz		Variable (Unit	
			min.	max.	min.	max.	
Data float after RD	t ₁₉ \$	SR	_	36 + t _F	_	2TCL - 14 + t _F	ns
Data valid to WR	t ₂₂ (CC	24 + t _C	_	2TCL - 26 + t _C	_	ns
Data hold after WR	t ₂₃ (CC	36 + t _F	_	2TCL - 14 + t _F	_	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t ₂₅ (CC	36 + t _F	_	2TCL - 14 + t _F	_	ns
Address hold after RD, WR	t ₂₇ (CC	36 + t _F	_	2TCL - 14 + t _F	_	ns
ALE falling edge to $\overline{\text{CS}}^{1)}$	t ₃₈ (CC	- 8 - t _A	10 - t _A	- 8 - t _A	10 - t _A	ns
CS low to Valid Data In ¹⁾	t ₃₉ \$	SR	_	47+ t _C + 2t _A	_	3TCL - 28 + t _C + 2t _A	ns
CS hold after RD, WR ¹⁾	t ₄₀ (CC	57 + t _F	_	3TCL - 18 + t _F	_	ns
ALE fall. edge to RdCS, WrCS (with RW delay)	t ₄₂ (CC	19 + t _A	_	TCL - 6 + t _A	_	ns
ALE fall. edge to RdCS, WrCS (no RW delay)	t ₄₃ (CC	- 6 + t _A	_	- 6 + t _A	_	ns
Address float after RdCS, WrCS (with RW delay)	t ₄₄ (CC	_	0	_	0	ns
Address float after RdCS, WrCS (no RW delay)	t ₄₅ (CC	_	25	_	TCL	ns
RdCS to Valid Data In (with RW delay)	t ₄₆ \$	SR	_	20 + t _C	_	2TCL - 30 + t _C	ns
RdCS to Valid Data In (no RW delay)	t ₄₇ \$	SR	_	45 + t _C	_	3TCL - 30 + t _C	ns
RdCS, WrCS Low Time (with RW delay)	t ₄₈ (CC	38 + t _C	_	2TCL - 12 + t _C	_	ns
RdCS, WrCS Low Time (no RW delay)	t ₄₉ (CC	63 + t _C	_	3TCL - 12 + t _C	_	ns



Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
Data valid to WrCS	t ₅₀ CC	28 + t _C	_	2TCL - 22 + t _C	_	ns
Data hold after RdCS	<i>t</i> ₅₁ SR	0	_	0	_	ns
Data float after RdCS	<i>t</i> ₅₂ SR	_	30 + t _F	_	2TCL - 20 + t _F	ns
Address hold after RdCS, WrCS	t ₅₄ CC	30 + t _F	_	2TCL - 20 + t _F	_	ns
Data hold after WrCS	t ₅₆ CC	30 + t _F	_	2TCL - 20 + t _F	_	ns

¹⁾ These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).



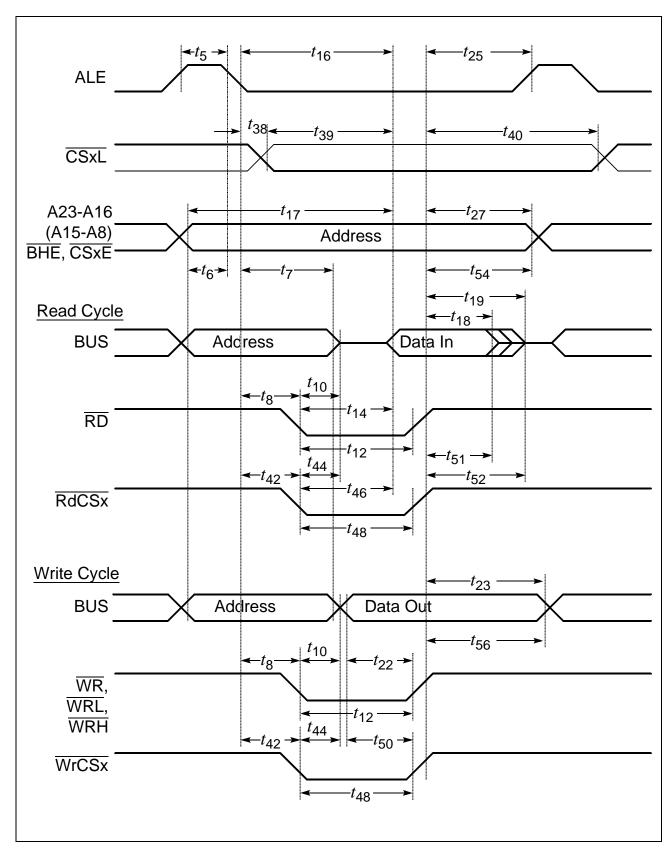


Figure 13 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Normal ALE



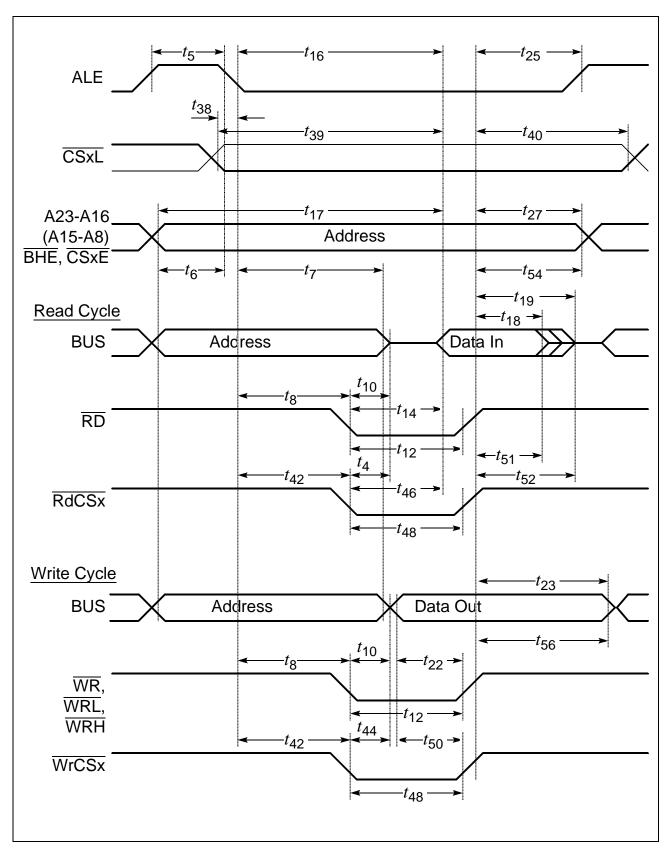


Figure 14 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Extended ALE



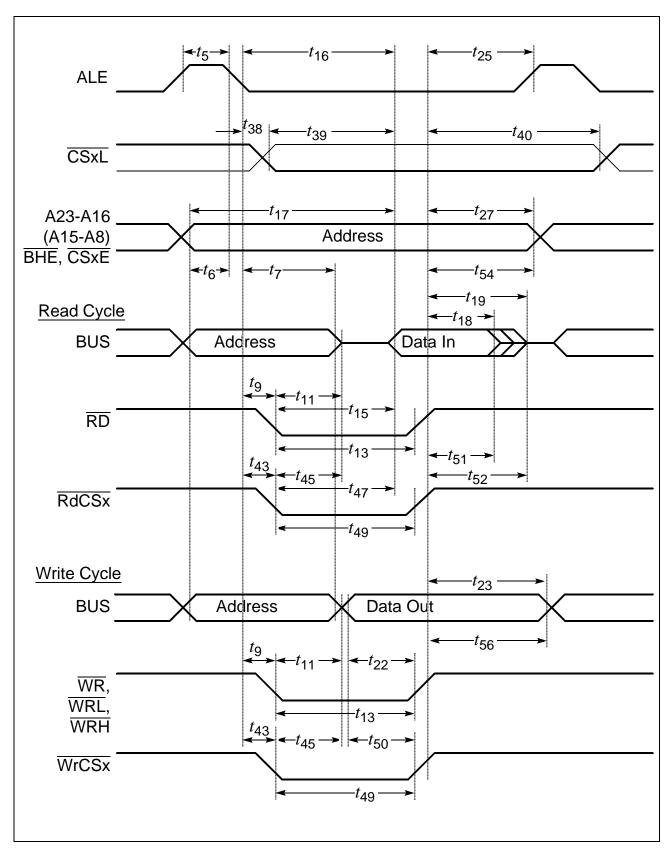


Figure 15 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Normal ALE



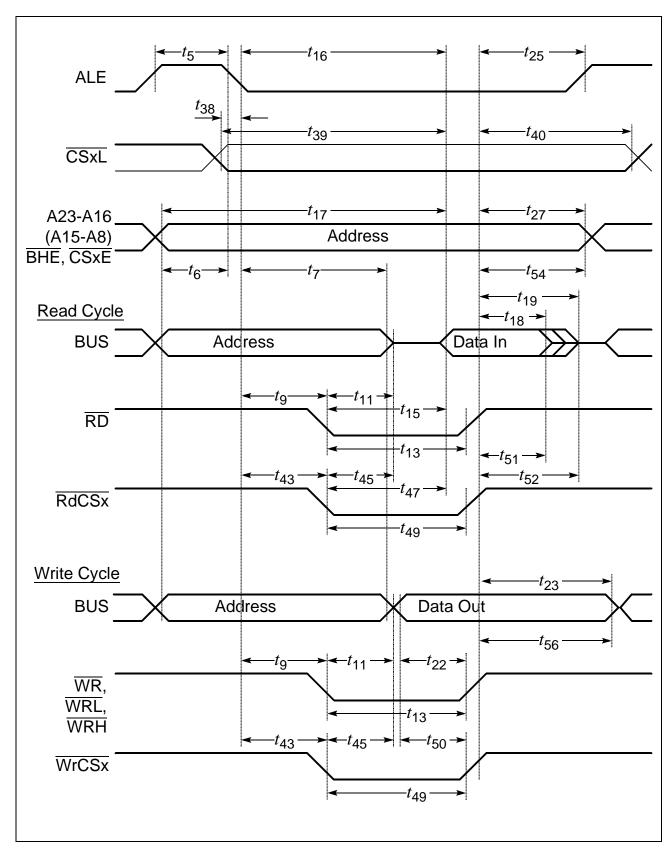


Figure 16 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Extended ALE



Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol			Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		
			min.	max.	min.	max.		
ALE high time	<i>t</i> ₅	CC	10 + t _A	_	TCL - 10 + t _A	_	ns	
Address setup to ALE	<i>t</i> ₆	CC	$4 + t_A$	_	TCL - 16 + t _A	_	ns	
ALE falling edge to RD, WR (with RW-delay)	<i>t</i> ₈	CC	10 + t _A	_	TCL - 10 + t _A	_	ns	
ALE falling edge to RD, WR (no RW-delay)	<i>t</i> ₉	CC	- 10 + t _A	_	- 10 + t _A	_	ns	
RD, WR low time (with RW-delay)	<i>t</i> ₁₂	CC	30 + t _C	_	2TCL - 10 + t _C	_	ns	
RD, WR low time (no RW-delay)	<i>t</i> ₁₃	CC	50 + t _C	_	3TCL - 10 + t _C	_	ns	
RD to valid data in (with RW-delay)	t ₁₄	SR	_	20 + t _C	_	2TCL - 20 + t _C	ns	
RD to valid data in (no RW-delay)	<i>t</i> ₁₅	SR	_	40 + t _C	_	3TCL - 20 + t _C	ns	
ALE low to valid data in	<i>t</i> ₁₆	SR	_	40 + t _A + t _C	_	3TCL - 20 + t _A + t _C	ns	
Address to valid data in	<i>t</i> ₁₇	SR	_	50 + 2t _A + t _C	_	4TCL - 30 + 2t _A + t _C	ns	
Data hold after RD rising edge	<i>t</i> ₁₈	SR	0	_	0	_	ns	
Data float after RD rising edge (with RW-delay ¹⁾)	t ₂₀	SR	_	$26 + 2t_A + t_F^{1)}$	-	2TCL - 14 + 22t _A + t _F ¹⁾	ns	
Data float after RD rising edge (no RW-delay ¹⁾)	t ₂₁	SR	_	$10 + 2t_A + t_F^{1)}$	_	TCL - 10 + 22t _A + t _F ¹⁾	ns	



Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol			PU Clock MHz	Variable (Unit	
			min.	max.	min.	max.	
Data valid to WR	t ₂₂	CC	20 + t _C	_	2TCL - 20	_	ns
					+ t _C		
Data hold after WR	t ₂₄	CC	10 + t _F	_	TCL - 10 + t _F	_	ns
ALE rising edge after RD, WR	t ₂₆	CC	- 10 + t _F	_	- 10 + t _F	_	ns
Address hold after WR ²⁾	t ₂₈	CC	0 + t _F	_	0 + t _F	_	ns
ALE falling edge to $\overline{\text{CS}}^{3)}$	t ₃₈	CC	- 4 - t _A	10 - t _A	- 4 - t _A	10 - t _A	ns
CS low to Valid Data In ³⁾	t ₃₉	SR	_	40 +	_	3TCL - 20	ns
				$t_{\rm C}$ + $2t_{\rm A}$		$+ t_{\rm C} + 2t_{\rm A}$	
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{3)}$	t ₄₁	CC	6 + t _F	_	TCL - 14 + <i>t</i> _F	_	ns
ALE falling edge to RdCS, WrCS (with RW-delay)	t ₄₂	CC	16 + t _A	_	TCL - 4 + t _A	_	ns
ALE falling edge to RdCS, WrCS (no RW-delay)	t ₄₃	CC	$-4 + t_{A}$	_	- 4 + t _A	_	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆	SR	_	16 + t _C	_	2TCL - 24 + t _C	ns
RdCS to Valid Data In (no RW-delay)	t ₄₇	SR	_	36 + t _C	_	3TCL - 24 + t _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈	CC	30 + t _C	_	2TCL - 10 + t _C	_	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉	CC	50 + t _C	_	3TCL - 10 + t _C	_	ns
Data valid to WrCS	t ₅₀	CC	26 + t _C	_	2TCL - 14 + t _C	_	ns
Data hold after RdCS	t ₅₁	SR	0	_	0	_	ns



Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbo		PU Clock 5 MHz	Variable 1 / 2TCL =	Unit	
		min.	max.	min.	max.	
Data float after RdCS (with RW-delay) ¹⁾	<i>t</i> ₅₃ SR	_	20 + t _F	_	2TCL - 20 + 2t _A + t _F	ns
Data float after RdCS (no RW-delay)1)	t ₆₈ SR	_	0 + t _F	_	TCL - 20 + 2t _A + t _F	ns
Address hold after RdCS, WrCS	t ₅₅ CC	- 6 + t _F	_	- 6 + t _F	_	ns
Data hold after WrCS	t ₅₇ CC	6 + t _F	_	TCL - 14 + t _F	_	ns

¹⁾ RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

²⁾ Read data are latched with the same clock edge that triggers the address change and the rising \overline{RD} edge. Therefore address changes before the end of \overline{RD} have no impact on read cycles.

³⁾ These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).



Demultiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
ALE high time	<i>t</i> ₅	CC	11 + t _A	_	TCL - 14 + t _A	_	ns
Address setup to ALE	<i>t</i> ₆	CC	$5 + t_A$	_	TCL - 20 + t _A	_	ns
ALE falling edge to RD, WR (with RW-delay)	<i>t</i> ₈	CC	15 + t _A	_	TCL - 10 + t _A	_	ns
ALE falling edge to RD, WR (no RW-delay)	<i>t</i> ₉	CC	- 10 + t _A	_	- 10 + t _A	_	ns
RD, WR low time (with RW-delay)	<i>t</i> ₁₂	CC	34 + t _C	_	2TCL - 16 + t _C	_	ns
RD, WR low time (no RW-delay)	<i>t</i> ₁₃	CC	59 + t _C	_	3TCL - 16 + t _C	_	ns
RD to valid data in (with RW-delay)	t ₁₄	SR	_	22 + t _C	_	2TCL - 28 + t _C	ns
RD to valid data in (no RW-delay)	<i>t</i> ₁₅	SR	_	47 + t _C	_	3TCL - 28 + t _C	ns
ALE low to valid data in	<i>t</i> ₁₆	SR	_	45 + t _A + t _C	_	3TCL - 30 + t _A + t _C	ns
Address to valid data in	t ₁₇	SR	_	57 + 2t _A + t _C	_	4TCL - 43 + 2t _A + t _C	ns
Data hold after RD rising edge	<i>t</i> ₁₈	SR	0	_	0	_	ns
Data float after RD rising edge (with RW-delay ¹⁾)	t ₂₀	SR	_	$36 + 2t_A + t_F^{1)}$	-	2TCL - 14 + 22t _A + t _F ¹⁾	ns
Data float after RD rising edge (no RW-delay ¹⁾)	t ₂₁	SR	_	$15 + 2t_A + t_F^{(1)}$	_	TCL - 10 + 22t _A + t _F ¹⁾	ns



Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		PU Clock) MHz		CPU Clock 1 to 20 MHz	Unit
		min.	max.	min.	max.	
Data valid to WR	t ₂₂ CC	24 + t _C	_	2TCL - 26 + t _C	_	ns
Data hold after WR	t ₂₄ CC	15 + t _F	_	TCL - 10 + t _F	_	ns
ALE rising edge after RD, WR	t ₂₆ CC	- 12 + t _F	_	- 12 + t _F	_	ns
Address hold after WR ²⁾	t ₂₈ CC	0 + t _F	_	0 + t _F	_	ns
ALE falling edge to $\overline{CS}^{3)}$	t ₃₈ CC	- 8 - t _A	10 - t _A	- 8 - t _A	10 - t _A	ns
CS low to Valid Data In ³⁾	<i>t</i> ₃₉ SR	_	$47 + t_{C} + 2t_{A}$	_	3TCL - 28 + t _C + 2t _A	ns
CS hold after RD, WR ³⁾	t ₄₁ CC	9 + t _F	_	TCL - 16 + t _F	_	ns
ALE falling edge to RdCS, WrCS (with RW-delay)	t ₄₂ CC	19 + t _A	_	TCL - 6 + t _A	-	ns
ALE falling edge to RdCS, WrCS (no RW-delay)	t ₄₃ CC	- 6 + t _A	_	- 6 + t _A	_	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆ SR	_	20 + t _C	_	2TCL - 30 + t _C	ns
RdCS to Valid Data In (no RW-delay)	<i>t</i> ₄₇ SR	_	45 + t _C	_	3TCL - 30 + t _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈ CC	38 + t _C	_	2TCL - 12 + t _C	_	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉ CC	63 + t _C	_	3TCL - 12 + t _C	_	ns
Data valid to WrCS	t ₅₀ CC	28 + t _C	_	2TCL - 22 + t _C	_	ns
Data hold after RdCS	<i>t</i> ₅₁ SR	0	_	0	_	ns



Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbo		PU Clock) MHz	Variable (Unit	
		min.	max.	min.	max.	
Data float after RdCS (with RW-delay) ¹⁾	t ₅₃ SF	-	30 + t _F	-	2TCL - 20 + 2t _A + t _F	ns
Data float after RdCS (no RW-delay)1)	t ₆₈ SF	_	5 + t _F	_	TCL - 20 + 2t _A + t _F	ns
Address hold after RdCS, WrCS	t ₅₅ CC	- 16 + t _F	_	- 16 + t _F	_	ns
Data hold after WrCS	t ₅₇ CC	9 + t _F	_	TCL - 16 + t _F	_	ns

¹⁾ RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

²⁾ Read data are latched with the same clock edge that triggers the address change and the rising \overline{RD} edge. Therefore address changes before the end of \overline{RD} have no impact on read cycles.

³⁾ These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).



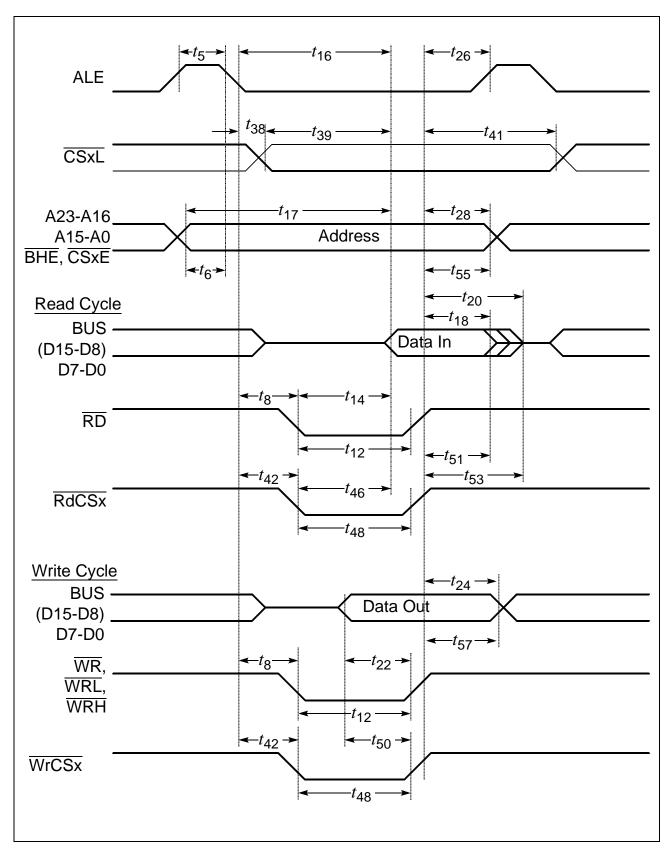


Figure 17 External Memory Cycle:
Demultiplexed Bus, With Read/Write Delay, Normal ALE



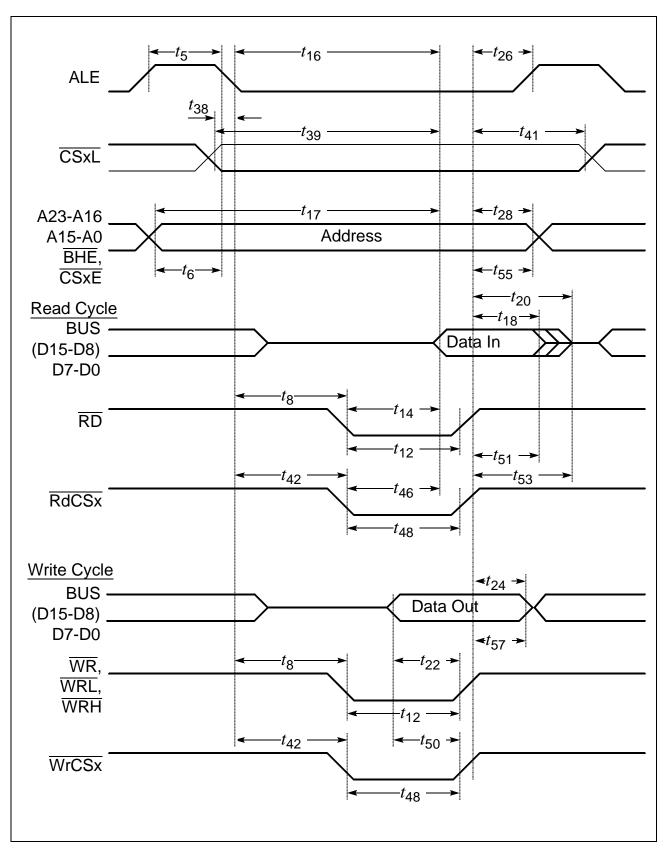


Figure 18 External Memory Cycle:
Demultiplexed Bus, With Read/Write Delay, Extended ALE



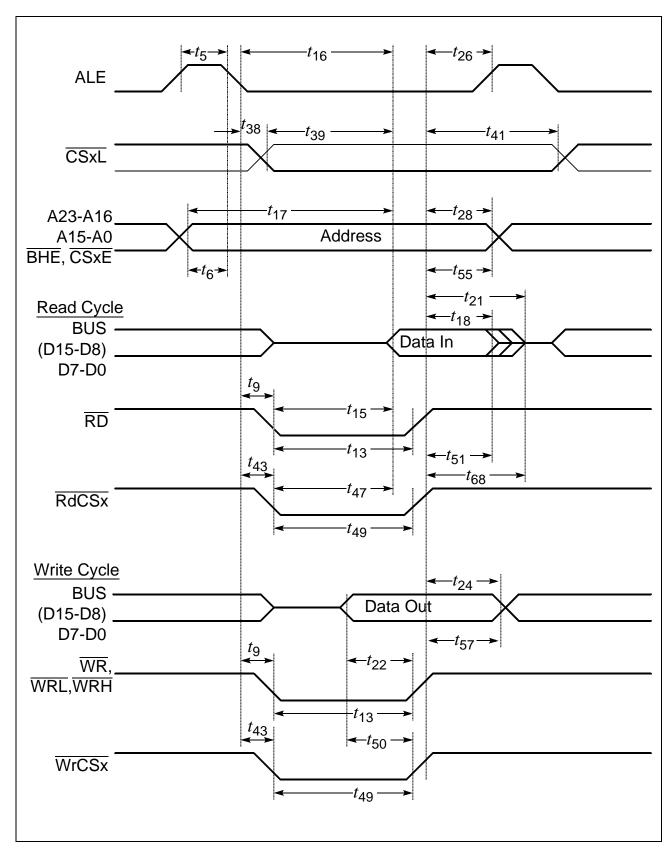


Figure 19 External Memory Cycle:
Demultiplexed Bus, No Read/Write Delay, Normal ALE



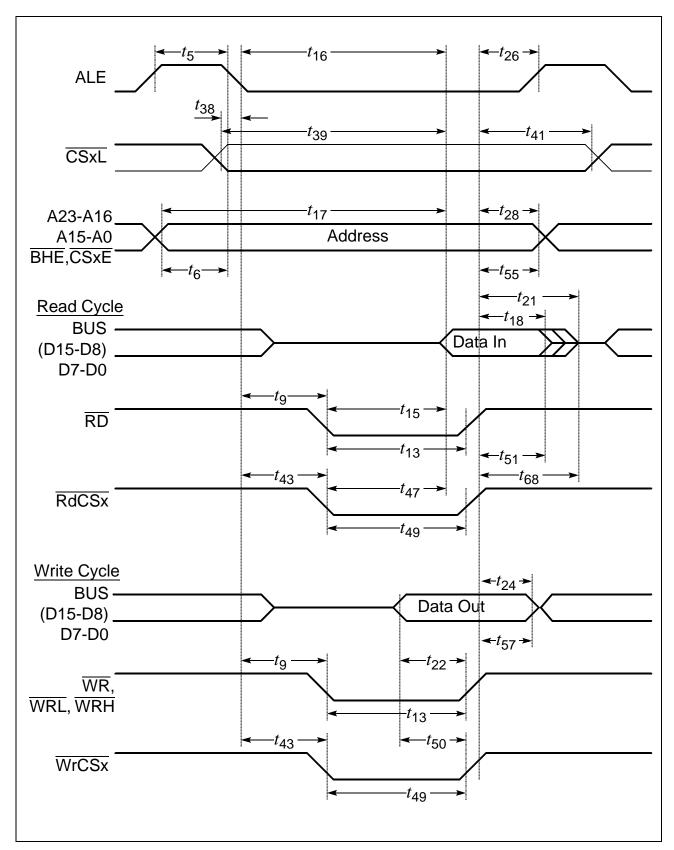


Figure 20 External Memory Cycle:
Demultiplexed Bus, No Read/Write Delay, Extended ALE



CLKOUT and READY (Standard Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t ₂₉	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t ₃₀	CC	14	_	TCL - 6	_	ns
CLKOUT low time	t ₃₁	CC	10	_	TCL - 10	_	ns
CLKOUT rise time	t ₃₂	CC	_	4	_	4	ns
CLKOUT fall time	t ₃₃	CC	_	4	_	4	ns
CLKOUT rising edge to ALE falling edge	t ₃₄	CC	$0 + t_{A}$	10 + t _A	0 + t _A	10 + t _A	ns
Synchronous READY setup time to CLKOUT	t ₃₅	SR	14	_	14	_	ns
Synchronous READY hold time after CLKOUT	t ₃₆	SR	4	_	4	_	ns
Asynchronous READY low time	t ₃₇	SR	54	_	2TCL + t ₅₈	_	ns
Asynchronous READY setup time ¹⁾	t ₅₈	SR	14	_	14	_	ns
Asynchronous READY hold time ¹⁾	t ₅₉	SR	4	_	4	_	ns
Async. READY hold time after RD, WR high (Demultiplexed Bus) ²⁾	<i>t</i> ₆₀	SR	0	0 + $2t_A$ + t_C + $t_F^{2)}$	0	TCL - 20 + 2t _A + t _C + t _F ²⁾	ns

¹⁾ These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

²⁾ Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.

The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.



CLKOUT and READY (Reduced Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t ₂₉	CC	50	50	2TCL	2TCL	ns
CLKOUT high time	t ₃₀	CC	15	_	TCL - 10	_	ns
CLKOUT low time	t ₃₁	CC	13	_	TCL - 12	_	ns
CLKOUT rise time	t ₃₂	CC	_	12	_	12	ns
CLKOUT fall time	t ₃₃	CC	_	8	_	8	ns
CLKOUT rising edge to ALE falling edge	t ₃₄	CC	$0 + t_{A}$	8 + t _A	0 + t _A	8 + t _A	ns
Synchronous READY setup time to CLKOUT	t ₃₅	SR	18	_	18	_	ns
Synchronous READY hold time after CLKOUT	t ₃₆	SR	4	_	4	_	ns
Asynchronous READY low time	t ₃₇	SR	68	_	2TCL + t ₅₈	_	ns
Asynchronous READY setup time ¹⁾	t ₅₈	SR	18	_	18	_	ns
Asynchronous READY hold time ¹⁾	t ₅₉	SR	4	_	4	_	ns
Async. READY hold time after RD, WR high (Demultiplexed Bus) ²⁾	t ₆₀	SR	0	$0 + 2t_A + t_C + t_F^{2)}$	0	TCL - 25 + 2t _A + t _C + t _F ²	ns

¹⁾ These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

²⁾ Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.

The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.



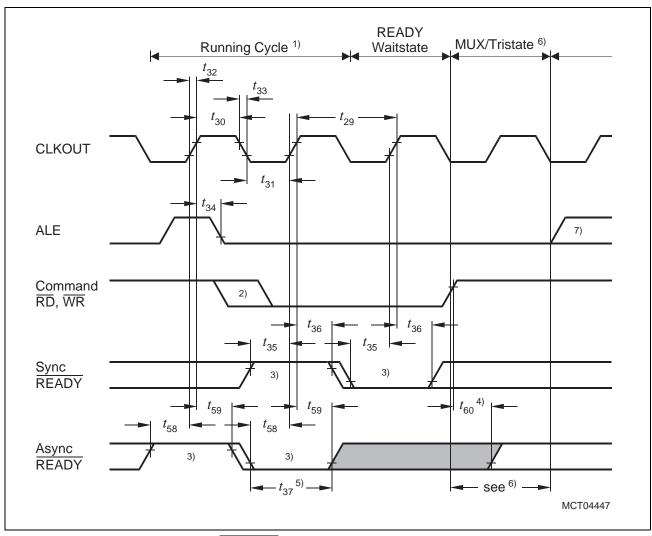


Figure 21 CLKOUT and READY

Notes

- 1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2) The leading edge of the respective command depends on RW-delay.
- READY sampled HIGH at this sampling point generates a READY controlled waitstate, READY sampled LOW at this sampling point terminates the currently running bus cycle.
- 4) READY may be deactivated in response to the trailing (rising) edge of the corresponding command (RD or WR).
- 5) If the Asynchronous READY signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).
- Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
 - For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
- 7) The next external bus cycle may start here.



External Bus Arbitration (Standard Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
HOLD input setup time to CLKOUT	<i>t</i> ₆₁ SR	20	_	20	_	ns
CLKOUT to HLDA high or BREQ low delay	t ₆₂ CC	_	20	_	20	ns
CLKOUT to HLDA low or BREQ high delay	t ₆₃ CC	_	20	_	20	ns
CSx release	t ₆₄ CC	_	20	_	20	ns
CSx drive	t ₆₅ CC	- 4	24	- 4	24	ns
Other signals release	t ₆₆ CC	_	20	_	20	ns
Other signals drive	t ₆₇ CC	- 4	24	- 4	24	ns

External Bus Arbitration (Reduced Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
HOLD input setup time to CLKOUT	<i>t</i> ₆₁ SR	30	_	30	_	ns
CLKOUT to HLDA high or BREQ low delay	t ₆₂ CC	_	20	_	20	ns
CLKOUT to HLDA low or BREQ high delay	t ₆₃ CC	_	20	_	20	ns
CSx release	t ₆₄ CC	_	20	_	20	ns
CSx drive	t ₆₅ CC	- 4	30	- 4	30	ns
Other signals release	t ₆₆ CC	_	20	_	20	ns
Other signals drive	t ₆₇ CC	- 4	30	- 4	30	ns



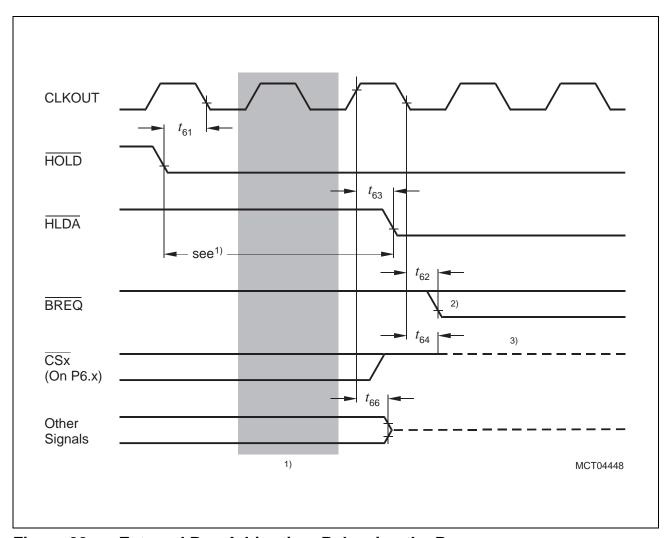


Figure 22 **External Bus Arbitration, Releasing the Bus**

Notes

- 1) The C165 will complete the currently running bus cycle before granting bus access.
- This is the first possibility for $\overline{\mathsf{BREQ}}$ to get active. The $\overline{\mathsf{CS}}$ outputs will be resistive high (pullup) after t_{64} .



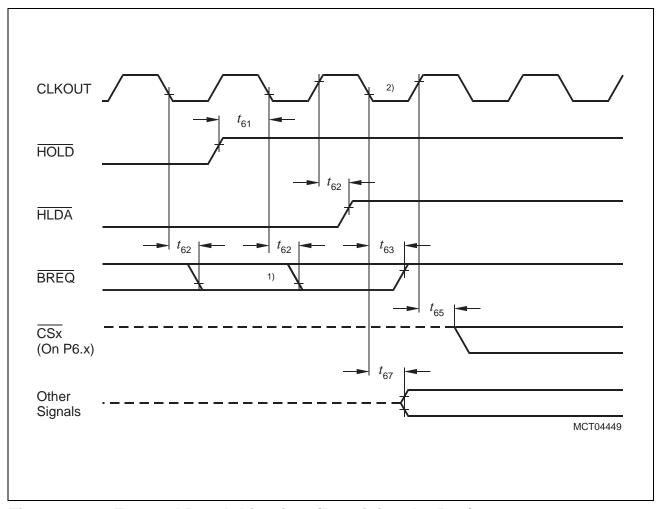


Figure 23 External Bus Arbitration, (Regaining the Bus)

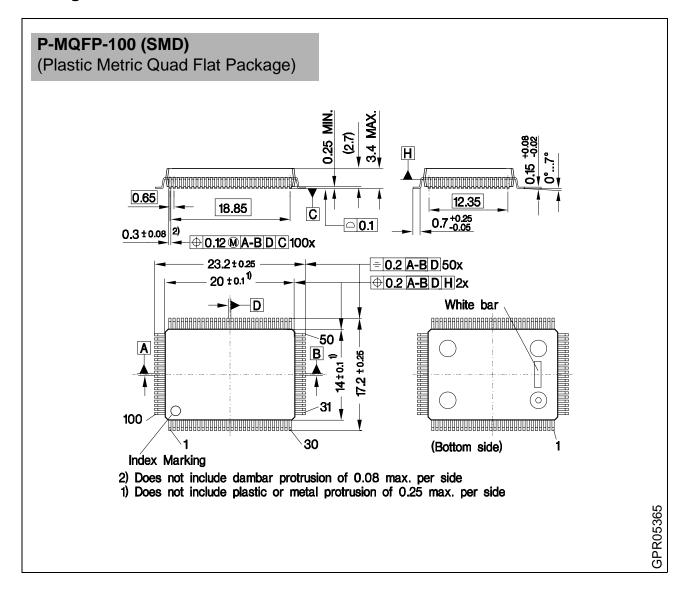
Notes

- This is the last chance for BREQ to trigger the indicated regain-sequence.

 Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the C165 requesting the bus.
- 2) The next C165 driven bus cycle may start here.



Package Outlines



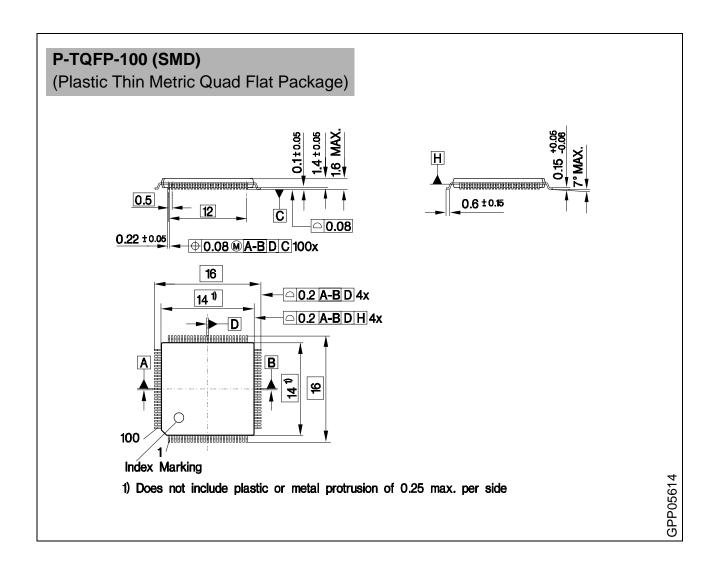
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm





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