

QS5U17

Silicon N-channel MOSFET
Schottky Barrier DIODE

- 1) The QS5U17 combines Nch MOSFET with a Schottky barrier diode in a single TSMT5 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) The Independently connected Schottky barrier diode has low forward voltage.

Load switch, DC / DC conversion

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS5U17		○

The drawing shows the mechanical specifications for a TSMT package. The top view includes dimensions for the overall width (2.9), the distance between the center of the leads (1.9), and the lead width (0.95). The leads are numbered (1) through (5). The side view shows the maximum height (1.0 MAX), the lead height (0.85), the lead thickness (0.7), the standoff height (1.6), the lead thickness (2.8), the lead width (0.1), the lead thickness (0.3-0.6), and the lead width (0.16).

Each lead has same dimensions

Abbreviated symbol : U17

The diagram shows a MOSFET with an ESD protection diode and a body diode. The MOSFET has a Gate terminal (1), a Source terminal (2), and a Drain terminal (3). An ESD protection diode (*1) is connected between the Gate and Source terminals. A body diode (*2) is connected between the Drain and Source terminals. The Drain terminal is also connected to a Cathode terminal (4) and a Drain terminal (5).

(1) Gate
(2) Source
(3) Anode
(4) Cathode
(5) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

Transistors

●Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	12	V
Drain current	Continuous	I_D	±2.0	A
	Pulsed	I_{DP} *1	±8.0	A
Source current (Body diode)	Continuous	I_S	0.8	A
	Pulsed	I_{SP} *1	3.2	A
Channel temperature		T_{ch}	150	°C
Power dissipation		P_D *3	0.9	W/ELEMENT

<Di>

Repetitive peak reverse voltage	V_{RM}	25	V
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	A
Forward current surge peak	I_{FSM} *2	3.0	A
Junction temperature	T_j	150	°C
Power dissipation	P_D *3	0.7	W/ELEMENT

<MOSFET AND Di>

Total power dissipation	P_D *3	1.25	W / TOTAL
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$ *2 60Hz-1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	10	μA	$V_{GS}=12V / V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	—	—	V	$I_D=1mA, / V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=30V / V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	—	1.5	V	$V_{DS}=10V / I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	71	100	m Ω	$I_D=2.0A, V_{GS}=4.5V$
		—	76	107	m Ω	$I_D=2.0A, V_{GS}=4V$
		—	110	154	m Ω	$I_D=2.0A, V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.5	—	—	S	$V_{DS}=10V, I_D=2.0A$
Input capacitance	C_{iss}	—	175	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	50	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	25	—	pF	$f=1MHz$
Turn-on delay time	$t_d(on)$ *	—	8	—	ns	$I_D=1.0A$
Rise time	t_r *	—	10	—	ns	$V_{DD} \doteq 15V$
Turn-off delay time	$t_d(off)$ *	—	21	—	ns	$V_{GS}=4.5V$
Fall time	t_f *	—	8	—	ns	$R_L=15\Omega$
Total gate charge	Q_g *	—	2.8	3.9	nC	$V_{DD} \doteq 15V$
Gate-source charge	Q_{gs} *	—	0.6	—	nC	$V_{GS}=4.5V$
Gate-drain charge	Q_{gd} *	—	0.8	—	nC	$I_D=2.0A$

*Pulsed

<Body diode (source-drain)>

Forward voltage	V_{SD} *	—	—	1.2	V	$I_S=3.2A / V_{GS}=0V$
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* Pulsed

<Di>

Forward voltage	V_F	—	—	0.45	V	$I_F=1.0A$
Reverse current	I_R	—	—	200	μA	$V_R=20V$

Transistors

●Electrical characteristic curves

<MOSFET>

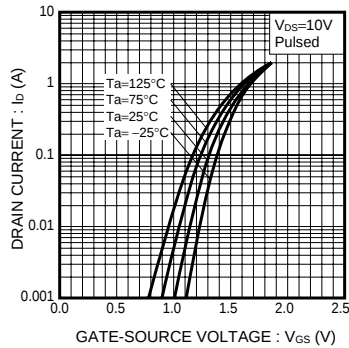


Fig.1 Typical Transfer Characteristics

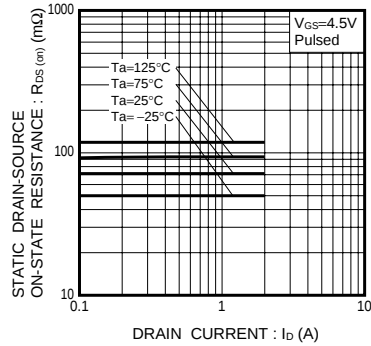


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

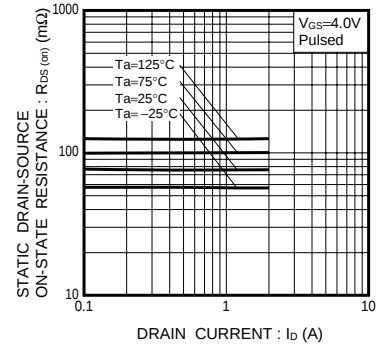


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

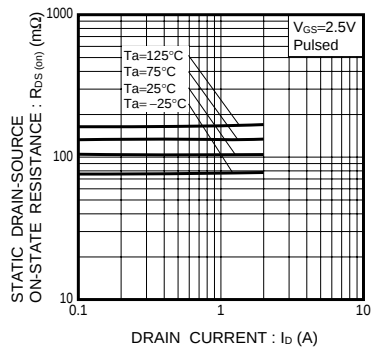


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

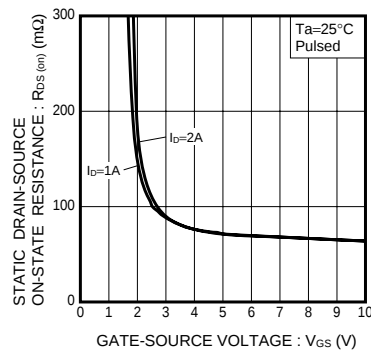


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

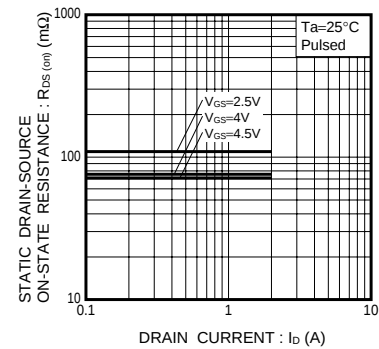


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

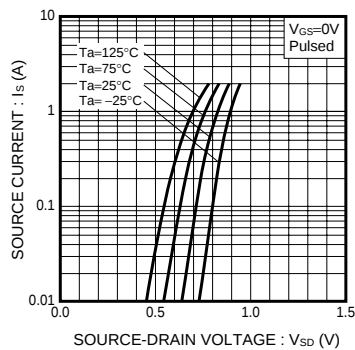


Fig.7 Reverse Drain Current vs. Source-Drain Current

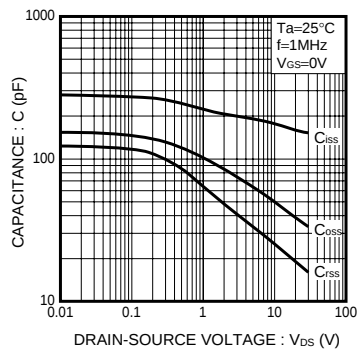


Fig.8 Typical Capacitance vs. Drain-Source Voltage

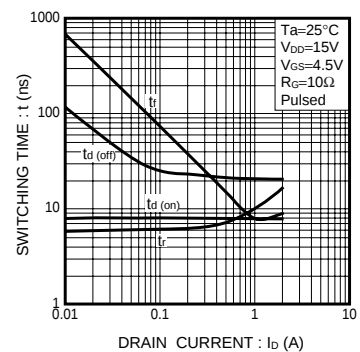


Fig.9 Switching Characteristics

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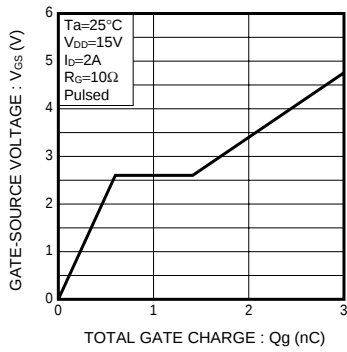


Fig.10 Dynamic Input Characteristics

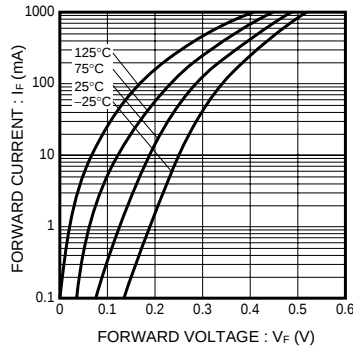


Fig.11 Forward Current vs. Forward Voltage

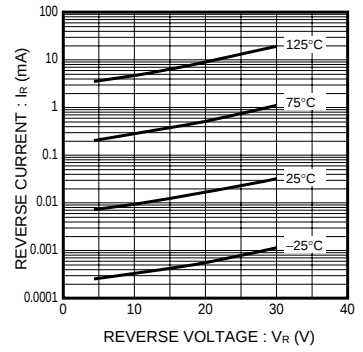


Fig.12 Reverse Current vs. Reverse Voltage

●Measurement circuits

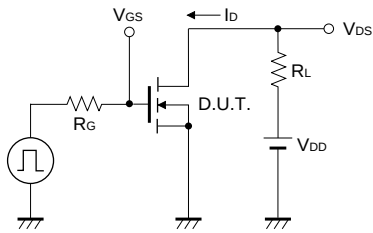


Fig.13 Switching Time Measurement Circuit

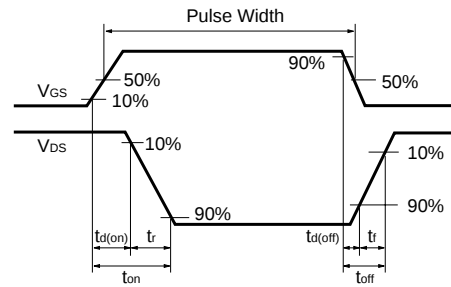


Fig.14 Switching Waveforms

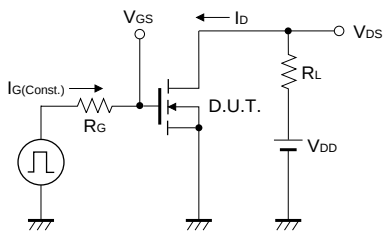


Fig.15 Gate Charge Measurement Circuit

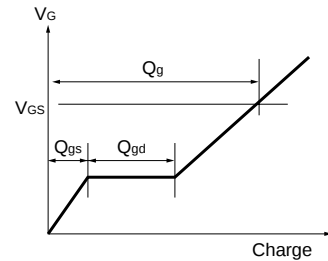


Fig.16 Gate Charge Waveform

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