

RJK5030DPP-M0

Silicon N Channel MOS FET
High Speed Power Switching

R07DS0227EJ0100

Rev.1.00

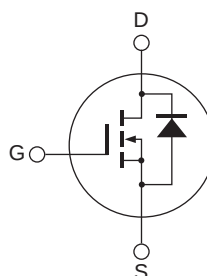
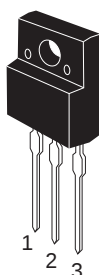
Dec 14, 2010

Features

- Low on-state resistance
 $R_{DS(on)} = 1.3 \Omega$ typ. (at $I_D = 2 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High speed switching

Outline

RENESAS Package code: PRSS0003AF-A
(Package name: TO-220FL)



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	20	A
Avalanche current	I_{AP} ^{Note3}	5	A
Channel dissipation	P_{ch} ^{Note 2}	28.5	W
Channel to case thermal Impedance	θ_{ch-c}	4.38	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. Pulse width limited by safe operating area.

2. Value at $T_c = 25^\circ\text{C}$

3. $ST_{ch} = 25^\circ\text{C}$, $T_{ch} \leq 150^\circ\text{C}$

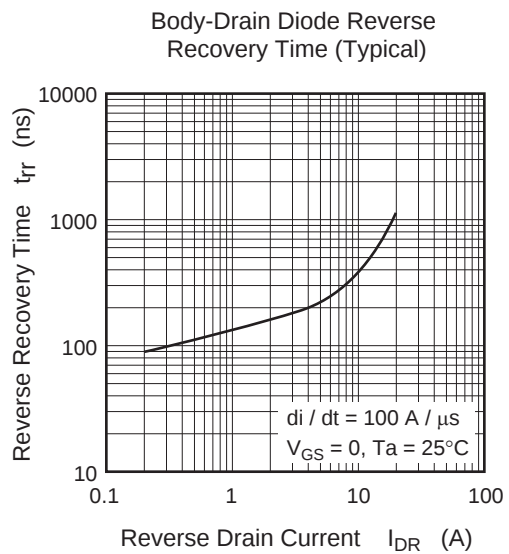
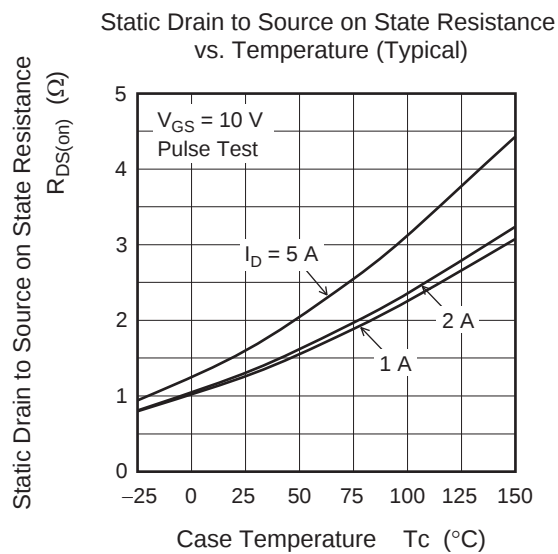
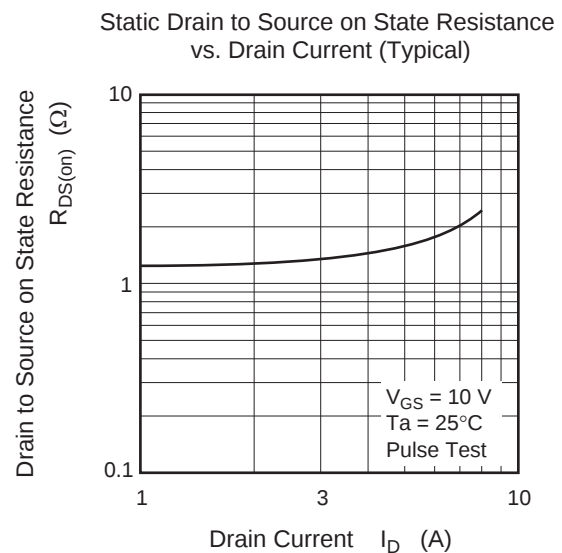
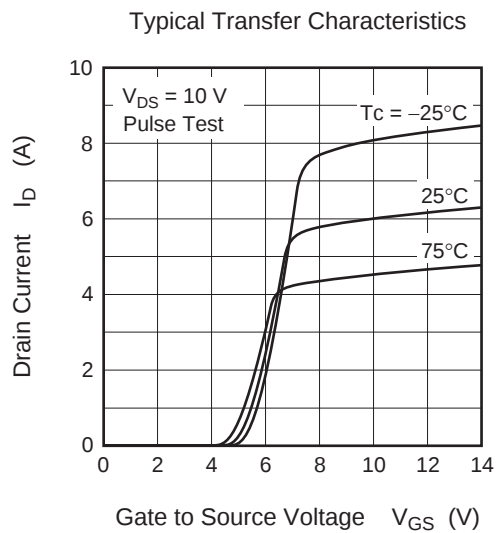
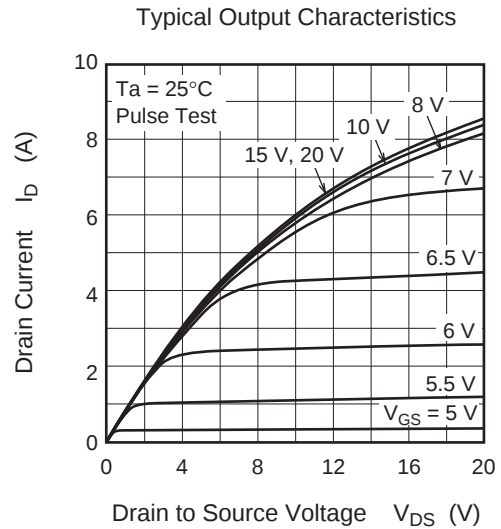
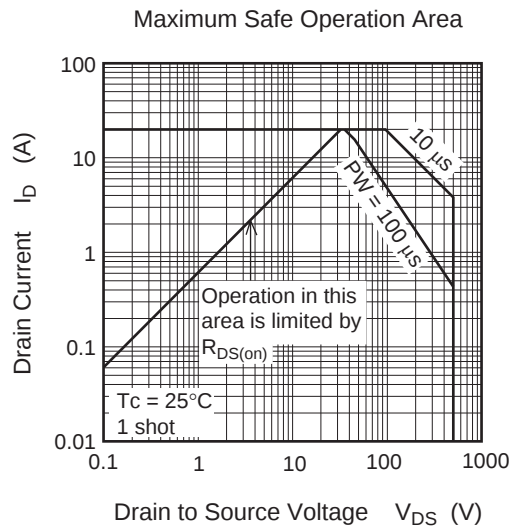
Electrical Characteristics

(Ta = 25°C)

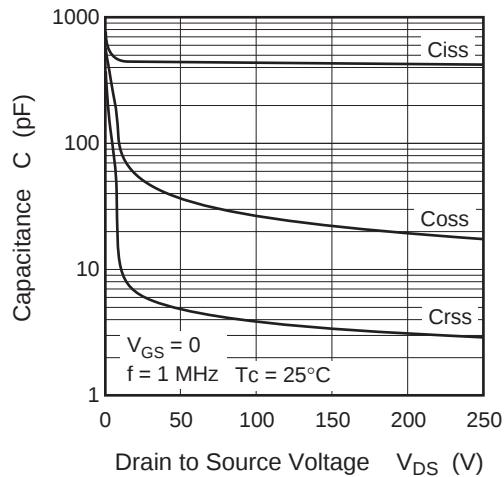
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR) DSS}$	500	—	—	V	$I_D = 1 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS (off)}$	3.5	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS (on)}$	—	1.3	1.6	Ω	$I_D = 2 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	550	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	60	—	pF	
Reverse transfer capacitance	C_{rss}	—	10	—	pF	
Turn-on delay time	$t_{d (on)}$	—	15	—	ns	$V_{DD} = 200 \text{ V}$ $I_D = 2 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_g = 25 \Omega$
Rise time	t_r	—	20	—	ns	
Turn-off delay time	$t_{d (off)}$	—	90	—	ns	
Fall time	t_f	—	30	—	ns	
Total gate charge	Q_g	—	13	—	nC	$V_{DD} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 5 \text{ A}$
Gate to source charge	Q_{gs}	—	3.3	—	nC	
Gate to drain charge	Q_{gd}	—	6.6	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.9	1.5	V	$I_F = 5 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body-drain diode reverse recovery time	t_{rr}	—	250	—	ns	$I_F = 5 \text{ A}$, $V_{GS} = 0$ $V_{DD} = 250 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

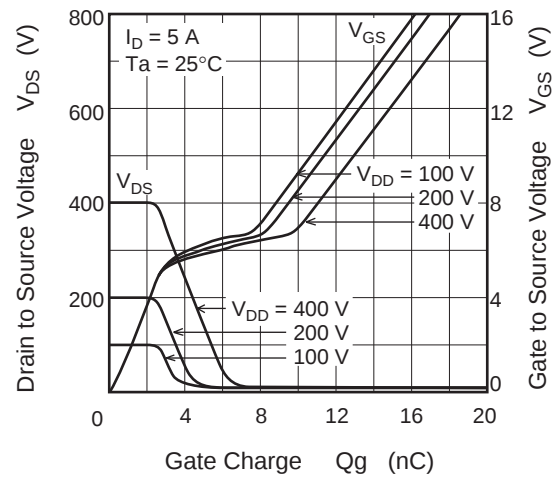
Main Characteristics



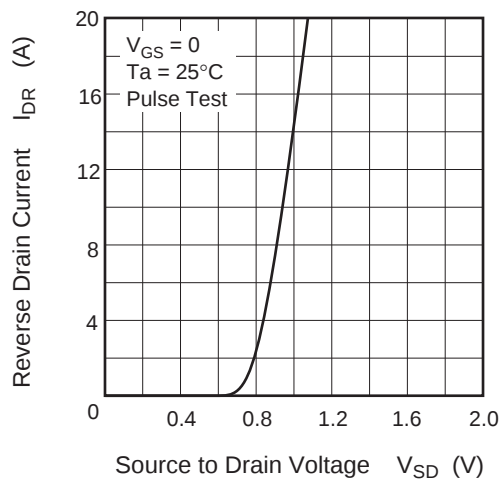
Typical Capacitance vs.
Drain to Source Voltage



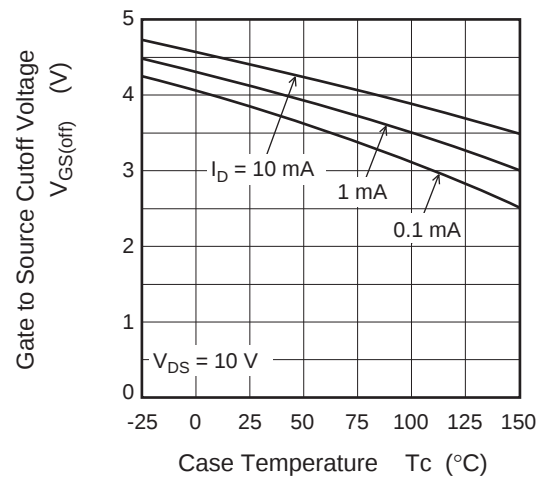
Dynamic Input Characteristics (Typical)

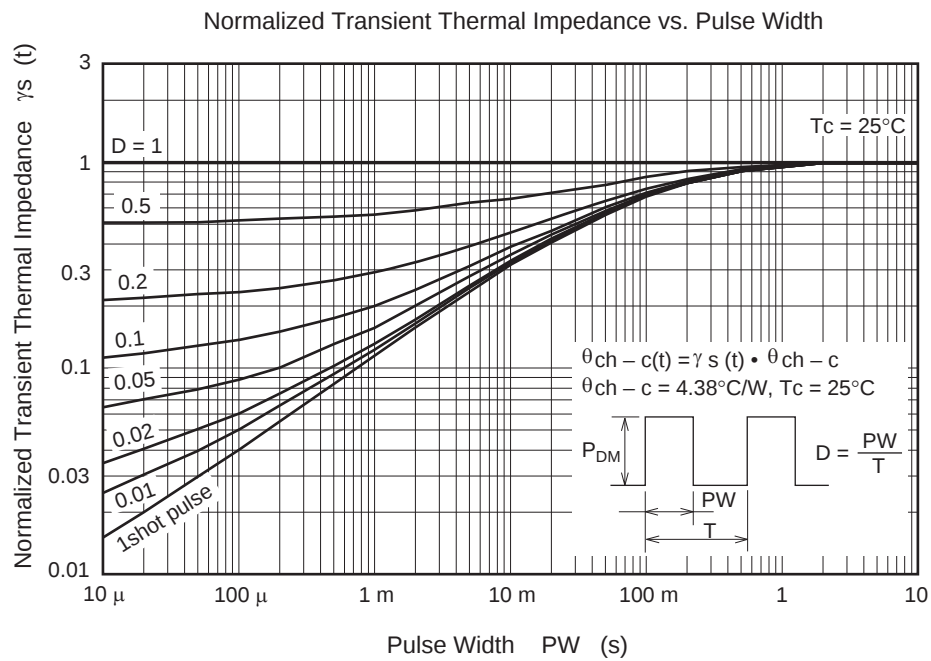


Reverse Drain Current vs.
Source to Drain Voltage (Typical)

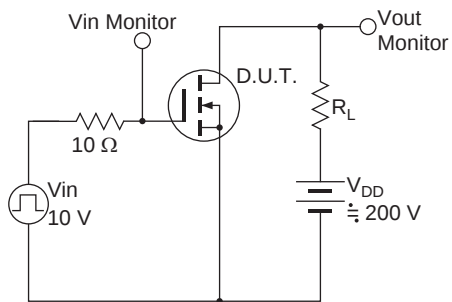


Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)

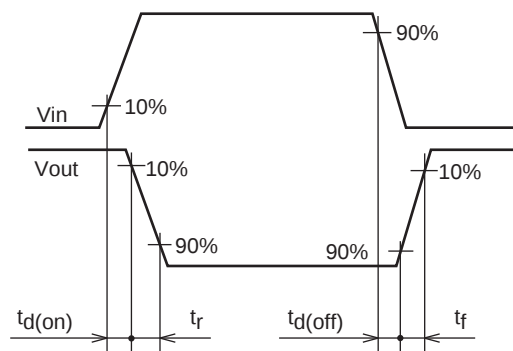




Switching Time Test Circuit



Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
TO-220FL	—	PRSS0003AF-A	TO-220FL	1.5g	

The drawing shows the mechanical specifications of the TO-220FL package. The top view indicates a square body with a width of 10.0 ± 0.3 mm and a height of 15.0 ± 0.3 mm. The mounting tab has a width of 6.5 ± 0.3 mm and a height of 3.0 ± 0.3 mm. The central hole has a diameter of $\phi 3.2 \pm 0.2$ mm. The side view shows a total height of 12.5 ± 0.5 mm, with a mounting tab height of 3.6 ± 0.3 mm. The lead length is 2.8 ± 0.2 mm, and the lead thickness is 0.40 ± 0.15 mm. The lead width at the base is 2.54 ± 0.25 mm. The detail view shows a lead thickness of 0.75 ± 0.15 mm and a lead width of 1.15 ± 0.2 mm. The bottom view shows a width of 2.6 ± 0.2 mm and a height of 4.5 ± 0.2 mm.

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK5030DPP-M0-T2	1050 pcs	Box (Tube)

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