WM8231

105 MSPS 3-Channel AFE with Sensor Timing Generation and LVDS/CMOS Data Output

DESCRIPTION

The WM8231 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 35 MSPS per channel.

The device has three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling (also Sample and Hold), Programmable Gain, Automatic Gain Control (AGC) and Offset adjust functions.

The output from each of these channels is time multiplexed, in pairs, into three high-speed 16-bit Analogue to Digital Converters. The digital data is available in a variety of output formats via the flexible data port.

The WM8231 has a user selectable LVDS or CMOS output architecture.

An internal 5-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

A programmable automatic Black-Level Calibration function is available to adjust the DC offset of the output data.

The WM8231 features a sensor timing clock generator for both CCD and CIS sensors. The clock generator can accept a slow or fast reference clock input and also has a flexible timing adjustment function for output timing clocks to allow use of many different sensors.

FEATURES

- 105 MSPS conversion rate
- 16-bit ADC resolution
- Current consumption – 230mA
- 3.3V single supply operation
- Sample and hold / correlated double sampling
- Programmable offset adjust (8-bit resolution)
- Flexible clamp timing
- Pixel clamp / line clamp mode
- Programmable clamp voltage
- Programmable CIS/CCD timing generator
- Internally generated voltage references
- Compliant for Spread Spectrum Clock
- LVDS/CMOS output options
  - LVDS 5-pair 315 MHz 35-bit data
  - CMOS 90 MHz output maximum
- Complete on chip clock generator. MCLK 5 – 35 MHz.
- Internal timing adjustment
- Automatic Gain Control
- Automatic Black Level Calibration
- 56-lead QFN package 8mm x 8mm
- Serial control interface

APPLICATIONS

- Digital copiers
- USB 2.0 compatible scanners
- Multi-function peripherals
- High-speed CCD/CIS sensor interface

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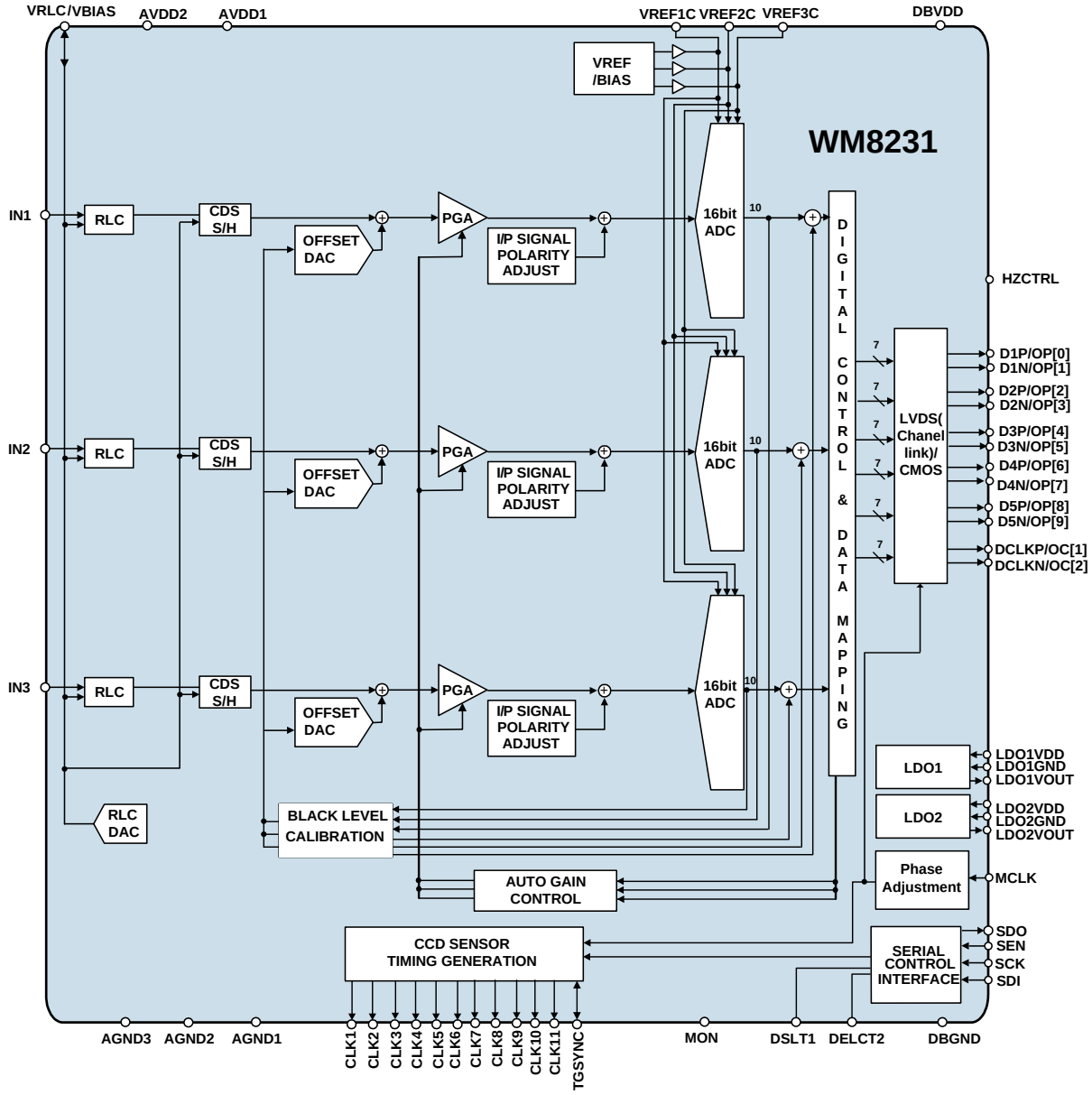
BLOCK DIAGRAM



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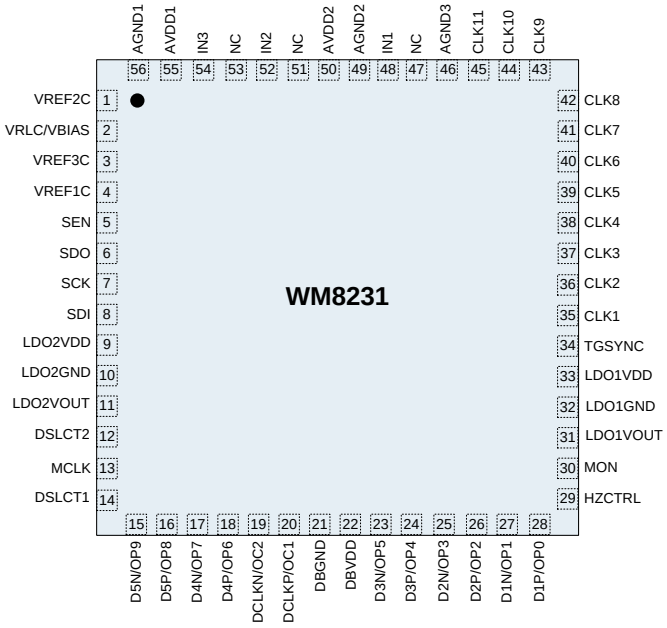
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8231GEFL/V	-40 to 85ºC	56-lead QFN (8 x 8 x 0.85 mm) (Pb-free)	MSL3	260°C
WM8231GEFL/RV	-40 to 85ºC	56-lead QFN (8 x 8 x 0.85 mm) (Pb-free, tape and reel)	MSL3	260°C

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	VREF2C	Analogue output	Mid reference voltage. This pin must be connected to AGND via a decoupling capacitor.
2	VRLC/VBIAS	Analogue I/O	Reference voltage input/output
3	VREF3C	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.
4	VREF1C	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.
5	SEN	Digital input	Enables the serial interface when high
6	SDO	Digital output	Serial interface data output
7	SCK	Digital input	Serial interface clock
8	SDI	Digital input	Serial interface data input
9	LDO2VDD	Supply	Analogue supply
10	LDO2GND	Supply	Analogue ground
11	LDO2VOUT	Supply	LDO output This pin must be connected to AGND via a decoupling capacitor.
12	DSLCT2	Analogue input	Device select 2
13	MCLK	Analogue input	Master clock
14	DSLCT1	Analogue input	Device select 1
15	D5N/OP[9]	LVDS output	LVDS Data output 5 – Negative / CMOS output 9
16	D5P/OP[8]	LVDS output	LVDS Data output 5 – Positive / CMOS output 8
17	D4N/OP[7]	LVDS output	LVDS Data output 4 – Negative / CMOS output 7
18	D4P/OP[6]	LVDS output	LVDS Data output 4 – Positive / CMOS output 6
19	DCLKN/OC[2]	LVDS output	LVDS Clock Output – Negative/ CMOS flag output
20	DCLKP/OC[1]	LVDS output	LVDS Clock Output – Positive/ CMOS clock output
21	DBGND	Supply	Analogue ground.
22	DBVDD	Supply	Analogue supply.
23	D3N/OP[5]	LVDS output	LVDS Data output 3 – Negative / CMOS output 5
24	D3P/OP[4]	LVDS output	LVDS Data output 3 – Positive / CMOS output 4
25	D2N/OP[3]	LVDS output	LVDS Data output 2 – Negative / CMOS output 3
26	D2P/OP[2]	LVDS output	LVDS Data output 2 – Positive / CMOS output 2
27	D1N/OP[1]	LVDS output	LVDS Data output 1 – Negative / CMOS output 1
28	D1P/OP[0]	LVDS output	LVDS Data output 1 – Positive / CMOS output 0
29	HZCTRL	Digital input	Internal use only. Must be connected to AGND.
30	MON	Analogue output	Clock monitor
31	LDO1VOUT	Supply	LDO output. This pin must be connected to AGND via a decoupling capacitor.
32	LDO1GND	Supply	Analogue ground
33	LDO1VDD	Supply	Analogue supply
34	TGSYNC	Digital I/O	Sensor Timing Sync pulse
35	CLK1	Digital output	Sensor Timing Output 1
36	CLK2	Digital output	Sensor Timing Output 2
37	CLK3	Digital output	Sensor Timing Output 3
38	CLK4	Digital output	Sensor Timing Output 4
39	CLK5	Digital output	Sensor Timing Output 5
40	CLK6	Digital output	Sensor Timing Output 6
41	CLK7	Digital output	Sensor Timing Output 7
42	CLK8	Digital output	Sensor Timing Output 8
43	CLK9	Digital output	Sensor Timing Output 9
44	CLK10	Digital output	Sensor Timing Output 10
45	CLK11	Digital output	Sensor Timing Output 11
46	AGND3	Supply	Analogue ground

PIN	NAME	TYPE	DESCRIPTION
47	NC	Not connect	Not connected internally
48	IN2	Analogue input	Analogue input 2
49	AGND2	Supply	Analogue ground
50	AVDD2	Supply	Analogue supply
51	NC	Not connect	Not connected internally
52	INP4	Analogue input	Analogue input 4
53	NC	Not connect	Not connected internally
54	INP6	Analogue input	Analogue input 6
55	AVDD1	Supply	Analogue supply
56	AGND1	Supply	Analogue ground

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD1-2, LDO1VDD-LDO2VDD, DBVDD	GND - 0.3V	GND + 5V
Analogue grounds: AGND1-3, LDO1GND-LDO2VDD, DBGND	GND - 0.3V	GND + 0.3V
Analogue inputs (IN1-6)	GND - 0.3V	AVDD + 0.3V
Other Analogue pins	GND - 0.3V	AVDD + 0.3V
Digital I/O pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	-40°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND, LDOGND and DBGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	-40		85	°C
Analogue Supply voltage	AVDD1-2 LDO1VDD-LDO2VDD DBVDD	2.97	3.3	3.63	V

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 10-bit ADC, PGA, Offset and CDS functions)						
Conversion rate per channel			5		35	MSPS
Full-scale input voltage (see Note 1)		ADCFS=0, Max Gain		0.12		Vp-p
		ADCFS=0, Min Gain		2.0		Vp-p
		ADCFS=1, Max Gain		0.18		Vp-p
		ADCFS=1, Min Gain		3.0		Vp-p
Input signal voltage range	V_{IN}	SF_INP=0	AGND		AVDD	V
		SF_INP=1	AGND		1.2	V
Input capacitance	C_{IN}	Inputs to AGND		10	12	pF
Full-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Zero-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Differential non-linearity	DNL	10-bit		+/-0.5	+/-1.5	LSB
Integral non-linearity (pk-pk/2)	INL	10-bit		+/-1	+/-4	LSB
Channel to channel gain matching	Min Gain			5		%
	Max Gain			15		%
Output noise		10-bit, Unity Gain (Unused channels grounded)		0.5	2.5	LSB rms
Channel to channel crosstalk		10-bit		+/-0.5		LSB
Channel to channel offset matching		BLC disabled		70	210	mV
Programmable Gain Amplifier						
Total Resolution (Ga + Gd)	G_T			12		bits
Analogue Gain	Ga		0.6 + 0.3 * AGAIN[4:0]			V/V
Max gain, each channel (Ga)	Ga_{MAX}	AGAIN[4:0] = 1F(hex)	8.00	9.9	11.43	V/V
Min gain, each channel (Ga)	Ga_{MIN}	AGAIN[4:0] = 0(hex)	0.44	0.6	0.77	V/V
Digital Gain	Gd		DGAIN[11:0] / 2^{11}			V/V
Max gain, each channel (Gd)	Gd_{MAX}	DGAIN[11:0] = FFF(hex)		2		V/V
Min gain, each channel (Gd)	Gd_{MIN}	DGAIN[11:0] = 400 (hex)		0.5		V/V
Max gain, each channel (Ga + Gd)	G_{TMAX}	AGAIN[4:0] = 1F(hex) DGAIN[11:0] = FFF(hex)		19.8		V/V
Min gain, each channel (Ga + Gd)	G_{TMIN}	AGAIN[4:0] = 0(hex) DGAIN[11:0] = 400 (hex)		0.3		V/V
Analogue to Digital Converter						
Resolution				16		bits
Speed					70	MSPS

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
References						
Upper reference voltage	V_{REF1C}	ADCFS=0		2.05		V
		ADCFS=1		2.25		V
Lower reference voltage	V_{REF3C}	ADCFS=0		1.25		V
		ADCFS=1		1.05		V
Input return bias voltage	V_{REF2C}		1.14	1.2	1.26	V
Diff. Reference voltage (VREF1C-VREF3C)	$V_{REF1C3C}$	ADCFS=0	0.72	0.8	0.88	V
		ADCFS=1	1.00	1.2	1.35	V
Output resistance VREF1C, VREF3C, VREF2C				1		Ω
VRLC/Reset-Level Clamp (RLC)						
VRLC input voltage range (see Note 2)	VRLC	SF_INP=0	0.11		3.0	V
		SF_INP=1	0.11		1.2	
RLC switching impedance				50		Ω
RLC short-circuit current				2		mA
RLC output resistance				2		Ω
RLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				5		bits
RLCDAC step size	$V_{RLCSTEP}$	VRLC_TOP_SEL=0		0.09		V/step
		VRLC_TOP_SEL=1		0.048		
RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=00000		0.2		V
		VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=00000		0.11		V
RLCDAC output voltage at code 1F(hex)	V_{RLCTOP}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=11111		3.0		V
		VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=11111		1.6		V
VRLC DNL				0.5		LSB
VRLC INL				0.5		LSB
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.5	1	LSB
Integral non-linearity	INL			0.5	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex)	-400	-250	-100	mV
		Code FF(hex)	+100	+250	+400	mV
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * AVDD			V
Low level input voltage	V_{IL}				0.2 * AVDD	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Outputs						
High level output voltage	V_{OH}	I_{OH} = 6mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
TG Outputs						
High level output voltage	V_{OHTG}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OLTG}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZTG}	Grounded			1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 * AVDD			V
Applied low level input voltage	V_{IL}				0.2 * AVDD	V
High level output voltage	V_{OH}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
Output Impedance	R_O	I_O = 1mA		22		Ω
High impedance output current	I_{OZ}				1	µA
LVDS Outputs						
Differential load impedance	R_L		90	100	110	Ω
Differential steady-state output voltage magnitude	$\|V_{OD}\|$	LVDS_AMP=011, R_L=100Ω		200		mV
Change in the steady-state differential output voltage magnitude between opposite binary states	$\Delta\|V_{OD}\|$	R_L=100Ω			15	mV
Steady-state common-mode output voltage	V_{OC}(SS)	R_L=100Ω		1.25		V
Peak-to-peak common-mode output	V_{OC}(PP)			20	50	mV
Short-circuit output current	I_{OS}		–6		6	mA
High-impedance state output current	I_{OZ}		–10		10	uA
Supply Currents						
Total supply current – active		SF_INP=0, SF_VRLC=0		230		mA
		SF_INP-1, SF_VRLC=1		250		mA
Total supply current – full power down mode				1.2		mA

Notes:

1. **Full-scale input voltage** denotes the differential input signal amplitude (V_{IN}-VRLC in non-CDS mode, V_{IN}-RESET level in CDS mode) that corresponds to the ADC full-scale input level.
2. **If AVDD < 3.0V, the VRLC input voltage must not exceed AVDD.**

INTERNAL POWER ON RESET CIRCUIT

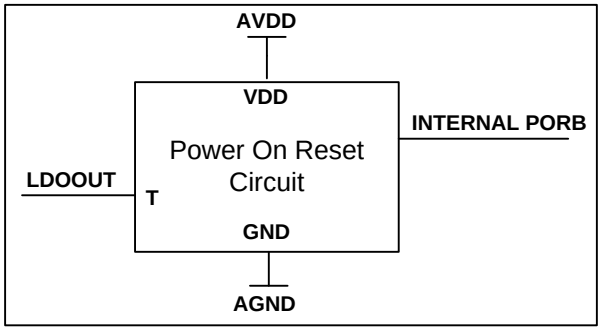


Figure 1 Internal Power On Reset Circuit Schematic

The WM8231 includes an internal Power-On-Reset Circuit, as shown in Figure 1, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors LDOOUT. It asserts PORB low if AVDD or LDOOUT is below a minimum threshold.

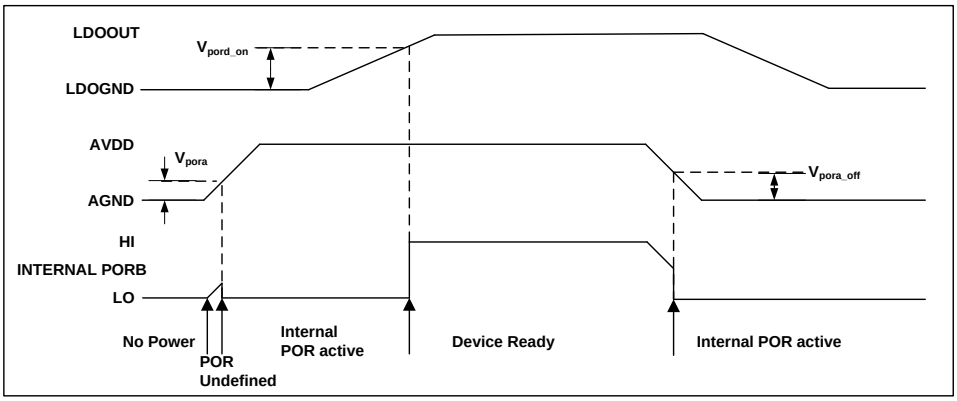


Figure 2 Typical Power up Sequence where AVDD is Powered before LDOOUT

Figure 2 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When LDOOUT rises to Vpord_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

SYMBOL	MIN	TYP	MAX	UNIT
Vpora	0.4	0.6	0.8	V
Vpora_off	0.4	0.6	0.8	V
Vpord_on	0.5	0.7	0.9	V

Table 1 Typical POR Operation (typical values, not tested)

SIGNAL TIMING REQUIREMENTS

SERIAL CONTROL INTERFACE

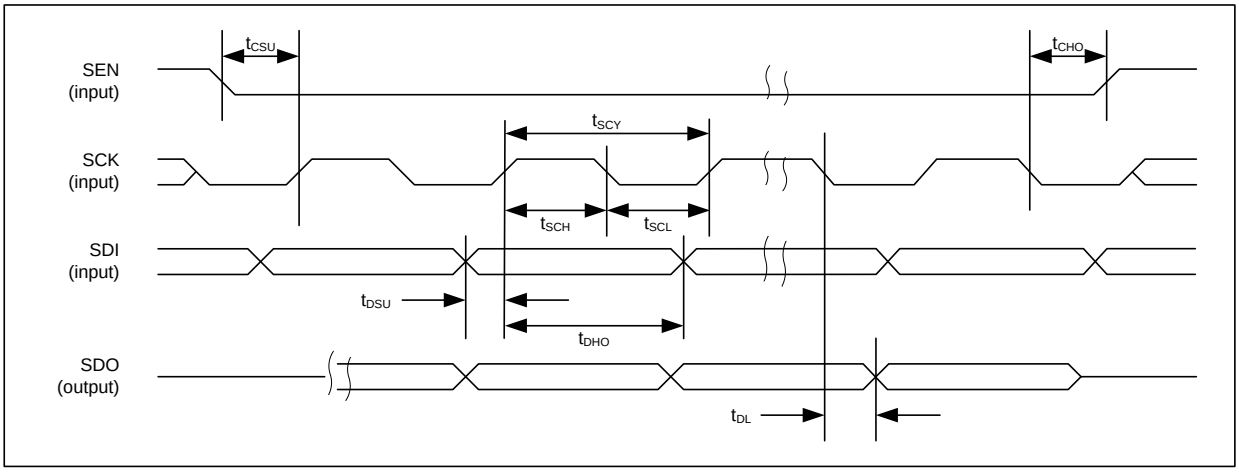


Figure 3 Serial Interface Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SEN falling edge to SCK rising edge	t_{CSU}		20			ns
SCK falling edge to SEN rising edge	t_{CHO}		20			ns
SCK pulse cycle time	t_{SCY}		83.3			ns
SCK pulse width low	t_{SCL}		33			ns
SCK pulse width high	t_{SCH}		33			ns
SDI to SCK set-up time	t_{DSU}		20			ns
SDI to SCK hold time	t_{DHO}		20			ns
SCK falling edge to SDO transition	t_{DL}				33	ns

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin SDO.

It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values.

DEVICE IDENTIFICATION

Up to 4 WM8231 devices can share a common set of serial interface pins. Each device on the common interface bus must be given a different device ID. The device ID is set by the input pin DSLCT2 and DSLCT1 as shown in Table 2.

DSLCT2	DSLCT1	DEVICE ID (ID[1:0])
L	L	00
L	H	01
H	L	10
H	H	11

Table 2 Device Identification

REGISTER WRITE

Figure 4 shows the sequence of operations for performing a register write. Three pins, SCK, SDI and SEN are used for the control interface. A 16-bit address (R/W, CS0, CS1, CS2, A11 to A0) is clocked in through SDI, MSB first, followed by an 8 –bit data word (b7 to b0), also MSB first. Setting address bit R/W to 0 indicates that the operation is a register write. The device ID bits (CS0 and CS1) indicate which device is being written to on a shared control bus. A register write with CS2 set to 1 writes data to all devices on the common bus. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a rising edge on the SEN pin transfers the data to the appropriate internal register.

CS2	CS1 (DSLCT2)	CS0 (DSLCT1)	DESCRIPTION
0	ID[1:0]		Indicated a device to write data
1	X	X	Writes data to all devices

Table 3 Device Identification

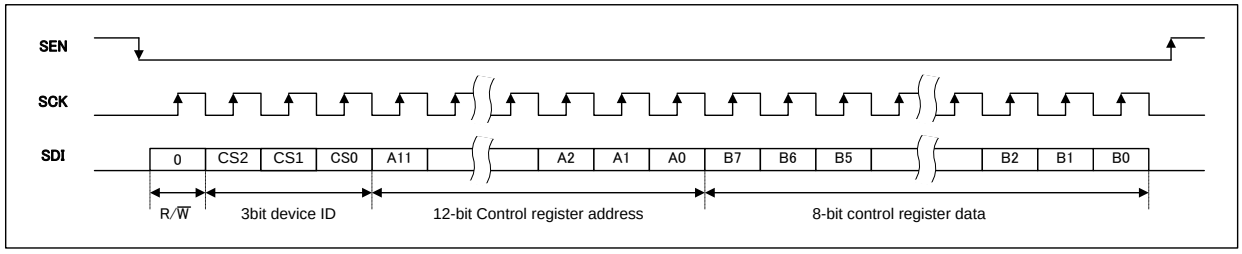


Figure 4 Serial Interface Register Write

REGISTER READ-BACK

Figure 5 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit R/W set to 1, followed by an 8-bit dummy data word. Writing address (A11 to A0) will cause the contents (B7 to B0) of corresponding register in the addressed device to be output MSB first on pin SDO (on the following edge of SCK). In this mode, the CS2 register should be set to 0.

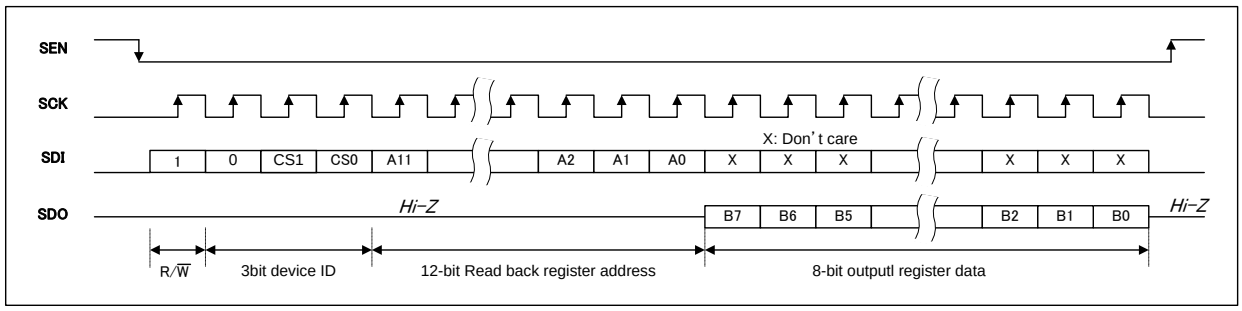


Figure 5 Serial Interface Register Read-back

INPUT VIDEO SAMPLING

NON-CDS (S/H) MODE

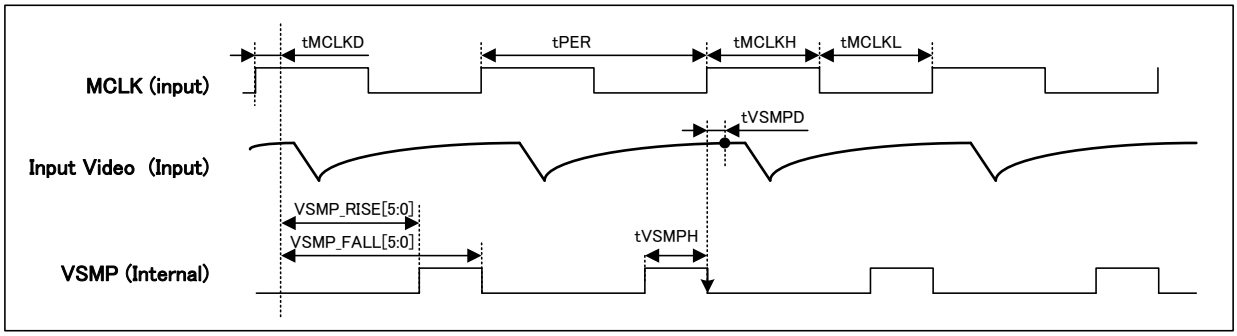


Figure 6 Input Video Timing (Non-CDS (S/H) mode)

CDS MODE

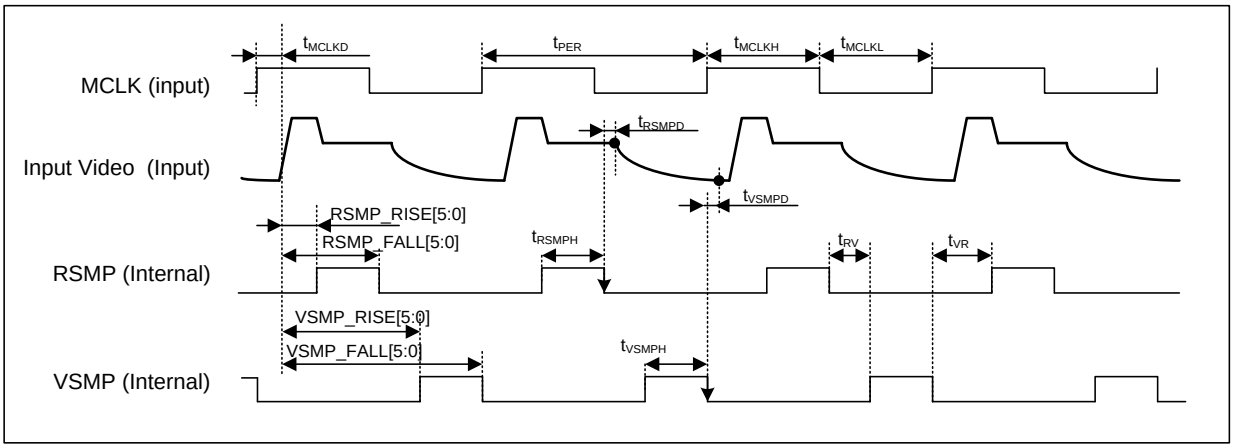


Figure 7 Input Video Timing (CDS mode)

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK cycle period (see note 2)	t_{PER}		28.6		200	ns
MCLK high period (see note 2)	t_{MCLKH}		0.4 * t_{PER}	0.5 * t_{PER}	0.6 * t_{PER}	ns
MCLK low period (see note 2)	t_{MCLKL}		0.4 * t_{PER}	0.5 * t_{PER}	0.6 * t_{PER}	ns
MCLK rising edge to DLL tap 0	t_{MCLKD}			18		ns
Aperture delay (from RSMP falling edge)	t_{RSMPD}			5		ns
Aperture delay (from VSMP falling edge)	t_{VSMPD}			5		ns
RSMP high period	t_{RSMPH}		5			ns
VSMP high period	t_{VSMPH}		5		28 * t_{PER}/60	ns
RSMP falling edge to VSMP rising edge	t_{RV}		0.5			ns
VSMP falling edge to RSMP rising edge	t_{VR}		0.5			ns
Output data latency (from 1st falling edge of VSMP)	LAT	LVDS 10-bit 5pair mode		18		clock
		LVDS 10-bit 3pair mode, CMOS 10-bit output mode		16		clock
		Other output modes		17		clock

Notes:

1. 1clock = t_{PER} (MCLK cycle period)
2. MCLK cycle period and MCLK high/low period are measured at 50% of the respective rising/falling edges

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R130 (82h) RSMP rise	5:0	RSMP_RISE[5:0]	01_1100	RSMP rise edge (0 to 59)
R131 (83h) RSMP fall	5:0	RSMP_FALL[5:0]	10_0110	RSMP fall edge (0 to 59)
R132 (84h) VSMP rise	5:0	VSMP_RISE[5:0]	00_1000	VSMP rise edge (0 to 59)
R133 (85h) VSMP fall	5:0	VSMP_FALL[5:0]	10_1000	VSMP fall edge (0 to 59)

OUTPUT DATA TIMING (CMOS OUTPUT)

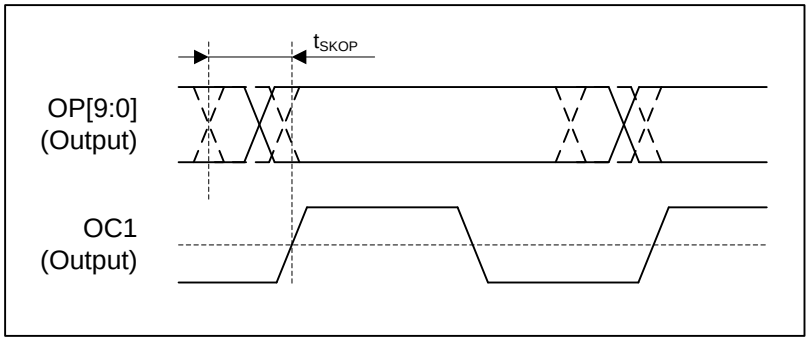


Figure 8 CMOS Output Data Timing

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 30MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data output skew	t_{SKOP}			+/-500		ps

OUTPUT DATA TIMING (LVDS OUTPUT)

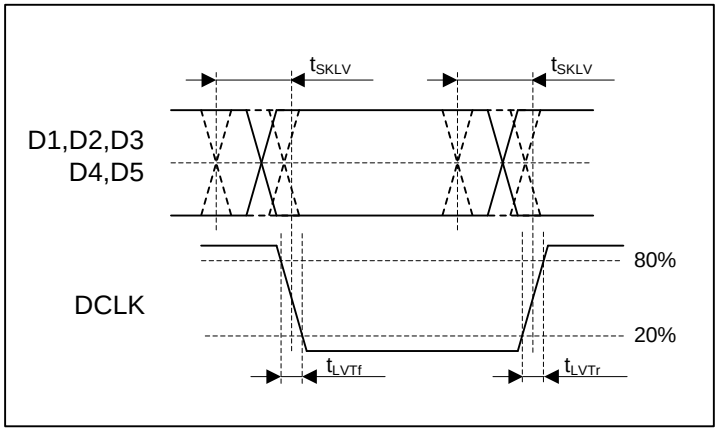


Figure 9 LVDS Output Data Timing

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LVDS output skew	t_{SKLV}			+/-250		ps
LVDS output signal rise time	t_{LVTr}				1	ns
LVDS output signal fall time	t_{LVTf}				1	ns

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on the front page of this datasheet.

The WM8231 samples up to three inputs (IN1, IN2 and IN3) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using between one and six processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 12-bit Programmable Gain Amplifier (PGA).

The ADC then converts each resulting analogue signal to a digital word. The digital output from the ADC is presented in a variety of possible output formats in LVDS and CMOS format.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

The device has an automatic Black-Level Calibration function which allows the D.C. offset determined during the optically-black pixels at the beginning of the linear sensor to be removed during the image-pixels.

The WM8231 also has an Automatic Gain Control function which automatically adjusts the gain to an appropriate level for a detected input level.

The device incorporates a sensor timing generation function which allows CCD and CMOS sensor timing to be controlled directly from the device using internal clock generation and register settings.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8231 lies within the supply voltage range (0V to AVDD), the output signal from a CCD is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8231 side of this capacitor to a suitable voltage through a CMOS switch during the CCD reset period (pixel clamping) or during the black pixels (line clamping). In order for clamping to produce correct results the input voltage during the clamping must be a constant value.

Note that if the A.C. coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the CLPMD register bit. Alternatively, if the input signal contains a stable reference/reset level, then pixel clamping should be used, and the voltage buffers need not be enabled.

The WM8231 allows the user to control the RLC switch in a variety of ways as illustrated in Figure 10. This figure shows a single channel; however, all 3 channels are identical, each with its own clamp switch controlled by the common CLMP signal.

The method of control chosen depends upon the characteristics of the input video. The VRLCEN register bit must be set to 1 to enable clamping; otherwise, the RLC switch cannot be closed (by default VRLCEN=1).

Note that unused inputs should be left floating, or grounded through a decoupling capacitor, if reset level clamping is used.

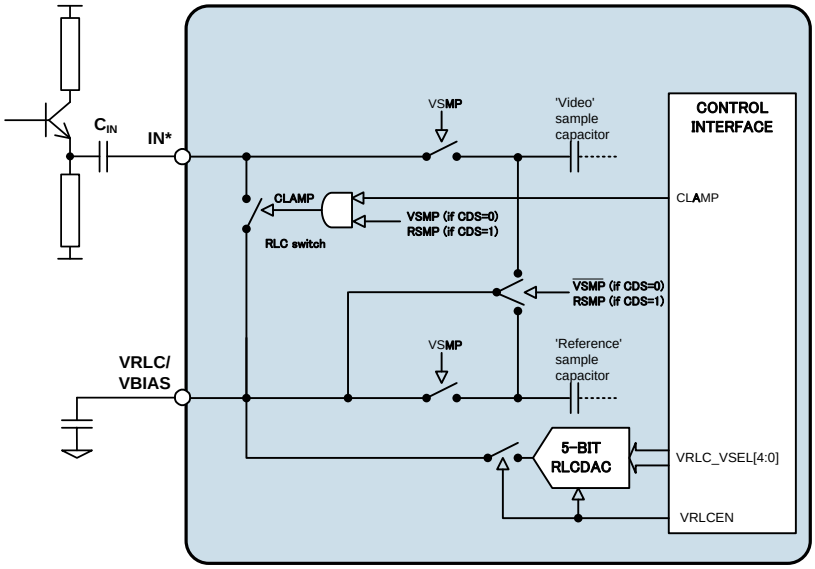


Figure 10 RLC Clamp Control Options

When an input waveform has a stable reference level on every pixel, it may be desirable to clamp every pixel during this period. Setting CLAMP=high means that the RLC switch is closed whenever the RSMP is high, as shown in Figure 11.

In non-CDS operation, setting CLAMP=high means that the RLC switch is closed whenever the VSMP is high, as shown in Figure 12.

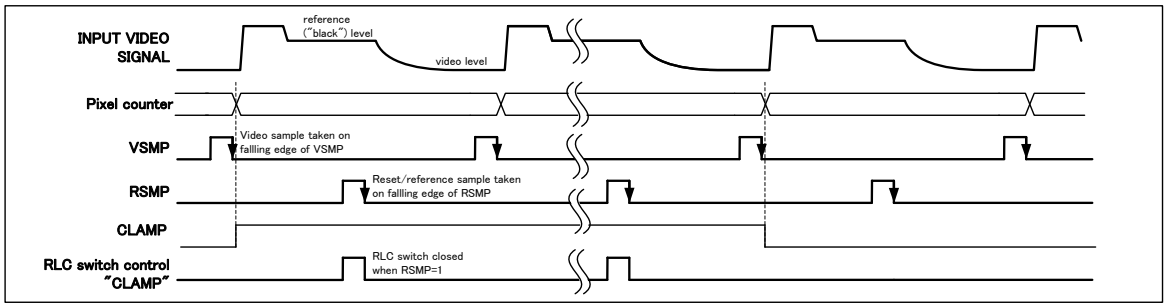


Figure 11 Reset Level Clamp Operation, CDS Operation Shown

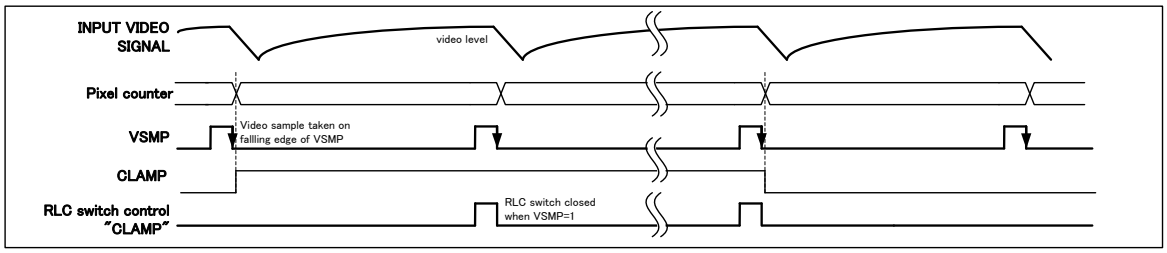


Figure 12 Line Clamp Operation, non-CDS operation shown

CDS/NON-CDS PROCESSING

For CCD type input signals, containing a fixed reference/reset level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing, the input waveform is sampled at two different points in time for each pixel, once during the reference/reset level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default = 0). This causes the signal reference to come from the video reference level as shown in Figure 13.

For input signals that do not contain a reference/reset level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as input samples the video level in this mode. Note that if the A.C. coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the CLPMD register bit. Alternatively, if the input signal contains a stable reference/reset level, then pixel clamping should be used, and the voltage buffers need not be enabled.

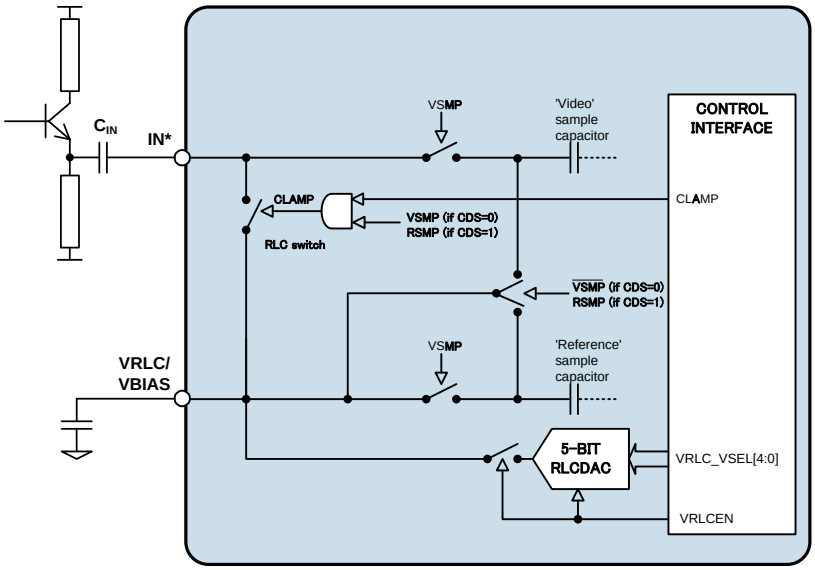


Figure 13 CDS/non-CDS Input Configuration

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 12-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DACINP[7:0] for the Offset DAC, and AGAIN[4:0] and DGAIN[11:0] for the PGA.

The gain characteristic of the WM8231 PGA is shown in Figure 14.

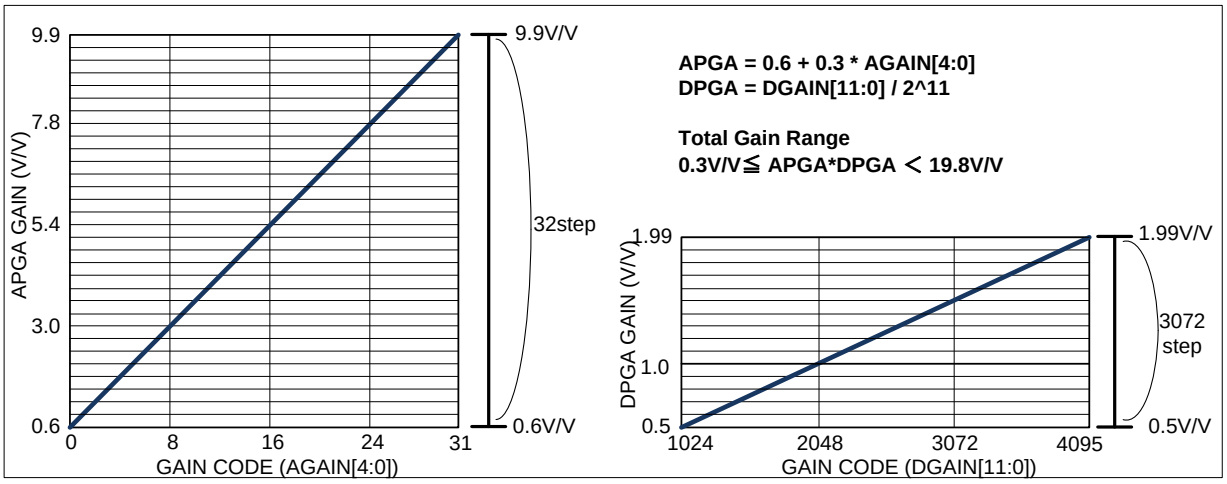


Figure 14 PGA Gain Characteristic

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA can be offset to match the full-scale range of the differential ADC (1.5*[VREF1C-VREF3C]).

For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS=0. For positive going input signals the black level should be offset to the bottom of the ADC range by setting PGAFS=1.

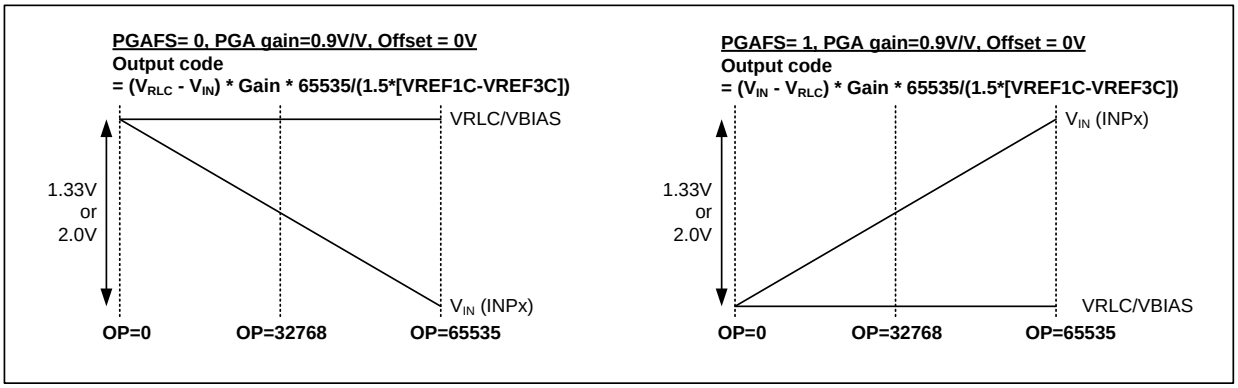


Figure 15 ADC Input Black Level Adjust Settings

OVERALL SIGNAL FLOW SUMMARY

Figure 16 represents the processing of the video signal through the WM8231.

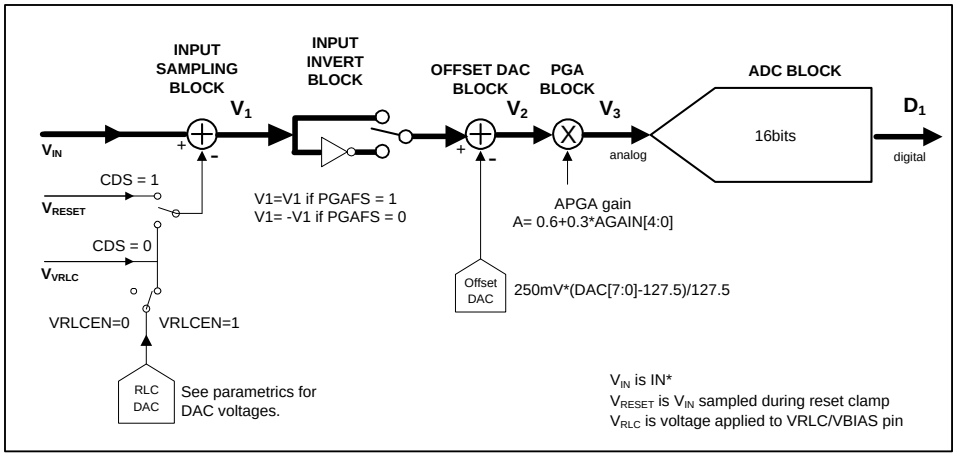


Figure 16 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

ADC PGA BIAS CURRENT CONTROL

The WM8231 can be changed the bias current for PGA and ADC comparator as the following step. It would be effective for high frequency operation.

1. R1C0h=1
2. R1CBh=11h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R448 (1C0h) User access control2	0	User_KEY2	0	0 = User access2 disabled 1 = User access2 enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R459 (1CBh) Comp control	1:0	PT_COMP	01	01 = Standard operation 11 = High performance operation Other = Inhibit.

Notes:

1. To change the Comp control, the USER_KEY2 bit must be set to '1'.
2. If it's not required to change this register, must be set as default.

PLL DLL SETUP

The WM8231 supports a wide range of MCLK input frequencies. The PLL_EXDIV_SEL[2:0], LVDLGAIN[1:0] and DLGAIN[1:0] fields must be configured according to the MCLK frequency and the applicable data-output format – see Table 4. Note the LVDLGAIN field is not used in CMOS mode.

Note that after PLL and DLL configuration, the device must be reset as follows:

- R03[1:0]=11 (PDMD=1, PD=1)
- Delay 1 ms
- R03[1:0]=00 (Normal operation)

Under default conditions, the LDO2 voltage is 1.8V. To select 2.0V output as noted in Table 4, the following control sequence is required:

- R1B0h[0]=1
- R1B4h=12h

Data Format	Max sample rate	MCLK frequency (MHz)	30.1 ~ 35.0	30.0	25.0 ~ 29.9	15.1 ~ 23.3	15.0	12.5 ~ 14.99	10.0 ~ 12.49	8.33 ~ 9.99	7.5 ~ 8.32	5.0 ~ 7.49
CMOS 10-bit	30 MHz	PLL_EXDIV_SEL[2:0]	—	000	000	001	001	001	001	001	010	010
		DLGAIN[1:0]	—	01	01	01	01	10	10	10	10	10
		LDO2 voltage	—	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 10-bit 5-pair	35 MHz	PLL_EXDIV_SEL[2:0]	001	001	001	010	010	010	011	011	011	100
		LVDLGAIN[1:0]	01	01	01	01	01	10	10	10	10	10
		DLGAIN[1:0]	01	01	01	01	01	10	10	10	10	10
		LDO2 voltage	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 16-bit 5-pair LVDS 10-bit 3-pair LVDS 12-bit 4-pair	30 MHz	PLL_EXDIV_SEL[2:0]	—	000	000	001	001	001	001	001	010	010
		LVDLGAIN[1:0]	—	00	01	01	01	01	01	10	10	10
		DLGAIN[1:0]	—	01	01	01	01	10	10	10	10	10
		LDO2 voltage	—	2.0V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 16-bit 3-pair	15 MHz	PLL_EXDIV_SEL[2:0]	—	—	—	—	001	001	001	001	010	010
		LVDLGAIN[1:0]	—	—	—	—	00	01	01	01	01	01
		DLGAIN[1:0]	—	—	—	—	01	10	10	10	10	10
		LDO2 voltage	—	—	—	—	2.0V	1.8V	1.8V	1.8V	1.8V	1.8V

Table 4 PLL and DLL Setting

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (1Ch) PLL divider control 1	6:4	PLL_EXDIV_ SEL[2:0]	001	Select EX DIV ratio. Need to set according to input frequency. See Table 4. 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 to 111 = reserved.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R128 (80h) DLL config 1	5:4	DLGAIN[1:0]	01	gain control of DLL delay line Need to set according to input frequency. See Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R129 (81h) DLL config 2	5:4	LVDLGAIN[1:0]	01	gain control of LVDS DLL delay line Need to set according to input frequency. See Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R432 (1B0h) User access control	0	USER_KEY	0	0 = User access disabled 1 = User access enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R436 (1B4h) LDO2 control	4:0	LDO2 VSEL	1_0000	1_0000 = 1.8V 1_0010 = 2.0V

Notes:

1. To change the LDO2 control, the USER_KEY bit must be set to '1'.
2. If it's not required to change this register, it must be set as default.

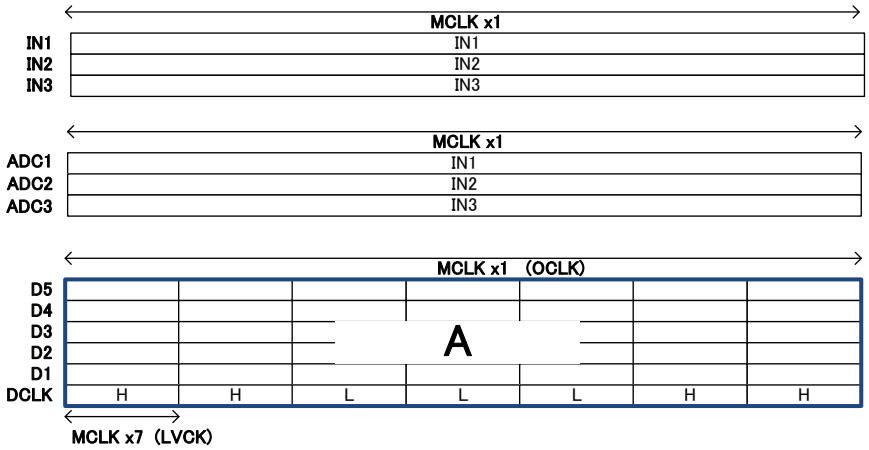
OUTPUT DATA FORMAT

The output from the WM8231 can be presented in several different formats under control of the CMOSMODE and the LVDSMODE register. Depending on the output modes as shown in Table 5.

MODES	DESCRIPTION	OUTPUT DATA RATE	MAXIMUM MCLK RATE
1	LVDS 10-bit 5-pair	MCLK x 7	35 MHz
2	LVDS 16-bit 5-pair	MCLK x 10.5	30 MHz
3	LVDS 10-bit 3-pair	MCLK x 10.5	30 MHz
4	LVDS 16-bit 3-pair	MCLK x 21	15 MHz
5	LVDS 12-bit 4-pair	MCLK x 10.5	30 MHz
6	CMOS 10-bit	MCLK x 3	30 MHz

Table 5 Output Format and Data Rate

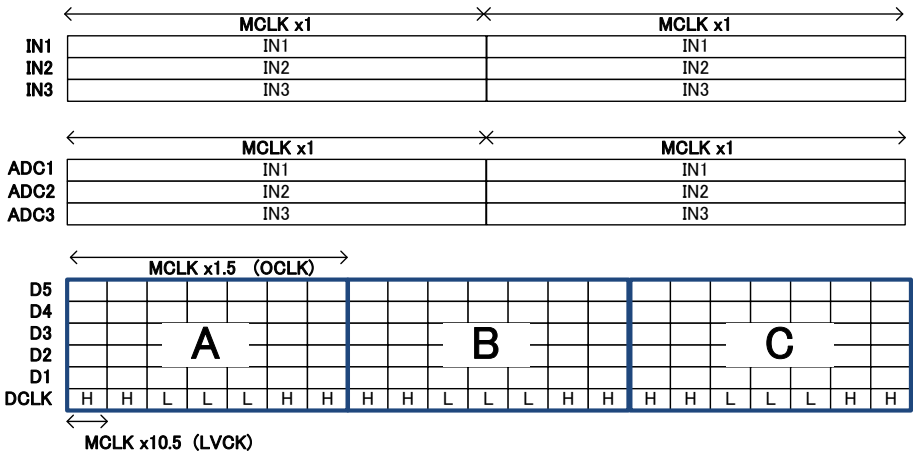
LVDS 10-BIT 5PAIR MODE



A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	S3
D3	S4	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

Table 6 10-bit 5pair LVDS Output Format

LVDS 16-BIT 5PAIR MODE



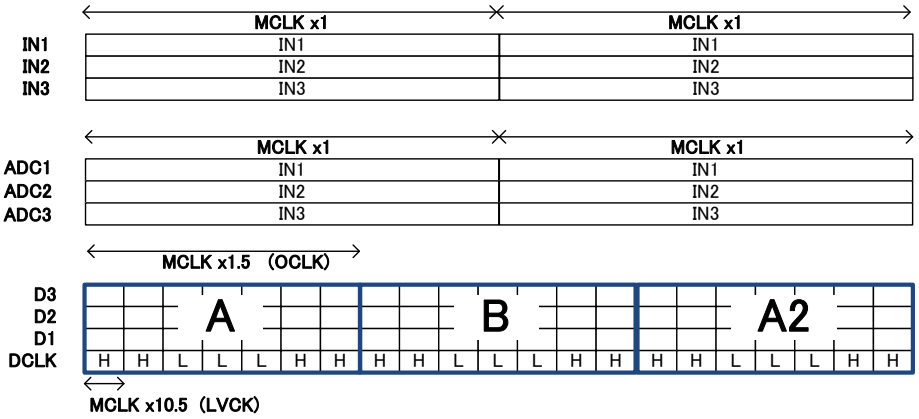
A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]
D3	IN1[11]	IN1[12]	IN1[13]	IN1[14]	IN1[15]	IN2[0]	IN2[1]
D2	IN2[2]	IN2[3]	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]
D1	IN2[9]	IN2[10]	IN211]	IN2[12]	IN2[13]	IN2[14]	IN2[15]
DCLK	H	H	L	L	L	H	H

B							
D5	S0	S1	S2	IN3[0]	IN3[1]	IN3[2]	IN3[3]
D4	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]	IN3[10]
D3	IN3[11]	IN3[12]	IN3[13]	IN3[14]	IN3[15]	IN1[0]	IN1[1]
D2	IN1[2]	IN1[3]	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]
D1	IN1[9]	IN1[10]	IN1[11]	IN1[12]	IN1[13]	IN1[14]	IN1[15]
DCLK	H	H	L	L	L	H	H

C							
D5	S0	S1	S2	IN2[0]	IN2[1]	IN2[2]	IN2[3]
D4	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN2[10]
D3	IN2[11]	IN2[12]	IN2[13]	IN2[14]	IN2[15]	IN3[0]	IN3[1]
D2	IN3[2]	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]
D1	IN3[9]	IN3[10]	IN3[11]	IN3[12]	IN3[13]	IN3[14]	IN3[15]
DCLK	H	H	L	L	L	H	H

Table 7 16-bit 5pair LVDS Output Format

LVDS 10-BIT 3PAIR MODE



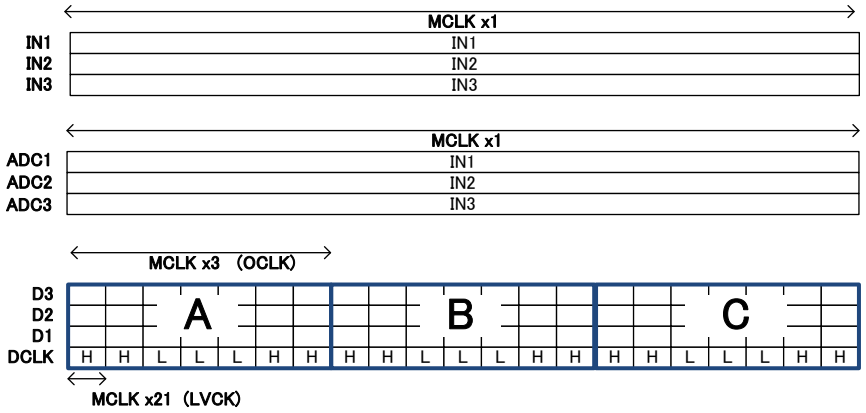
A							
D3	S0	IN1[0]	IN1[1]	IN1[2]	IN1[3]	IN1[4]	IN1[5]
D2	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN2[0]	IN2[1]	IN2[2]
D1	IN2[3]	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]
DCLK	H	H	L	L	L	H	H

B							
D3	S0	IN3[0]	IN3[1]	IN3[2]	IN3[3]	IN3[4]	IN3[5]
D2	IN3[6]	IN3[7]	IN3[8]	IN3[9]	IN1[0]	IN1[1]	IN1[2]
D1	IN1[3]	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]
DCLK	H	H	L	L	L	H	H

A2							
D3	S0	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

Table 8 10-bit 3pair LVDS Output Format

LVDS 16-BIT 3PAIR MODE



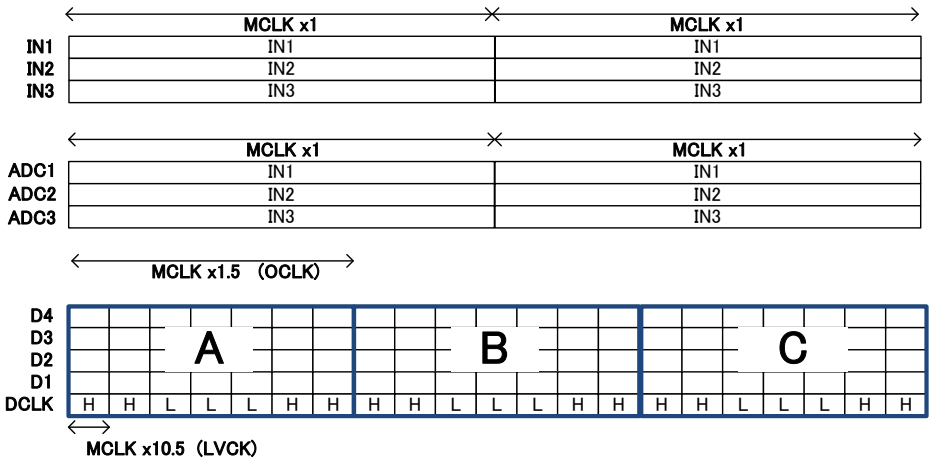
A							
D3	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D2	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]
D1	IN1[11]	IN1[12]	IN1[13]	IN1[14]	IN1[15]	S3	S4
DCLK	H	H	L	L	L	H	H

B							
D3	S0	S1	S2	IN2[0]	IN2[1]	IN2[2]	IN2[3]
D2	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN2[10]
D1	IN2[11]	IN2[12]	IN2[13]	IN2[14]	IN2[15]	S3	S4
DCLK	H	H	L	L	L	H	H

C							
D3	S0	S1	S2	IN3[0]	IN3[1]	IN3[2]	IN3[3]
D2	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]	IN3[10]
D1	IN3[11]	IN3[12]	IN3[13]	IN3[14]	IN3[15]	S3	S4
DCLK	H	H	L	L	L	H	H

Table 9 16-bit 3pair LVDS Output Format

LVDS 12-BIT 4PAIR MODE



A							
D4	S0	IN1[0]	IN1[1]	IN1[2]	IN1[3]	IN1[4]	IN1[5]
D3	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]	IN1[11]	S1
D2	S2	S3	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]
D1	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN2[10]	IN2[11]
DCLK	H	H	L	L	L	H	H

B							
D4	S0	IN3[0]	IN3[1]	IN3[2]	IN3[3]	IN3[4]	IN3[5]
D3	IN3[6]	IN3[7]	IN3[8]	IN3[9]	IN3[10]	IN3[11]	S1
D2	S2	S3	IN1[0]	IN1[1]	IN1[2]	IN1[3]	IN1[4]
D1	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]	IN1[11]
DCLK	H	H	L	L	L	H	H

C							
D4	S0	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D3	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN2[10]	IN2[11]	S1
D2	S2	S3	IN3[0]	IN3[1]	IN3[2]	IN3[3]	IN3[4]
D1	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]	IN3[10]	IN3[11]
DCLK	H	H	L	L	L	H	H

Table 10 12-bit 4pair LVDS Output Format

LVDS SYNCHRONOUS OUTPUT

The LVDS synchronous output function can be used in LVDS 16-bit 5pair mode, 10-bit 3pair mode and 12-bit 4 pair mode. In these LVDS output mode, the output data packet cycle is not same as MCLK clock period, so that the output data at pixel counter = 0 will not be same format when the line length is odd number.

If OUTSYNC = 1, the LVDS output format will be synchronized to pixel counter = 0.

When the line length is even number, the output data at pixel counter = 0 will be always same format, so that the OUTSYNC is invalid. Also, the OUTSYNC is invalid in other LVDS and CMOS format. The following shows detailed information of this mode.

Odd number line length

In odd number line length operation, the output data at pixel counter = 0 will not be same format as shown in Figure 17. When set the OUTSYNC register, the LVDS output format will be synchronized to pixel counter = 0 as shown in Figure 18 below.

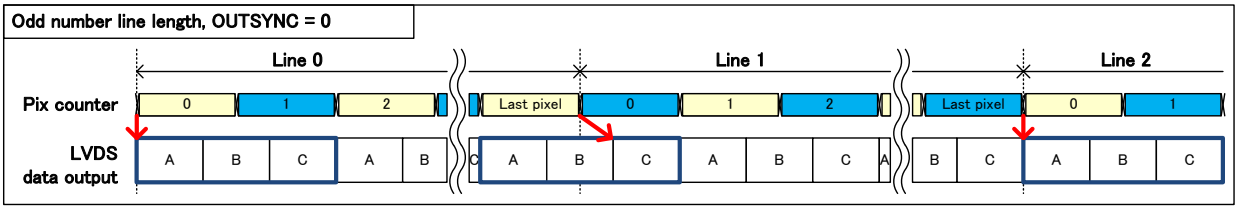


Figure 17 LVDS output data cycle (odd number line length, OUTSYNC=0)

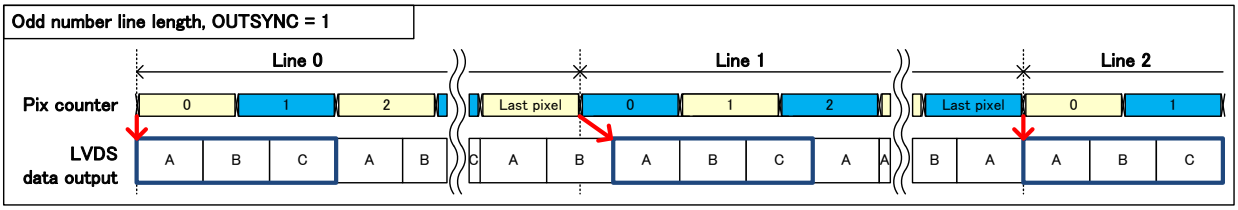


Figure 18 LVDS output data cycle (odd number line length, OUTSYNC=1)

Even number line length

When the line length is even number, the output data at pixel counter = 0 will be always same format, so that the OUTSYNC is invalid.

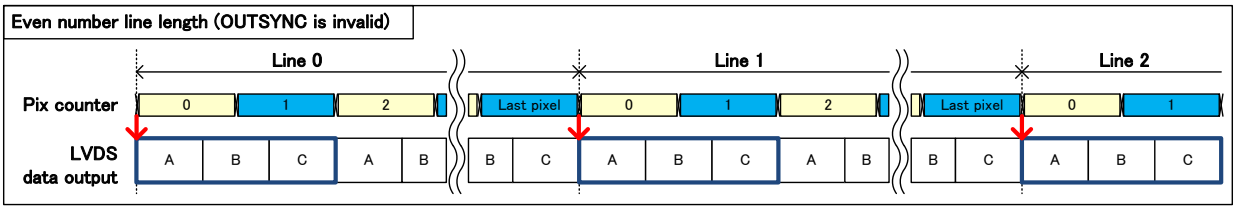


Figure 19 LVDS output data cycle (even number line length)

LVDS DATA OUTPUT ORDER

The WM8231 can be presented 2 types of LVDS data output order, Ascending order mode and Descending order mode as the following.

Ascending Order Mode

10bit 5pair mode

D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	S3
D3	S4	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

16bit 5pair mode

D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]
D3	IN1[11]	IN1[12]	IN1[13]	IN1[14]	IN1[15]	IN2[0]	IN2[1]
D2	IN2[2]	IN2[3]	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]
D1	IN2[9]	IN2[10]	IN211]	IN2[12]	IN2[13]	IN2[14]	IN2[15]
DCLK	H	H	L	L	L	H	H

10bit 3pair mode

D3	S0	IN1[0]	IN1[1]	IN1[2]	IN1[3]	IN1[4]	IN1[5]
D2	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN2[0]	IN2[1]	IN2[2]
D1	IN2[3]	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]
DCLK	H	H	L	L	L	H	H

16bit 3pair mode

D3	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D2	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]
D1	IN111]	IN1[12]	IN1[13]	IN1[14]	IN1[15]	S3	S4
DCLK	H	H	L	L	L	H	H

12bit 4pair mode

D4	S0	IN1[0]	IN1[1]	IN1[2]	IN1[3]	IN1[4]	IN1[5]
D3	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]	IN1[11]	S1
D2	S2	S3	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]
D1	IN2[5]	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN2[10]	IN211]
DCLK	H	H	L	L	L	H	H

Decending Order Mode

10bit 5pair mode

D5	S4	S3	S2	IN1[9]	IN1[8]	IN1[7]	IN1[6]
D4	IN1[5]	IN1[4]	IN1[3]	IN1[2]	IN1[1]	IN1[0]	S1
D3	S0	IN2[9]	IN2[8]	IN2[7]	IN2[6]	IN2[5]	IN2[4]
D2	IN2[3]	IN2[2]	IN2[1]	IN2[0]	IN3[9]	IN3[8]	IN3[7]
D1	IN3[6]	IN3[5]	IN3[4]	IN3[3]	IN3[2]	IN3[1]	IN3[0]
DCLK	H	H	L	L	L	H	H

16bit 5pair mode

D5	S2	S1	S0	IN1[15]	IN1[14]	IN1[13]	IN1[12]
D4	IN1[11]	IN1[10]	IN1[9]	IN1[8]	IN1[7]	IN1[6]	IN1[5]
D3	IN1[4]	IN1[3]	IN1[2]	IN1[1]	IN1[0]	IN2[15]	IN2[14]
D2	IN2[13]	IN2[12]	IN2[11]	IN2[10]	IN2[9]	IN2[8]	IN2[7]
D1	IN2[6]	IN2[5]	IN2[4]	IN2[3]	IN2[2]	IN2[1]	IN2[0]
DCLK	H	H	L	L	L	H	H

10bit 3pair mode

D3	S0	IN1[9]	IN1[8]	IN1[7]	IN1[6]	IN1[5]	IN1[4]
D2	IN1[3]	IN1[2]	IN1[1]	IN1[0]	IN2[9]	IN2[8]	IN2[7]
D1	IN2[6]	IN2[5]	IN2[4]	IN2[3]	IN2[2]	IN2[1]	IN2[0]
DCLK	H	H	L	L	L	H	H

16bit 3pair mode

D3	S4	S3	S2	IN1[15]	IN1[14]	IN1[13]	IN1[12]
D2	IN1[11]	IN1[10]	IN1[9]	IN1[8]	IN1[7]	IN1[6]	IN1[5]
D1	IN1[4]	IN1[3]	IN1[2]	IN1[1]	IN1[0]	S1	S0
DCLK	H	H	L	L	L	H	H

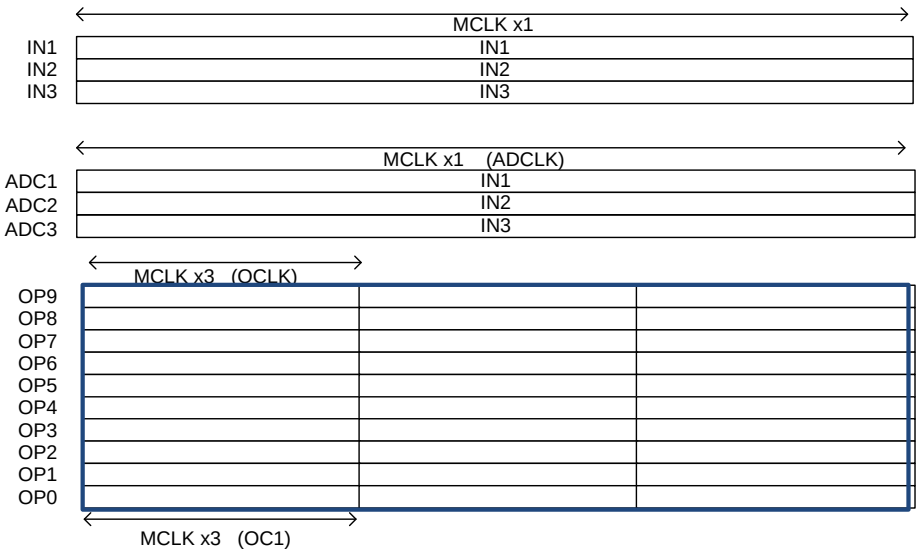
12bit 4pair mode

D4	S3	IN1[11]	IN1[10]	IN1[9]	IN1[8]	IN1[7]	IN1[6]
D3	IN1[5]	IN1[4]	IN1[3]	IN1[2]	IN1[1]	IN1[0]	S2
D2	S1	S0	IN2[11]	IN2[10]	IN2[9]	IN2[8]	IN2[7]
D1	IN2[6]	IN2[5]	IN2[4]	IN2[3]	IN2[2]	IN2[1]	IN2[0]
DCLK	H	H	L	L	L	H	H

Table 11 LVDS DATA OUTPUT ORDER

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) output control	3	LVDSORDER	0	control LVDS data output order 0 = descending order 1 = ascending order

CMOS OUTPUT MODE



A			
OP9	IN1[9]	IN2[9]	IN3[9]
OP8	IN1[8]	IN2[8]	IN3[8]
OP7	IN1[7]	IN2[7]	IN3[7]
OP6	IN1[6]	IN2[6]	IN3[6]
OP5	IN1[5]	IN2[5]	IN3[5]
OP4	IN1[4]	IN2[4]	IN3[4]
OP3	IN1[3]	IN2[3]	IN3[3]
OP2	IN1[2]	IN2[2]	IN3[2]
OP1	IN1[1]	IN2[1]	IN3[1]
OP0	IN1[0]	IN2[0]	IN3[0]

Table 12 10-bit CMOS Output Format

CLOCK TIMING CONFIGURATION

The RSMP signal, VSMP signal and clock output from CLK pin are generated internally by 60 tap DLL circuit. The rising and falling timing of each clock is set by DLL tap setting. The following setting and timing chart shows example configuration for RSMP, VSMP and CLK1.

RSMP: 0x82(RSMP_RISE)=0x07(dec7), 0x83(RSMP_FALL)=0x10(dec16)

VSMP: 0x84(VSMP_RISE)=0x1C(dec28), 0x85(VSMP_FALL=0x29(dec41)

CLK1: 0x87(CLK1_RISE)=0x39(dec57), 0x88(CLK1_FALL)=0x0B(dec11)

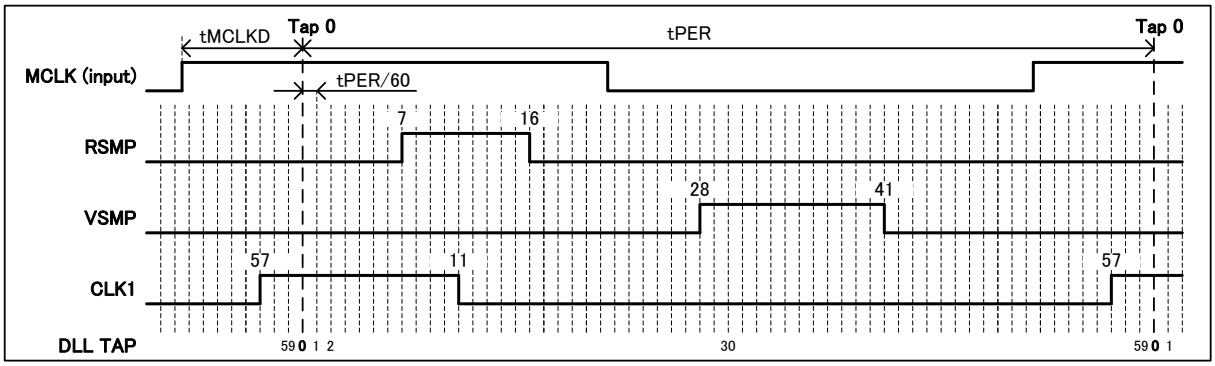
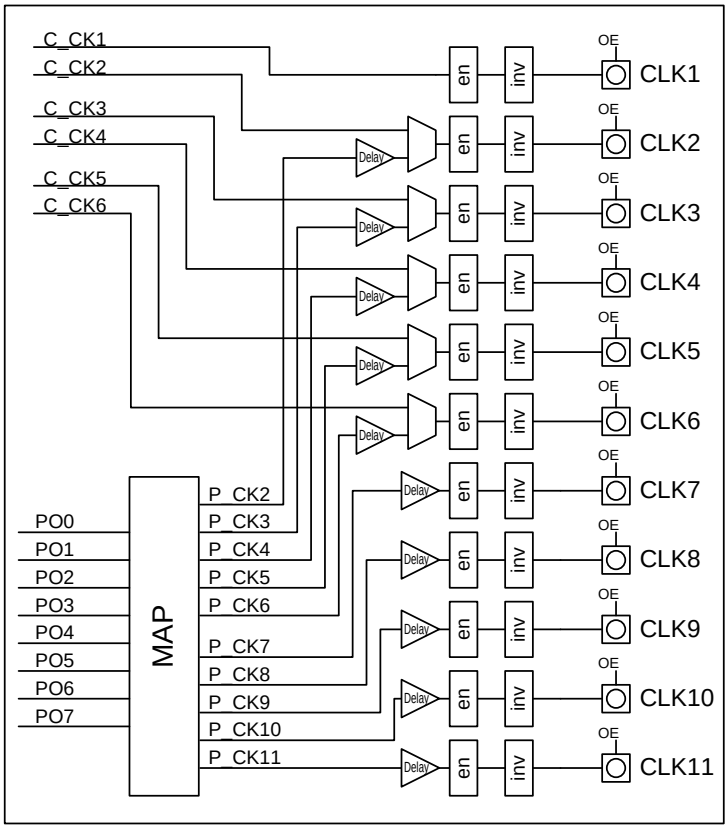


Figure 20 Clock Timing Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R130 (82h) RSMP rise	5:0	RSMP_RISE [5:0]	01_1100	RSMP rise edge
R131 (83h) RSMP fall	5:0	RSMP_FALL [5:0]	10_0110	RSMP fall edge
R132 (84h) VSMP rise	5:0	VSMP_RISE [5:0]	10_1000	VSMP rise edge
R133 (85h) VSMP fall	5:0	VSMP_FALL [5:0]	00_1000	VSMP fall edge
R134 (86h) TGCKO rise	5:0	TCLKO_RISE [5:0]	11_0111	TCLKO rise edge
R135 (87h) CLK1 rise	5:0	CLK1_RISE[5:0]	00_1010	CLK1 rise edge
R136 (88h) CLK1 fall	5:0	CLK1_FALL[5:0]	01_1001	CLK1 fall edge
R137 (89h) CLK2 rise	5:0	CLK2_RISE[5:0]	01_1001	CLK2 rise edge
R138 (8Ah) CLK2fall	5:0	CLK2_FALL[5:0]	10_1000	CLK2 fall edge
R139 (8Bh) CLK3 rise	5:0	CLK3_RISE[5:0]	10_1000	CLK3 rise edge
R140 (8Ch) CLK3 fall	5:0	CLK3_FALL[5:0]	00_1010	CLK3 fall edge
R141 (8Dh) CLK4 rise	5:0	CLK4_RISE[5:0]	00_0000	CLK4 rise edge
R143 (8Fh) CLK5 rise	5:0	CLK5_RISE[5:0]	00_1010	CLK5 rise edge
R144 (90h) CLK5 fall	5:0	CLK5_FALL[5:0]	10_1000	CLK5 fall edge
R145 (91h) CLK6 rise	5:0	CLK6_RISE[5:0]	00_1010	CLK6 rise edge
R146 (92h) CLK6 fall	5:0	CLK6_FALL[5:0]	10_1000	CLK6 fall edge

SENSOR TIMING GENERATION

The WM8231 provides two types of clock internally. C_CK* are high speed clocks, these clocks can set the clock phase by using fine pitch phase control. P_CK* are pixel rate signals which is selected by PO0 to PO7. The WM8231 has eleven sensor TG outputs pins. CLK1 is for clock type use only. CLK2, CLK3, CLK4, CLK5 and CLK6 are selectable high speed type signal or pulse type signal. CLK7, CLK8, CLK9, CLK10 and CLK11 are pulse type use only.



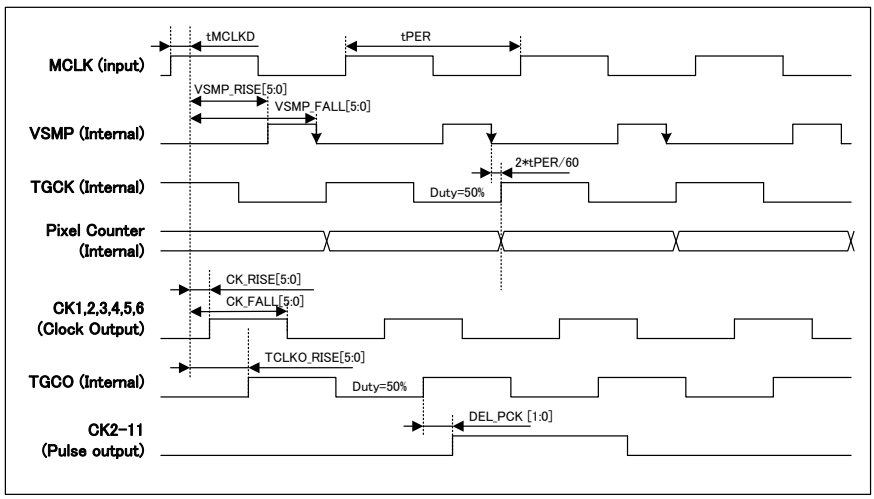


Figure 21 TG Output Timing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R176 (B0h) – R177 (B1h)	5:0	DEL_PCK*[1:0]	00	control delay for pulse output 00 = 0nsec, 01 = 1nsec, 10 = 2nsec, 11 = 3nsec
R135 (81h) – R146 (92h)	5:0	CLK*_RISE[5:0]		CLK* rise edge (0 to 59)
	5:0	CLK*_FALL[5:0]		CLK* fall edge (0 to 59)

TG MASTER MODE OPERATION

In master mode, line length is defined by LLENGTH register.

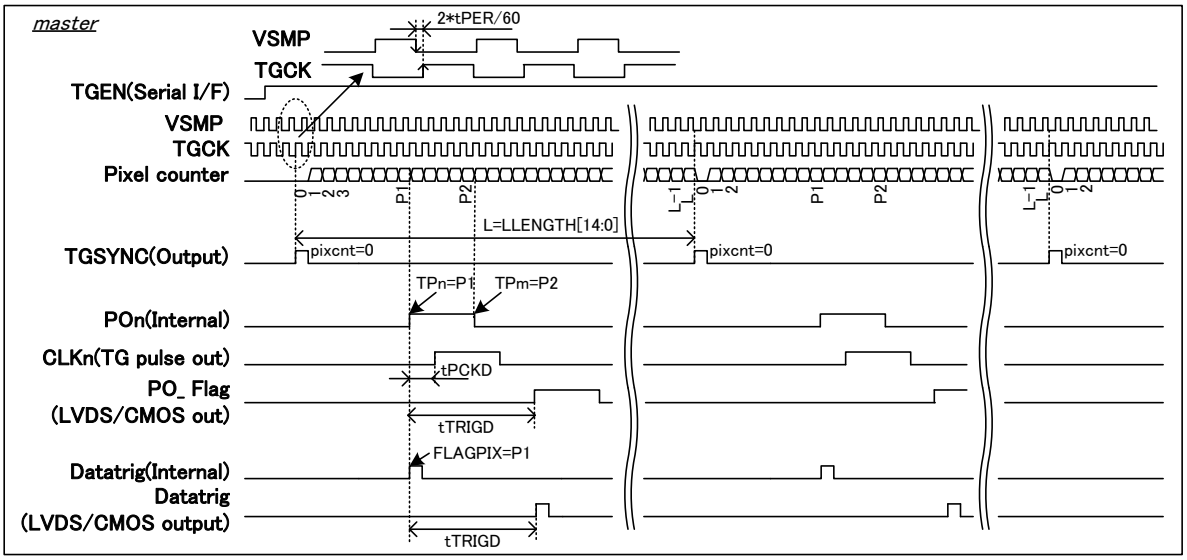


Figure 22 Master Mode Pixel Counter and Line Start Timing

TG SLAVE MODE OPERATION

In slave mode, line length depends on TGSYNC input. The pixel counter is reset by TGSYNC input.

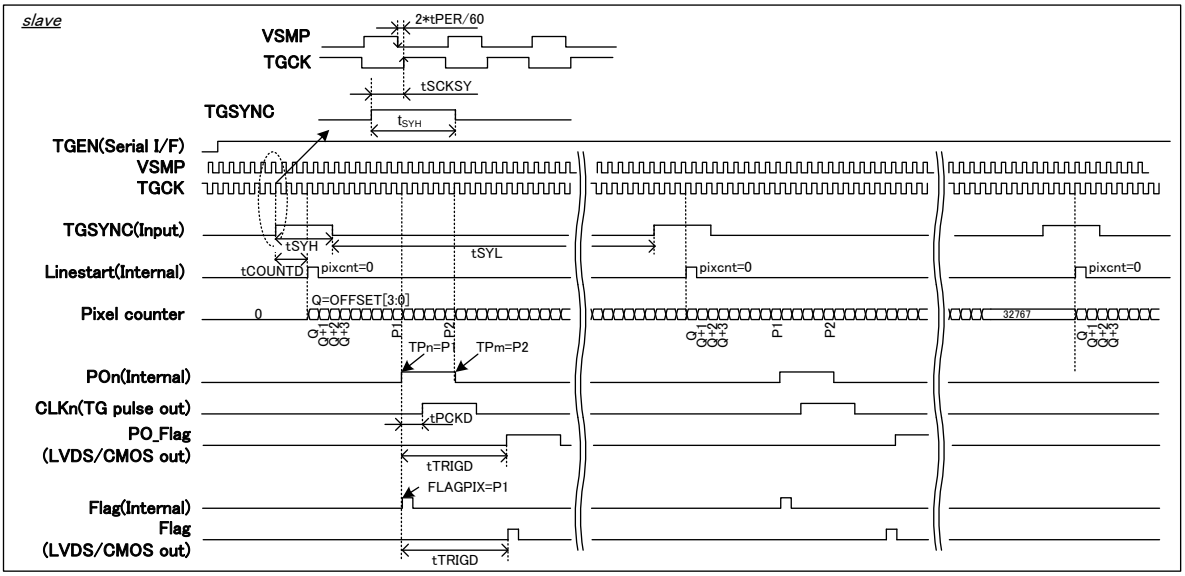


Figure 23 Slave Mode Pixel Counter and Line Start Timing

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TGSYNC Setup time (only for slave mode)	t_{SCKSY}		t_{PER} / 4	t_{PER} / 2	3 * t_{PER} / 4	ns
Pixel counter start timing (only for slave mode)	t_{COUNTD}			2		clock
TGSYNC high period (only for slave mode)	t_{SYH}		1			clock
TGSYNC low period (only for slave mode)	t_{SYL}		1			clock
Data trigger timing delay	t_{TRIGD}	LVDS 10-bit 5pair mode		22		clock
		LVDS 10-bit 3pair mode CMOS 10-bit output mode		20		clock
		Other output mode		21		clock
TG pulse output timing delay	t_{PCKD}			2		clock

Note:

1clock = t_{PER} (MCLK cycle period)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R160 (A0h)	7:4	OFFSET[3:0]	0000	offset count (only for slave mode)
	2	POLSYNC	0	polarity of Sync signal 0 = positive edge, 1 = negative edge
	1	TGMD	0	TG operation mode 0 = slave, 1 = master
	0	TG_EN	0	TG enable 0 = disable, 1 = enable
R161 (A1h)	7:0	LLENGTH[7:0]	0000_0000	the number of pixels in 1line (only for master mode)
R162 (A2h)	6:0	LLENGTH[6:0]	000_0000	the number of pixels in 1line (only for master mode)

TG PULSE AND TRIGGER DATA

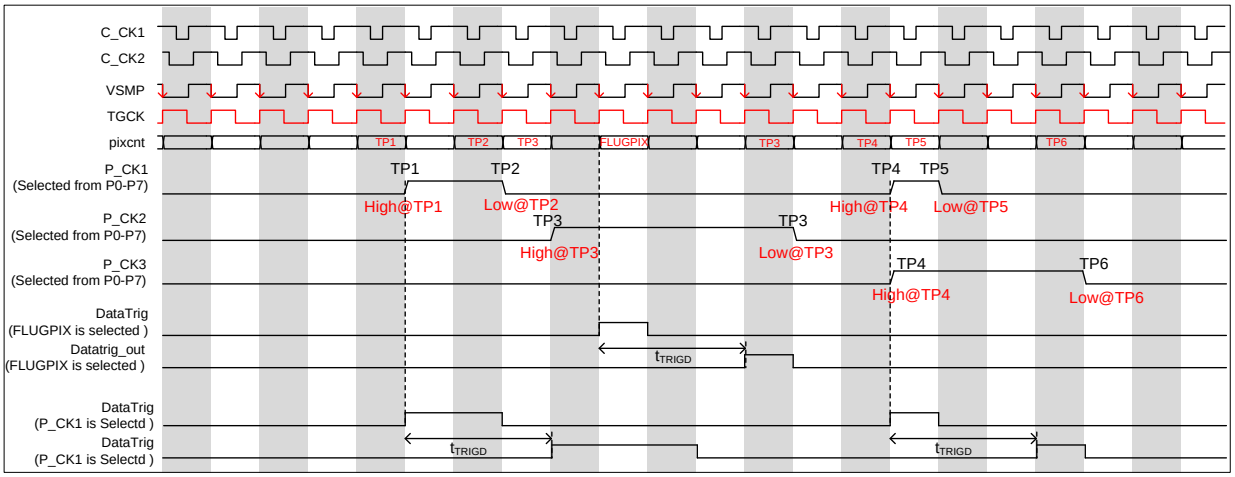


Figure 24 TG Pulse Toggle Setting and Data Trigger Timing

TG PULSE

The WM8231 can generate 8 TG pulses internally (PO0 – PO7). These pulses are generated by the toggle point setting registers (TP*) and polarity setting registers (POL*_PO*). WM8231 provided up to 32 toggle point by using TP0 to TP31. PO0-PO7 signals can be assigned to CLK2-CLK11 by SEL_PCK* and SEL_CLK* register.

TRIGGER DATA

The WM8231 can implement trigger data in LVDS output.(S0,S1,S2,S3 and S4) This can be selected by two methods. One is the FLAGPIX register which can be set one pixel for each line. The other is to apply a PO* pulse. Figure 24 shows the trigger data implementation timing.

CHANNEL ID

Also WM8231 can implement channel identification data instead of trigger data. Table 13 shows the matrix of input channel and channel ID.

	ID[1]	ID[0]
IN1	0	1
IN2	1	0
IN3	1	1

Table 13 Channel ID

Channel ID can be assigned to flag data (S0, S1, S2, S3 or S4). The following is the example of channel ID assignment.

Example: Assigned channel ID to flag data as ID[1]=S2, ID[0]=S3.

If output data is as follows, channel ID will be IN1. (i.e. ID[1]=S2=0, ID[0]=S3=1)

A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]		S3
D3	S4	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

Channel ID Setting Limitation

There are some notices to assign channel ID. It's depending on LVDS output format (refer to OUTPUT DATA FORMAT).

1) 10-bit 5pair mode LVDS output

In this mode, channel ID will be IN1 only.

ID indicate IN1

A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	S3
D3	S4	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

2) 16-bit 5pair mode LVDS output

In this mode, channel ID will be IN1, IN2 and IN3.

A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	IN1[10]
D3	IN1[11]	IN1[12]	IN1[13]	IN1[14]	IN1[15]	IN2[0]	IN2[1]
D2	IN2[2]	IN2[3]	IN2[4]	IN2[5]	IN2[6]	IN2[7]	IN2[8]
D1	IN2[9]	IN2[10]	IN2[11]	IN2[12]	IN2[13]	IN2[14]	IN2[15]
DCLK	H	H	L	L	L	H	H

B							
D5	S0	S1	S2	INP3[0]	INP3[1]	INP3[2]	INP3[3]
D4	INP3[4]	INP3[5]	INP3[6]	INP3[7]	INP3[8]	INP3[9]	INP3[10]
D3	INP3[11]	INP3[12]	INP3[13]	INP3[14]	INP3[15]	INP1[0]	INP1[1]
D2	INP1[2]	INP1[3]	INP1[4]	INP1[5]	INP1[6]	INP1[7]	INP1[8]
D1	INP1[9]	INP1[10]	INP1[11]	INP1[12]	INP1[13]	INP1[14]	INP1[15]
DCLK	H	H	L	L	L	H	H

C							
D5	S0	S1	S2	INP2[0]	INP2[1]	INP2[2]	INP2[3]
D4	INP2[4]	INP2[5]	INP2[6]	INP2[7]	INP2[8]	INP2[9]	INP2[10]
D3	INP2[11]	INP2[12]	INP2[13]	INP2[14]	INP2[15]	INP3[0]	INP3[1]
D2	INP3[2]	INP3[3]	INP3[4]	INP3[5]	INP3[6]	INP3[7]	INP3[8]
D1	INP3[9]	INP3[10]	INP3[11]	INP3[12]	INP3[13]	INP3[14]	INP3[15]
DCLK	H	H	L	L	L	H	H

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R171 (ABh) - R175 (AFh)		SEL_PCK*	000	pulse mapping control for CLK* 000 = PO1, 001 = PO2, 010 = PO3, 011 = PO4 100 = PO5, 101 = PO6, 110 = PO7, 111 = PO8
		SEL_CLK*	0	mapping control 0 = output clock, 1 = output pulse
R208 (D0h) - R270 (10Eh)	7	EN_TP*	0	enable toggle point 0 = disable and subsequent toggle point 1 = enable toggle point
	6:0	TP*		pixel count of toggle point
R271 (10Fh) - R310 (136h)		POL*_PO*		polarity of PO* pulse at TP*
R163 (A3h)	7:0	FLAGPIX[7:0]	0000_0000	flag pixel
R164 (A4h)	6:0	FLAGPIX[6:0]	000_0000	flag pixel
R180 (B4h)	3:0	SEL_FLAG[3:0]	0000	select signal to be output as datatrig 0xxx = flagpix, 1000 = PO0, 1001 = PO1, 1010 = PO2, 1011 = PO3, 1100 = PO4, 1101 = PO5, 1110 = PO6 1111 = PO7
R10 (0Ah)	7:4	FLAG_S1[3:0]	0001	output dataflag as S1 (valid only LVDS mode) 0000 = always low, 0001 = start flag 0010 = reserved, 0011 = reserved, 0100 = reserved 0101 = channel ID[0], 0110 = channel ID[1], 0111 = reserved, 1000 = reserved 1001 = reserved, 1010 = reserved, 1011 = reserved, 1100 = reserved, 1101 = reserved, 1110 = reserved 1111 = always high
	3:0	FLAG_S0[3:0]	0000	output dataflag as S0 (valid only LVDS mode) 0000 = always low, 0001 = start flag 0010 = reserved, 0011 = reserved, 0100 = reserved 0101 = channel ID[0], 0110 = channel ID[1], 0111 = reserved, 1000 = reserved 1001 = reserved, 1010 = reserved, 1011 = reserved, 1100 = reserved, 1101 = reserved, 1110 = reserved 1111 = always high
R11 (0Bh)	7:4	FLAG_S3[3:0]	0001	output dataflag as S3 (valid only LVDS mode) 0000 = always low, 0001 = start flag 0010 = reserved, 0011 = reserved, 0100 = reserved 0101 = channel ID[0], 0110 = channel ID[1], 0111 = reserved, 1000 = reserved 1001 = reserved, 1010 = reserved, 1011 = reserved, 1100 = reserved, 1101 = reserved, 1110 = reserved 1111 = always high
	3:0	FLAG_S2[3:0]	0000	output dataflag as S2 (valid only LVDS mode) 0000 = always low, 0001 = start flag 0010 = reserved, 0011 = reserved, 0100 = reserved 0101 = channel ID[0], 0110 = channel ID[1], 0111 = reserved, 1000 = reserved 1001 = reserved, 1010 = reserved, 1011 = reserved, 1100 = reserved, 1101 = reserved, 1110 = reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				1111 = always high
R12 (0Ch)	3:0	FLAG_S4[3:0]	0000	output dataflag as S4 (valid only LVDS mode) 0000 = always low, 0001 = start flag 0010 = reserved, 0011 = reserved, 0100 = reserved 0101 = channel ID[0], 0110 = channel ID[1], 0111 = reserved, 1000 = reserved 1001 = reserved, 1010 = reserved, 1011 = reserved, 1100 = reserved, 1101 = reserved, 1110 = reserved 1111 = always high

TG MASK TIMING

The WM8231 has a TG clock mask function. M1, M2 and M3 pulses specify the mask period; T1 and T2 pulses are used for changing the signal polarity during the mask period. C_CK1 and C_CK2 are applied to the M pulse only; they cannot be applied to the T pulse. C_CK3 and C_CK4 are applied to M1 and T1; C_CK5 and C_CK6 are applied to M2 and T2. The mask timing is synchronized with TGCKO rise edge.

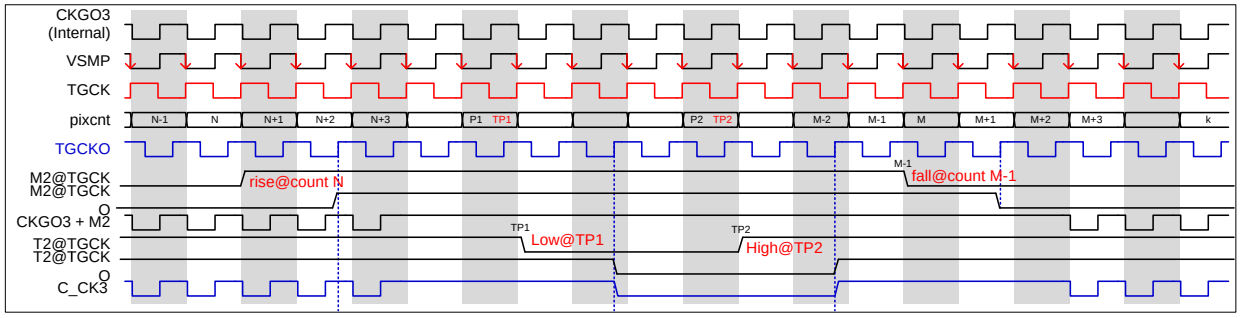


Figure 25 TG Mask Timing

TG CLOCK	APPLIED "M" PULSE	APPLIED "T" PULSE
C_CK1 C_CK2	M3	none
C_CK3 C_CK4	M1	T1
C_CK5 C_CK6	M2	T2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R195 (C3h)	7:0	M1_RISE[7:0]	0000_0000	M1 pulse rise count (mask start)
R196 (C4h)	6:0	M1_RISE[6:0]	000_0000	M1 pulse rise count (mask start)
R197 (C5h)	7:0	M1_FALL[7:0]	0000_0000	M1 pulse fall count (mask end)
R198 (C6h)	6:0	M1_FALL[6:0]	000_0000	M1 pulse fall count (mask end)
R199 (C7h)	7:0	M2_RISE[7:0]	0000_0000	M2 pulse rise count (mask start)
R200 (C8h)	6:0	M2_RISE[6:0]	000_0000	M2 pulse rise count (mask start)
R201 (C9h)	7:0	M2_FALL[7:0]	0000_0000	M2 pulse fall count (mask end)
R202 (CAh)	6:0	M2_FALL[6:0]	000_0000	M2 pulse fall count (mask end)
R203 (CBh)	7:0	M3_RISE[7:0]	0000_0000	M3 pulse rise count (mask start)
R204 (CCh)	6:0	M3_RISE[6:0]	000_0000	M3 pulse rise count (mask start)
R205 (CDh)	7:0	M3_FALL[7:0]	0000_0000	M3 pulse fall count (mask end)
R206 (CEh)	6:0	M3_FALL[6:0]	000_0000	M3 pulse fall count (mask end)
R271 (010Fh) – R278 (116h)	7:0	POL*_T1	1111_1111	polarity of T1 pulse at TP*
	7:0	POL*_T2	1111_1111	polarity of T2 pulse at TP*

TG CYCLE MODE

The TG cycle mode can set a different TG pulse line by line. This mode can only be used in slave mode.

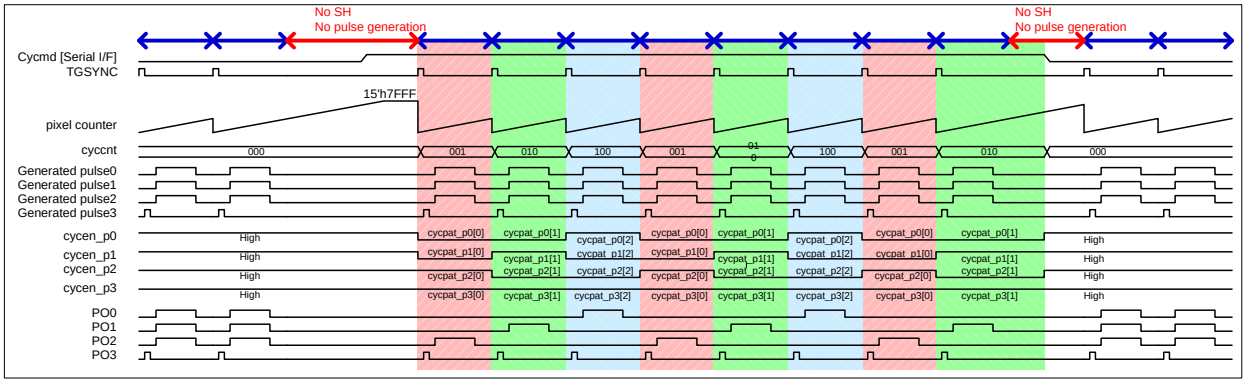


Figure 26 TG Cycle Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R160 (A0h)	3	CYCMD	0	cycle mode enable 0 = normal (same operation at every line) 1 = cycle mode
R181 (B5h) – R184 (B8h)		CYCPAT_PO*[2:0]	000	PO* cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3

TG DIVIDE MODE

Some CCD sensors require TG clocking as half of pixel rate. The WM8231 supports this operation using TG divide mode (TGDIVMD=1). TG divide mode is applied to CLK3,4,5 and 6. CLK1 and 2 are not affected by this mode. To operate TG divide mode correctly, the mask period and reset period must be configured for CLK3,4,5 and 6. Reset period can be set by SEL_PO* and POL*_PO* register setting. Reset period should be set as inside of mask period. During the mask period, signal polarity can be changed by T1 and T2 register settings; Also, output signal polarity can be changed using the INV_CK* bits.

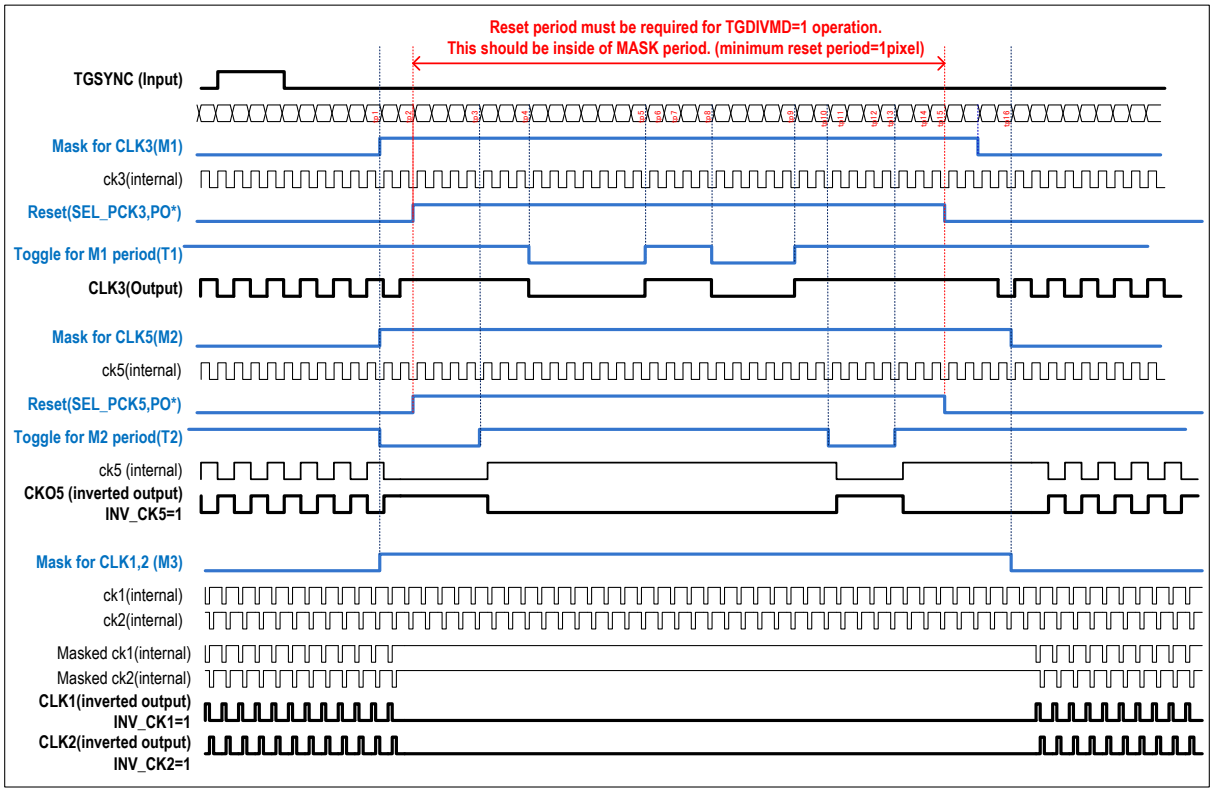


Figure 27 TG Divide Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h)	4	TGDIVMD	0	enable TG clock divide mode 0 = normal (TG clock rate = MCLK clock rate) 1 = enable TG clock divide mode (TG clock rate is half of MCLK clock rate)
R167 (A7h)		INV_CLK*	0	invert signal output assigned to CLK* 0 = non-inverted, 1 = inverted
R169 (A9h)		EN_CLK*	0	enable signal output CLK* 0 = disable, 1 = enable
R171 (ABh) - R175 (AFh)		SEL_PCK*	000	pulse mapping control for CLK* 000 = PO1, 001 = PO2, 010 = PO3, 011 = PO4 100 = PO5, 101 = PO6, 110 = PO7, 111 = PO8
		SEL_CLK*	0	mapping control 0 = output clock, 1 = output pulse
R195 (C3h)	7:0	M1_RISE[7:0]	0000_0000	M1 pulse rise count (mask start)
R196 (C4h)	6:0	M1_RISE[6:0]	000_0000	M1 pulse rise count (mask start)
R197 (C5h)	7:0	M1_FALL[7:0]	0000_0000	M1 pulse fall count (mask end)
R198 (C6h)	6:0	M1_FALL[6:0]	000_0000	M1 pulse fall count (mask end)
R199 (C7h)	7:0	M2_RISE[7:0]	0000_0000	M2 pulse rise count (mask start)
R200 (C8h)	6:0	M2_RISE[6:0]	000_0000	M2 pulse rise count (mask start)
R201 (C9h)	7:0	M2_FALL[7:0]	0000_0000	M2 pulse fall count (mask end)
R202 (CAh)	6:0	M2_FALL[6:0]	000_0000	M2 pulse fall count (mask end)
R203 (CBh)	7:0	M3_RISE[7:0]	0000_0000	M3 pulse rise count (mask start)
R204 (CCh)	6:0	M3_RISE[6:0]	000_0000	M3 pulse rise count (mask start)
R205 (CDh)	7:0	M3_FALL[7:0]	0000_0000	M3 pulse fall count (mask end)
R206 (CEh)	6:0	M3_FALL[6:0]	000_0000	M3 pulse fall count (mask end)
R208 (D0h) - R270 (10Eh)	7	EN_TP*	0	enable toggle point 0 = disable and subsequent toggle point 1 = enable toggle point
	6:0	TP*		pixel count of toggle point
R271 (10Fh) - R278 (116h)		POL*_T1	1111_1111	polarity of T* pulse at TP*
R279 (117h) – R310 (136h)		POL*_PO*	0000_0000	polarity of TPO* pulse at TP*

PROGRAMMABLE AUTOMATIC BLACK LEVEL CALIBRATION (BLC)

The Programmable Automatic Black-Level Calibration (BLC) function is to adjust the D.C. offset of the output data such that the digital output code for black pixels is calibrated to a target black level value. The D.C. offset is determined during the optically-black pixels at the beginning of the linear sensor and removed during the image-pixels as shown in Figure 28.

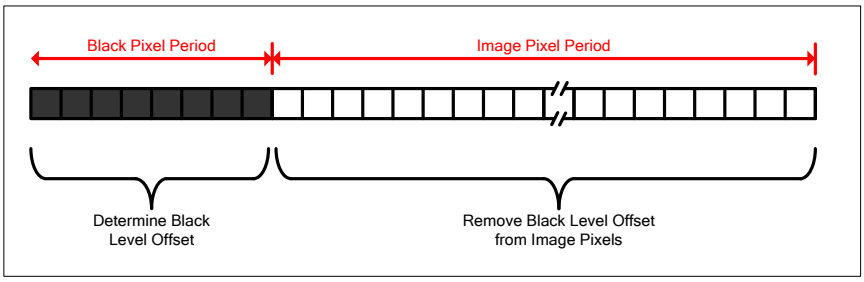


Figure 28 Linear Sensor Model

The automatic black level calibration operates assuming 12 bits ADC resolution. Adjustments to calculations must be made for different ADC resolutions.

The black level calibration process occurs in two stages as shown in Figure 29 below:

- **Coarse Adjust Calibration -** This is a mixed signal loop which removes the coarse offset by adjusting the offset DAC.
- **Fine Adjust Calibration -** This is a digital loop which removes the remaining offset with better noise tolerance, utilising ADC over-range to improve the dynamic range of the system.

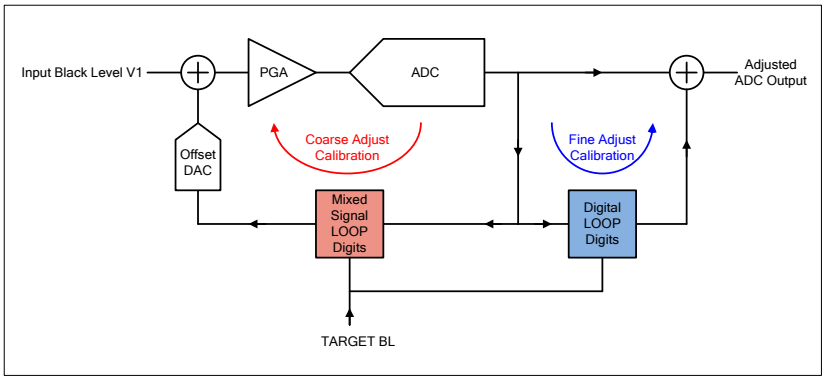


Figure 29 BLC Top-Level Circuitry

TARGET CODES

The user must specify a target black level for each channel through the registers TARGETINP*. If, during the black-pixel period, the average ADC output code was, for example, 100 and the user specified the target black level code to be 10, the BLC circuitry would determine 90 codes should be subtracted from the ADC output. These 90 codes will then be subtracted from every image-pixel code output from the ADC.

Note – changing the PGA gain affects the black-level through the device; the gain should therefore not be changed during a BLC procedure. If the PGA gain changes, then the BLC routine should be re-run.

The automatic black level calibration feature operates with the assumption of a 12-bit ADC resolution. The register settings for Target Codes (TARGETINP*) should be set differently depending on the ADC

resolution being used. As TARGETINP* is an 8 bit register, the 4 MSBs of a data output code cannot be changed.

16-bit ADC Resolution

For 16bit resolution the target code entered into TARGETINP* will ignore the 4 MSBs and 4 LSBs of the 16-bit data output. For example if the desired code out is 0000111111110001, the value entered into TARGETINP* would be 11111111.

10-bit ADC Resolution

For 10bit resolution the 4 MSBs of the 10bit data output code will be ignored. The 2 LSBs of the target code should be set to '00'. For example if the desired code out is 0000111111, the value entered into TARGETINP* would be 11111100.

BLC SCENARIOS OF OPERATION

The BLC can be used in various ways to suit the application, for example calibration can be done once per page or once per line. Three potential scenarios of operation are suggested below.

Note: The registers FRAME_START and SEQ_START when set high by the user will automatically be set low by the device.

SCENARIO 1

In this scenario, Coarse Adjust Calibration is enabled for the 1st line; Fine Adjust Calibration is enabled for every line, with the Fine Adjust Calibration result recalculated every line. This scenario is suitable for dealing with large amounts of D.C. drift throughout a frame; but this is at a cost of potential line-by-line variation in the Fine Adjust result (dependent on sensor noise and the PGA gain). Table 14 shows which registers are required for this scenario with example settings.

SETUP REGISTER	BPIX_AVAIL	CADUR	FRAME_START	FA_EVERYLINE
Value	50	2	1	1

Table 14 Example Register Settings for Scenario 1

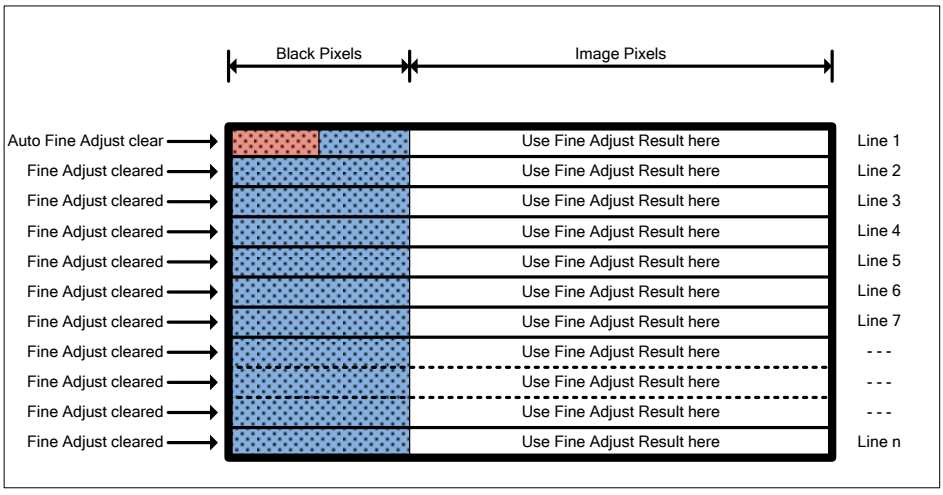


Figure 30 Scenario 1

SCENARIO 2

In this scenario, Coarse Adjust and Fine Adjust Calibration is enabled for the 1st line, with the Fine Adjust result updated on the 1st line only. This scenario is suitable for adjusting for black-level D.C. drift on a frame-by-frame basis; there will be no line-by-line variation in the black-level from the BLC circuitry. Table 15 shows which registers are required for this scenario with example settings.

SETUP REGISTER	BPIX_AVAIL	CADUR	FRAME_START
Value	50	2	1

Table 15 Example Register Settings for Scenario 2

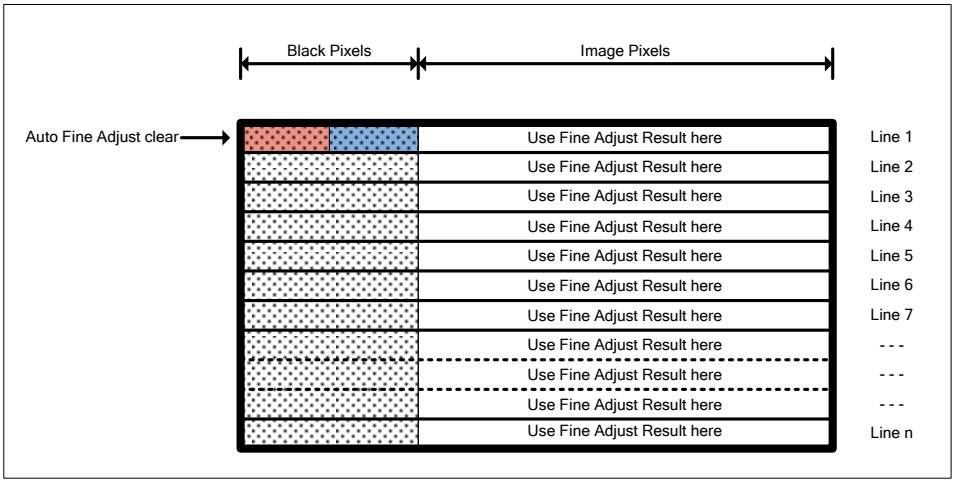


Figure 31 Scenario 2

SCENARIO 3

In this scenario, Coarse Adjust Calibration is enabled for the 1st line; Fine Adjust Calibration is enabled for every line, with the Fine Adjust result accumulated throughout frame and used every line. This scenario allows any variation in the black-level to be tracked throughout the frame by accumulating the Fine Adjust result over multiple lines. This method does not deal with as large amounts of D.C. drift throughout the frame as scenario 1, but it will produce less line-by-line variation. Table 16 shows which registers are required for this scenario with example settings.

SETUP REGISTER	BPIX_AVAIL	CADUR	FRAME_START	FA_EVERYLINE	FA_ACCUM
Value	50	2	1	1	1

Table 16 Example Register Settings for Scenario 3

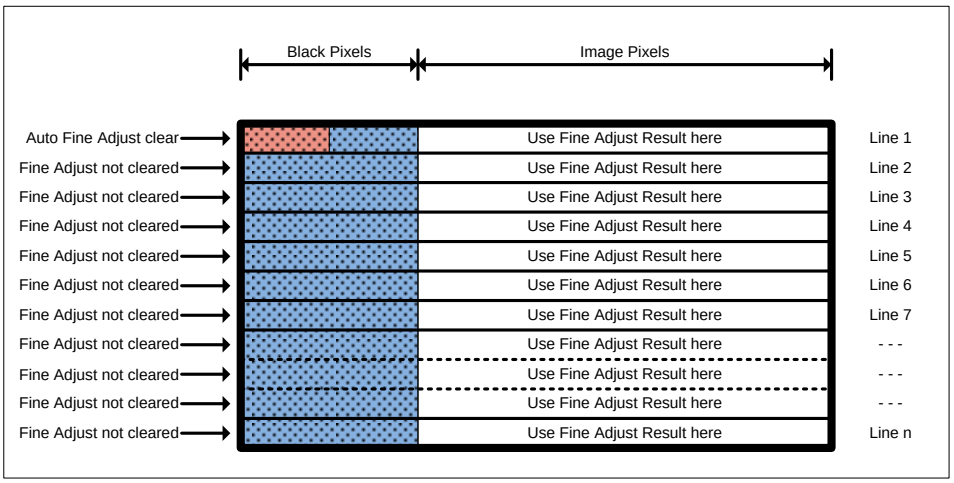


Figure 32 Scenario 3

AUTOMATIC GAIN CONTROL (AGC)

The Automatic Gain Control (AGC) function is to adjust the gain to an appropriate level for a range of input signal levels. The AGC function is enabled by AGC_EN register set to 1. The gain control process has three stages as shown in Figure 33 below:

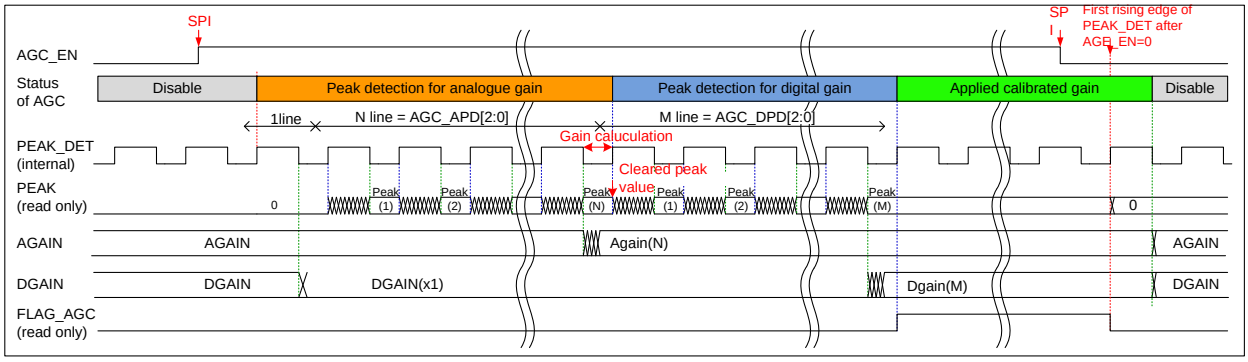


Figure 33 Automatic Gain Control

Analogue Gain Calibration

The analogue gain is kept to the previous setting for (AGAIN), and the digital gain is set to x1 (DGAIN=12'd2048) automatically. During the PEAK_DET=high period, peak detection is executed and then calculates an appropriate analogue gain (Again(N)) while PEAK_DET=low period. This period requires at least 200 pixels. The number of peak detection cycle is selectable by the AGC_APD register. The minimum cycle is 0 (In this case the analogue gain calibration is not executed), and the maximum cycle is 7 lines. The peak value is cleared when the analogue peak detection finished.

Digital Gain Calibration

The analogue gain is set to the calibrated value (Again(N)), and the digital gain is set to x1 (DGAIN=12'd2048) automatically. The peak detection and digital gain calibration functions are then executed. The number of peak detection lines is selectable by the AGC_DPD register. The minimum cycle is 0 (In this case the digital gain calibration is not executed), and the maximum cycle is 7 lines.

Applied Calibrated Analogue and Digital Gain

The analogue and digital gain are holding calibrated value until AGC_EN register set to 0.

Again(N) = AGC_TARGETINP* / peak(n) x AGAIN

Dgain(M) = (AGC_TARGETINP* – TARGETINP*) / (peak(M) – TARGETINP*)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R74 (4Ah)	7:0	TARGETIN1[7:0]	0000_0000	target black level for IN1[7:0]
R77 (4Dh)	7:0	TARGETIN2[7:0]	0000_0000	target black level for IN2[7:0]
R80 (50h)	7:0	TARGETIN3[7:0]	0000_0000	target black level for IN3[7:0]
R87 (57h)	7:4	AGCAVE[3:0]	0000	averaging factor before peak detection 0000 = no average, 0001 = 2, 0010 = 4, 0011 = 8 …, 1010 = 1024 (1011 = 1100 = 1101 = 1110 = 1111 = reserved)
	2	AGC_ERRFLAG	0	AGC error flag 0 = no error detected, 1 = AGC finish with error
	1	AGC_ENDFLAG	0	AGC end flag 0 = not end or not run, 1 = AGC sequence was done
	0	AGC_EN	0	AGC enable 0 = disable, 1 = enable
R88 (58h)	6:4	AGC_DPD[2:0]	000	the number of peak detection iterations to calculate digital gain
	2:0	AGC_APD[2:0]	000	the number of peak detection iterations to calculate analogue gain
R93 (5Dh)	7:0	AGC_TARGETIN1 [7:0]	0000_0000	LSB of AGC target level for IN1
R94 (5Eh)	1:0	AGC_TARGETIN1 [9:8]	00	MSB of AGC target level for IN1
R99 (63h)	7:0	AGC_TARGETIN2 [7:0]	0000_0000	LSB of AGC target level for IN2
R100 (64h)	1:0	AGC_TARGETIN2 [9:8]	00	MSB of AGC target level for IN2
R105 (69h)	7:0	AGC_TARGETIN3 [7:0]	0000_0000	LSB of AGC target level for IN3
R106 (6Ah)	1:0	AGC_TARGETIN3 [9:8]	00	MSB of AGC target level for IN3
R191 (BFh)	7:0	PEAKDET_RISE [7:0]	0000_0000	LSB of PEAKDET_RISE[14:0] peak detection start pixel count
R192 (C0h)	6:0	PEAKDET_RISE [14:8]	000_0000	MSB of PEAKDET_RISE[14:0] peak detection start pixel count
R193 (C1h)	7:0	PEAKDET_FALL [7:0]	0000_0000	LSB of PEAKDET_FALL[14:0] peak detection start pixel count
R194 (C2h)	6:0	PEAKDET_FALL [14:8]	000_0000	MSB of PEAKDET_FALL[14:0] peak detection start pixel count

LINE-BY-LINE OPERATION

Certain linear sensors give colour output on a line-by-line basis. i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels.

The WM8231 can accommodate this type of input by setting the LINEBYLINE register bit high. The offset and gain values that are applied to every input channel can be selected, by internal multiplexers, to come from IN1, IN2 or IN3 offset and gain registers. This allows the gain and offset values for each of the input colours to be setup individually at the start of a scan.

When register bit ACYC=0 the gain and offset multiplexers are controlled via the INTM[1:0] register bits. When INTM=00 the IN1 offset and gain control registers are used to control every input channel, INTM=01 selects the IN2 offset and gain registers and INTM=10 selects the IN3 offset and gain registers to control every input channel.

When register bit ACYC=1, 'auto-cycling' is enabled, and the input channel switches to the next offset and gain registers in the sequence by TGSYNC. The sequence is IN1 → IN2 → IN3 → IN1… offset and gain registers applied to every input channel.

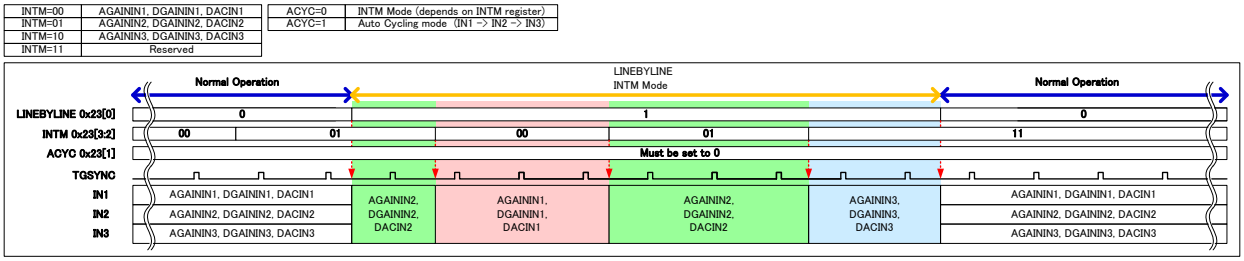


Figure 34 Line-by-Line Operation (ACYC=0, INTM mode)

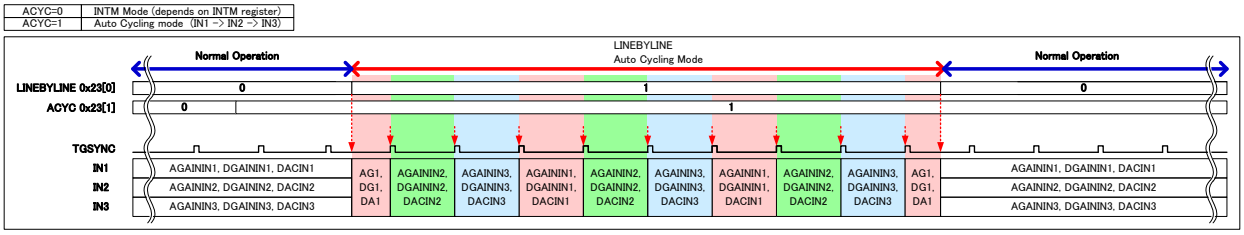


Figure 35 Line-by-Line Operation (ACYC=1, Auto-cycling mode)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) Cycle mode control	3:2	INTM[1:0]	00	When LINEBYLINE=1, controls the GAIN and DAC mux selector when ACYC=0 00 = IN1 01 = IN2 10 = IN3 11 = reserved
	1	ACYC	0	when LINEBYLINE=1, determines the function of the MUX control 0 = decided by INTM register 1= auto-cycling enabled
	0	LINEBYLINE	0	select line by line operation 0=normal operation 1=Line by Line operation

TEST PATTERN GENERATOR

WM8231 has test pattern generator which can be used for interface verification between AFE data output and back-end devices without sensor signal input. This function can be presented in several different patterns by PGPAT[1:0] and PGMARCH registers as shown below. The PGLEVEL, PGWIDTH1 and PGWIDTH2 are the parameter to define the pattern level and width. The PGLEVEL register has 16bit length, PGWIDTH1 and PGWIDTH2 has 8bit length.

Note that test pattern generator is required TGSYNC input. (i.e. this can be used under TG slave mode operation only.)

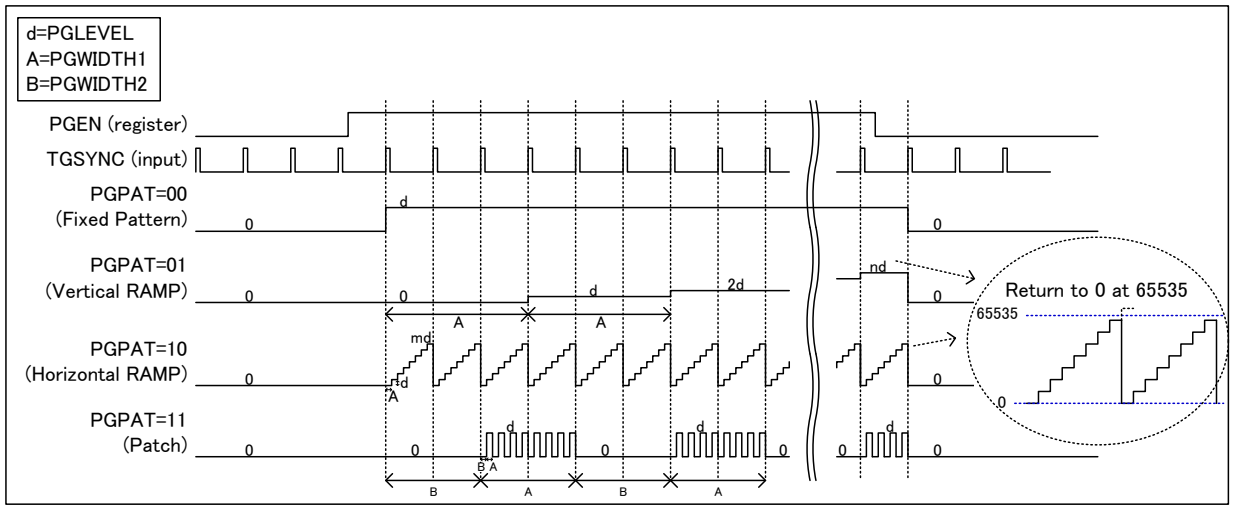


Figure 36 Test Pattern Output Data Formats

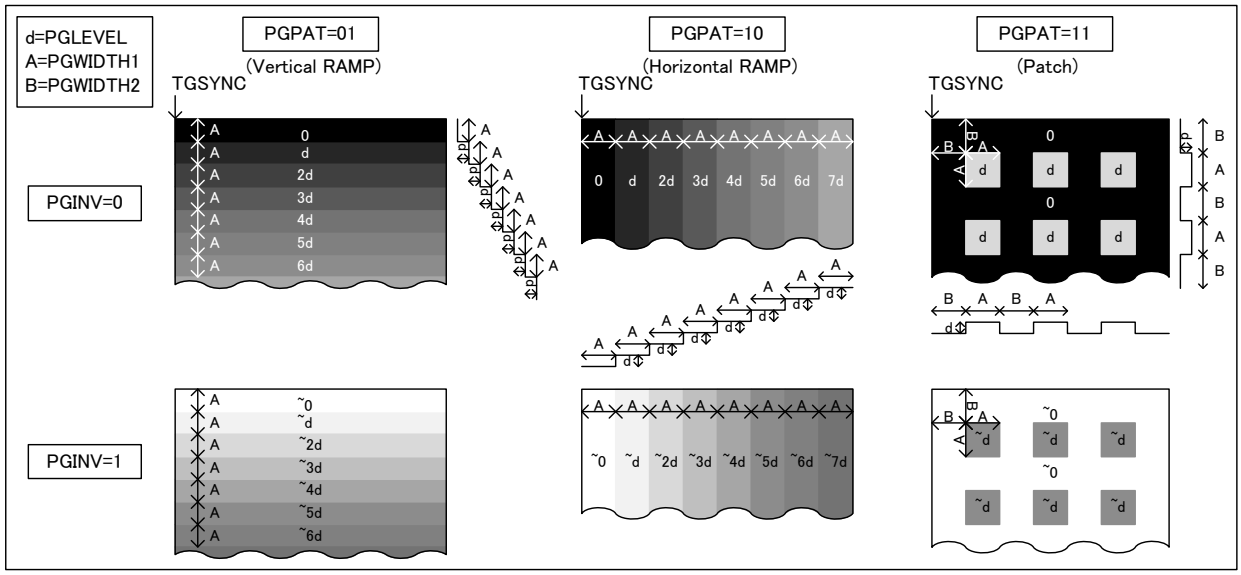


Figure 37 Test Pattern Output image

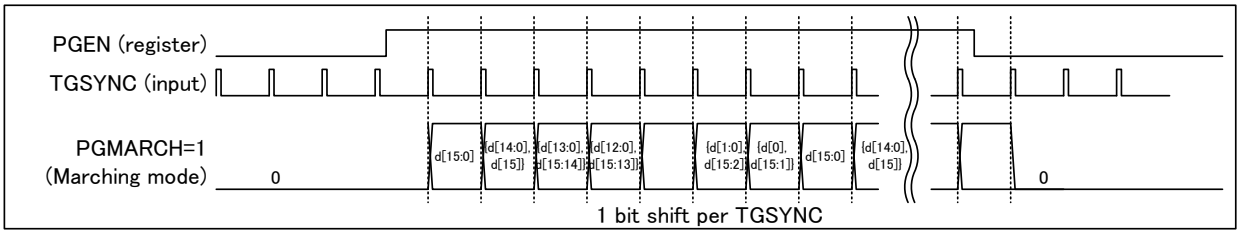


Figure 38 Test Pattern Output Data Formats (Marching mode)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) PG config	7	PGMARCH	0	pattern generator marching mode enable 0 = controlled by PGPAT 1 = marching pattern
	6:5	PGPAT[1:0]	00	select pattern generator output 00 = fixed value 01 = vertical ramp 10 = horizontal ramp 11 = patch
	4	PGINV	0	invert pattern generator output 0 = normal 1 = invert
	3	SEL_PGZ	0	select output of pattern generator (IN3) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs
	2	SEL_PGY	0	select output of pattern generator (IN2) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs
	1	SEL_PGX	0	select output of pattern generator (IN1) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs
	0	PGEN	0	enable pattern generator 0 = disable 1 = enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) PGCODE LSB	7:0	PGLEVEL[7:0]	0000_0000	parameter of pattern generator

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) PGCODE MSB	7:0	PGLEVEL[7:0]	0000_0000	parameter of pattern generator

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) PG width 1	7:0	PGWIDTH1[7:0]	0000_0000	parameter of pattern generator

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) PG width 2	7:0	PGWIDTH2[7:0]	0000_0000	parameter of pattern generator

REGISTER SETTING PROCEDURE

OVERALL

Figure 39 shows the overall procedure for WM8231 register setting. Every register can be configured without MCLK and TGSYNC input, but the following Note1~3 must be followed before starting normal operation.

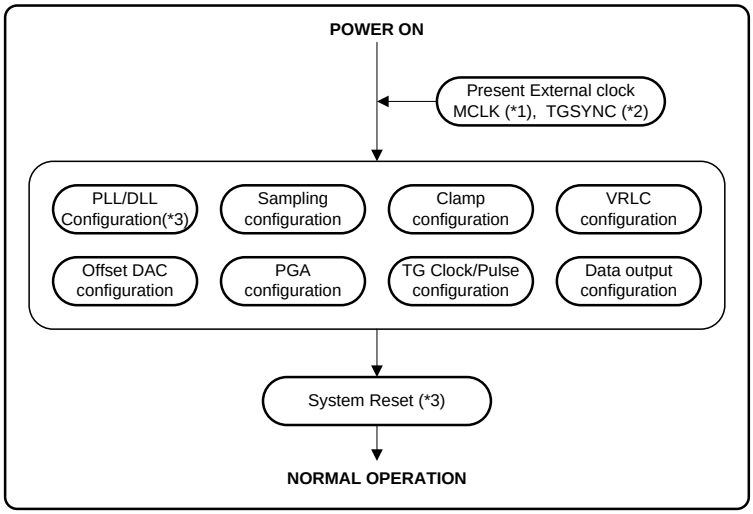


Figure 39 Overall Procedure

Notes:

1. MCLK must be present before System Reset. Also, System Reset must be done when MCLK is interrupted during normal operation.
2. TGSYNC input is required in TG slave mode. Also, this must be present before normal operation.
3. System Reset must be done after PLL/DLL configuration.

PLL/DLL CONFIGURATION

PLL and DLL registers must be configured depending on the MCLK frequency and data output format. See “PLL DLL Setup” section for details of configuring PLL/DLL registers. The device must be reset after PLL/DLL configuration as shown in Figure 40.

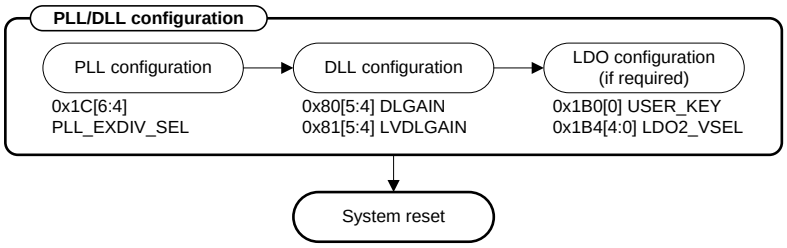


Figure 40 PLL/DLL Configuration

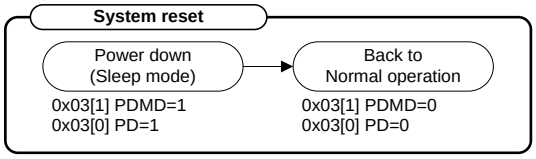


Figure 41 System Reset

SAMPLING CONFIGURATION

Sampling configuration is the setting for input signal polarity and sampling timing. See “CDS/Non-CDS Processing” section for details of configuring this register.

Non-CDS mode (S/H mode): RSMP configuration is not required.

CDS mode: RSMP and VSMP configurations are required.

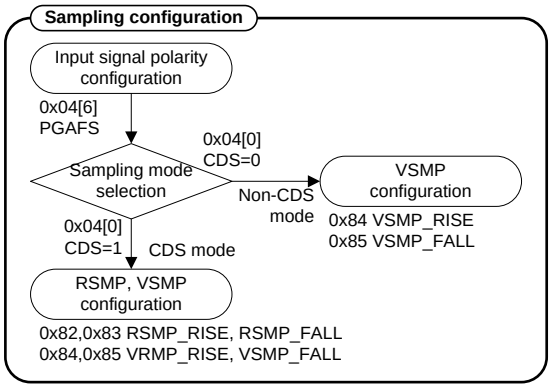


Figure 42 Sampling Configuration

CLAMP CONFIGURATION

Clamp configuration is the setting for clamp modes and clamp timing configuration in line clamp mode. See “Reset Level Clamping (RLC)” section and “CDS/Non-CDS Processing” section for details of configuring this register.

TG enabled: This must be enabled when AGC function is used.

Line clamp configuration: Line clamp operation is enabled during CLAMP_RISE ~ CLAMP_FALL period. Also, the source follower should be set to prevent clamp voltage drop in line clamp mode.

Pixel clamp (Bit clamp) mode: The pixel clamping is enabled during RSMP = high period. This mode can be used in CDS operation only.

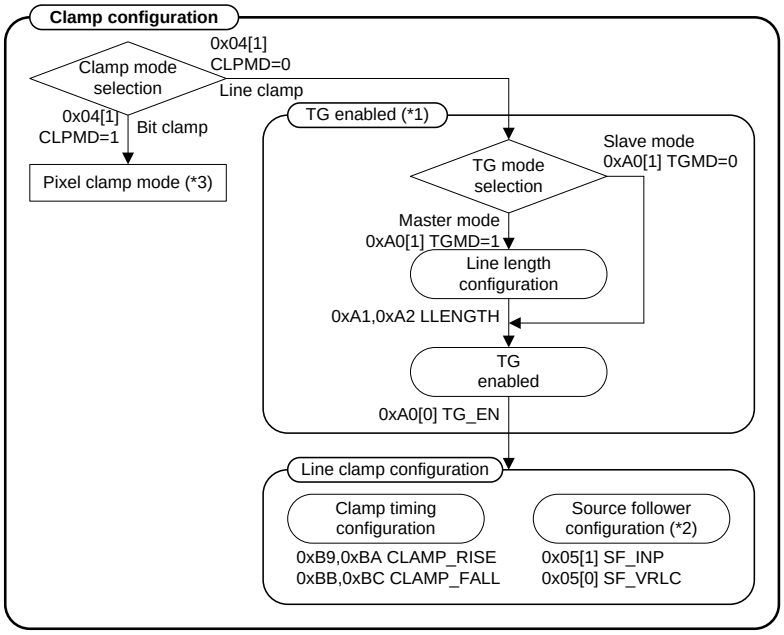


Figure 43 Clamp Configuration

Notes:

1. This must be set when Line clamp is used.
2. SF_INP and SF_VRLC must be set both when source follower enabled
3. Pixel clamp can be used in CDS operation only.

VRLC CONFIGURATION

VRLC configuration is the setting for VRLC voltage which, is used for input signal clamp voltage at line clamp operation. The VRLC voltage is also used as the reference level of non-CDS (S/H) operation. See “Reset Level Clamping (RLC)” section and “CDS/Non-CDS Processing” section for details of configuring this register.

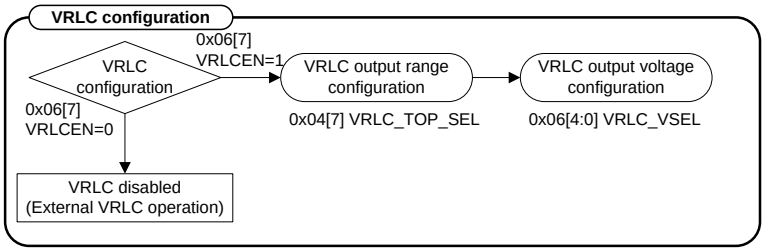


Figure 44 VRLC Configuration

OFFSET DAC CONFIGURATION

The offset DAC is used for black level offset compensation. WM8231 has BLC function to calibrate black level. In this mode, the offset DAC will be configured automatically. When this function is not needed, the offset DAC can be configured manually. See “Overall Signal Flow Summary” section for details of offset DAC configuration, and see “BLC Scenarios of Operation” for details of BLC sequence.

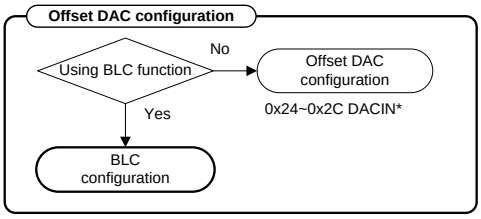


Figure 45 Offset DAC Configuration

BLC Configuration

TG enabled: This must be enabled when AGC function is used.

BLC start pixel configuration: This is start pixel configuration for BLC.

BLC period configuration: BLC will operate while this period from BLC start pixel.

BLC target level configuration: This is configuration for the target level of black pixel.

Coarse adjust configuration:

CADUR: This is the coarse adjust iteration setting during BLC period.

CA_EVERYLINE: When this register set, coarse adjust will operate on every line.

Fine adjust configuration: This is configuration for Coarse adjust iteration.

FA_EN: When this register set, fine adjust will operate during BLC period.

FA_EVERYLINE: When this register set, fine adjust will operate on every line.

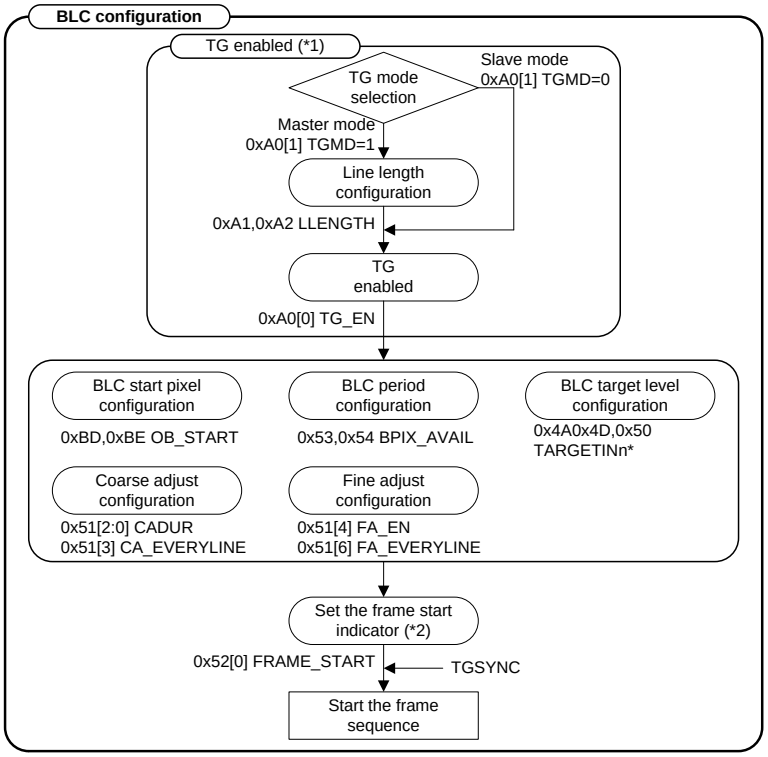


Figure 46 BLC Configuration

Notes:

1. This must be set when BLC is used.
2. With this register set, frame sequence will be started after TGSYNC is recognized. Therefore this should be set within the last line of previous frame.

PGA CONFIGURATION

The WM8231 provides an Automatic Gain Control (AGC) function. The output code is calibrated to target level by this automatic gain control function. See “Automatic Gain Control (AGC)” section for details of AGC sequence. Also, see the following instruction to configure AGC related registers. The analogue PGA (APGA) and digital PGA (DPGA) can be configured manually when AGC is not required. See “Offset Adjust and Programmable Gain” section for details of PGA configuration.

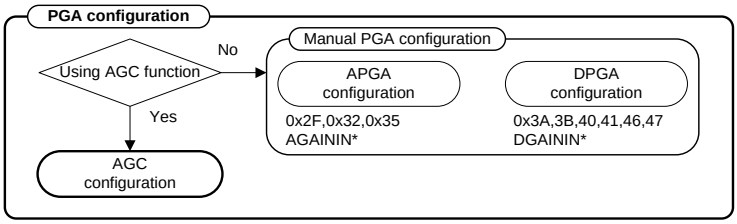


Figure 47 PGA Configuration

AGC CONFIGURATION

Figure 48 shows the procedure for AGC Configuration.

TG enabled: This must be enabled when AGC function is used.

AGC averaging factor configuration: This is averaging factor for peak level detection.

AGC APD/DPD configuration: This is line iteration setting for peak level detection.

AGC target level configuration: The output code will be calibrated to this target level after APGA and DPGA calibration. APGA and DPGA keep calibrated gain value while AGC is enabled. (AGC_EN=1)

Peak detection period configuration: This is the setting for peak detection period.

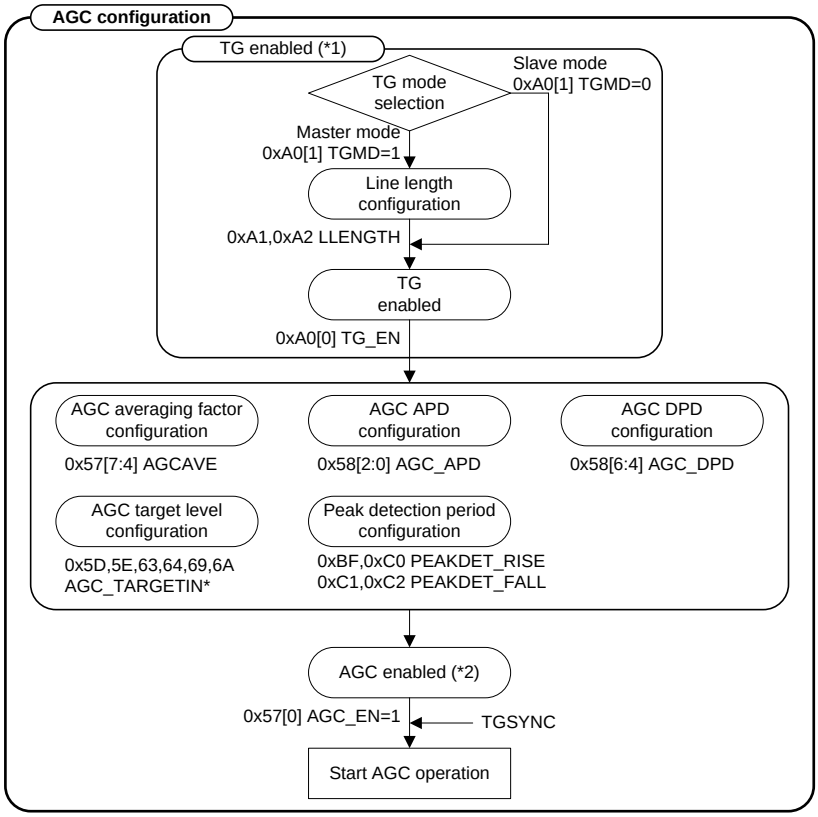


Figure 48 AGC Configuration

Notes:

1. This must be set when AGC is used.
2. With this register set, AGC sequence will be started after TGSYNC is recognized.

TG CLOCK CONFIGURATION

Figure 49 shows the procedure for TG Clock Timing and Mask Configuration. CLK1~CLK6 can be configured as clock type output. See “Sensor Timing Generation” section for details of TG function.

TG enabled: This must be enabled when TG mask function is used.

Mask period configuration: TG clock will be masked while mask signal is high. The rising and falling timing is configured by M*_RISE/FALL register. See “TG Mask Timing” section for details of this function.

Toggle point configuration: Pulse toggle timing is configured by toggle point setting (TP0~TP31). TP* register consists of toggle point setting bit (TP value bit) and enable bit. The enable bit must be set when TP is used. Unused TP can be disabled, but it must be followed Note-2 as described below.

T1 and T2 polarity configuration: T1 and T2 are internal signal to set the TG signal polarity during mask period. See “TG Mask Timing” section for details of this function.

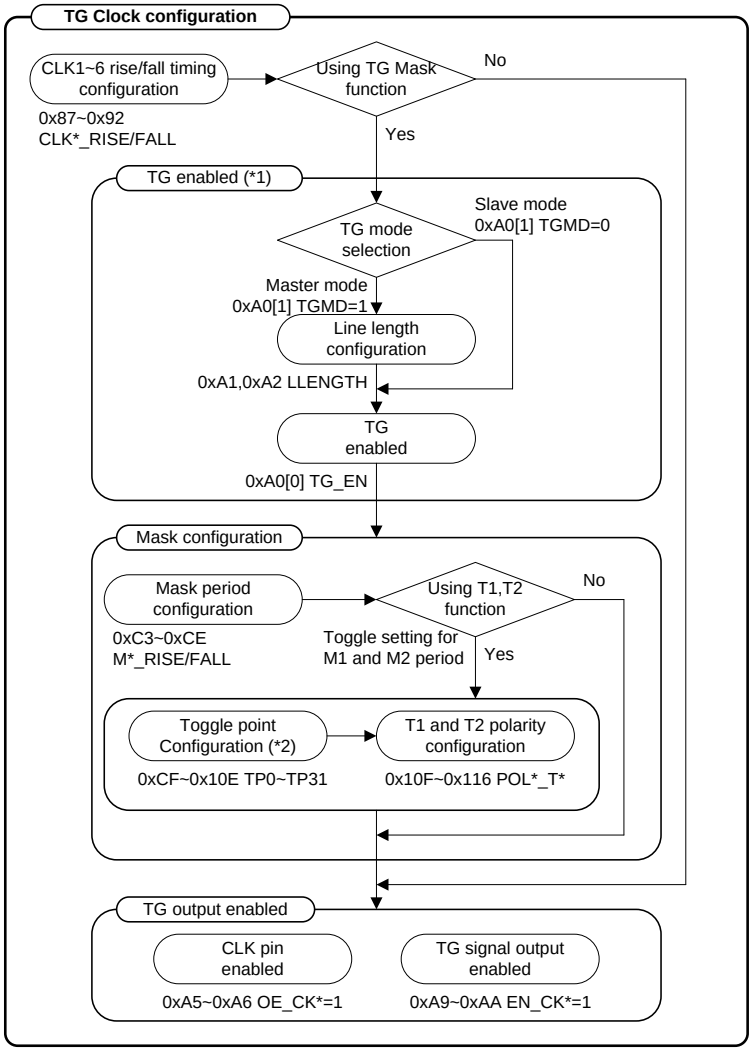


Figure 49 TG Clock Configuration

Notes:

1. This must be set when the TG-MASK function is used.
2. When configure Toggle point (TP), it must be used from TP0 in ascending order. Also, TP pixel counter value must be set as TP0<TP1<TP2 …..

TG PULSE CONFIGURATION

Figure 50 shows the procedure for TG Pulse Configuration. CLK2~CLK11 can be configured as pulse type output. See “Sensor Timing Generation” section for details of TG function.

TG enabled: This must be enabled when TG pulse function is used.

Toggle point configuration: Pulse toggle timing is configured by toggle point setting (TP0~TP31). TP* register consists of toggle point setting bit (TP pixel counter value bit) and enable bit. The enable bit must be set when TP is used. Unused TP can be disabled, but this must be followed Note-1 as described below.

PO0~PO7 configuration: PO0~PO7 are internal pulse for CLK pulse output. Pulse toggle timing is configured by polarity setting register (0x117~0x136 POL*_PO*).

CLK2~6 pulse out configuration: CLK2~CLK6 can select output signal type, clock type or pulse type by SEL_CK* register bit. This register must be set when pulse output is required.

PO assignment: Internal PO* pulse will be assigned to CLK2~CLK11 pin with this register.

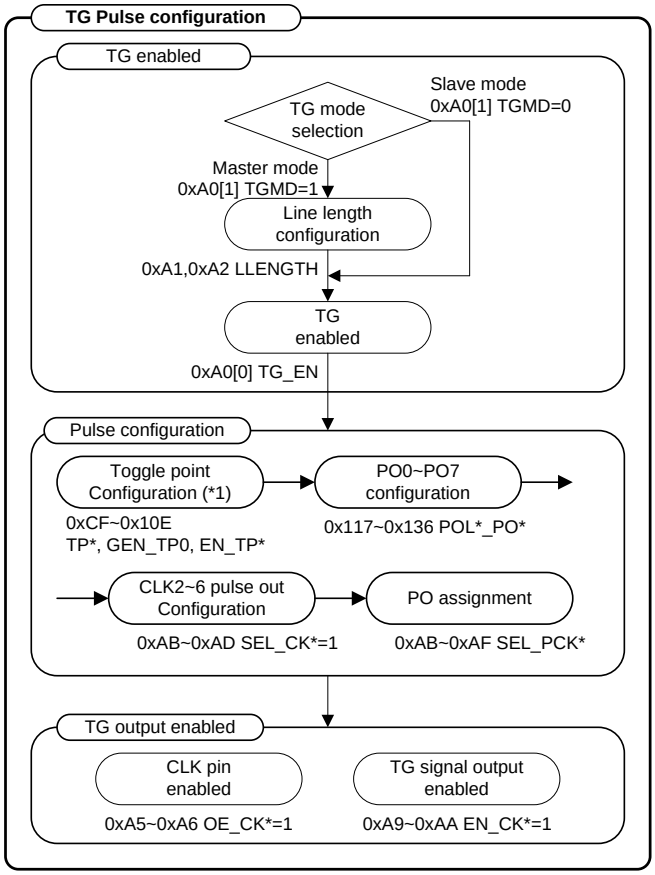


Figure 50 TG Pulse Configuration

Notes:

1. When configure Toggle point (TP), it must be used from TP0 in ascending order. Also, TP pixel counter value must be set as TP0<TP1<TP2

DATA OUTPUT CONFIGURATION

Figure 51 shows the procedure for Data Output Configuration. WM8231 provides 10-bit CMOS output and various LVDS output formats. See “Output Data Format” section for details of LVDS and CMOS output format.

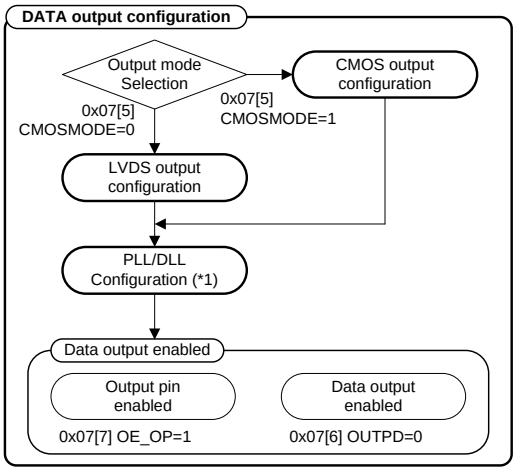


Figure 51 Data Output Configuration

Notes: 1. For details, see “PLL/DLL Configuration” section.

CMOS Output Configuration

Figure 52 shows the procedure for CMOS Output Configuration. Output drivability must be set when CMOS output is selected. In CMOS output mode, flag signal will be output from DCLKN/OC[2] pin.

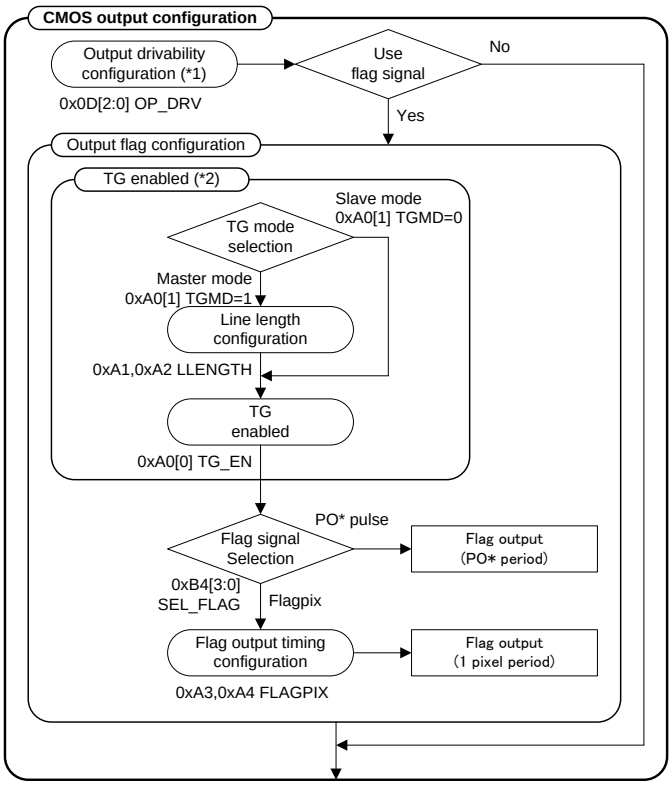


Figure 52 CMOS Output Configuration

Notes:

1. OP_DRV is valid when 0x0D[3] DRV_CTRL set to 0.When DRV_CTRL set to 1, OP_DRV is invalid, and drivability of output pin can be configured individually by 0x0E~0x13 OP*_DRV and OC*_DRV.
2. This must be set when flag is used.

LVDS Output Configuration

Figure 53 shows the procedure for LVDS Output Configuration.

LVDS format configuration: LVDS format can be configured by this register. See "Output Data Format" section for details of each format.

Data output order configuration: Data output order can be set by this register. See "LVDS Data Output Order" section for details of output order.

LVDS amplitude configuration: This is LVDS signal amplitude configuration. The LVDS amplitude is configured using the LVDS_AMP register field. Selections in the range 50mV to 200mV are supported. Note that the default code (110) should not be used.

LVDS VCM level configuration: This is LVDS common mode voltage configuration.

LVDS DCLK pattern configuration: This is DCLK output pattern configuration.

Output flag configuration: Flag type can be selected from start flag or cannel ID. See "Trigger Data" and "Channel ID" section for details of output flag. When this is not used, flag data (S~S4) will be always 0.

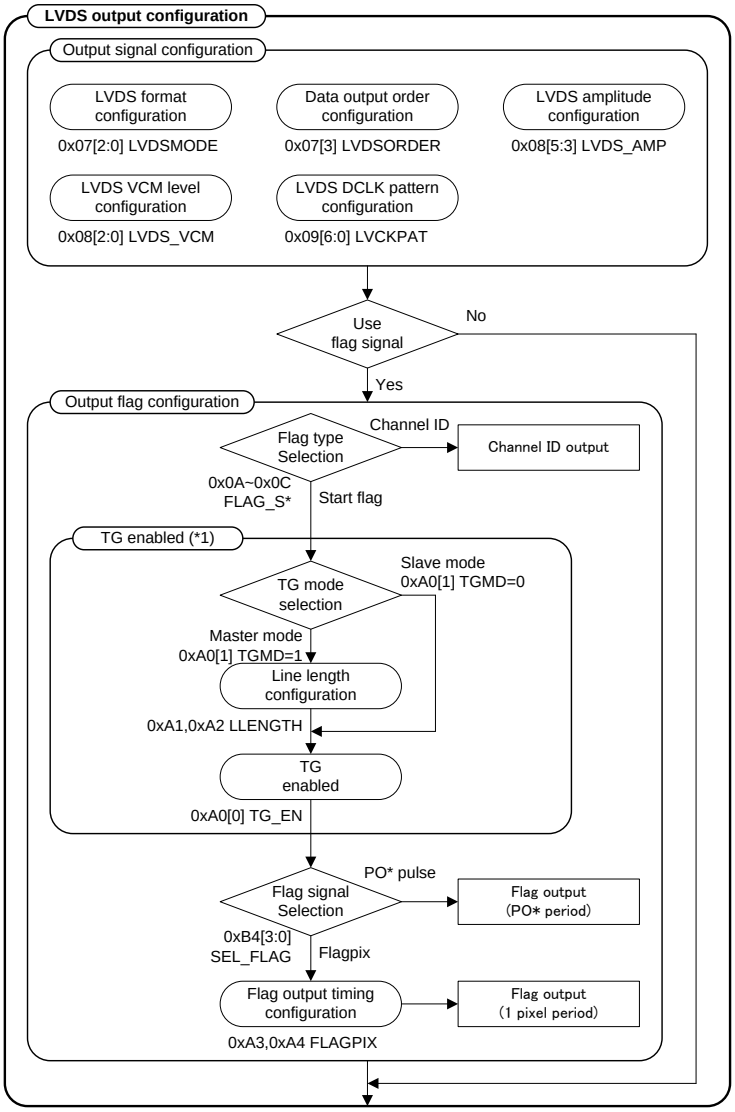


Figure 53 LVDS Output Configuration

Notes:

1. This must be set when start flag is used.

REGISTER MAP

The following table describes the location of each control bit used to determine the operation of the WM8231. Not all registers are used and any registers not listed should be set to zero.

REG	NAME	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset/Chip ID 1	SW_RESET_CHIP_ID[7:0]								32h
R1 (1h)	Chip ID 2	CHIP_ID[7:0]								82h
R2 (2h)	Chip Rev	0	0	0	0	CHIP_REV[3:0]				00h
R3 (3h)	Setup Reg 1	0	0	0	CHZPD	CHYPD	CHXPD	PDMD	PD	00h
R4 (4h)	Setup Reg 2	VVRLC_TOP_SEL	PGAFS	ADCFS	TGDIVMD	0	0	CLPMD	CDS	00h
R5 (5h)	Setup Reg 3	0	0	0	SF_BYPLS	PT_SF[1:0]		SF_INP	SF_VRLC	1Ch
R6 (6h)	VRLC control	VRLCEN	VRLC_ISEL[1:0]		VRLC_VSEL[4:0]					8Ah
R7 (7h)	output control	OE_OP	OUTPD	CMOSMODE	OUTSYNC	LVDSORDER	LVDSMODE[2:0]			40h
R8 (8h)	LVDS control	0	LVDS_POL	LVDS_AMP[2:0]			LVDS_VCM[2:0]			35h
R9 (9h)	LVDS clock pattern	0	LVCKPAT[6:0]							63h
R10 (Ah)	flag control 1	FLAG_S1[3:0]				FLAG_S0[3:0]				10h
R11 (Bh)	flag control 2	FLAG_S3[3:0]				FLAG_S2[3:0]				00h
R12 (Ch)	flag control 3	0	0	0	0	FLAG_S4[3:0]				00h
R13 (Dh)	CMOS drivability control 1	0	0	0	0	DRV_CTRL	OP_DRV[2:0]			00h
R14 (Eh)	CMOS drivability control 2	0	OP1_DRV[2:0]			0	OP0_DRV[2:0]			00h
R15 (Fh)	CMOS drivability control 3	0	OP3_DRV[2:0]			0	OP2_DRV[2:0]			00h
R16 (10h)	CMOS drivability control 4	0	OP5_DRV[2:0]			0	OP4_DRV[2:0]			00h
R17 (11h)	CMOS drivability control 5	0	OP7_DRV[2:0]			0	OP6_DRV[2:0]			00h
R18 (12h)	CMOS drivability control 6	0	OP9_DRV[2:0]			0	OP8_DRV[2:0]			00h
R19 (13h)	CMOS drivability control 7	0	OC2_DRV[2:0]			0	OC1_DRV[2:0]			00h
R20 (14h)	PG config	PGMARCH	PGPAT[1:0]		PGINV	SEL_PGZ	SEL_PGY	SEL_PGX	PGEN	00h
R21 (15h)	PGCODE LSB	PGLEVEL[7:0]								00h
R22 (16h)	PGCODE MSB	PGLEVEL[7:0]								00h
R23 (17h)	PG width 1	PGWIDTH1[7:0]								00h
R24 (18h)	PG width 2	PGWIDTH2[7:0]								00h
R25 (19h)	clock monitor	0	0	0	0	0	MONCLK[2:0]			00h
R26 (1Ah)	PLL control 1	0	0	0	0	0	PLL_LPF_RST	PLL_CP_PD	PLL_VCO_PD	00h
R27 (1Bh)	PLL control 2	0	PLL_LPF_SEL	0	0	PLL_PFD_CTRL[1:0]		PLL_CP_GAIN[1:0]		09h
R28 (1Ch)	PLL divider control 1	0	PLL_EXDIV_SEL[2:0]			PLL_FBDIV_SEL[3:0]				11h
R29 (1Dh)	PLL divider control 2	0	0	PLL_POSTDIV2_SEL[1:0]		PLL_POSTDIV1_SEL[3:0]				11h
R35 (23h)	Cycle mode control	0	0	0	0	INTM[1:0]		ACYC	LINBYLINE	00h
R38 (26h)	DAC IN1	DACIN1[7:0]								80h
R41 (29h)	DAC IN2IN2	DACIN2IN2[7:0]								80h
R44 (2Ch)	DAC INP3	DACINP3[7:0]								80h
R47 (2Fh)	AGAIN IN1	0	0	0	AGAININ1[4:0]					01h
R50 (32h)	AGAIN IN2IN2	0	0	0	AGAININ2IN2[4:0]					01h
R53 (35h)	AGAIN INP3	0	0	0	AGAININP3[4:0]					01h
R58 (3Ah)	DGAIN IN1 LSB	DGAININ1[3:0]				0	0	0	0	00h
R59 (3Bh)	DGAIN IN1 MSB	DGAININ1[11:4]								80h
R64 (40h)	DGAIN IN2IN2 LSB	DGAININ2IN2[3:0]				0	0	0	0	00h
R65 (41h)	DGAIN IN2IN2 MSB	DGAININ2IN2[11:4]								80h
R70 (46h)	DGAIN INP3 LSB	DGAININP3[3:0]				0	0	0	0	00h
R71 (47h)	DGAIN INP3 MSB	DGAININP3[11:4]								80h
R74 (4Ah)	BLC IN1 target	TARGETIN1[7:0]								00h
R77 (4Dh)	BLC IN2IN2 target	TARGETIN2IN2[7:0]								00h

REG	NAME	7	6	5	4	3	2	1	0	DEFAULT
R80 (50h)	BLC INP3 target	TARGETINP3[7:0]								00h
R81 (51h)	BLC control 1	FRAME_SEQ	FA_EVERYLINE	FA_ACCUM	FA_EN	CA_EVERYLINE	CADUR[2:0]			00h
R82 (52h)	BLC control 2	0	0	0	0	0	0	SEQ_START	FRAME_START	00h
R83 (53h)	BLC control 3	BPIX_AVAIL[7:0]								00h
R84 (54h)	BLC control 4	0	0	0	0	0	0	BPIX_AVAIL[9:8]		00h
R85 (55h)	BLC control 5	LINE_DEL[7:0]								00h
R86 (56h)	BLC control 6	0	0	0	0	0	0	0	LINE_DEL[8]	00h
R87 (57h)	AGC config 1	AGCAVE[3:0]				0	AGC_ERRFLAG	AGC_ENDFLAG	AGC_EN	00h
R88 (58h)	AGC config 2	0	AGC_DPD[2:0]			0	AGC_APD[2:0]			00h
R93 (5Dh)	AGC target IN1 LSB	AGC_TARGETIN1[7:0]								00h
R94 (5Eh)	AGC target IN1 MSB	0	0	0	0	0	0	AGC_TARGETIN1[9:8]		00h
R99 (63h)	AGC target IN2IN2 LSB	AGC_TARGETIN2IN2[7:0]								00h
R100 (64h)	AGC target IN2IN2 MSB	0	0	0	0	0	0	AGC_TARGETIN2[9:8]		00h
R105 (69h)	AGC target IN3 LSB	AGC_TARGETIN3[7:0]								00h
R106 (6Ah)	AGC target IN3 MSB	0	0	0	0	0	0	AGC_TARGETIN3[9:8]		00h
R111 (6Fh)	AGC peak level IN1 LSB	PEAK_IN1[7:0]								00h
R112 (70h)	AGC peak level IN1 MSB	0	0	0	0	0	0	PEAK_IN1[9:8]		00h
R117 (75h)	AGC peak level IN2 LSB	PEAK_IN2[7:0]								00h
R118 (76h)	AGC peak level IN2 MSB	0	0	0	0	0	0	PEAK_IN2[9:8]		00h
R123 (7Bh)	AGC peak level IN3 LSB	PEAK_IN3[7:0]								00h
R124 (7Ch)	AGC peak level IN3 MSB	0	0	0	0	0	0	PEAK_IN3[9:8]		00h
R128 (80h)	DLL config 1	0	0	DLGAIN[1:0]		0	DLLRST	CKOSTB	AFECKSTB	10h
R129 (81h)	DLL config 2	0	0	LVDLGAIN[1:0]		0	0	LVDLLRST	LVDLLSTB	10h
R130 (82h)	RSMP rise	0	0	RSMP_RISE[5:0]						1Ch
R131 (83h)	RSMP fall	0	0	RSMP_FALL[5:0]						26h
R132 (84h)	VSMP rise	0	0	VSMP_RISE[5:0]						28h
R133 (85h)	VSMP fall	0	0	VSMP_FALL[5:0]						08h
R134 (86h)	TGCKO rise	0	0	TCLKO_RISE[5:0]						37h
R135 (87h)	CLK1 rise	0	0	CLK1_RISE[5:0]						0Ah
R136 (88h)	CLK1 fall	0	0	CLK1_FALL[5:0]						19h
R137 (89h)	CLK2 rise	0	0	CLK2_RISE[5:0]						19h
R138 (8Ah)	CLK2fall	0	0	CLK2_FALL[5:0]						28h
R139 (8Bh)	CLK3 rise	0	0	CLK3_RISE[5:0]						28h
R140 (8Ch)	CLK3 fall	0	0	CLK3_FALL[5:0]						0Ah
R141 (8Dh)	CLK4 rise	0	0	CLK4_RISE[5:0]						00h
R142 (8Eh)	CLK4 fall	0	0	CLK4_FALL[5:0]						00h
R143 (8Fh)	CLK5 rise	0	0	CLK5_RISE[5:0]						0Ah
R144 (90h)	CLK5 fall	0	0	CLK5_FALL[5:0]						28h
R145 (91h)	CLK6 rise	0	0	CLK6_RISE[5:0]						0Ah
R146 (92h)	CLK6 fall	0	0	CLK6_FALL[5:0]						28h
R160 (A0h)	TG config 1	OFFSET[3:0]				CYCMD	POLSYNC	TGMD	TG_EN	00h
R161 (A1h)	TG config 2	LLENGTH[7:0]								00h
R162 (A2h)	TG config 3	0	LLENGTH[14:8]							00h
R163 (A3h)	TG config 4	FLAGPIX[7:0]								00h
R164 (A4h)	TG config 5	0	FLAGPIX[14:8]							00h
R165 (A5h)	TG config 6	OE_CLK8	OE_CLK7	OE_CLK6	OE_CLK5	OE_CLK4	OE_CLK3	OE_CLK2	OE_CLK1	FFh
R166 (A6h)	TG config 7	0	0	0	0	0	OE_CLK11	OE_CLK10	OE_CLK9	07h
R167 (A7h)	TG config 8	INV_CLK8	INV_CLK7	INV_CLK6	INV_CLK5	INV_CLK4	INV_CLK3	INV_CLK2	INV_CLK1	00h
R168 (A8h)	TG config 9	0	0	0	0	0	INV_CLK11	INV_CLK10	INV_CLK9	00h

REG	NAME	7	6	5	4	3	2	1	0	DEFAULT
R169 (A9h)	TG config 10	EN_CLK8	EN_CLK7	EN_CLK6	EN_CLK5	EN_CLK4	EN_CLK3	EN_CLK2	EN_CLK1	00h
R170 (AAh)	TG config 11	0	0	0	0	0	EN_CLK11	EN_CLK10	EN_CLK9	00h
R171 (ABh)	TG config 12	SEL_CLK3	SEL_PCK3[2:0]			SEL_CLK2	SEL_PCK2[2:0]			00h
R172 (ACh)	TG config 13	SEL_CLK5	SEL_PCK5[2:0]			SEL_CLK4	SEL_PCK4[2:0]			00h
R173 (ADh)	TG config 14	0	SEL_PCK7[2:0]			SEL_CLK6	SEL_PCK6[2:0]			00h
R174 (AEh)	TG config 15	0	SEL_PCK9[2:0]			0	SEL_PCK8[2:0]			00h
R175 (AFh)	TG config 16	0	SEL_PCK11[2:0]			0	SEL_PCK10[2:0]			00h
R176 (B0h)	TG config 17	DEL_PCK5[1:0]		DEL_PCK4[1:0]		DEL_PCK3[1:0]		DEL_PCK2[1:0]		00h
R177 (B1h)	TG config 18	DEL_PCK9[1:0]		DEL_PCK8[1:0]		DEL_PCK7[1:0]		DEL_PCK6[1:0]		00h
R178 (B2h)	TG config 19	0	0	0	0	DEL_PCK11[1:0]		DEL_PCK10[1:0]		00h
R179 (B3h)	TG config 20	0	0	0	INV_M3	INV_M2	INV_M1	INV_T2	INV_T1	00h
R180 (B4h)	TG config 21	0	0	0	0	SEL_FLAG[3:0]				00h
R181 (B5h)	TG config 22	0	CYCPAT_PO1[2:0]			0	CYCPAT_PO0[2:0]			00h
R182 (B6h)	TG config 23	0	CYCPAT_PO3[2:0]			0	CYCPAT_PO2[2:0]			00h
R183 (B7h)	TG config 24	0	CYCPAT_PO5[2:0]			0	CYCPAT_PO4[2:0]			00h
R184 (B8h)	TG config 25	0	CYCPAT_PO7[2:0]			0	CYCPAT_PO6[2:0]			00h
R185 (B9h)	clamp enable rise LSB	CLAMP_RISE[7:0]								00h
R186 (BAh)	clamp enable rise MSB	0	CLAMP_RISE[14:8]							00h
R187 (BBh)	clamp enable fall LSB	CLAMP_FALL[7:0]								00h
R188 (BCh)	clamp enable fall MSB	0	CLAMP_FALL[14:8]							00h
R189 (BDh)	OB start LSB	OB_START[7:0]								00h
R190 (BEh)	OB start MSB	0	OB_START[14:8]							00h
R191 (BFh)	peak_det rise LSB	PEAKDET_RISE[7:0]								00h
R192 (C0h)	peak_det rise MSB	0	PEAKDET_RISE[14:8]							00h
R193 (C1h)	peak_det fall LSB	PEAKDET_FALL[7:0]								00h
R194 (C2h)	peak_det fall MSB	0	PEAKDET_FALL[14:8]							00h
R195 (C3h)	Mask pulse 1 rise LSB	M1_RISE[7:0]								00h
R196 (C4h)	Mask pulse 1 rise MSB	0	M1_RISE[14:8]							00h
R197 (C5h)	Mask pulse 1 fall LSB	M1_FALL[7:0]								00h
R198 (C6h)	Mask pulse 1 fall MSB	0	M1_FALL[14:8]							00h
R199 (C7h)	Mask pulse 2 rise LSB	M2_RISE[7:0]								00h
R200 (C8h)	Mask pulse 2 rise MSB	0	M2_RISE[14:8]							00h
R201 (C9h)	Mask pulse 2 fall LSB	M2_FALL[7:0]								00h
R202 (CAh)	Mask pulse 2 fall MSB	0	M2_FALL[14:8]							00h
R203 (CBh)	Mask pulse 3 rise LSB	M3_RISE[7:0]								00h
R204 (CCh)	Mask pulse 3 rise MSB	0	M3_RISE[14:8]							00h
R205 (CDh)	Mask pulse 3 fall LSB	M3_FALL[7:0]								00h
R206 (CEh)	Mask pulse 3 fall MSB	0	M3_FALL[14:8]							00h
R207 (CFh)	Toggle point 0 LSB	TP0[7:0]								00h
R208 (D0h)	Toggle point 0 MSB	GEN_TP0	TP0[14:8]							00h
R209 (D1h)	Toggle point 1 LSB	TP1[7:0]								00h
R210 (D2h)	Toggle point 1 MSB	EN_TP1	TP1[14:8]							00h
R211 (D3h)	Toggle point 2 LSB	TP2[7:0]								00h
R212 (D4h)	Toggle point 2 MSB	EN_TP2	TP2[14:8]							00h
R213 (D5h)	Toggle point 3 LSB	TP3[7:0]								00h
R214 (D6h)	Toggle point 3 MSB	EN_TP3	TP3[14:8]							00h
R215 (D7h)	Toggle point 4 LSB	TP4[7:0]								00h
R216 (D8h)	Toggle point 4 MSB	EN_TP4	TP4[14:8]							00h
R217 (D9h)	Toggle point 5 LSB	TP5[7:0]								00h

REG	NAME	7	6	5	4	3	2	1	0	DEFAULT
R218 (DAh)	Toggle point 5 MSB	EN_TP5	TP5[14:8]							00h
R219 (DBh)	Toggle point 6 LSB	TP6[7:0]								00h
R220 (DCh)	Toggle point 6 MSB	EN_TP6	TP6[14:8]							00h
R221 (DDh)	Toggle point 7 LSB	TP7[7:0]								00h
R222 (DEh)	Toggle point 7 MSB	EN_TP7	TP7[14:8]							00h
R223 (DFh)	Toggle point 8 LSB	TP8[7:0]								00h
R224 (E0h)	Toggle point 8 MSB	EN_TP8	TP8[14:8]							00h
R225 (E1h)	Toggle point 9 LSB	TP9[7:0]								00h
R226 (E2h)	Toggle point 9 MSB	EN_TP9	TP9[14:8]							00h
R227 (E3h)	Toggle point 10 LSB	TP10[7:0]								00h
R228 (E4h)	Toggle point 10 MSB	EN_TP10	TP10[14:8]							00h
R229 (E5h)	Toggle point 11 LSB	TP11[7:0]								00h
R230 (E6h)	Toggle point 11 MSB	EN_TP11	TP11[14:8]							00h
R231 (E7h)	Toggle point 12 LSB	TP12[7:0]								00h
R232 (E8h)	Toggle point 12 MSB	EN_TP12	TP12[14:8]							00h
R233 (E9h)	Toggle point 13 LSB	TP13[7:0]								00h
R234 (EAh)	Toggle point 13 MSB	EN_TP13	TP13[14:8]							00h
R235 (EBh)	Toggle point 14 LSB	TP14[7:0]								00h
R236 (ECh)	Toggle point 14 MSB	EN_TP14	TP14[14:8]							00h
R237 (EDh)	Toggle point 15 LSB	TP15[7:0]								00h
R238 (EEh)	Toggle point 15 MSB	EN_TP15	TP15[14:8]							00h
R239 (EFh)	Toggle point 16 LSB	TP16[7:0]								00h
R240 (F0h)	Toggle point 16 MSB	EN_TP16	TP16[14:8]							00h
R241 (F1h)	Toggle point 17 LSB	TP17[7:0]								00h
R242 (F2h)	Toggle point 17 MSB	EN_TP17	TP17[14:8]							00h
R243 (F3h)	Toggle point 18 LSB	TP18[7:0]								00h
R244 (F4h)	Toggle point 18 MSB	EN_TP18	TP18[14:8]							00h
R245 (F5h)	Toggle point 19 LSB	TP19[7:0]								00h
R246 (F6h)	Toggle point 19 MSB	EN_TP19	TP19[14:8]							00h
R247 (F7h)	Toggle point 20 LSB	TP20[7:0]								00h
R248 (F8h)	Toggle point 20 MSB	EN_TP20	TP20[14:8]							00h
R249 (F9h)	Toggle point 21 LSB	TP21[7:0]								00h
R250 (FAh)	Toggle point 21 MSB	EN_TP21	TP21[14:8]							00h
R251 (FBh)	Toggle point 22 LSB	TP22[7:0]								00h
R252 (FCh)	Toggle point 22 MSB	EN_TP22	TP22[14:8]							00h
R253 (FDh)	Toggle point 23 LSB	TP23[7:0]								00h
R254 (FEh)	Toggle point 23 MSB	EN_TP23	TP23[14:8]							00h
R255 (FFh)	Toggle point 24 LSB	TP24[7:0]								00h
R256 (100h)	Toggle point 24 MSB	EN_TP24	TP24[14:8]							00h
R257 (101h)	Toggle point 25 LSB	TP25[7:0]								00h
R258 (102h)	Toggle point 25 MSB	EN_TP25	TP25[14:8]							00h
R259 (103h)	Toggle point 26 LSB	TP26[7:0]								00h
R260 (104h)	Toggle point 26 MSB	EN_TP26	TP26[14:8]							00h
R261 (105h)	Toggle point 27 LSB	TP27[7:0]								00h
R262 (106h)	Toggle point 27 MSB	EN_TP27	TP27[14:8]							00h
R263 (107h)	Toggle point 28 LSB	TP28[7:0]								00h
R264 (108h)	Toggle point 28 MSB	EN_TP28	TP28[14:8]							00h
R265 (109h)	Toggle point 29 LSB	TP29[7:0]								00h
R266 (10Ah)	Toggle point 29 MSB	EN_TP29	TP29[14:8]							00h

REG	NAME	7	6	5	4	3	2	1	0	DEFAULT
R267 (10Bh)	Toggle point 30 LSB	TP30[7:0]								00h
R268 (10Ch)	Toggle point 30 MSB	EN_TP30	TP30[14:8]							00h
R269 (10Dh)	Toggle point 31 LSB	TP31[7:0]								00h
R270 (10Eh)	Toggle point 31 MSB	EN_TP31	TP31[14:8]							00h
R271 (10Fh)	Polarity setting of T1 1	POL7_T1	POL6_T1	POL5_T1	POL4_T1	POL3_T1	POL2_T1	POL1_T1	POL0_T1	FFh
R272 (110h)	Polarity setting of T1 2	POL15_T1	POL14_T1	POL13_T1	POL12_T1	POL11_T1	POL10_T1	POL9_T1	POL8_T1	FFh
R273 (111h)	Polarity setting of T1 3	POL23_T1	POL22_T1	POL21_T1	POL20_T1	POL19_T1	POL18_T1	POL17_T1	POL16_T1	FFh
R274 (112h)	Polarity setting of T1 4	POL31_T1	POL30_T1	POL29_T1	POL28_T1	POL27_T1	POL26_T1	POL25_T1	POL24_T1	FFh
R275 (113h)	Polarity setting of T2 1	POL7_T2	POL6_T2	POL5_T2	POL4_T2	POL3_T2	POL2_T2	POL1_T2	POL0_T2	FFh
R276 (114h)	Polarity setting of T2 2	POL15_T2	POL14_T2	POL13_T2	POL12_T2	POL11_T2	POL10_T2	POL9_T2	POL8_T2	FFh
R277 (115h)	Polarity setting of T2 3	POL23_T2	POL22_T2	POL21_T2	POL20_T2	POL19_T2	POL18_T2	POL17_T2	POL16_T2	FFh
R278 (116h)	Polarity setting of T2 4	POL31_T2	POL30_T2	POL29_T2	POL28_T2	POL27_T2	POL26_T2	POL25_T2	POL24_T2	FFh
R279 (117h)	Polarity setting of P0 1	POL7_PO0	POL6_PO0	POL5_PO0	POL4_PO0	POL3_PO0	POL2_PO0	POL1_PO0	POL0_PO0	00h
R280 (118h)	Polarity setting of P0 2	POL15_PO0	POL14_PO0	POL13_PO0	POL12_PO0	POL11_PO0	POL10_PO0	POL9_PO0	POL8_PO0	00h
R281 (119h)	Polarity setting of P0 3	POL23_PO0	POL22_PO0	POL21_PO0	POL20_PO0	POL19_PO0	POL18_PO0	POL17_PO0	POL16_PO0	00h
R282 (11Ah)	Polarity setting of P0 4	POL31_PO0	POL30_PO0	POL29_PO0	POL28_PO0	POL27_PO0	POL26_PO0	POL25_PO0	POL24_PO0	00h
R283 (11Bh)	Polarity setting of P1 1	POL7_PO1	POL6_PO1	POL5_PO1	POL4_PO1	POL3_PO1	POL2_PO1	POL1_PO1	POL0_PO1	00h
R284 (11Ch)	Polarity setting of P1 2	POL15_PO1	POL14_PO1	POL13_PO1	POL12_PO1	POL11_PO1	POL10_PO1	POL9_PO1	POL8_PO1	00h
R285 (11Dh)	Polarity setting of P1 3	POL23_PO1	POL22_PO1	POL21_PO1	POL20_PO1	POL19_PO1	POL18_PO1	POL17_PO1	POL16_PO1	00h
R286 (11Eh)	Polarity setting of P1 4	POL31_PO1	POL30_PO1	POL29_PO1	POL28_PO1	POL27_PO1	POL26_PO1	POL25_PO1	POL24_PO1	00h
R287 (11Fh)	Polarity setting of P2 1	POL7_PO2	POL6_PO2	POL5_PO2	POL4_PO2	POL3_PO2	POL2_PO2	POL1_PO2	POL0_PO2	00h
R288 (120h)	Polarity setting of P2 2	POL15_PO2	POL14_PO2	POL13_PO2	POL12_PO2	POL11_PO2	POL10_PO2	POL9_PO2	POL8_PO2	00h
R289 (121h)	Polarity setting of P2 3	POL23_PO2	POL22_PO2	POL21_PO2	POL20_PO2	POL19_PO2	POL18_PO2	POL17_PO2	POL16_PO2	00h
R290 (122h)	Polarity setting of P2 4	POL31_PO2	POL30_PO2	POL29_PO2	POL28_PO2	POL27_PO2	POL26_PO2	POL25_PO2	POL24_PO2	00h
R291 (123h)	Polarity setting of P3 1	POL7_PO3	POL6_PO3	POL5_PO3	POL4_PO3	POL3_PO3	POL2_PO3	POL1_PO3	POL0_PO3	00h
R292 (124h)	Polarity setting of P3 2	POL15_PO3	POL14_PO3	POL13_PO3	POL12_PO3	POL11_PO3	POL10_PO3	POL9_PO3	POL8_PO3	00h
R293 (125h)	Polarity setting of P3 3	POL23_PO3	POL22_PO3	POL21_PO3	POL20_PO3	POL19_PO3	POL18_PO3	POL17_PO3	POL16_PO3	00h
R294 (126h)	Polarity setting of P3 4	POL31_PO3	POL30_PO3	POL29_PO3	POL28_PO3	POL27_PO3	POL26_PO3	POL25_PO3	POL24_PO3	00h
R295 (127h)	Polarity setting of P4 1	POL7_PO4	POL6_PO4	POL5_PO4	POL4_PO4	POL3_PO4	POL2_PO4	POL1_PO4	POL0_PO4	00h
R296 (128h)	Polarity setting of P4 2	POL15_PO4	POL14_PO4	POL13_PO4	POL12_PO4	POL11_PO4	POL10_PO4	POL9_PO4	POL8_PO4	00h
R297 (129h)	Polarity setting of P4 3	POL23_PO4	POL22_PO4	POL21_PO4	POL20_PO4	POL19_PO4	POL18_PO4	POL17_PO4	POL16_PO4	00h
R298 (12Ah)	Polarity setting of P4 4	POL31_PO4	POL30_PO4	POL29_PO4	POL28_PO4	POL27_PO4	POL26_PO4	POL25_PO4	POL24_PO4	00h
R299 (12Bh)	Polarity setting of P5 1	POL7_PO5	POL6_PO5	POL5_PO5	POL4_PO5	POL3_PO5	POL2_PO5	POL1_PO5	POL0_PO5	00h
R300 (12Ch)	Polarity setting of P5 2	POL15_PO5	POL14_PO5	POL13_PO5	POL12_PO5	POL11_PO5	POL10_PO5	POL9_PO5	POL8_PO5	00h
R301 (12Dh)	Polarity setting of P5 3	POL23_PO5	POL22_PO5	POL21_PO5	POL20_PO5	POL19_PO5	POL18_PO5	POL17_PO5	POL16_PO5	00h
R302 (12Eh)	Polarity setting of P5 4	POL31_PO5	POL30_PO5	POL29_PO5	POL28_PO5	POL27_PO5	POL26_PO5	POL25_PO5	POL24_PO5	00h
R303 (12Fh)	Polarity setting of P6 1	POL7_PO6	POL6_PO6	POL5_PO6	POL4_PO6	POL3_PO6	POL2_PO6	POL1_PO6	POL0_PO6	00h
R304 (130h)	Polarity setting of P6 2	POL15_PO6	POL14_PO6	POL13_PO6	POL12_PO6	POL11_PO6	POL10_PO6	POL9_PO6	POL8_PO6	00h
R305 (131h)	Polarity setting of P6 3	POL23_PO6	POL22_PO6	POL21_PO6	POL20_PO6	POL19_PO6	POL18_PO6	POL17_PO6	POL16_PO6	00h
R306 (132h)	Polarity setting of P6 4	POL31_PO6	POL30_PO6	POL29_PO6	POL28_PO6	POL27_PO6	POL26_PO6	POL25_PO6	POL24_PO6	00h
R307 (133h)	Polarity setting of P7 1	POL7_PO7	POL6_PO7	POL5_PO7	POL4_PO7	POL3_PO7	POL2_PO7	POL1_PO7	POL0_PO7	00h
R308 (134h)	Polarity setting of P7 2	POL15_PO7	POL14_PO7	POL13_PO7	POL12_PO7	POL11_PO7	POL10_PO7	POL9_PO7	POL8_PO7	00h
R309 (135h)	Polarity setting of P7 3	POL23_PO7	POL22_PO7	POL21_PO7	POL20_PO7	POL19_PO7	POL18_PO7	POL17_PO7	POL16_PO7	00h
R310 (136h)	Polarity setting of P7 4	POL31_PO7	POL30_PO7	POL29_PO7	POL28_PO7	POL27_PO7	POL26_PO7	POL25_PO7	POL24_PO7	00h

EXTENDED PAGE REGISTERS

R432 (1B0h)	User access control	0	0	0	0	0	0	0	USER_KEY	00h
R436 (1B4h)	LDO2 control	0	0	0	LDO2 VSEL					10h
R448 (1C0h)	USER_KEY2	0	0	0	0	0	0	0	USER_KEY2	00h
R459 (1CBh)	Comp control	0	0	0	0	0	0	PT_COMP[1:0]		01h

Notes:

1. To change the LDO2 control, the USER_KEY bit must be set to '1'.
2. If it's not required to change this register, it must be set as default.
3. To change the Comp control, the USER_KEY2 bit must be set to '1'.
4. If it's not required to change this register, must be set as default.

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Software Reset/Chip ID 1	7:0	SW_RESET_ CHIP_ID[7:0]	0011_0010	A write issues a software reset, and returns all control registers to their default values. A read returns lower bits of the device ID	

Register 00h Software Reset/Chip ID 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Chip ID 2	7:0	CHIP_ID[7:0]	1000_0010	A read returns upper bits of the device ID	

Register 01h Chip ID 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Chip Rev	3:0	CHIP_REV[3:0]	0000	A read returns the device revision number	

Register 02h Chip Rev

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) Setup Reg 1	4	CHZPD	0	ADC powerdown control for channel 3 (related PGA and digits goes power down) 0 = normal operation 1 = power down	
	3	CHYPD	0	ADC powerdown control for channel 2 (related PGA and digits goes power down) 0 = normal operation 1 = power down	
	2	CHXPD	0	ADC powerdown control for channel 1 (related PGA and digits goes power down) 0 = normal operation 1 = power down	
	1	PDMD	0	power down mode 0 : standby 1 : sleep	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	PD	0	power down 0 : normal operation 1 : power down	

Register 03h Setup Reg 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) Setup Reg 2	7	VRLC_TOP_ SEL	0	selects output range of VRLCDAC 0 = AVDD 1 = 1.6V	
	6	PGAFS	0	control PGA input polarity 0 = negative 1 = positive	
	5	ADCFS	0	control ADC full scale range 0 = 1.2V 1 = 1.8V	
	4	TGDIVMD	0	enable TG clock divide mode 0 = normal (TG clock rate = MCLK clock rate) 1 = enable TG clock divide mode (TG clock rate is half of MCLK clock rate)	
	1	CLPMD	0	select clamp mode 0 = line clamp 1 = bit clamp	
	0	CDS	0	CDS mode control 0 = S/H mode 1 = CDS mode	

Register 04h Setup Reg 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) Setup Reg 3	4	SF_BYPLS	1	bypass level shift of VRLC source follower 0 = use level shifter 1 = bypass level shifter	
	3:2	PT_SF[1:0]	11	source follower power trim 00 = 1mA 01 = 2mA 10 = 3mA 11 = 4mA	
	1	SF_INP	0	control source follower on signal inputs INP* 0 = disabled 1 = enabled	
	0	SF_VRLC	0	control source follower on VRLC 0 = disabled 1 = enabled	

Register 05h Setup Reg 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) VRLC control	7	VRLCEN	1	enable for VRLC DAC 0 = disabled 1 = enabled	
	6:5	VRLC_ISEL[1:0]	00	selects output current capability 00 = Up to 2mA 01 = Up to 3mA 10 = Up to 4mA 11 = reserved (Up to 2mA)	
	4:0	VRLC_VSEL[4:0]	0_1010	VRLC output voltage setting when VRLC_TOP_SEL=0 (AVDD) 3.3/AVDD * (0.2 + 0.09xVRLC_VSEL[4:0]) when VRLC_TOP_SEL=1 (1.6V) 1.6 - 0.048*(31-VRLC_VSEL[4:0])	

Register 06h VRLC control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R7 (07h) output control	7	OE_OP	0	output enable of dataout (CMOS/LVDS) when HIZCTRL=0 0= Hi-Z 1= enable dataout when HIZCTRL=1 OE_OP state is neglected and enable dataout	
	6	OUTPD	1	control data output 0 = enable data output 1 = mask data output (data out=0)	
	5	CMOSMODE	0	enable CMOS output mode 0 = LVDS output mode based on LVDSMODE[2:0] 1 = CMOS output mode	
	4	OUTSYNC	0	enable synchronous output mode 0 = continuous 1 = synchronized dataout with LineStart signal	
	3	LVDSORDER	0	control LVDS data output order 0 = descending order 1 = ascending order	
	2:0	LVDSMODE [2:0]	000	select LVDS dataoutput format 000 = 10bit 5pair + clk 001 = 10bit 3pair + clk 011 = 12bit 4pair + clk 101 = 16bit 5pair + clk 110 = 16bit 3pair + clk Others = reserved	

Register 07h output control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R8 (08h) LVDS control	6	LVDS_POL	0	invert LVDS outputs polarity 0 = normal	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = inverted	
	5:3	LVDS_AMP[2:0]	110	LVDS amplitude select 000 = 50mV 001 = 100mV 010 = 150mV 011 = 200mV All other codes are Reserved. Note that the default code (110) should not be used.	
	2:0	LVDS_VCM[2:0]	101	LVDS common mode select 000 = 0.70V 001 = 0.80V 010 = 0.90V 011 = 1.00V 100 = 1.15V 101 = 1.25V 110 = 1.35V 111 = 1.45V	

Register 08h LVDS control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R9 (09h) LVDS clock pattern	6:0	LVCKPAT[6:0]	110_0011	LVDS clock pattern (output MSB first)	

Register 09h LVDS clock pattern

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R10 (0Ah) flag control 1	7:4	FLAG_S1[3:0]	0001	output dataflag as S1 (valid only LVDS mode) 0000 = always low 0001 = start flag 0010 = reserved 0011 = reserved 0100 = reserved 0101 = channel ID[0] 0110 = channel ID[1] 0111 = channel ID[2] 1000 = channel ID[3] 1001 = reserved 1010 = reserved 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = always high	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	FLAG_S0[3:0]	0000	output dataflag as S0 (valid only LVDS mode) 0000 = always low 0001 = start flag 0010 = reserved 0011 = reserved 0100 = reserved 0101 = channel ID[0] 0110 = channel ID[1] 0111 = channel ID[2] 1000 = channel ID[3] 1001 = reserved 1010 = reserved 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = always high	

Register 0Ah flag control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R11 (0Bh) flag control 2	7:4	FLAG_S3[3:0]	0000	output dataflag as S3 (valid only LVDS mode) 0000 = always low 0001 = start flag 0010 = reserved 0011 = reserved 0100 = reserved 0101 = channel ID[0] 0110 = channel ID[1] 0111 = channel ID[2] 1000 = channel ID[3] 1001 = reserved 1010 = reserved 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = always high	
	3:0	FLAG_S2[3:0]	0000	output dataflag as S2 (valid only LVDS mode) 0000 = always low 0001 = start flag 0010 = reserved 0011 = reserved 0100 = reserved 0101 = channel ID[0] 0110 = channel ID[1] 0111 = channel ID[2] 1000 = channel ID[3] 1001 = reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1010 = reserved 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = always high	

Register 0Bh flag control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12 (0Ch) flag control 3	3:0	FLAG_S4[3:0]	0000	output dataflag as S4 (valid only LVDS mode) 0000 = always low 0001 = start flag 0010 = reserved 0011 = reserved 0100 = reserved 0101 = channel ID[0] 0110 = channel ID[1] 0111 = channel ID[2] 1000 = channel ID[3] 1001 = reserved 1010 = reserved 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = always high	

Register 0Ch flag control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R13 (0Dh) CMOS drivability control 1	3	DRV_CTRL	0	CMOS output drivability control mode 0 = OP_DRV controls drivability of all output pins OP* 1 = OP_DRV is invalid, and OP*_DRV control drivability of output pin OP*	
	2:0	OP_DRV[2:0]	000	CMOS output drivability control when DRV_CTRL=0 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 0Dh CMOS drivability control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R14 (0Eh)	6:4	OP1_DRV[2:0]	000	CMOS output (OP2) drivability	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
CMOS drivability control 2				000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	
	2:0	OP0_DRV[2:0]	000	CMOS output (OP1) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 0Eh CMOS drivability control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R15 (0Fh) CMOS drivability control 3	6:4	OP3_DRV[2:0]	000	CMOS output (OP4) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	
	2:0	OP2_DRV[2:0]	000	CMOS output (OP3) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 0Fh CMOS drivability control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16 (10h) CMOS drivability control 4	6:4	OP5_DRV[2:0]	000	CMOS output (OP6) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	OP4_DRV[2:0]	000	CMOS output (OP5) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 10h CMOS drivability control 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R17 (11h) CMOS drivability control 5	6:4	OP7_DRV[2:0]	000	CMOS output (OP8) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	
	2:0	OP6_DRV[2:0]	000	CMOS output (OP7) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 11h CMOS drivability control 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R18 (12h) CMOS drivability control 6	6:4	OP9_DRV[2:0]	000	CMOS output (OP10) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	
	2:0	OP8_DRV[2:0]	000	CMOS output (OP9) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 12h CMOS drivability control 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R19 (13h) CMOS drivability control 7	6:4	OC2_DRV[2:0]	000	CMOS output (OC2) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	
	2:0	OC1_DRV[2:0]	000	CMOS output (OC1) drivability 000: Hi-Z 001: 1mA 010: 2mA 011: 3mA 100: 4mA 101: 5mA 110/111: 6mA	

Register 13h CMOS drivability control 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R20 (14h) PG config	7	PGMARCH	0	pattern generator marching mode enable 0 = controlled by PGPAT 1 = marching pattern	
	6:5	PGPAT[1:0]	00	select pattern generator output 00 = fixed value 01 = vertical ramp 10 = horizontal ramp 11 = patch	
	4	PGINV	0	invert pattern generator output 0 = normal 1 = invert	
	3	SEL_PGZ	0	select output of pattern generator (IN3) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs	
	2	SEL_PGY	0	select output of pattern generator (IN2) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs	
	1	SEL_PGX	0	select output of pattern generator (IN1) 0 = normal ouput 1 = output generated digital pattern instead of ADC outputs	
	0	PGEN	0	enable pattern generator 0 = disable 1 = enable	

Register 14h PG config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R21 (15h) PGCODE	7:0	PGLEVEL[7:0]	0000_0000	parameter of pattern generator	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
LSB					

Register 15h PGCODE LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R22 (16h) PGCODE MSB	7:0	PGLEVEL[7:0]	0000_0000	parameter of pattern generator	

Register 16h PGCODE MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R23 (17h) PG width 1	7:0	PGWIDTH1[7:0]	0000_0000	parameter of pattern generator	

Register 17h PG width 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) PG width 2	7:0	PGWIDTH2[7:0]	0000_0000	parameter of pattern generator	

Register 18h PG width 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) clock monitor	2:0	MONCLK[2:0]	000	select monitor output 0xx = Low (monitor disabled) 100 = RSMP 101 = VSMP 110 = ACLK 111 = OCLK	

Register 19h clock monitor

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) PLL control 1	2	PLL_LPF_RST	0	Reset Loop Filter. 0 = normal 1 = reset	
	1	PLL_CP_PD	0	power down Charge Pump. 0 = normal 1 = power down	
	0	PLL_VCO_PD	0	power down VCO 0 = normal 1 = power down	

Register 1Ah PLL control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) PLL control 2	6	PLL_LPF_SEL	0	Control Loop Filter to improve the performance. Note: these settings are applicable for the specific conditions. 0 = normal filter 1 = larger resistor to improve PLL cutoff freq (for SSC)	
	3:2	PLL_PFD_CTRL [1:0]	10	Control reset delay to improve PFD sensitivity. 00 = 1ns delay 01 = 2.2ns delay 10 = 3.4ns delay (default) 11 = 5.8ns delay	
	1:0	PLL_CP_GAIN [1:0]	01	Control Charge Pump current. 00 = 0.5uA 01 = 1uA (default) 10 = 2uA 11 = 4uA	

Register 1Bh PLL control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) PLL divider control 1	6:4	PLL_EXDIV_ SEL[2:0]	001	Select EX DIV ratio. Need to set according to input frequency. See details in "PLL DLL Setup" 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 to 111 = reserved.	
	3:0	PLL_FBDIV_ SEL[3:0]	0001	Select FB DIV ratio. (ReadOnly) 0000 = 1 0001 = 2 0010 = 3 0011 = 4 0100 = 6 0101 = 8 0110 = 9 0111 = 12 1000 = 18 1001 to 1111 = reserved.	

Register 1Ch PLL divider control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) PLL divider control 2	5:4	PLL_POSTDIV2 _SEL[1:0]	01	Select POST DIV2 ratio. (Read Only) 00 = 1 01 = 2 10 = 4 11 = 6	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	PLL_POSTDIV1 _SEL[3:0]	0001	Select POST DIV1 ratio. (Read Only) 0000 = 1 0001 = 2 0010 = 3 0011 = 4 0100 = 6 0101 = 8 0110 = 9 0111 = 12 1000 = 18 1001 to 1111 = reserved.	

Register 1Dh PLL divider control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R35 (23h) Cycle mode control	3:2	INTM[1:0]	00	When LINEBYLINE=1, controls the GAIN and DAC mux selector when ACYC=0 00 = IN1 01 = IN2 10 = IN3 11 = reserved	
	1	ACYC	0	when LINEBYLINE=1, determines the function of the MUX control 0 = decided by INTM register 1= auto-cycling enabled	
	0	LINEBYLINE	0	select line by line operation 0=normal operation 1=Line by Line operation	

Register 23h cycle mode control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R38 (26h) DAC IN1	7:0	DACIN1[7:0]	1000_0000	DACIN1offset value 250 * (DACIN1[7:0] -127.5) / 127.5 [mV]	

Register 26h DAC IN1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R41 (29h) DAC IN2	7:0	DACIN2[7:0]	1000_0000	DACIN2 offset value 250 * (DACIN2[7:0] -127.5) / 127.5 [mV]	

Register 29h DAC IN2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R44 (2Ch) DAC IN3	7:0	DACIN3[7:0]	1000_0000	DACIN3offset value 250 * (DACIN3[7:0] -127.5) / 127.5 [mV]	

Register 2Ch DAC IN3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R47 (2Fh) AGAIN IN1	4:0	AGAININ1[4:0]	0_0001	PGA IN1 gain code gain(V/V) = 0.6 + 0.3*AGAIN*[4:0]	

Register 2Fh AGAIN IN1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R50 (32h) AGAIN IN2	4:0	AGAININ2[4:0]	0_0001	PGA IN2 gain code gain(V/V) = 0.6 + 0.3*AGAIN*[4:0]	

Register 32h AGAIN IN2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R53 (35h) AGAIN IN3	4:0	AGAININ3[4:0]	0_0001	PGA IN3 gain code gain(V/V) = 0.6 + 0.3*AGAIN*[4:0]	

Register 35h AGAIN IN3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R58 (3Ah) DGAIN IN1 LSB	7:4	DGAININ1[3:0]	0000	lower bits of digital gain IN1 1111_1111_1111_1111 = 1.99[V/V] ... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 3Ah DGAIN IN1 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R59 (3Bh) DGAIN IN1 MSB	7:0	DGAININ1[11:4]	1000_0000	upper bits of digital gain IN1 1111_1111_1111_1111 = 1.99[V/V] ... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 3Bh DGAIN IN1 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R64 (40h) DGAIN IN2	7:4	DGAININ2[3:0]	0000	lower bits of digital gain IN2 1111_1111_1111_1111 = 1.99[V/V]	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
LSB				... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 40h DGAIN IN2 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R65 (41h) DGAIN IN2 MSB	7:0	DGAININ2[11:4]	1000_0000	upper bits of digital gain IN2 1111_1111_1111_1111 = 1.99[V/V] ... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 41h DGAIN IN2 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R70 (46h) DGAIN IN3 LSB	7:4	DGAININ3[3:0]	0000	lower bits of digital gain IN3 1111_1111_1111_1111 = 1.99[V/V] ... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 46h DGAIN IN3 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R71 (47h) DGAIN IN3 MSB	7:0	DGAININ3[11:4]	1000_0000	upper bits of digital gain IN3 1111_1111_1111_1111 = 1.99[V/V] ... 1000_0000_0000_0000 = 1.0[V/V] ... 0100_0000_0000_0000 = 0.5[V/V] 0011_1111_1111_1111 = reserved … 0000_0000_0000_0000 = reserved	

Register 47h DGAIN IN3 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R74 (4Ah) BLC IN1 target	7:0	TARGETIN1[7:0]	0000_0000	target black level for IN1	

Register 4Ah BLC IN1 target

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R77 (4Dh) BLC IN2 target	7:0	TARGETIN2[7:0]	0000_0000	target black level for IN2	

Register 4Dh BLC IN2 target

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R80 (50h) BLC IN3 target	7:0	TARGETIN3[7:0]	0000_0000	target black level for IN3	

Register 50h BLC IN3 target

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R81 (51h) BLC control 1	7	FRAME_SEQ	0	control frame sequence mode 0 = line by line 1 = frame sequence mode	
	6	FA_EVERYLINE	0	control fine adjustment 0 = Fine adjust only used on the 1st line of a frame 1 = Fine adjust used on every line of a frame	
	5	FA_ACCUM	0	makes the fine adjust calibration accumulate a result over multiple lines 0 = not accumulate 1 = accumulate	
	4	FA_EN	0	enables the fine adjust operation 0 = disable 1 = enable	
	3	CA_EVERYLINE	0	control coarse ajustment 0 = Coarse adjust only used on the 1st line of a frame 1 = Coarse adjust used on every line of a frame	
	2:0	CADUR[2:0]	000	controls the number of coarse adjust iterations to be perfomed 000 = disable 001 = 1time 010 = 2time 011 = 3time … 111 = 7time	

Register 51h BLC control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R82 (52h) BLC control 2	1	SEQ_START	0	register flag to indicate that the next start-of-line indicator is the first line of the first frame in a frame-sequence. This register is automatically set to zero at the end of the BLC operation on the first line 0 = no effect 1 = first frame of frame-sequence mode	
	0	FRAME_START	0	Register flag to indicate that the next start-of-line indicator is the first line in a frame. This register is automatically set to zero at the end of the BLC operation on the first line 0 = no effect 1 = start of line	

Register 52h BLC control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R83 (53h) BLC control 3	7:0	BPIX_AVAIL[7:0]	0000_0000	LSBs of the number of black-pixels available over which to perform the coarse and/or fine adjust calibration 00_0000_0000 = no pixel available 11_1111_1111 = 1023 pixels	

Register 53h BLC control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R84 (54h) BLC control 4	1:0	BPIX_AVAIL[9:8]	00	MSBs of the number of black-pixels available over which to perform the coarse and/or fine adjust calibration 00_0000_0000 = no pixel available 11_1111_1111 = 1023 pixels	

Register 54h BLC control 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R85 (55h) BLC control 5	7:0	LINE_DEL[7:0]	0000_0000	LSBs of the number of lines from the start of a frame to delay the start of BLC operation 0_0000_0000 = no delay 1_1111_1111 = 511 line	

Register 55h BLC control 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R86 (56h) BLC control 6	0	LINE_DEL[8]	0	MSBs of the number of lines from the start of aframe to delay the start of BLC operation 0_0000_0000 = no delay 1_1111_1111 = 511 line	

Register 56h BLC control 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R87 (57h)	7:4	AGCAVE[3:0]	0000	averaging factor before peak detection	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
AGC config 1				0000 = no average 0001 = 2 0010 = 4 0011 = 8 … 1010 = 1024 1011 = reserved 1100 = reserved 1101 = reserved 1110 = reserved 1111 = reserved	
	2	AGC_ERRFLAG	0	AGC error flag 0 = no error detected 1 = AGC finish with error	
	1	AGC_ENDFLAG	0	AGC end flag 0 = not end or not run 1 = AGC sequence was done	
	0	AGC_EN	0	AGC enable 0 = disable 1 = enable	

Register 57h AGC config 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R88 (58h) AGC config 2	6:4	AGC_DPD[2:0]	000	the number of peak detection iterations to calculate digital gain 000 = no digital gain adjustment 001 = 1line 010 = 2line … 111 = 7line	
	2:0	AGC_APD[2:0]	000	the number of peak detection iterations to calculate analogue gain 000 = no analogue gain adjustment 001 = 1line 010 = 2line … 111 = 7line	

Register 58h AGC config 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R93 (5Dh) AGC target IN1 LSB	7:0	AGC_TARGET IN1[7:0]	0000_0000	LSBs of AGC target level for IN1	

Register 5Dh AGC target IN1 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R94 (5Eh)	1:0	AGC_TARGET	00	MSBs of AGC target level for IN1	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
AGC target IN1 MSB		IN1[9:8]			

Register 5Eh AGC target IN1 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R99 (63h) AGC target IN2 LSB	7:0	AGC_TARGET IN2[7:0]	0000_0000	LSBs of AGC target level for IN2	

Register 63h AGC target IN2 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R100 (64h) AGC target IN2 MSB	1:0	AGC_TARGET IN2[9:8]	00	MSBs of AGC target level for IN2	

Register 64h AGC target IN2 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R105 (69h) AGC target IN3 LSB	7:0	AGC_TARGET IN3[7:0]	0000_0000	LSBs of AGC target level for IN3	

Register 69h AGC target IN3 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R106 (6Ah) AGC target IN3 MSB	1:0	AGC_TARGET IN3[9:8]	00	MSBs of AGC target level for IN3	

Register 6Ah AGC target IN3 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R111 (6Fh) AGC peak level IN1 LSB	7:0	PEAK_IN1[7:0]	0000_0000	LSBs of detected peak level of IN1 (Read Only)	

Register 6Fh AGC peak level IN1 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R112 (70h) AGC peak level IN1 MSB	1:0	PEAK_IN1[9:8]	00	MSBs of detected peak level of IN1 (Read Only)	

Register 70h AGC peak level IN1 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R117 (75h) AGC peak level IN2 LSB	7:0	PEAK_IN2[7:0]	0000_0000	LSBs of detected peak level of IN2 (Read Only)	

Register 75h AGC peak level IN2 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R118 (76h) AGC peak level IN2 MSB	1:0	PEAK_IN2[9:8]	00	MSBs of detected peak level of IN2 (Read Only)	

Register 76h AGC peak level IN2 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R123 (7Bh) AGC peak level IN3 LSB	7:0	PEAK_IN3[7:0]	0000_0000	LSBs of detected peak level of IN3 (Read Only)	

Register 7Bh AGC peak level IN3 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R124 (7Ch) AGC peak level IN3 MSB	1:0	PEAK_IN3[9:8]	00	MSBs of detected peak level of IN3 (Read Only)	

Register 7Ch AGC peak level IN3 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R128 (80h) DLL config 1	5:4	DLGAIN[1:0]	01	gain control of DLL delay line Need to set according to input frequency. See details in "PLL DLL Setup"	
	2	DLLRST	0	reset DLL delay line 0 = normal 1= reset DLL	
	1	CKOSTB	0	standby TG clock output 0 = generate TG clock 1 = stop generation of TG clock	
	0	AFECKSTB	0	standby AFE clock (VSMP/RSMP/ADCK) output 0 = generate AFE clock 1 = stop generation of AFE clock	

Register 80h DLL config 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R129 (81h) DLL config 2	5:4	LVDLGAIN[1:0]	01	gain control of LVDS DLL delay line Need to set according to input frequency. See details in "PLL DLL Setup"	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	LVDLLRST	0	reset LVDS DLL delay line 0 = normal 1 = reset LVDS DLL	
	0	LVDLLSTB	0	standby LVDS serializer clock generation 0 = generate LVDS serializer clock 1 = stop generation of LVDS serializer clock	

Register 81h DLL config 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R130 (82h) RSMP rise	5:0	RSMP_RISE [5:0]	01_1100	RSMP rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 82h RSMP rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R131 (83h) RSMP fall	5:0	RSMP_FALL [5:0]	10_0110	RSMP fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 83h RSMP fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R132 (84h) VSMP rise	5:0	VSMP_RISE [5:0]	10_1000	VSMP rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 84h VSMP rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R133 (85h) VSMP fall	5:0	VSMP_FALL [5:0]	00_1000	VSMP fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 85h VSMP fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R134 (86h) TGCKO rise	5:0	TCLKO_RISE [5:0]	11_0111	TCLKO rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 86h TGCKO rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R135 (87h) CLK1 rise	5:0	CLK1_RISE[5:0]	00_1010	CLK1 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 87h CLK1 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R136 (88h) CLK1 fall	5:0	CLK1_FALL[5:0]	01_1001	CLK1 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 88h CLK1 fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R137 (89h) CLK2 rise	5:0	CLK2_RISE[5:0]	01_1001	CLK2 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 89h CLK2 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R138 (8Ah) CLK2fall	5:0	CLK2_FALL[5:0]	10_1000	CLK2 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Ah CLK2fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R139 (8Bh) CLK3 rise	5:0	CLK3_RISE[5:0]	10_1000	CLK3 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Bh CLK3 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R140 (8Ch) CLK3 fall	5:0	CLK3_FALL[5:0]	00_1010	CLK3 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Ch CLK3 fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R141 (8Dh) CLK4 rise	5:0	CLK4_RISE[5:0]	00_0000	CLK4 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Dh CLK4 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R142 (8Eh) CLK4 fall	5:0	CLK4_FALL[5:0]	00_0000	CLK4 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Eh CLK4 fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R143 (8Fh) CLK5 rise	5:0	CLK5_RISE[5:0]	00_1010	CLK5 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 8Fh CLK5 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R144 (90h) CLK5 fall	5:0	CLK5_FALL[5:0]	10_1000	CLK5 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				11_1110 = reserved 11_1111 = reserved	

Register 90h CLK5 fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R145 (91h) CLK6 rise	5:0	CLK6_RISE[5:0]	00_1010	CLK6 rise edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 91h CLK6 rise

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R146 (92h) CLK6 fall	5:0	CLK6_FALL[5:0]	10_1000	CLK6 fall edge 00_0000 = tap0 00_0001 = tap1 … 11_1011 = tap59 11_1100 = reserved 11_1101 = reserved 11_1110 = reserved 11_1111 = reserved	

Register 92h CLK6 fall

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R160 (A0h) TG config 1	7:4	OFFSET[3:0]	0000	pixel counter offset (valid only in slave mode)	
	3	CYCMD	0	cycle mode enable 0 = normal (same operation at everyline) 1 = cycle mode	
	2	POLSYNC	0	polarity of tgync signal 0 = reset pixel counter at positive edge of tgsync 1 = reset pixel counter at negative edge of tgsync	
	1	TGMD	0	TG operation mode 0 = slave 1 = master	
	0	TG_EN	0	TG enable 0 = disable 1 = enable	

Register A0h TG config 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R161 (A1h) TG config 2	7:0	LLENGTH[7:0]	0000_0000	LSBs of LLENGTH[14:0] the number of pixels in a line (valid only in master mode)	

Register A1h TG config 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R162 (A2h) TG config 3	6:0	LLENGTH[14:8]	000_0000	MSBs of LLENGTH the number of pixels in a line (valid only in master mode)	

Register A2h TG config 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R163 (A3h) TG config 4	7:0	FLAGPIX[7:0]	0000_0000	LSBs of FLAGPIX[14:0] flag pixel control pulse flagpix is high when pixel counter equals to flagpix[14:0]	

Register A3h TG config 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R164 (A4h) TG config 5	6:0	FLAGPIX[14:8]	000_0000	MSBs of FLAGPIX[14:0] flag pixel control pulse flagpix is high when pixel counter equals to flagpix[14:0]	

Register A4h TG config 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R165 (A5h) TG config 6	7	OE_CLK8	1	output enable of "CLK8" 0 = Hi-Z 1 = output	
	6	OE_CLK7	1	output enable of "CLK7" 0 = Hi-Z 1 = output	
	5	OE_CLK6	1	output enable of "CLK6" 0 = Hi-Z 1 = output	
	4	OE_CLK5	1	output enable of "CLK5" 0 = Hi-Z 1 = output	
	3	OE_CLK4	1	output enable of "CLK4" 0 = Hi-Z 1 = output	
	2	OE_CLK3	1	output enable of "CLK3" 0 = Hi-Z 1 = output	
	1	OE_CLK2	1	output enable of "CLK2" 0 = Hi-Z	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = output	
	0	OE_CLK1	1	output enable of "CLK1" 0 = Hi-Z 1 = output	

Register A5h TG config 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R166 (A6h) TG config 7	2	OE_CLK11	1	output enable of "CLK11" 0 = Hi-Z 1 = output	
	1	OE_CLK10	1	output enable of "CLK10" 0 = Hi-Z 1 = output	
	0	OE_CLK9	1	output enable of "CLK9" 0 = Hi-Z 1 = output	

Register A6h TG config 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R167 (A7h) TG config 8	7	INV_CLK8	0	invert signal output assigned to CLK8 0 = non-inverted 1 = inverted	
	6	INV_CLK7	0	invert signal output assigned to CLK7 0 = non-inverted 1 = inverted	
	5	INV_CLK6	0	invert signal output assigned to CLK6 0 = non-inverted 1 = inverted	
	4	INV_CLK5	0	invert signal output assigned to CLK5 0 = non-inverted 1 = inverted	
	3	INV_CLK4	0	invert signal output assigned to CLK4 0 = non-inverted 1 = inverted	
	2	INV_CLK3	0	invert signal output assigned to CLK3 0 = non-inverted 1 = inverted	
	1	INV_CLK2	0	invert signal output assigned to CLK2 0 = non-inverted 1 = inverted	
	0	INV_CLK1	0	invert signal output assigned to CLK1 0 = non-inverted 1 = inverted	

Register A7h TG config 8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R168 (A8h) TG config 9	2	INV_CLK11	0	invert signal output assigned to CLK11 0 = non-inverted 1 = inverted	
	1	INV_CLK10	0	invert signal output assigned to CLK10 0 = non-inverted 1 = inverted	
	0	INV_CLK9	0	invert signal output assigned to CLK9 0 = non-inverted 1 = inverted	

Register A8h TG config 9

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R169 (A9h) TG config 10	7	EN_CLK8	0	enable signal output CLK8 0 = disable 1 = enable	
	6	EN_CLK7	0	enable signal output CLK7 0 = disable 1 = enable	
	5	EN_CLK6	0	enable signal output CLK6 0 = disable 1 = enable	
	4	EN_CLK5	0	enable signal output CLK5 0 = disable 1 = enable	
	3	EN_CLK4	0	enable signal output CLK4 0 = disable 1 = enable	
	2	EN_CLK3	0	enable signal output CLK3 0 = disable 1 = enable	
	1	EN_CLK2	0	enable signal output CLK2 0 = disable 1 = enable	
	0	EN_CLK1	0	enable signal output CLK1 0 = disable 1 = enable	

Register A9h TG config 10

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R170 (AAh) TG config 11	2	EN_CLK11	0	enable signal output CLK11 0 = disable 1 = enable	
	1	EN_CLK10	0	enable signal output CLK10 0 = disable 1 = enable	
	0	EN_CLK9	0	enable signal output CLK9 0 = disable 1 = enable	

Register AAh TG config 11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R171 (ABh) TG config 12	7	SEL_CLK3	0	select signal for CLK3 0 = output clock 1 = output pulse (select by SEL_PCK3[2:0])	
	6:4	SEL_PCK3[2:0]	000	select pulse assigned to CLK3 (valid only when SEL_CLK3=1) 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	
	3	SEL_CLK2	0	select signal for CLK2 0 = output clock 1 = output pulse (select by SEL_PCK2[2:0])	
	2:0	SEL_PCK2[2:0]	000	select pulse assigned to CLK2 (valid only when SEL_CLK2=1) 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	

Register ABh TG config 12

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R172 (ACh) TG config 13	7	SEL_CLK5	0	select signal for CLK5 0 = output clock 1 = output pulse (select by SEL_PCK5[2:0])	
	6:4	SEL_PCK5[2:0]	000	select pulse assigned to CLK5 (valid only when SEL_CLK5=1) 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	
	3	SEL_CLK4	0	select signal for CLK4 0 = output clock 1 = output pulse (select by SEL_PCK4[2:0])	
	2:0	SEL_PCK4[2:0]	000	select pulse assigned to CLK4 (valid only when SEL_CLK4=1) 000 = PO0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	

Register ACh TG config 13

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R173 (ADh) TG config 14	6:4	SEL_PCK7[2:0]	000	select pulse assigned to CLK7 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	
	3	SEL_CLK6	0	select signal for CLK6 0 = output clock 1 = output pulse (select by SEL_PCK6[2:0])	
	2:0	SEL_PCK6[2:0]	000	select pulse assigned to CLK6 (valid only when SEL_CLK6=1) 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	

Register ADh TG config 14

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R174 (AEh) TG config 15	6:4	SEL_PCK9[2:0]	000	select pulse assigned to CLK9 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	
	2:0	SEL_PCK8[2:0]	000	select pulse assigned to CLK8 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	

Register AEh TG config 15

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R175 (AFh)	6:4	SEL_PCK11[2:0]	000	select pulse assigned to CLK11	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
TG config 16				000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	
	2:0	SEL_PCK10[2:0]	000	select pulse assigned to CLK10 000 = PO0 001 = PO1 010 = PO2 011 = PO3 100 = PO4 101 = PO5 110 = PO6 111 = PO7	

Register AFh TG config 16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R176 (B0h) TG config 17	7:6	DEL_PCK5[1:0]	00	control delay of pulse output assigned to CLK5 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	5:4	DEL_PCK4[1:0]	00	control delay of pulse output assigned to CLK4 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	3:2	DEL_PCK3[1:0]	00	control delay of pulse output assigned to CLK3 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	1:0	DEL_PCK2[1:0]	00	control delay of pulse output assigned to CLK2 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	

Register B0h TG config 17

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R177 (B1h) TG config 18	7:6	DEL_PCK9[1:0]	00	control delay of pulse output assigned to CLK9 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5:4	DEL_PCK8[1:0]	00	control delay of pulse output assigned to CLK8 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	3:2	DEL_PCK7[1:0]	00	control delay of pulse output assigned to CLK7 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	1:0	DEL_PCK6[1:0]	00	control delay of pulse output assigned to CLK6 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	

Register B1h TG config 18

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R178 (B2h) TG config 19	3:2	DEL_PCK11[1:0]	00	control delay of pulse output assigned to CLK11 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	
	1:0	DEL_PCK10[1:0]	00	control delay of pulse output assigned to CLK10 00 = 0nsec 01 = 1nsec 10 = 2nsec 11 = 3nsec	

Register B2h TG config 19

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R179 (B3h) TG config 20	4	INV_M3	0	invert mask pulse "M3" 0 = non-inverted 1 = inverted	
	3	INV_M2	0	invert mask pulse "M2" 0 = non-inverted 1 = inverted	
	2	INV_M1	0	invert mask pulse "M1" 0 = non-inverted 1 = inverted	
	1	INV_T2	0	invert toggle pulse "T2" 0 = non-inverted 1 = inverted	
	0	INV_T1	0	invert toggle pulse "T1" 0 = non-inverted 1 = inverted	

Register B3h TG config 20

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R180 (B4h) TG config 21	3:0	SEL_FLAG[3:0]	0000	select signal to be output as datatrig 0xxx = flagpix 1000 = PO0 1001 = PO1 1010 = PO2 1011 = PO3 1100 = PO4 1101 = PO5 1110 = PO6 1111 = PO7	

Register B4h TG config 21

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R181 (B5h) TG config 22	6:4	CYCPAT_PO1 [2:0]	000	PO1 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	
	2:0	CYCPAT_PO0 [2:0]	000	PO0 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	

Register B5h TG config 22

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R182 (B6h) TG config 23	6:4	CYCPAT_PO3 [2:0]	000	PO3 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	
	2:0	CYCPAT_PO2 [2:0]	000	PO2 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	

Register B6h TG config 23

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R183 (B7h) TG config 24	6:4	CYCPAT_PO5 [2:0]	000	PO5 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	
	2:0	CYCPAT_PO4 [2:0]	000	PO4 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	

Register B7h TG config 24

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R184 (B8h) TG config 25	6:4	CYCPAT_PO7 [2:0]	000	PO7 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	
	2:0	CYCPAT_PO6 [2:0]	000	PO6 cycle mode control [0] = pulse enable at cycle-1 [1] = pulse enable at cycle-2 [2] = pulse enable at cycle-3	

Register B8h TG config 25

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R185 (B9h) clamp enable rise LSB	7:0	CLAMP_RISE [7:0]	0000_0000	LSBs of CLAMP_RISE clamp enable pulse rise pixel	

Register B9h clamp enable rise LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R186 (BAh) clamp enable rise MSB	6:0	CLAMP_RISE [14:8]	000_0000	MSBs of CLAMP_RISE clamp enable pulse rise pixel	

Register BAh clamp enable rise MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R187 (BBh) clamp enable fall LSB	7:0	CLAMP_FALL [7:0]	0000_0000	LSBs of CLAMP_FALL clamp enable pulse fall pixel	

Register BBh clamp enable fall LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R188 (BCh) clamp enable fall MSB	6:0	CLAMP_FALL [14:8]	000_0000	MSBs of CLAMP_FALL clamp enable pulse fall pixel	

Register BCh clamp enable fall MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R189 (BDh) OB start LSB	7:0	OB_START[7:0]	0000_0000	LSBs of OB_START optical black caribration start pixel count	

Register BDh OB start LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R190 (BEh) OB start MSB	6:0	OB_START[14:8]	000_0000	MSBs of OB_START optical black caribration start pixel count	

Register BEh OB start MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R191 (BFh) peak_det rise LSB	7:0	PEAKDET_RISE [7:0]	0000_0000	LSBs of PEAKDET_RISE[14:0] peak detection start pixel count	

Register BFh peak_det rise LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R192 (C0h) peak_det rise MSB	6:0	PEAKDET_RISE [14:8]	000_0000	MSBs of PEAKDET_RISE[14:0] peak detection start pixel count	

Register C0h peak_det rise MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R193 (C1h) peak_det fall LSB	7:0	PEAKDET_FALL [7:0]	0000_0000	LSBs of PEAKDET_FALL[14:0] peak detection end pixel count	

Register C1h peak_det fall LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R194 (C2h) peak_det fall MSB	6:0	PEAKDET_FALL [14:8]	000_0000	MSBs of PEAKDET_FALL[14:0] peak detection end pixel count	

Register C2h peak_det fall MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R195 (C3h) Mask pulse 1 rise LSB	7:0	M1_RISE[7:0]	0000_0000	LSBs of M1_RISE[14:0] mask puse "M1" rise pixel count	

Register C3h Mask pulse 1 rise LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R196 (C4h) Mask pulse 1 rise MSB	6:0	M1_RISE[14:8]	000_0000	MSBs of M1_RISE[14:0] mask puse "M1" rise pixel count	

Register C4h Mask pulse 1 rise MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R197 (C5h) Mask pulse 1 fall LSB	7:0	M1_FALL[7:0]	0000_0000	LSBs of M1_FALL[14:0] mask puse "M1" fall pixel count	

Register C5h Mask pulse 1 fall LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R198 (C6h) Mask pulse 1 fall MSB	6:0	M1_FALL[14:8]	000_0000	MSBs of M1_FALL[14:0] mask puse "M1" fall pixel count	

Register C6h Mask pulse 1 fall MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R199 (C7h) Mask pulse 2 rise LSB	7:0	M2_RISE[7:0]	0000_0000	LSBs of M2_RISE[14:0] mask puse "M2" rise pixel count	

Register C7h Mask pulse 2 rise LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R200 (C8h) Mask pulse 2 rise MSB	6:0	M2_RISE[14:8]	000_0000	MSBs of M2_RISE[14:0] mask puse "M2" rise pixel count	

Register C8h Mask pulse 2 rise MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R201 (C9h) Mask pulse 2 fall LSB	7:0	M2_FALL[7:0]	0000_0000	LSBs of M2_FALL[14:0] mask puse "M2" fall pixel count	

Register C9h Mask pulse 2 fall LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R202 (CAh) Mask pulse 2 fall MSB	6:0	M2_FALL[14:8]	000_0000	MSBs of M2_FALL[14:0] mask puse "M2" fall pixel count	

Register CAh Mask pulse 2 fall MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R203 (CBh) Mask pulse 3 rise LSB	7:0	M3_RISE[7:0]	0000_0000	LSBs of M3_RISE mask pulse "M3" rise pixel count	

Register CBh Mask pulse 3 rise LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R204 (CCh) Mask pulse 3 rise MSB	6:0	M3_RISE[14:8]	000_0000	MSBs of M3_RISE mask pulse "M3" rise pixel count	

Register CCh Mask pulse 3 rise MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R205 (CDh) Mask pulse 3 fall LSB	7:0	M3_FALL[7:0]	0000_0000	LSBs of M3_FALL mask pulse "M3" fall pixel count	

Register CDh Mask pulse 3 fall LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R206 (CEh) Mask pulse 3 fall MSB	6:0	M3_FALL[14:8]	000_0000	MSBs of M3_FALL mask pulse "M3" fall pixel count	

Register CEh Mask pulse 3 fall MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R207 (CFh) Toggle point 0 LSB	7:0	TP0[7:0]	0000_0000	pixel count of toggle point "TP0"	

Register CFh Toggle point 0 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R208 (D0h) Toggle point 0 MSB	7	GEN_TP0	0	global enable of toggle point 0 = disable all toggle point 1 = enable toggle point "TP0"	
	6:0	TP0[14:8]	000_0000	pixel count of toggle point "TP0	

Register D0h Toggle point 0 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R209 (D1h) Toggle point 1 LSB	7:0	TP1[7:0]	0000_0000	pixel count of toggle point "TP1"	

Register D1h Toggle point 1 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R210 (D2h) Toggle point 1 MSB	7	EN_TP1	0	enable toggle point "TP1" 0 = disable "TP1" and all subsequent toggle point 1 = enable toggle point "TP1"	
	6:0	TP1[14:8]	000_0000	pixel count of toggle point "TP1"	

Register D2h Toggle point 1 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R211 (D3h) Toggle point 2 LSB	7:0	TP2[7:0]	0000_0000	pixel count of toggle point "TP2"	

Register D3h Toggle point 2 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R212 (D4h) Toggle point 2 MSB	7	EN_TP2	0	enable toggle point "TP2" 0 = disable "TP2" and all subsequent toggle point 1 = enable toggle point "TP2"	
	6:0	TP2[14:8]	000_0000	pixel count of toggle point "TP2"	

Register D4h Toggle point 2 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R213 (D5h) Toggle point 3 LSB	7:0	TP3[7:0]	0000_0000	pixel count of toggle point "TP3"	

Register D5h Toggle point 3 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R214 (D6h) Toggle point 3 MSB	7	EN_TP3	0	enable toggle point "TP3" 0 = disable "TP3" and all subsequent toggle point 1 = enable toggle point "TP3"	
	6:0	TP3[14:8]	000_0000	pixel count of toggle point "TP3"	

Register D6h Toggle point 3 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R215 (D7h) Toggle point 4 LSB	7:0	TP4[7:0]	0000_0000	pixel count of toggle point "TP4"	

Register D7h Toggle point 4 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R216 (D8h) Toggle point 4 MSB	7	EN_TP4	0	enable toggle point "TP4" 0 = disable "TP4" and all subsequent toggle point 1 = enable toggle point "TP4"	
	6:0	TP4[14:8]	000_0000	pixel count of toggle point "TP4"	

Register D8h Toggle point 4 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R217 (D9h) Toggle point 5 LSB	7:0	TP5[7:0]	0000_0000	pixel count of toggle point "TP5"	

Register D9h Toggle point 5 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R218 (DAh) Toggle point 5 MSB	7	EN_TP5	0	enable toggle point "TP5" 0 = disable "TP5" and all subsequent toggle point 1 = enable toggle point "TP5"	
	6:0	TP5[14:8]	000_0000	pixel count of toggle point "TP5"	

Register DAh Toggle point 5 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R219 (DBh) Toggle point 6 LSB	7:0	TP6[7:0]	0000_0000	pixel count of toggle point "TP1"	

Register DBh Toggle point 6 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R220 (DCh) Toggle point 6 MSB	7	EN_TP6	0	enable toggle point "TP6" 0 = disable "TP6" and all subsequent toggle point 1 = enable toggle point "TP6"	
	6:0	TP6[14:8]	000_0000	pixel count of toggle point "TP6"	

Register DCh Toggle point 6 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R221 (DDh) Toggle point 7 LSB	7:0	TP7[7:0]	0000_0000	pixel count of toggle point "TP7"	

Register DDh Toggle point 7 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R222 (DEh) Toggle point 7 MSB	7	EN_TP7	0	enable toggle point "TP7" 0 = disable "TP7" and all subsequent toggle point 1 = enable toggle point "TP7"	
	6:0	TP7[14:8]	000_0000	pixel count of toggle point "TP7"	

Register DEh Toggle point 7 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R223 (DFh)	7:0	TP8[7:0]	0000_0000	pixel count of toggle point "TP8"	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
Toggle point 8 LSB					

Register DFh Toggle point 8 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R224 (E0h) Toggle point 8 MSB	7	EN_TP8	0	enable toggle point "TP8" 0 = disable "TP8" and all subsequent toggle point 1 = enable toggle point "TP8"	
	6:0	TP8[14:8]	000_0000	pixel count of toggle point "TP8"	

Register E0h Toggle point 8 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R225 (E1h) Toggle point 9 LSB	7:0	TP9[7:0]	0000_0000	pixel count of toggle point "TP9"	

Register E1h Toggle point 9 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R226 (E2h) Toggle point 9 MSB	7	EN_TP9	0	enable toggle point "TP9" 0 = disable "TP9" and all subsequent toggle point 1 = enable toggle point "TP9"	
	6:0	TP9[14:8]	000_0000	pixel count of toggle point "TP9"	

Register E2h Toggle point 9 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R227 (E3h) Toggle point 10 LSB	7:0	TP10[7:0]	0000_0000	pixel count of toggle point "TP10"	

Register E3h Toggle point 10 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R228 (E4h) Toggle point 10 MSB	7	EN_TP10	0	enable toggle point "TP10" 0 = disable "TP10" and all subsequent toggle point 1 = enable toggle point "TP10"	
	6:0	TP10[14:8]	000_0000	pixel count of toggle point "TP10"	

Register E4h Toggle point 10 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R229 (E5h) Toggle point	7:0	TP11[7:0]	0000_0000	pixel count of toggle point "TP11"	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
11 LSB					

Register E5h Toggle point 11 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R230 (E6h) Toggle point 11 MSB	7	EN_TP11	0	enable toggle point "TP11" 0 = disable "TP11" and all subsequent toggle point 1 = enable toggle point "TP11"	
	6:0	TP11[14:8]	000_0000	pixel count of toggle point "TP11"	

Register E6h Toggle point 11 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R231 (E7h) Toggle point 12 LSB	7:0	TP12[7:0]	0000_0000	pixel count of toggle point "TP12"	

Register E7h Toggle point 12 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R232 (E8h) Toggle point 12 MSB	7	EN_TP12	0	enable toggle point "TP12" 0 = disable "TP12" and all subsequent toggle point 1 = enable toggle point "TP12"	
	6:0	TP12[14:8]	000_0000	pixel count of toggle point "TP12"	

Register E8h Toggle point 12 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R233 (E9h) Toggle point 13 LSB	7:0	TP13[7:0]	0000_0000	pixel count of toggle point "TP13"	

Register E9h Toggle point 13 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R234 (EAh) Toggle point 13 MSB	7	EN_TP13	0	enable toggle point "TP13" 0 = disable "TP13" and all subsequent toggle point 1 = enable toggle point "TP13"	
	6:0	TP13[14:8]	000_0000	pixel count of toggle point "TP13"	

Register EAh Toggle point 13 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R235 (EBh) Toggle point 14 LSB	7:0	TP14[7:0]	0000_0000	pixel count of toggle point "TP14"	

Register EBh Toggle point 14 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R236 (ECh) Toggle point 14 MSB	7	EN_TP14	0	enable toggle point "TP14" 0 = disable "TP14" and all subsequent toggle point 1 = enable toggle point "TP14"	
	6:0	TP14[14:8]	000_0000	pixel count of toggle point "TP14"	

Register ECh Toggle point 14 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R237 (EDh) Toggle point 15 LSB	7:0	TP15[7:0]	0000_0000	pixel count of toggle point "TP15"	

Register EDh Toggle point 15 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R238 (EEh) Toggle point 15 MSB	7	EN_TP15	0	enable toggle point "TP15" 0 = disable "TP15" and all subsequent toggle point 1 = enable toggle point "TP15"	
	6:0	TP15[14:8]	000_0000	pixel count of toggle point "TP15"	

Register EEh Toggle point 15 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R239 (EFh) Toggle point 16 LSB	7:0	TP16[7:0]	0000_0000	pixel count of toggle point "TP16"	

Register EFh Toggle point 16 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R240 (F0h) Toggle point 16 MSB	7	EN_TP16	0	enable toggle point "TP16" 0 = disable "TP16" and all subsequent toggle point 1 = enable toggle point "TP16"	
	6:0	TP16[14:8]	000_0000	pixel count of toggle point "TP16"	

Register F0h Toggle point 16 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R241 (F1h) Toggle point 17 LSB	7:0	TP17[7:0]	0000_0000	pixel count of toggle point "TP17"	

Register F1h Toggle point 17 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R242 (F2h) Toggle point 17 MSB	7	EN_TP17	0	enable toggle point "TP17" 0 = disable "TP17" and all subsequent toggle point 1 = enable toggle point "TP17"	
	6:0	TP17[14:8]	000_0000	pixel count of toggle point "TP17"	

Register F2h Toggle point 17 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R243 (F3h) Toggle point 18 LSB	7:0	TP18[7:0]	0000_0000	pixel count of toggle point "TP18"	

Register F3h Toggle point 18 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R244 (F4h) Toggle point 18 MSB	7	EN_TP18	0	enable toggle point "TP18" 0 = disable "TP18" and all subsequent toggle point 1 = enable toggle point "TP18"	
	6:0	TP18[14:8]	000_0000	pixel count of toggle point "TP18"	

Register F4h Toggle point 18 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R245 (F5h) Toggle point 19 LSB	7:0	TP19[7:0]	0000_0000	pixel count of toggle point "TP19"	

Register F5h Toggle point 19 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R246 (F6h) Toggle point 19 MSB	7	EN_TP19	0	enable toggle point "TP19" 0 = disable "TP19" and all subsequent toggle point 1 = enable toggle point "TP19"	
	6:0	TP19[14:8]	000_0000	pixel count of toggle point "TP19"	

Register F6h Toggle point 19 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R247 (F7h) Toggle point 20 LSB	7:0	TP20[7:0]	0000_0000	pixel count of toggle point "TP20"	

Register F7h Toggle point 20 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R248 (F8h)	7	EN_TP20	0	enable toggle point "TP20"	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
Toggle point 20 MSB				0 = disable "TP20" and all subsequent toggle point 1 = enable toggle point "TP20"	
	6:0	TP20[14:8]	000_0000	pixel count of toggle point "TP20"	

Register F8h Toggle point 20 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R249 (F9h) Toggle point 21 LSB	7:0	TP21[7:0]	0000_0000	pixel count of toggle point "TP21"	

Register F9h Toggle point 21 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R250 (FAh) Toggle point 21 MSB	7	EN_TP21	0	enable toggle point "TP21" 0 = disable "TP21" and all subsequent toggle point 1 = enable toggle point "TP21"	
	6:0	TP21[14:8]	000_0000	pixel count of toggle point "TP21"	

Register FAh Toggle point 21 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R251 (FBh) Toggle point 22 LSB	7:0	TP22[7:0]	0000_0000	pixel count of toggle point "TP22"	

Register FBh Toggle point 22 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R252 (FCh) Toggle point 22 MSB	7	EN_TP22	0	enable toggle point "TP22" 0 = disable "TP22" and all subsequent toggle point 1 = enable toggle point "TP22"	
	6:0	TP22[14:8]	000_0000	pixel count of toggle point "TP22"	

Register FCh Toggle point 22 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R253 (FDh) Toggle point 23 LSB	7:0	TP23[7:0]	0000_0000	pixel count of toggle point "TP23"	

Register FDh Toggle point 23 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R254 (FEh) Toggle point	7	EN_TP23	0	enable toggle point "TP23" 0 = disable "TP23" and all subsequent toggle point	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
23 MSB				1 = enable toggle point "TP23"	
	6:0	TP23[14:8]	000_0000	pixel count of toggle point "TP23"	

Register FEh Toggle point 23 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R255 (FFh) Toggle point 24 LSB	7:0	TP24[7:0]	0000_0000	pixel count of toggle point "TP24"	

Register FFh Toggle point 24 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R256 (0100h) Toggle point 24 MSB	7	EN_TP24	0	enable toggle point "TP24" 0 = disable "TP24" and all subsequent toggle point 1 = enable toggle point "TP24"	
	6:0	TP24[14:8]	000_0000	pixel count of toggle point "TP24"	

Register 0100h Toggle point 24 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R257 (0101h) Toggle point 25 LSB	7:0	TP25[7:0]	0000_0000	pixel count of toggle point "TP25"	

Register 0101h Toggle point 25 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R258 (0102h) Toggle point 25 MSB	7	EN_TP25	0	enable toggle point "TP25" 0 = disable "TP25" and all subsequent toggle point 1 = enable toggle point "TP25"	
	6:0	TP25[14:8]	000_0000	pixel count of toggle point "TP25"	

Register 0102h Toggle point 25 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R259 (0103h) Toggle point 26 LSB	7:0	TP26[7:0]	0000_0000	pixel count of toggle point "TP26"	

Register 0103h Toggle point 26 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R260 (0104h) Toggle point 26 MSB	7	EN_TP26	0	enable toggle point "TP26" 0 = disable "TP26" and all subsequent toggle point 1 = enable toggle point "TP26"	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	TP26[14:8]	000_0000	pixel count of toggle point "TP26"	

Register 0104h Toggle point 26 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R261 (0105h) Toggle point 27 LSB	7:0	TP27[7:0]	0000_0000	pixel count of toggle point "TP27"	

Register 0105h Toggle point 27 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R262 (0106h) Toggle point 27 MSB	7	EN_TP27	0	enable toggle point "TP27" 0 = disable "TP27" and all subsequent toggle point 1 = enable toggle point "TP27"	
	6:0	TP27[14:8]	000_0000	pixel count of toggle point "TP27"	

Register 0106h Toggle point 27 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R263 (0107h) Toggle point 28 LSB	7:0	TP28[7:0]	0000_0000	pixel count of toggle point "TP28"	

Register 0107h Toggle point 28 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R264 (0108h) Toggle point 28 MSB	7	EN_TP28	0	enable toggle point "TP28" 0 = disable "TP28" and all subsequent toggle point 1 = enable toggle point "TP28"	
	6:0	TP28[14:8]	000_0000	pixel count of toggle point "TP28"	

Register 0108h Toggle point 28 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R265 (0109h) Toggle point 29 LSB	7:0	TP29[7:0]	0000_0000	pixel count of toggle point "TP29"	

Register 0109h Toggle point 29 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R266 (010Ah) Toggle point 29 MSB	7	EN_TP29	0	enable toggle point "TP29" 0 = disable "TP29" and all subsequent toggle point 1 = enable toggle point "TP29"	
	6:0	TP29[14:8]	000_0000	pixel count of toggle point "TP29"	

Register 010Ah Toggle point 29 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R267 (010Bh) Toggle point 30 LSB	7:0	TP30[7:0]	0000_0000	pixel count of toggle point "TP30"	

Register 010Bh Toggle point 30 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R268 (010Ch) Toggle point 30 MSB	7	EN_TP30	0	enable toggle point "TP30" 0 = disable "TP30" and all subsequent toggle point 1 = enable toggle point "TP30"	
	6:0	TP30[14:8]	000_0000	pixel count of toggle point "TP30"	

Register 010Ch Toggle point 30 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R269 (010Dh) Toggle point 31 LSB	7:0	TP31[7:0]	0000_0000	pixel count of toggle point "TP31"	

Register 010Dh Toggle point 31 LSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R270 (010Eh) Toggle point 31 MSB	7	EN_TP31	0	enable toggle point "TP31" 0 = disable "TP31" 1 = enable toggle point "TP31"	
	6:0	TP31[14:8]	000_0000	pixel count of toggle point "TP31"	

Register 010Eh Toggle point 31 MSB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R271 (010Fh) Polarity setting of T1 1	7	POL7_T1	1	logic level of T1 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_T1	1	logic level of T1 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_T1	1	logic level of T1 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_T1	1	logic level of T1 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_T1	1	logic level of T1 pulse at toggle point TP3 0 = low at TP3	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP3	
	2	POL2_T1	1	logic level of T1 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_T1	1	logic level of T1 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_T1	1	logic level of T1 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 010Fh Polarity setting of T1 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R272 (0110h) Polarity setting of T1 2	7	POL15_T1	1	logic level of T1 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_T1	1	logic level of T1 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_T1	1	logic level of T1 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_T1	1	logic level of T1 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_T1	1	logic level of T1 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_T1	1	logic level of T1 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_T1	1	logic level of T1 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_T1	1	logic level of T1 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0110h Polarity setting of T1 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R273 (0111h) Polarity setting of T1 3	7	POL23_T1	1	logic level of T1 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_T1	1	logic level of T1 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_T1	1	logic level of T1 pulse at toggle point TP21 0 = low at TP21	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP21	
	4	POL20_T1	1	logic level of T1 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_T1	1	logic level of T1 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_T1	1	logic level of T1 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_T1	1	logic level of T1 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_T1	1	logic level of T1 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0111h Polarity setting of T1 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R274 (0112h) Polarity setting of T1 4	7	POL31_T1	1	logic level of T1 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_T1	1	logic level of T1 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_T1	1	logic level of T1 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_T1	1	logic level of T1 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_T1	1	logic level of T1 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_T1	1	logic level of T1 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_T1	1	logic level of T1 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_T1	1	logic level of T1 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 0112h Polarity setting of T1 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R275 (0113h) Polarity	7	POL7_T2	1	logic level of T2 pulse at toggle point TP7 0 = low at TP7	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
setting of T2 1				1 = high at TP7	
	6	POL6_T2	1	logic level of T2 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_T2	1	logic level of T2 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_T2	1	logic level of T2 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_T2	1	logic level of T2 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_T2	1	logic level of T2 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_T2	1	logic level of T2 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_T2	1	logic level of T2 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 0113h Polarity setting of T2 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R276 (0114h) Polarity setting of T2 2	7	POL15_T2	1	logic level of T2 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_T2	1	logic level of T2 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_T2	1	logic level of T2 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_T2	1	logic level of T2 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_T2	1	logic level of T2 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_T2	1	logic level of T2 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_T2	1	logic level of T2 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_T2	1	logic level of T2 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0114h Polarity setting of T2 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R277 (0115h) Polarity setting of T2 3	7	POL23_T2	1	logic level of T2 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_T2	1	logic level of T2 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_T2	1	logic level of T2 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_T2	1	logic level of T2 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_T2	1	logic level of T2 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_T2	1	logic level of T2 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_T2	1	logic level of T2 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_T2	1	logic level of T2 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0115h Polarity setting of T2 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R278 (0116h) Polarity setting of T2 4	7	POL31_T2	1	logic level of T2 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_T2	1	logic level of T2 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_T2	1	logic level of T2 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_T2	1	logic level of T2 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_T2	1	logic level of T2 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_T2	1	logic level of T2 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_T2	1	logic level of T2 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_T2	1	logic level of T2 pulse at toggle point TP24	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = low at TP24 1 = high at TP24	

Register 0116h Polarity setting of T2 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R279 (0117h) Polarity setting of P0 1	7	POL7_PO0	0	logic level of PO0 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO0	0	logic level of PO0 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO0	0	logic level of PO0 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO0	0	logic level of PO0 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO0	0	logic level of PO0 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO0	0	logic level of PO0 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO0	0	logic level of PO0 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO0	0	logic level of PO0 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 0117h Polarity setting of P0 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R280 (0118h) Polarity setting of P0 2	7	POL15_PO0	0	logic level of PO0 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO0	0	logic level of PO0 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO0	0	logic level of PO0 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO0	0	logic level of PO0 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO0	0	logic level of PO0 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO0	0	logic level of PO0 pulse at toggle point TP10	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = low at TP10 1 = high at TP10	
	1	POL9_PO0	0	logic level of PO0 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO0	0	logic level of PO0 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0118h Polarity setting of P0 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R281 (0119h) Polarity setting of P0 3	7	POL23_PO0	0	logic level of PO0 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO0	0	logic level of PO0 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO0	0	logic level of PO0 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO0	0	logic level of PO0 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO0	0	logic level of PO0 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO0	0	logic level of PO0 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO0	0	logic level of PO0 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO0	0	logic level of PO0 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0119h Polarity setting of P0 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R282 (011Ah) Polarity setting of P0 4	7	POL31_PO0	0	logic level of PO0 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO0	0	logic level of PO0 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO0	0	logic level of PO0 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO0	0	logic level of PO0 pulse at toggle point TP28	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = low at TP28 1 = high at TP28	
	3	POL27_PO0	0	logic level of PO0 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO0	0	logic level of PO0 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO0	0	logic level of PO0 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO0	0	logic level of PO0 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 011Ah Polarity setting of P0 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R283 (011Bh) Polarity setting of P1 1	7	POL7_PO1	0	logic level of PO1 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO1	0	logic level of PO1 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO1	0	logic level of PO1 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO1	0	logic level of PO1 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO1	0	logic level of PO1 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO1	0	logic level of PO1 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO1	0	logic level of PO1 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO1	0	logic level of PO1 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 011Bh Polarity setting of P1 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R284 (011Ch) Polarity setting of	7	POL15_PO1	0	logic level of PO1 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO1	0	logic level of PO1 pulse at toggle point TP14	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
P1 2				0 = low at TP14 1 = high at TP14	
	5	POL13_PO1	0	logic level of PO1 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO1	0	logic level of PO1 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO1	0	logic level of PO1 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO1	0	logic level of PO1 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO1	0	logic level of PO1 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO1	0	logic level of PO1 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 011Ch Polarity setting of P1 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R285 (011Dh) Polarity setting of P1 3	7	POL23_PO1	0	logic level of PO1 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO1	0	logic level of PO1 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO1	0	logic level of PO1 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO1	0	logic level of PO1 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO1	0	logic level of PO1 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO1	0	logic level of PO1 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO1	0	logic level of PO1 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO1	0	logic level of PO1 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 011Dh Polarity setting of P1 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R286 (011Eh) Polarity setting of P1 4	7	POL31_PO1	0	logic level of PO1 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO1	0	logic level of PO1 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO1	0	logic level of PO1 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO1	0	logic level of PO1 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO1	0	logic level of PO1 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO1	0	logic level of PO1 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO1	0	logic level of PO1 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO1	0	logic level of PO1 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 011Eh Polarity setting of P1 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R287 (011Fh) Polarity setting of P2 1	7	POL7_PO2	0	logic level of PO2 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO2	0	logic level of PO2 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO2	0	logic level of PO2 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO2	0	logic level of PO2 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO2	0	logic level of PO2 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO2	0	logic level of PO2 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO2	0	logic level of PO2 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO2	0	logic level of PO2 pulse at toggle point TP0 0 = low at TP0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP0	

Register 011Fh Polarity setting of P2 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R288 (0120h) Polarity setting of P2 2	7	POL15_PO2	0	logic level of PO2 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO2	0	logic level of PO2 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO2	0	logic level of PO2 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO2	0	logic level of PO2 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO2	0	logic level of PO2 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO2	0	logic level of PO2 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO2	0	logic level of PO2 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO2	0	logic level of PO2 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0120h Polarity setting of P2 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R289 (0121h) Polarity setting of P2 3	7	POL23_PO2	0	logic level of PO2 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO2	0	logic level of PO2 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO2	0	logic level of PO2 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO2	0	logic level of PO2 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO2	0	logic level of PO2 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO2	0	logic level of PO2 pulse at toggle point TP18 0 = low at TP18	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP18	
	1	POL17_PO2	0	logic level of PO2 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO2	0	logic level of PO2 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0121h Polarity setting of P2 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R290 (0122h) Polarity setting of P2 4	7	POL31_PO2	0	logic level of PO2 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO2	0	logic level of PO2 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO2	0	logic level of PO2 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO2	0	logic level of PO2 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO2	0	logic level of PO2 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO2	0	logic level of PO2 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO2	0	logic level of PO2 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO2	0	logic level of PO2 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 0122h Polarity setting of P2 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R291 (0123h) Polarity setting of P3 1	7	POL7_PO3	0	logic level of PO3 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO3	0	logic level of PO3 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO3	0	logic level of PO3 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO3	0	logic level of PO3 pulse at toggle point TP4 0 = low at TP4	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP4	
	3	POL3_PO3	0	logic level of PO3 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO3	0	logic level of PO3 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO3	0	logic level of PO3 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO3	0	logic level of PO3 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 0123h Polarity setting of P3 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R292 (0124h) Polarity setting of P3 2	7	POL15_PO3	0	logic level of PO3 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO3	0	logic level of PO3 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO3	0	logic level of PO3 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO3	0	logic level of PO3 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO3	0	logic level of PO3 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO3	0	logic level of PO3 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO3	0	logic level of PO3 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO3	0	logic level of PO3 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0124h Polarity setting of P3 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R293 (0125h) Polarity setting of P3 3	7	POL23_PO3	0	logic level of PO3 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO3	0	logic level of PO3 pulse at toggle point TP22 0 = low at TP22	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP22	
	5	POL21_PO3	0	logic level of PO3 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO3	0	logic level of PO3 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO3	0	logic level of PO3 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO3	0	logic level of PO3 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO3	0	logic level of PO3 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO3	0	logic level of PO3 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0125h Polarity setting of P3 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R294 (0126h) Polarity setting of P3 4	7	POL31_PO3	0	logic level of PO3 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO3	0	logic level of PO3 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO3	0	logic level of PO3 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO3	0	logic level of PO3 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO3	0	logic level of PO3 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO3	0	logic level of PO3 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO3	0	logic level of PO3 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO3	0	logic level of PO3 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 0126h Polarity setting of P3 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R295 (0127h) Polarity setting of P4 1	7	POL7_PO4	0	logic level of PO4 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO4	0	logic level of PO4 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO4	0	logic level of PO4 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO4	0	logic level of PO4 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO4	0	logic level of PO4 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO4	0	logic level of PO4 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO4	0	logic level of PO4 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO4	0	logic level of PO4 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 0127h Polarity setting of P4 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R296 (0128h) Polarity setting of P4 2	7	POL15_PO4	0	logic level of PO4 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO4	0	logic level of PO4 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO4	0	logic level of PO4 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO4	0	logic level of PO4 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO4	0	logic level of PO4 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO4	0	logic level of PO4 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO4	0	logic level of PO4 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO4	0	logic level of PO4 pulse at toggle point TP8 0 = low at TP8	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP8	

Register 0128h Polarity setting of P4 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R297 (0129h) Polarity setting of P4 3	7	POL23_PO4	0	logic level of PO4 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO4	0	logic level of PO4 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO4	0	logic level of PO4 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO4	0	logic level of PO4 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO4	0	logic level of PO4 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO4	0	logic level of PO4 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO4	0	logic level of PO4 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO4	0	logic level of PO4 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0129h Polarity setting of P4 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R298 (012Ah) Polarity setting of P4 4	7	POL31_PO4	0	logic level of PO4 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO4	0	logic level of PO4 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO4	0	logic level of PO4 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO4	0	logic level of PO4 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO4	0	logic level of PO4 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO4	0	logic level of PO4 pulse at toggle point TP26 0 = low at TP26	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP26	
	1	POL25_PO4	0	logic level of PO4 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO4	0	logic level of PO4 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 012Ah Polarity setting of P4 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R299 (012Bh) Polarity setting of P5 1	7	POL7_PO5	0	logic level of PO5 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO5	0	logic level of PO5 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO5	0	logic level of PO5 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO5	0	logic level of PO5 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO5	0	logic level of PO5 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO5	0	logic level of PO5 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO5	0	logic level of PO5 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO5	0	logic level of PO5 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 012Bh Polarity setting of P5 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R300 (012Ch) Polarity setting of P5 2	7	POL15_PO5	0	logic level of PO5 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO5	0	logic level of PO5 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO5	0	logic level of PO5 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO5	0	logic level of PO5 pulse at toggle point TP12 0 = low at TP12	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP12	
	3	POL11_PO5	0	logic level of PO5 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO5	0	logic level of PO5 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO5	0	logic level of PO5 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO5	0	logic level of PO5 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 012Ch Polarity setting of P5 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R301 (012Dh) Polarity setting of P5 3	7	POL23_PO5	0	logic level of PO5 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO5	0	logic level of PO5 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO5	0	logic level of PO5 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO5	0	logic level of PO5 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO5	0	logic level of PO5 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO5	0	logic level of PO5 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO5	0	logic level of PO5 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO5	0	logic level of PO5 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 012Dh Polarity setting of P5 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R302 (012Eh) Polarity setting of P5 4	7	POL31_PO5	0	logic level of PO5 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO5	0	logic level of PO5 pulse at toggle point TP30 0 = low at TP30	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP30	
	5	POL29_PO5	0	logic level of PO5 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO5	0	logic level of PO5 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO5	0	logic level of PO5 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO5	0	logic level of PO5 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO5	0	logic level of PO5 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO5	0	logic level of PO5 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 012Eh Polarity setting of P5 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R303 (012Fh) Polarity setting of P6 1	7	POL7_PO6	0	logic level of PO6 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO6	0	logic level of PO6 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO6	0	logic level of PO6 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO6	0	logic level of PO6 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO6	0	logic level of PO6 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO6	0	logic level of PO6 pulse at toggle point TP2 0 = low at TP2 1 = high at TP2	
	1	POL1_PO6	0	logic level of PO6 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO6	0	logic level of PO6 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 012Fh Polarity setting of P6 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R304 (0130h) Polarity setting of P6 2	7	POL15_PO6	0	logic level of PO6 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO6	0	logic level of PO6 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO6	0	logic level of PO6 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO6	0	logic level of PO6 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO6	0	logic level of PO6 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO6	0	logic level of PO6 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO6	0	logic level of PO6 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO6	0	logic level of PO6 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0130h Polarity setting of P6 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R305 (0131h) Polarity setting of P6 3	7	POL23_PO6	0	logic level of PO6 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO6	0	logic level of PO6 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO6	0	logic level of PO6 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO6	0	logic level of PO6 pulse at toggle point TP20 0 = low at TP20 1 = high at TP20	
	3	POL19_PO6	0	logic level of PO6 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO6	0	logic level of PO6 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO6	0	logic level of PO6 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO6	0	logic level of PO6 pulse at toggle point TP16 0 = low at TP16	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP16	

Register 0131h Polarity setting of P6 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R306 (0132h) Polarity setting of P6 4	7	POL31_PO6	0	logic level of PO6 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO6	0	logic level of PO6 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO6	0	logic level of PO6 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO6	0	logic level of PO6 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO6	0	logic level of PO6 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO6	0	logic level of PO6 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO6	0	logic level of PO6 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO6	0	logic level of PO6 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 0132h Polarity setting of P6 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R307 (0133h) Polarity setting of P7 1	7	POL7_PO7	0	logic level of PO7 pulse at toggle point TP7 0 = low at TP7 1 = high at TP7	
	6	POL6_PO7	0	logic level of PO7 pulse at toggle point TP6 0 = low at TP6 1 = high at TP6	
	5	POL5_PO7	0	logic level of PO7 pulse at toggle point TP5 0 = low at TP5 1 = high at TP5	
	4	POL4_PO7	0	logic level of PO7 pulse at toggle point TP4 0 = low at TP4 1 = high at TP4	
	3	POL3_PO7	0	logic level of PO7 pulse at toggle point TP3 0 = low at TP3 1 = high at TP3	
	2	POL2_PO7	0	logic level of PO7 pulse at toggle point TP2 0 = low at TP2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP2	
	1	POL1_PO7	0	logic level of PO7 pulse at toggle point TP1 0 = low at TP1 1 = high at TP1	
	0	POL0_PO7	0	logic level of PO7 pulse at toggle point TP0 0 = low at TP0 1 = high at TP0	

Register 0133h Polarity setting of P7 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R308 (0134h) Polarity setting of P7 2	7	POL15_PO7	0	logic level of PO7 pulse at toggle point TP15 0 = low at TP15 1 = high at TP15	
	6	POL14_PO7	0	logic level of PO7 pulse at toggle point TP14 0 = low at TP14 1 = high at TP14	
	5	POL13_PO7	0	logic level of PO7 pulse at toggle point TP13 0 = low at TP13 1 = high at TP13	
	4	POL12_PO7	0	logic level of PO7 pulse at toggle point TP12 0 = low at TP12 1 = high at TP12	
	3	POL11_PO7	0	logic level of PO7 pulse at toggle point TP11 0 = low at TP11 1 = high at TP11	
	2	POL10_PO7	0	logic level of PO7 pulse at toggle point TP10 0 = low at TP10 1 = high at TP10	
	1	POL9_PO7	0	logic level of PO7 pulse at toggle point TP9 0 = low at TP9 1 = high at TP9	
	0	POL8_PO7	0	logic level of PO7 pulse at toggle point TP8 0 = low at TP8 1 = high at TP8	

Register 0134h Polarity setting of P7 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R309 (0135h) Polarity setting of P7 3	7	POL23_PO7	0	logic level of PO7 pulse at toggle point TP23 0 = low at TP23 1 = high at TP23	
	6	POL22_PO7	0	logic level of PO7 pulse at toggle point TP22 0 = low at TP22 1 = high at TP22	
	5	POL21_PO7	0	logic level of PO7 pulse at toggle point TP21 0 = low at TP21 1 = high at TP21	
	4	POL20_PO7	0	logic level of PO7 pulse at toggle point TP20 0 = low at TP20	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = high at TP20	
	3	POL19_PO7	0	logic level of PO7 pulse at toggle point TP19 0 = low at TP19 1 = high at TP19	
	2	POL18_PO7	0	logic level of PO7 pulse at toggle point TP18 0 = low at TP18 1 = high at TP18	
	1	POL17_PO7	0	logic level of PO7 pulse at toggle point TP17 0 = low at TP17 1 = high at TP17	
	0	POL16_PO7	0	logic level of PO7 pulse at toggle point TP16 0 = low at TP16 1 = high at TP16	

Register 0135h Polarity setting of P7 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R310 (0136h) Polarity setting of P7 4	7	POL31_PO7	0	logic level of PO7 pulse at toggle point TP31 0 = low at TP31 1 = high at TP31	
	6	POL30_PO7	0	logic level of PO7 pulse at toggle point TP30 0 = low at TP30 1 = high at TP30	
	5	POL29_PO7	0	logic level of PO7 pulse at toggle point TP29 0 = low at TP29 1 = high at TP29	
	4	POL28_PO7	0	logic level of PO7 pulse at toggle point TP28 0 = low at TP28 1 = high at TP28	
	3	POL27_PO7	0	logic level of PO7 pulse at toggle point TP27 0 = low at TP27 1 = high at TP27	
	2	POL26_PO7	0	logic level of PO7 pulse at toggle point TP26 0 = low at TP26 1 = high at TP26	
	1	POL25_PO7	0	logic level of PO7 pulse at toggle point TP25 0 = low at TP25 1 = high at TP25	
	0	POL24_PO7	0	logic level of PO7 pulse at toggle point TP24 0 = low at TP24 1 = high at TP24	

Register 0136h Polarity setting of P7 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R432 (1B0h) User access control	0	USER_KEY	0	0 = User access disabled 1 = User access enabled	

Register 01B0h User access control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R436 (1B4h) LDO2 control	4:0	LDO2 VSEL	1_0000	1_0000 = 1.8V 1_0010 = 2.0V	

Register 01B4h LDO2 control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R448 (1C0h) User access control2	0	User_KEY2	0	0 = User access2 disabled 1 = User access2 enabled	

Register 1C0h User access control2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R459 (1CBh) Comp control	1:0	PT_COMP	01	01 = Standard operation 11 = High performance operation Other = Inhibit.	

Register 1CBh Comp control

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

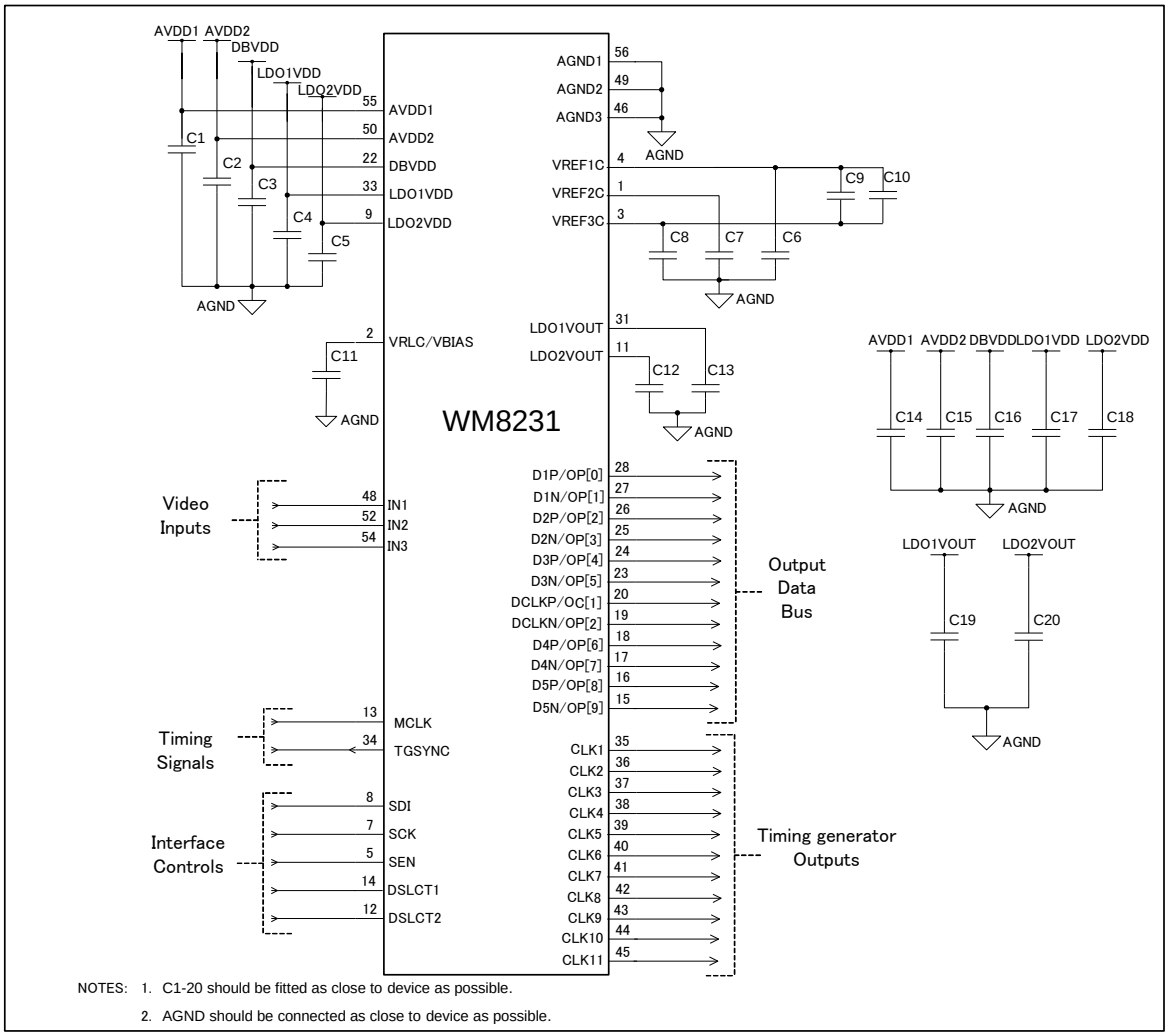


Figure 54 External Components Diagram

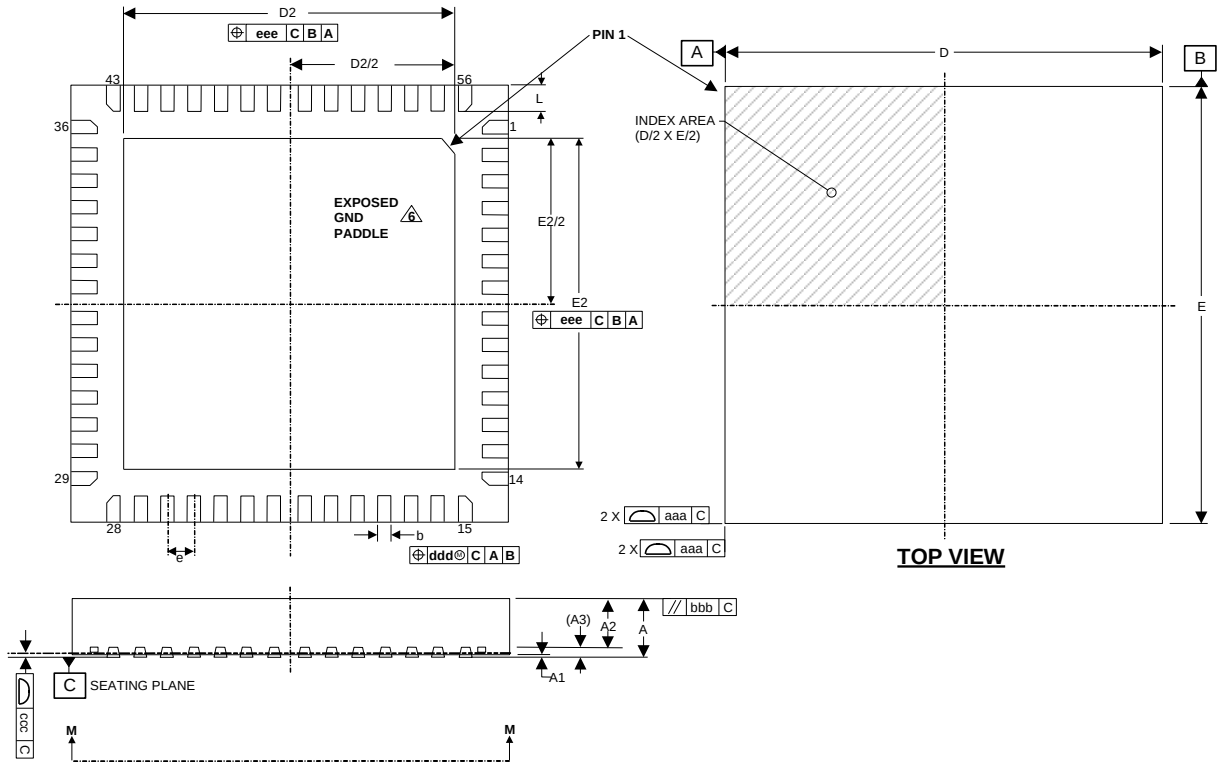
RECOMMENDED EXTERNAL COMPONENT DESCRIPTION

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	0.1uF	De-coupling for AVDD1
C2	0.1uF	De-coupling for AVDD2
C3	0.1uF	De-coupling for DBVDD
C4	0.1uF	De-coupling for LDO1VDD
C5	0.1uF	De-coupling for LDO2VDD
C6	0.1uF	De-coupling for VREF1C
C7	0.1uF	De-coupling for VREF2C
C8	0.1uF	De-coupling for VREF3C
C9	0.01uF	High frequency decoupling between VREF1C and VREF3C
C10	10uF	Low frequency decoupling between VREF1C and VREF3C
C11	1uF	De-coupling for VRLC/VBIAS
C12	1uF	De-coupling for LDO1VOUT
C13	1uF	De-coupling for LDO2VOUT
C14	10uF	Reservoir capacitor for AVDD1
C15	10uF	Reservoir capacitor for AVDD2
C16	10uF	Reservoir capacitor for DBVDD
C17	10uF	Reservoir capacitor for LDO1VDD
C18	10uF	Reservoir capacitor for LDO2VDD
C19	10uF	Reservoir capacitor for LDOOUT
C20	10uF	Reservoir capacitor for LDOOUT

Table 17 External Components Descriptions

PACKAGE DIMENSIONS

FL: 56 PIN QFN PLASTIC PACKAGE 8 x 8 x 0.85 mm BODY, 0.50 mm LEAD PITCH **DM091.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A2	-	0.65	0.67	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		8.00 BSC		
D2	5.95	6.05	6.15	
E		8.00 BSC		
E2	5.95	6.05	6.15	
e		0.5 BSC		
L	0.35	0.4	0.45	
Tolerances of Form and Position				
aaa		0.10		
bbb		0.10		
ccc		0.08		
ddd		0.10		
eee		0.10		
REF	JEDEC, MO-220, VARIATION VLLD-2			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES	PAGE
14/12/12	4.0	AA	Added channel to channel offset matching specification	9
			Corrected offset DAC INL DNL spec	10
			Corrected supply current for full power down mode	11
			Updated timing specification	15,17,33-35
			Corrected figure for ADC INPUT BLACK LEVEL ADJUST	21
			Corrected figure for overall signal flow	22
			Added description for ADC, PGA Bias Current Control.	22
			Added description for PLL DLL setup	23
			Added description for 3pair and 4pair LVDS format	27-29
			Added LVDS output order	30
			Corrected TG timing diagram	32-35
			Added EXTENDED REGISTERES	53,120
			Corrected description for R28	64
			Corrected description for R128,R129	72
17/02/14	4.1	AA	Corrected description of conversion rate	1
			Corrected description of reference DAC resolution	1
			Corrected spec of conversion rate per channel	9
			Updated test condition for output noise specification	9
			Corrected device ID descriptions (Table 2 and Table 3)	13,14
			Corrected RESET CLAMPING description	18,19
			Corrected CDS/Non-CDS PROCESSING description	20
			Corrected ADC INPUT BLACK LEVEL ADJUST description	21
			Updated PLL and DLL setting table	23
			Corrected TG-master/slave mode timing chart	35,36
			Added TGSYNC low period specification	36
			Added description for LINE BY LINE operation	52,62,78
			Added description for TEST PATTERN GENERATOR	53,54,75,76
			Added description for Register setting procedure	55~61
22/05/14	4.2	AA	Added data latency specification	15
			Updated tPER, tMCLKH and tMCLKL description	15
			Corrected test condition for LVDS output data timing	17
			Added description of LVDS synchronous output	30
			Removed tPER and tMCLKD description	33,36
			Removed tTRGD and tPCKD description	36
			Updated Data trigger timing delay specification	37
			Corrected Trigger data, Channel ID description	38
			Corrected TG MASK TIMING description	42
			Added description for Data Output Configuration	61,62
			Corrected register description of LVDS ORDER(R07h[3])	70
			Corrected register description of SEL_PCK7,8,9,10,11	96,97
19/08/14	4.3	AA	Corrected pin name (PO0~PO9)	5,63,73,74
20/10/15	4.4	PH	Test limit (min/max) conditions added in Elec Chars	8-10
			Signal timing limits added	15, 36
			Amendment to LVDS_AMP description	62, 71
27/11/15	4.5	PH	Electrical characteristics updated	8-10
25/03/16	4.6	PH	Digital pin output impedance updated	10
27/03/18	4.7	PH	Formatting update – no change in content	ALL
04/10/18	4.8	PH	Supported operating frequencies (MCLK, sample rate) updated	1, 16, 23, 25

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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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