CIRRUS LOGIC®

CS42L56

Ultralow Power, Stereo Codec with Class H Headphone Amp

DIGITAL to ANALOG FEATURES

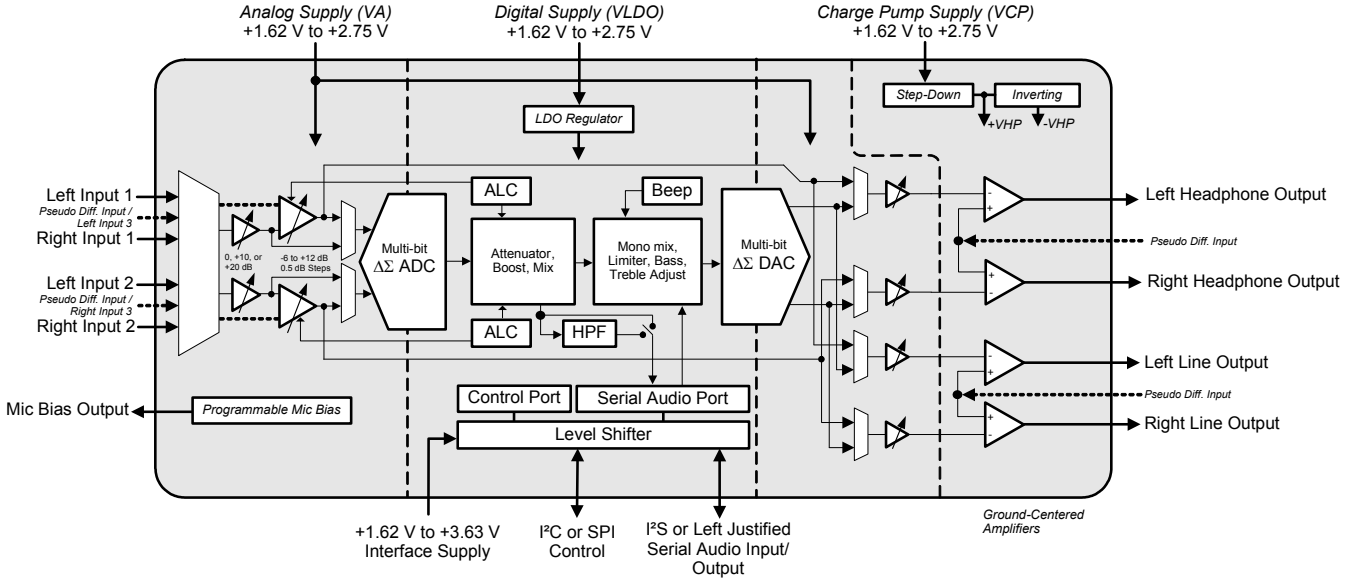
- 5 mW Stereo Playback Power Consumption
- 99 dB Dynamic Range (A-wtd)
- -86 dB THD+N
- Digital Signal Processing Engine
  - Bass & Treble Tone Control, De-emphasis
  - Master Volume Control (+12 to -102 dB in 0.5 dB steps)
  - Soft-ramp & Zero-cross Transitions
  - Programmable Peak-detect and Limiter
  - Beep Generator with Full Tone Control

Stereo Headphone and Line Amplifiers

- Step-down/Inverting Charge Pump
- Class H Amplifier - Automatic Supply Adj.
  - High Efficiency
  - Low EMI
- Pseudo-differential Ground-centered Outputs
- High HP Power Output at -75 dB THD+N
  - 2 x 20 mW Into 16 Ω @ 1.8 V
- 1 V_{RMS} Line Output @ 1.8 V
- Analog Vol. Ctl. (+12 to -60 dB in 1 dB steps)
- Analog In to Analog Out Passthrough
- Pop and Click Suppression

ANALOG to DIGITAL FEATURES

- 3.5 mW Stereo Record Power Consumption
- 95 dB Dynamic Range (A-wtd)
- -87 dB THD+N
- Configurable Analog Inputs
  - Two Pseudo-differential Stereo Inputs or
  - One Pseudo-differential Stereo Inputs + One Standard Stereo Input + One Standard Mono Input or
  - Three Standard Stereo Inputs
  - Pseudo-differential Inputs Reduce Common Mode Signal Noise
  - 3:1 Stereo Input MUX for ADC or Passthrough
- Analog Programmable Gain Amplifier (PGA)
  - +12 to -6 dB in 0.5 dB steps
  - +10 dB or +20 dB Additional Gain for Microphone Inputs
- Programmable, Low-noise MIC Bias Output
- Programmable Automatic Level Control (ALC)
  - Noise Gate for Noise Suppression
  - Programmable Threshold & Attack/Release Rates
- Independent ADC Channel Control
- High-pass Filter Disable for DC Measurements



SYSTEM FEATURES

- Audio (11.2896 MHz or 12.288 MHz) or USB (12 MHz) Master Clock Input
- Low-power Operation
  - Stereo Anlg. Passthrough: 3.3 mW @1.8 V
  - Stereo Rec. and Playback: 8.3 mW @1.8 V
- Headphone Detect Input
- High Performance 24-bit Converters
  - Multi-bit Delta–Sigma Architecture
- Integrated High Efficient Power Management Reduces Power Consumption
  - Step-down Charge Pump Improves Efficiency
  - Inverting Charge Pump Accommodates Low System Voltage by Providing Negative Rail for HP/Line Amp
  - LDO Reg. Provides Low Digital Supply Voltage
- Digital Power Reduction
  - Very Low ADC/DAC Oversampling Rate
  - Bursted Serial Clock Providing up to 24 Bits per Sample
- Power Down Management
  - ADC, DAC, CODEC, PGA, DSP
- Analog & Digital Routing/Mixes
  - Line/Headphone Out = Analog In (ADC Bypassed)
  - Line/Headphone Out = ADC Out
  - Internal Digital Loopback
  - Mono Mixes
- I²C or SPI™ Control Port
- I²S or Left-justified Digital Interface Format
- Flexible Clocking Options
  - Master or Slave Operation
  - Wide Range of Sample Rates Supported

APPLICATIONS

- HDD and Flash-based Portable Audio Players
- PDAs
- Personal Media Players
- Portable Game Consoles
- Digital Voice Recorders
- MD Players/Recorders
- Digital Camcorders
- Digital Cameras
- Smart Phones

GENERAL DESCRIPTION

The CS42L56 is a highly integrated, 24-bit, ultra-low-power stereo CODEC based on multi-bit delta-sigma modulation. Both the ADC and DAC offer many features suitable for low power portable system applications.

The **analog input path** allows independent channel control of a variety of features. The Programmable Gain Amplifier (PGA) provides analog gain with zero cross transitions. The ADC path includes a digital volume attenuator with soft ramp transitions and a programmable ALC and noise gate monitor the input signals and adjust the volume appropriately. An **analog passthrough** also exists, accommodating a lower noise, lower power analog in to analog out path to the headphone and line amplifiers, bypassing the ADC and DAC.

The **DAC output path** includes a fixed-function digital signal processing engine. Tone control provides bass and treble adjustment at four selectable corner frequencies. The digital mixer provides independent volume control for both the ADC output and PCM input signal paths, as well as a master volume control. Digital volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC path also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The Class H stereo headphone amplifier combines the efficiency of an integrated **step-down and inverting charge pump** with the linearity and low EMI of a Class AB amplifier. A step-down/inverting charge pump operates in two modes: ±VCP mode or ±VCP/2) mode. Based on the amplifier's output signal, internal logic automatically adjusts the output of the charge pump, +VHPFILT and –VHPFILT, to optimize efficiency. With these features, the amplifier delivers a ground-centered output with a large signal swing even at low voltages and eliminates the need for external DC-blocking capacitors.

These features make the CS42L56 the ideal solution for portable applications which require extremely low power consumption in a minimal amount of space.

The CS42L56 is available in a 40-pin QFN package for the Commercial (-40 to +85° C) grade. The CDB42L56 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 93 for complete details.

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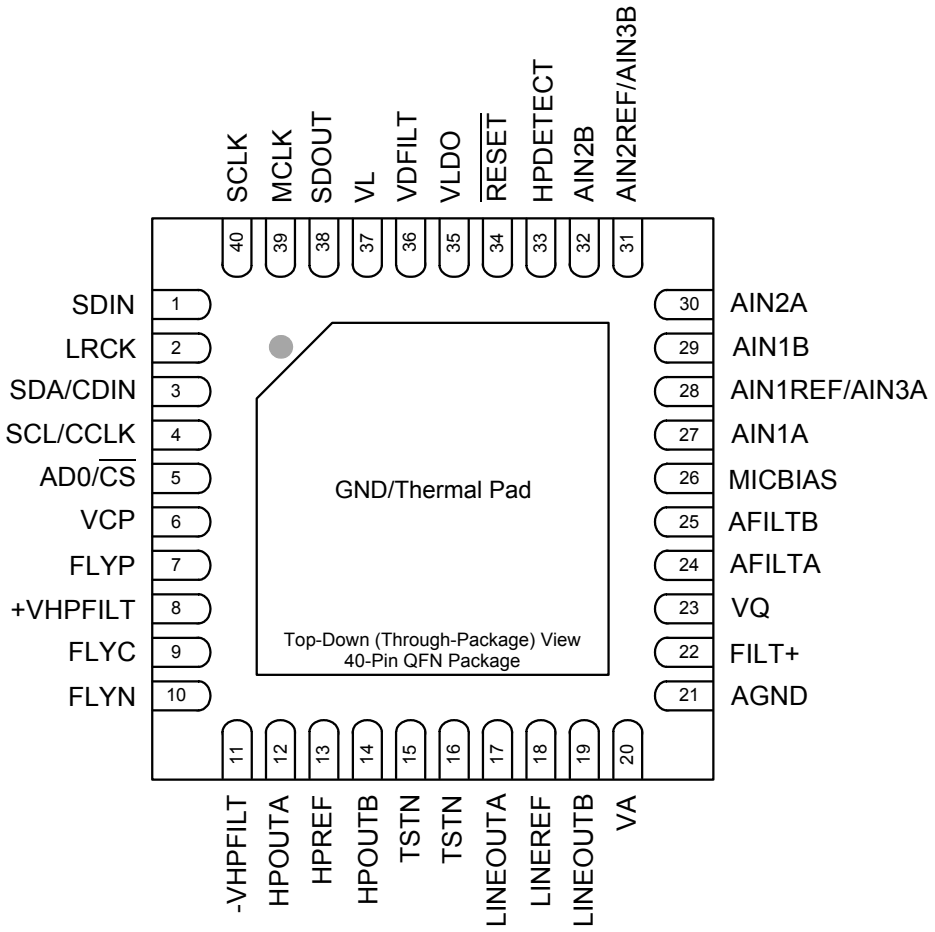
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio data lines.
SDA/CDIN	3	**Serial Control Data** (*Input*/*Output*) - SDA is the bidirectional data pin for the I²C control interface. CDIN is the input data pin for the SPI control interface.
SCL/CCLK	4	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C and SPI control interfaces.
AD0/$\overline{CS}$	5	**Chip Address (I²C) / Chip Select (SPI)** (*Input*) - For I²C operation, this pin must remain static high or low. For SPI, $\overline{CS}$ is the chip-select pin.
VCP	6	**Step-Down Charge Pump Power** *(Input)* - Power supply for the step-down charge pump.
FLYP	7	**Charge Pump Cap Positive Node** *(Output)* - Positive node for the step-down charge pump's flying capacitor.
+VHPFILT	8	**Step-Down Charge Pump Filter Connection** *(Output)* - Power supply from the step-down charge pump that provides the positive rail for the headphone and line amplifiers
FLYC	9	**Charge Pump Cap Common Node** *(Output)* - Common positive node for the step-down and inverting charge pumps' flying capacitors.
FLYN	10	**Charge Pump Cap Negative Node** *(Output)* - Negative node for the inverting charge pump's flying capacitor.

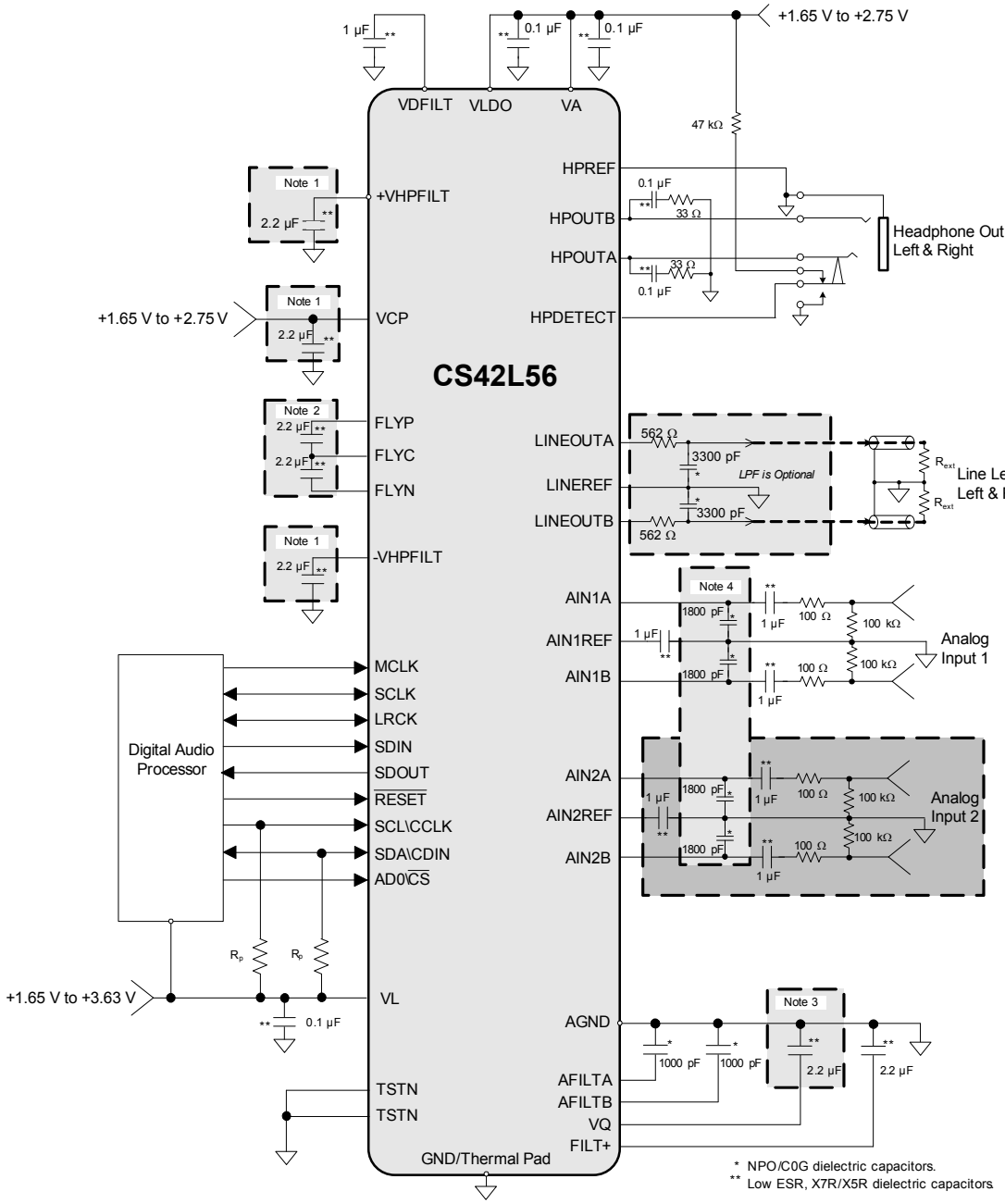
-VHPFILT	11	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the headphone and line amplifiers.
HPOUTA HPOUTB	12 14	**Headphone Audio Output** (*Output*) - The full-scale output level is specified in "HP Output Characteristics" on page 19.
HPREF	13	**Pseudo Diff. Headphone Output Reference** (*Input*) - Ground reference for the headphone amplifiers
TSTN	15 16	**Test Input** *(Input)* **-** This pin is an input used for test purposes only and should be tied to ground for normal operation.
LINEOUTA LINEOUTB	17 19	**Line Audio Output** (*Output*) - The full-scale output level is specified in "Line Output Characteristics" on page 20.
LINEREF	18	**Pseudo Diff. Line Output Reference** (*Input*) - Ground reference for the line amplifiers.
VA	20	**Analog Power** *(Input)* - Power supply for the internal analog section.
AGND	21	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	22	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	23	**Quiescent Voltage** (*Output*) **-** Filter connection for the internal quiescent voltage.
AFILTA AFILTB	24 25	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the ADC inputs.
MICBIAS	26	**Microphone Bias** (*Output*) - Low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN1A AIN1B AIN2A AIN2B	27 29 30 32	**Analog Inputs 1 & 2** (*Input*) **-** The full-scale level is specified in "Analog Input Characteristics" on page 14.
AIN1REF/AIN3A AIN2REF/AIN3B	28 31	**Pseudo Differential Analog Input Reference/Analog Input 3** (*Input*) - Configurable as the ground reference for the programmable gain amplifiers (PGA) or as additional analog inputs. The full-scale level is specified in "Analog Input Characteristics" on page 14.
HPDETECT	33	**Headphone Detect** (*Input*) - The HPDETECT circuit can be set to control the power down of the left and/or right channel of the line and/or headphone outputs as described in "Headphone Power Control" on page 59 and "Line Power Control" on page 60 and/or cause an interrupt. This pin is debounced such that the signal must remain stable in the new state for approximately 10 ms before a change is passed on to the internal HPDETECT circuit.
$\overline{\text{RESET}}$	34	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VLDO	35	**Low Dropout Regulator (LDO) Power** *(Input)* - Power supply for the LDO regulator.
VDFILT	36	**Low Dropout Regulator (LDO) Filter Connection** *(Output)* - Power supply from the LDO regulator that provides the low voltage power to the digital section.
VL	37	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and I²C control port.
SDOUT	38	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MCLK	39	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	40	**Serial Clock** *(Input/Output)* **-** Serial clock for the serial audio interface.
GND/ Thermal Pad	-	Ground reference for the internal charge pump and digital section; thermal relief pad.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Internal Connections	Driver	Receiver
VL	$\overline{\text{RESET}}$	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	SCL	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	SDA	Input/Output	-	CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
	AD0	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	CCLK	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	CDIN	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	$\overline{\text{CS}}$	Input	-	-	1.8 V - 3.3 V, with Hysteresis
	MCLK	Input	-	-	1.8 V - 3.3 V
	LRCK	Input/Output	Weak Pull-up (~1 MΩ)	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	SCLK	Input/Output	Weak Pull-up (~1 MΩ)	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
	SDOUT	Output	Weak Pull-up (~1 MΩ)	1.8 V - 3.3 V, CMOS	-
	SDIN	Input	-	-	1.8 V - 3.3 V
VA	HPDETECT	Input	-	-	1.8 V - 2.5 V, with Hysteresis

2. TYPICAL CONNECTION DIAGRAMS



Notes:

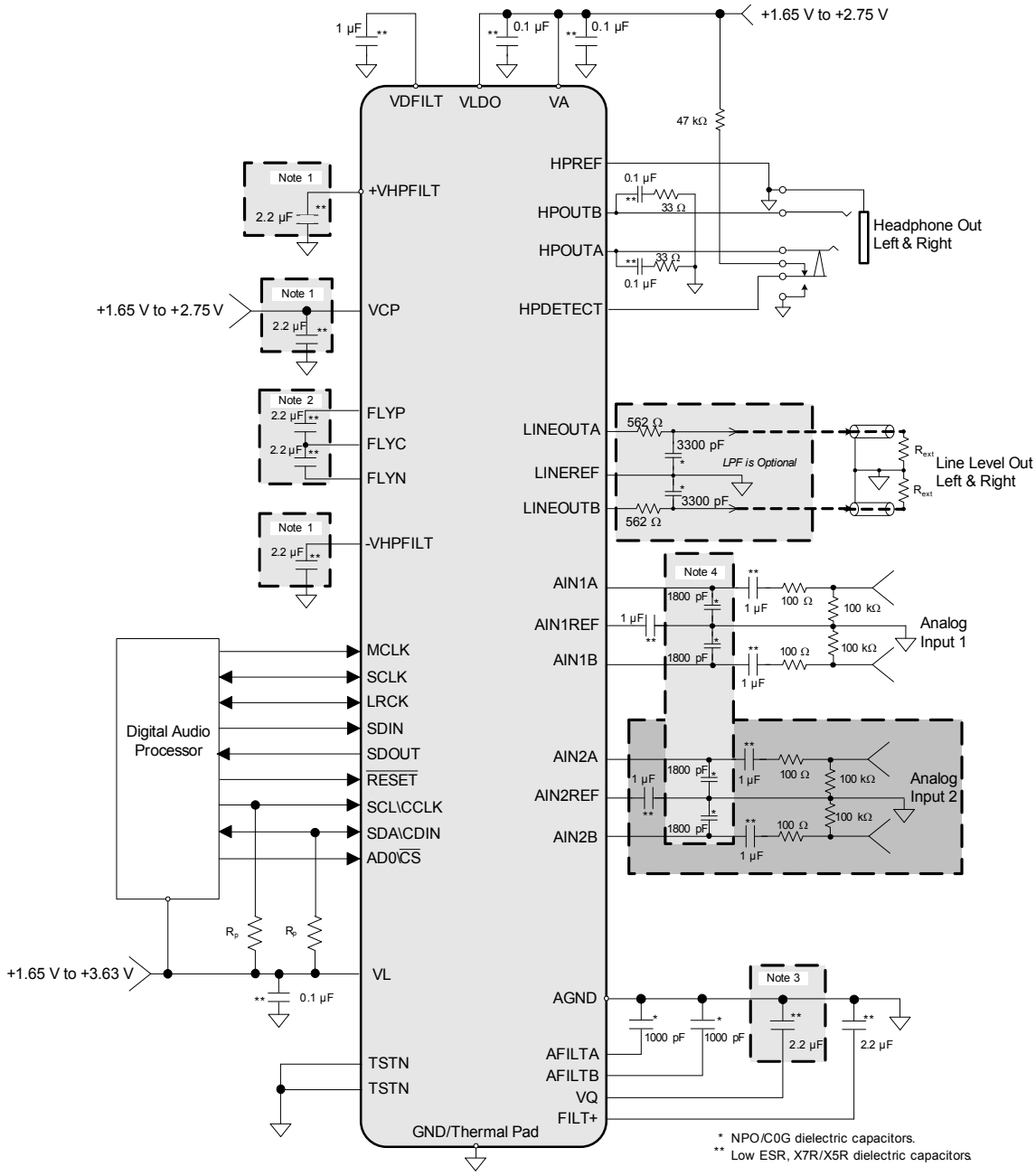
1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.

2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.

3. Additional bulk capacitance may be added to improve PSRR at low frequencies.

4. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs. They are only needed when the PGA (Programmable Gain Amplifier) is bypassed.

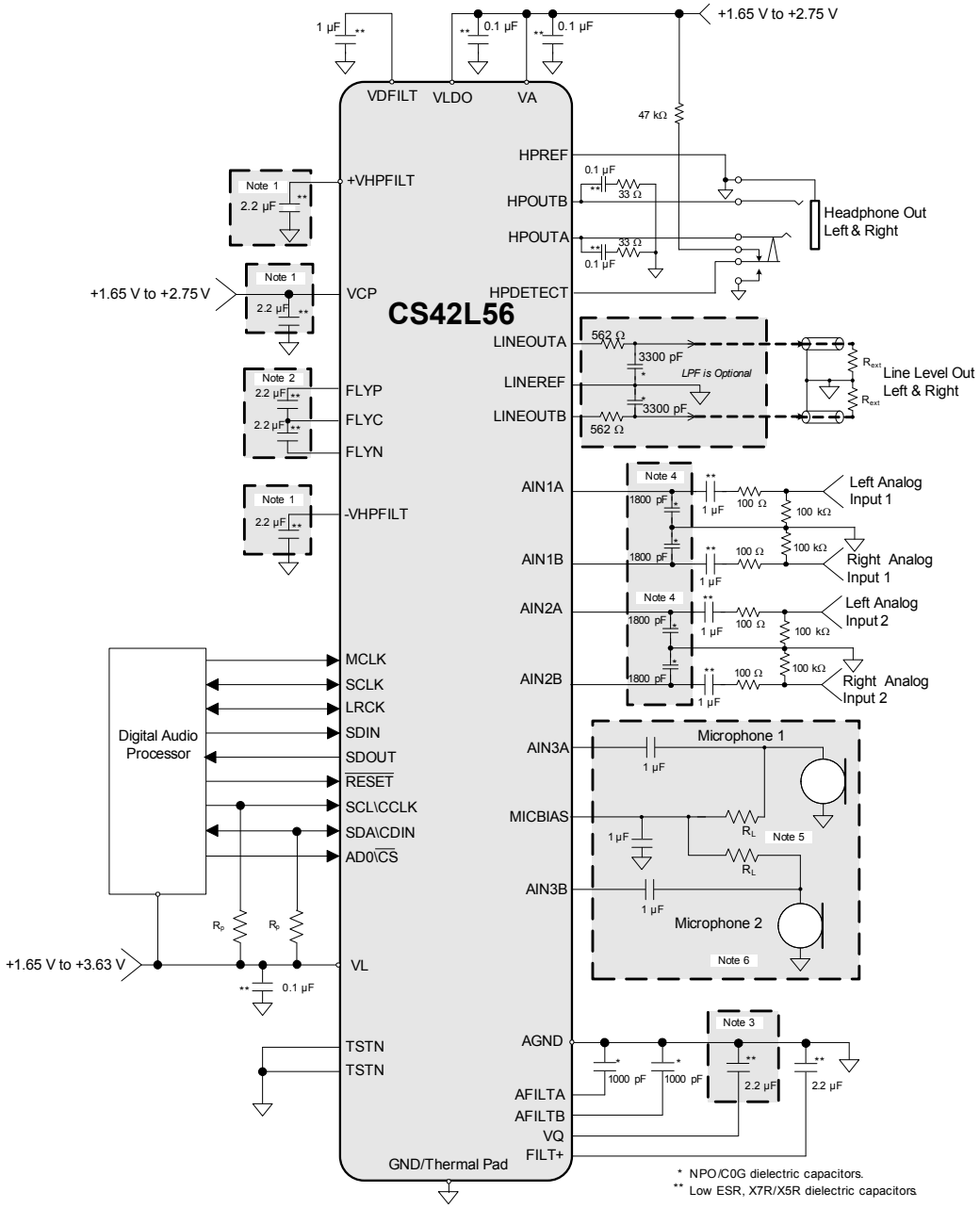
Figure 1. Typical Connection Diagram - Four Pseudo-Differential Analog Inputs



Notes:

1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.
2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.
3. Additional bulk capacitance may be added to improve PSRR at low frequencies.
4. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs. They are only needed when the PGA (Programmable Gain Amplifier) is bypassed.
5. The value of R_L, a current-limiting resistor used with electret condenser microphones, is dictated by the microphone cartridge.
6. The negative terminal of the microphone inputs connects to the ground pin of the microphone cartridge. Gain is applied only to the positive terminal.

Figure 2. Typical Connection Diagram - Two Pseudo-Differential / Three Single-Ended Analog Inputs



Notes:

1. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown. Larger capacitance reduces the ripple on the internal amplifiers' supplies and in turn reduces the amplifier's distortion at high output power levels. Smaller capacitance may not sufficiently reduce ripple to achieve the rated output power and distortion. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power and maximum distortion required.
2. The headphone amplifier's output power and distortion are rated using the nominal capacitance shown and using the default charge pump switching frequency. The required capacitance follows an inverse relationship with the charge pump's switching frequency. When increasing the switching frequency, the capacitance may decrease; when lowering the switching frequency, the capacitance must increase. Since the actual value of typical X7R/X5R ceramic capacitors deviates from the nominal value by a percentage specified in the manufacturer's data sheet, capacitors should be selected based on the minimum output power, maximum distortion and maximum charge pump switching frequency required.
3. Additional bulk capacitance may be added to improve PSRR at low frequencies.
4. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs. They are only needed when the PGA (Programmable Gain Amplifier) is bypassed.
5. The value of R_L, a current-limiting resistor used with electret condenser microphones, is dictated by the microphone cartridge.
6. The negative terminal of the microphone inputs connects to the ground pin of the microphone cartridge. Gain is applied only to the positive terminal.

Figure 3. Typical Connection Diagram - Six Single-Ended Analog Inputs

3. CHARACTERISTIC AND SPECIFICATION TABLES

RECOMMENDED OPERATING CONDITIONS

GND = AGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog	(Note 1)	VA	1.62	2.75	V
Charge Pump	(Note 1)	VCP	1.62	VA	V
LDO Regulator for Digital		VLDO	1.62	2.75	V
Serial/Control Port Interface		VL	1.62	3.63	V
Ambient Temperature	Commercial - CNZ	T_A	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS

GND = AGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog, Charge Pump, LDO	VA, VCP, VLDO	-0.3	3.0	V
	Serial/Control Port Interface	VL	-0.3	4.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
External Voltage Applied to Analog Input	(Note 3)	V_{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output	(Note 4)	V_{IN}	-VHPFILT - 0.3	+VHPFILT + 0.3	V
External Voltage Applied to Digital Input	(Note 3)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)		T_A	-50	+115	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. Due to the existence of parasitic body diodes between VCP and VA, current flows from VCP to VA whenever the VA power supply is lower than VCP. This causes a “back-powering” effect on the VA power supply rails internal to the part; therefore, VA should be maintained at an equal or greater voltage than VCP at all times. While “back-powering” does not have any adverse effects on device operation with respect to performance and reliability, it does lead to extra power consumption and therefore should be avoided.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.
4. VHPFILT is specified in “DC Characteristics” on page 27.

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the “Typical Connection Diagrams” on page 11; Input test signal is a 1 kHz sine wave through the passive input filter, PGA = 0 dB; All Supplies = VA;
GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz. Measurement signal path is AINxx to SDOUT.

Parameter	VA = 2.5 V			VA = 1.8 V			Unit
	Min	Typ	Max	Min	Typ	Max	
Analog In to ADC (PGA bypassed)							

ANALOG INPUT CHARACTERISTICS (CONTINUED)

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; Input test signal is a 1 kHz sine wave through the passive input filter, PGA = 0 dB; All Supplies = VA; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz. Measurement signal path is AINxx to SDOUT.

Dynamic Range	A-weighted	89	95	-	86	92	-	dB
	unweighted	86	92	-	83	89	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-85	-79	-	-85	-79	dB
	-20 dBFS	-	-72	-	-	-69	-	dB
	-60 dBFS	-	-32	-26	-	-29	-23	dB
Analog In to PGA to ADC, PREAMPx[1:0]=00 (0 dB Gain + PGA Setting)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	88	94	-	85	91	-	dB
	unweighted	85	91	-	82	88	-	dB
PGA Setting: +12 dB	A-weighted	81	87	-	78	84	-	dB
	unweighted	78	84	-	75	81	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-87	-81	-	-85	-79	dB
	-60 dBFS	-	-31	-25	-	-28	-22	dB
PGA Setting: +12 dB	-1 dBFS	-	-83	-77	-	-81	-75	dB
Common Mode Rejection	(Note 5)	-	66	-	-	66	-	dB
Analog In to PGA to ADC, PREAMPx[1:0]=01 (+10 dB Gain + PGA Setting)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	91	-	-	88	-	dB
	unweighted	-	88	-	-	86	-	dB
PGA Setting: +12 dB	A-weighted	-	81	-	-	78	-	dB
	unweighted	-	78	-	-	75	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-77	-	-	-77	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-64	-	-	-64	-	dB
Common Mode Rejection	(Note 5)	-	66	-	-	66	-	dB
Analog In to PGA to ADC, PREAMPx[1:0]=10 (+20 dB Gain + PGA Setting)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	85	-	-	82	-	dB
	unweighted	-	82	-	-	79	-	dB
PGA Setting: +12 dB	A-weighted	-	73	-	-	70	-	dB
	unweighted	-	70	-	-	67	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-71	-	-	-71	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-63	-	-	-63	-	dB
Common Mode Rejection	(Note 5)	-	58	-	-	58	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	(Note 6)	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation (1 kHz)	(Note 7)	-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation	R_L = 3 kΩ	-	90	-	-	90	-	dB
	R_L = 16 Ω	-	83	-	-	83	-	dB
Full-scale Input Voltage	ADC	0.76•VA	0.80•VA	0.84•VA	0.76•VA	0.80•VA	0.84•VA	Vpp
	PGA (-1.5 dB)		0.95•VA			0.95•VA		Vpp
	PGA (0 dB)	0.78•VA	0.82•VA	0.86•VA	0.78•VA	0.82•VA	0.86•VA	Vpp
	PGA (+12 dB)		0.198•VA			0.198•VA		

ANALOG INPUT CHARACTERISTICS (CONTINUED)

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; Input test signal is a 1 kHz sine wave through the passive input filter, PGA = 0 dB; All Supplies = VA; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz. Measurement signal path is AINxx to SDOUT.

Full-scale Signal Input Voltage (Note 8)							
ADC	0.76•VA	0.80•VA	0.84•VA	0.76•VA	0.80•VA	0.84•VA	Vpp
PGA=-1.5 dB, PREAMPx[1:0]=00	-	0.95•VA	-	-	0.95•VA	-	Vpp
PGA=0 dB, PREAMPx[1:0]=00	0.78•VA	0.82•VA	0.86•VA	0.78•VA	0.82•VA	0.86•VA	Vpp
PGA=+12 dB, PREAMPx[1:0]=00	-	0.198•VA	-	-	0.198•VA	-	Vpp
PGA=0 dB, PREAMPx[1:0]=01	-	0.259•VA	-	-	0.259•VA	-	Vpp
PGA=0 dB, PREAMPx[1:0]=10	-	0.082•VA	-	-	0.082•VA	-	Vpp
PGA=+12 dB, PREAMPx[1:0]=01	-	0.064•VA	-	-	0.064•VA	-	Vpp
PGA=+12 dB, PREAMPx[1:0]=10	-	0.020•VA	-	-	0.020•VA	-	Vpp
AINxREF Input Voltage (Pseudo-Diff Mode)(Note 10)	-	-	0.300	-	-	0.300	Vpp
Input Impedance (Note 9) ADC	-	60	-	-	60	-	kΩ
PGA, PREAMPx[1:0]=00	-	40	-	-	40	-	kΩ
PGA, PREAMPx[1:0]=01	-	12.65	-	-	12.65	-	kΩ
PGA, PREAMPx[1:0]=10	-	4	-	-	4	-	kΩ
DC Voltage at Analog Input (Pin Floating)	-	VA/2	-	-	VA/2	-	V

Notes:

5. See Figure 4.
6. SDOUT Code with HPFx=1 and HPFRZx=0.
7. See "Parameter Definitions" on page 91.
8. The full scale input voltage values given in the table refers to the maximum voltage difference between the AINxx and AINxREF pins. Providing an input signal at these pins that exceeds the full scale input voltage may result in clipping the analog input.
9. Measured between AINxx and AGND.
10. Providing a signal level higher than 300 mVpp on the AINxREF pin may degrade the PGA linearity and adversely affect analog input performance. See Figure 5.

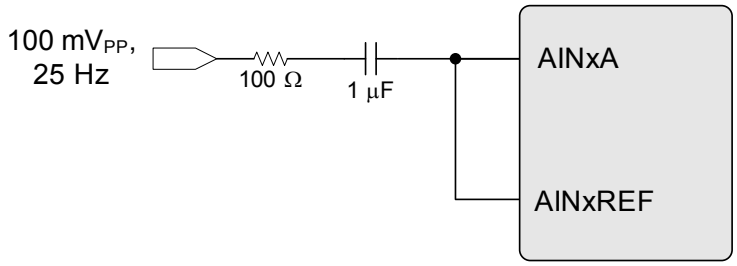


Figure 4. CMRR Test Configuration

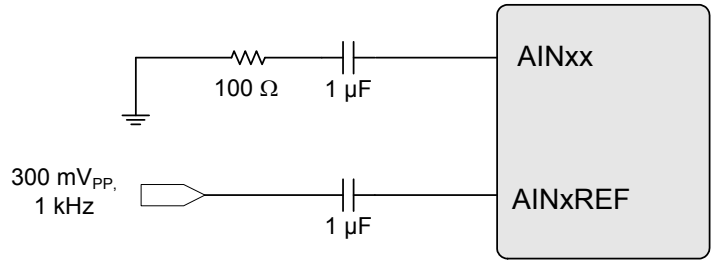


Figure 5. AINxREF Input Voltage Test Configuration

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 11)		Min	Typ	Max	Unit
Frequency Response (20 Hz to 20 kHz)		-0.07	-	+0.02	dB
Passband	to -0.05 dB corner	-	0.421	-	Fs
	to -3 dB corner	-	0.495	-	Fs
Stopband		0.52	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	4.3/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs) (Note 12)					
Passband	to -3.0 dB corner	-	1.87	-	Hz
	to -0.05 dB corner	-	17.15	-	Hz
Frequency Response		-	-	0.15	dB
Phase Deviation @ 20 Hz		-	5.3	-	Deg
Filter Settling Time (Note 13)		-	10^5/Fs	-	s

Notes:

11. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 41 to Note 44 on page 90) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.
12. Characteristics are based on the default setting in register "HPF Control (Address 1Bh)" on page 75.
13. Settling time decreases at higher corner frequency settings.

HP OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 10 kΩ, C_L = 150 pF for a line load, and test load R_L = 16 Ω, C_L = 150 pF for a headphone load (See Figure 6 on page 21); Measurement signal path is SDIN to HPOUTx.

Parameter (Note 15)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Line Load R_L = 10 kΩ (+2 dB Analog Gain) (Note 14)								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	90	96	-	dB
	unweighted	89	95	-	87	93	-	dB
16-Bit	A-weighted	-	96	-	-	94	-	dB
	unweighted	-	94	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 16)							
18 to 24-Bit	0 dB	-	-84	-78	-	-85	-79	dB
	-20 dB	-	-75	-	-	-73	-	dB
	-60 dB	-	-35	-30	-	-33	-28	dB
16-Bit	0 dB	-	-82	-	-	-83	-	dB
	-20 dB	-	-74	-	-	-72	-	dB
	-60 dB	-	-34	-	-	-32	-	dB
Full-scale Output Voltage	(Note 17)	1.56•VA	1.64•VA	1.73•VA	1.56•VA	1.64•VA	1.73•VA	V_{PP}
HP Load R_L = 16 Ω (-4 dB Analog Gain) (Note 14)								
Dynamic Range								
18 to 24-Bit	A-weighted	89	95	-	88	94	-	dB
	unweighted	86	92	-	85	91	-	dB
16-Bit	A-weighted	-	93	-	-	92	-	dB
	unweighted	-	90	-	-	89	-	dB
Total Harmonic Distortion + Noise	(Note 16)	-	-75	-69	-	-75	-69	dB
Full-scale Output Voltage	(Note 17)	0.76•VA	0.82•VA	0.88•VA	0.76•VA	0.82•VA	0.88•VA	V_{PP}
Output Power	(Note 16)	-	32	-	-	17	-	mW
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Interchannel Isolation	10 kΩ	-	90	-	-	90	-	dB
(Note 17)	16 Ω	-	90	-	-	90	-	dB
Interchannel Gain Mismatch	(Note 17)	-	0.1	0.28	-	0.1	0.28	dB
Output Offset	Mute	-	0.5	1.0	-	0.5	1.0	mV
(Note 17)	0 dB Analog Gain	-	3.9	±15.1	-	3.1	±11.4	mV
Gain Drift	(Note 17)	-	±100	-	-	±100	-	ppm/°C
Load Resistance (R_L)	(Note 17)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 17)	-	-	150	-	-	150	pF

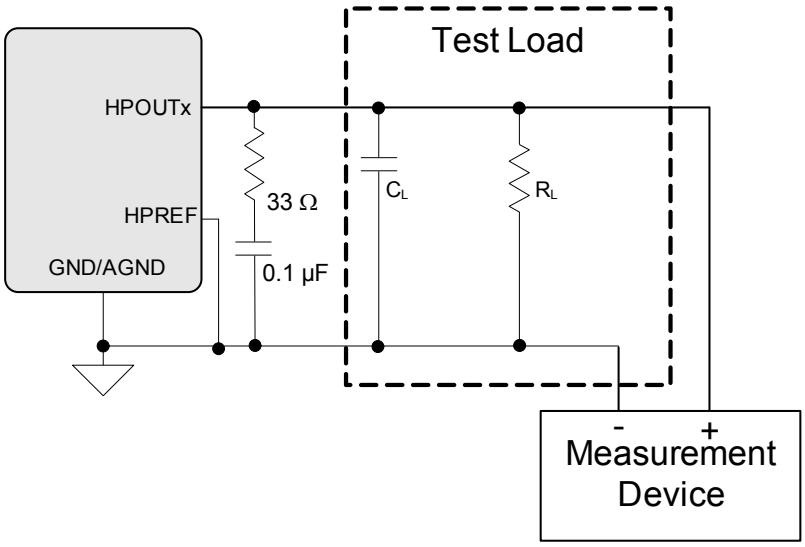
LINE OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; Input test signal is a full-scale 997 Hz sine wave; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load R_L = 10 kΩ, C_L = 150 pF (see Figure 6 on page 21); Measurement signal path is SDIN to LINEOUTx.

Parameter (Note 15)		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
(+2 dB Analog Gain) (Note 14)								
Dynamic Range								
18 to 24-Bit	A-weighted	93	99	-	91	97	-	dB
	unweighted	90	96	-	88	94	-	dB
16-Bit	A-weighted	-	96	-	-	94	-	dB
	unweighted	-	94	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 16)							
18 to 24-Bit	0 dB	-	-84	-78	-	-86	-80	dB
	-20 dB	-	-76	-	-	-74	-	dB
	-60 dB	-	-36	-30	-	-34	-28	dB
16-Bit	0 dB	-	-82	-	-	-84	-	dB
	-20 dB	-	-74	-	-	-72	-	dB
	-60 dB	-	-34	-	-	-32	-	dB
Full-scale Output Voltage	(Note 17)	1.50•VA	1.58•VA	1.71•VA	1.50•VA	1.58•VA	1.71•VA	V_{PP}
Other Characteristics								
Interchannel Isolation	(Note 17)	-	90	-	-	90	-	dB
Interchannel Gain Mismatch	(Note 17)	-	0.1	0.32	-	0.1	0.32	dB
Output Offset	Mute	-	0.5	1.0	-	0.5	1.0	mV
(Note 17)	0 dB Analog Gain	-	3.6	±14.6	-	2.8	±10.6	mV
Gain Drift	(Note 17)	-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
Load Resistance (R_L)	(Note 17)	10	-	-	10	-	-	kΩ
Load Capacitance (C_L)	(Note 17)	-	-	150	-	-	150	pF

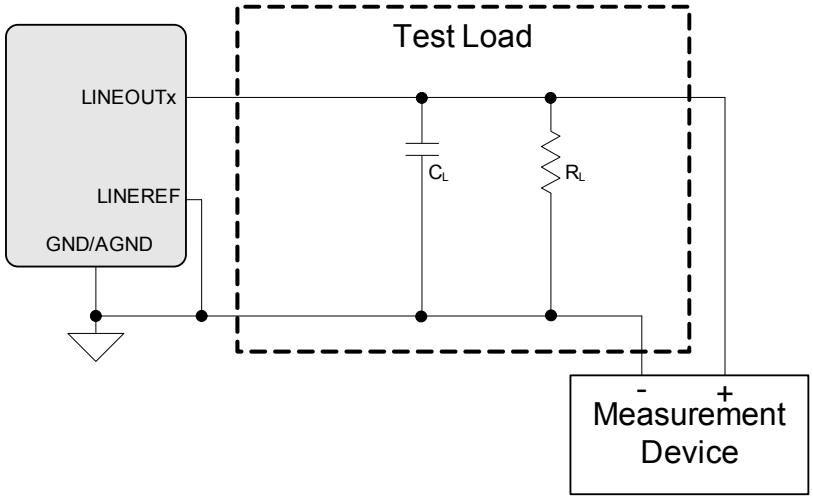
Notes:

14. The analog gain setting ("Headphone Volume Control" on page 84 or "Line Volume Control" on page 84) must be configured as indicated to achieve the specified output characteristics.
15. One LSB of triangular PDF dither is added to data.
16. VCP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the specified THD+N performance at full-scale output voltage and power may not be achieved.
17. See Figure 6 and Figure 7. Refer to "Parameter Definitions" on page 91.
18. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 45 to Note 48 on page 90) have been normalized to Fs and can be denormalized by multiplying the X-axis scale by Fs.
19. Measurement bandwidth is from Stopband to 3 Fs.



Symbolized component values are specified in table "HP Output Characteristics" on page 19

Figure 6. HP Output Test Configuration



Symbolized component values are specified in table "Line Output Characteristics" on page 20

Figure 7. Line Output Test Configuration

ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; Input test signal is a 1 kHz sine wave through the passive input filter shown in Figure 1, PGA and HP/Line gain = 0 dB; All Supplies = VA, VCP Mode; GND = AGND = 0 V; T_A = +25°C; Measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Measurement signal path is AINxx to HPOUTx or LINEOUTx.

Parameter		VA = 2.5 V Min	VA = 2.5 V Typ	VA = 2.5 V Max	VA = 1.8 V Min	VA = 1.8 V Typ	VA = 1.8 V Max	Unit
Analog In to HP Amp (ADC is powered down)								
R_L = 10 kΩ (+2 dB Output Analog Gain) (Note 14)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	(Note 16)							
	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage	(Note 8)	-	0.80•VA	-	-	0.80•VA	-	Vpp
Full-scale Output Voltage	(Note 17)	-	0.93•VA	-	-	0.93•VA	-	Vpp
Frequency Response		-	0/-0.3	-	-	0/-0.3	-	dB
R_L = 16 Ω (-4 dB Output Analog Gain) (Note 14)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	(Note 16)							
	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage	(Note 8)	-	0.80•VA	-	-	0.80•VA	-	Vpp
Output Power	(Note 16)	-	12	-	-	6.5	-	mW
Frequency Response		-	0/-0.3	-	-	0/-0.3	-	dB
Analog In to Line Amp (ADC is powered down)								
R_L = 10 kΩ (+2 dB Output Analog Gain) (Note 14)								
Dynamic Range	A-weighted	-	94	-	-	91	-	dB
	unweighted	-	91	-	-	88	-	dB
Total Harmonic Distortion + Noise	(Note 16)							
	-1 dB	-	-70	-	-	-80	-	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
Full-scale Input Voltage	(Note 8)	-	0.80•VA	-	-	0.80•VA	-	Vpp
Full-scale Output Voltage	(Note 17)	-	0.89•VA	-	-	0.89•VA	-	Vpp
Frequency Response		-	0/-0.3	-	-	0/-0.3	-	dB

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 18)		Min	Typ	Max	Unit
Frequency Response 20 Hz to 20 kHz	Fs = 48.000 kHz	-0.007	-	+0.007	dB
	Fs = 44.118 kHz	-0.081	-	+0.081	dB
Passband	to -0.05 dB corner	-	0.48	-	Fs
	to -3 dB corner	-	0.49	-	Fs
Stopband		0.55	-	-	Fs
Stopband Attenuation	(Note 19)	49	-	-	dB
Total Group Delay		-	6.5/Fs	-	s
De-emphasis Error	Fs = 44.118 kHz	-	-	+0.05/-0.25	dB

SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = GND = AGND, Logic 1 = VL, LRCK, SCLK, SDOUT C_{LOAD} = 15 pF.

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width	(Note 20)		1	-	ms
MCLK Frequency			(See "Serial Port Clocking" on page 47)		MHz
MCLK Duty Cycle			45	55	%
Slave Mode (Figure 8)					
Input Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 47)		kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_{Ps}$	-	$68 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{ss(LK-SK)}$	40	-	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{ss(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{hs(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{ss(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{hs}	20	-	ns
Master Mode (Figure 9)					
Output Sample Rate (LRCK)		F_s	(See "Serial Port Clocking" on page 47)		Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency	SCLK = MCLK mode	$1/t_{Pm}$	-	12.0000	MHz
	All Other Modes	$1/t_{Pm}$	-	$68 \cdot F_s$	Hz
SCLK Duty Cycle	RATIO[4:0] = 'xxx00' or 'xxx11'		45	55	%
	RATIO[4:0] = 'xxx01' (Note 21)		33	66	%
LRCK Time Before SCLK Falling Edge		$t_{sm(LK-SK)}$	-	±2	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{sm(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{hm(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{sm(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{hm}	20	-	ns

Notes:

20. After powering up the CS42L56, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled. This specification is valid with the recommended capacitor on VDFILT.
21. When the RATIO[1:0] = '01', the device will periodically extend the SCLK high time to compensate for the resulting fractional MCLK/SCLK ratio.

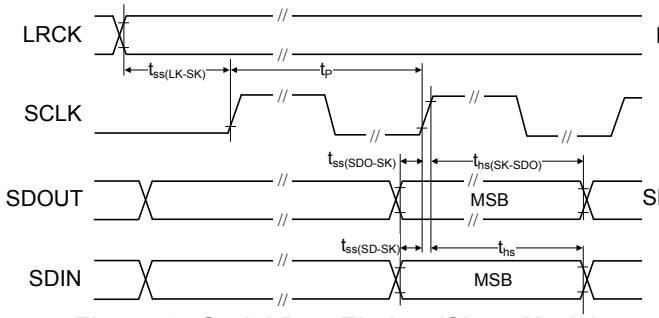


Figure 8. Serial Port Timing (Slave Mode)

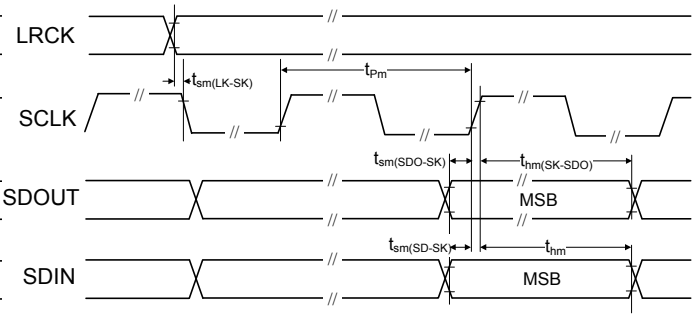


Figure 9. Serial Port Timing (Master Mode)

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

Inputs: Logic 0 = GND = AGND, Logic 1 = VL (Note 22) .

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
SCL Clock Frequency	f_{scl}	-	550	kHz
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	0.6	-	µs
Clock Low Time	t_{low}	1.3	-	µs
Clock High Time	t_{high}	0.6	-	µs
Setup Time for Repeated Start Condition	t_{sust}	0.6	-	µs
SDA Input Hold Time from SCL Falling (Note 23)	t_{hddi}	0	0.9	µs
SDA Output Hold Time from SCL Falling	t_{hddo}	0.2	0.9	µs
SDA Setup Time to SCL Rising	t_{sud}	100	-	ns
Rise Time of SCL and SDA	t_{rc}	-	300	ns
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	0.6	-	µs
Bus Free Time Between Transmissions	t_{buf}	1.3	-	µs
SDA Bus Capacitance	C_L	-	400	pF
SDA Pull-Up Resistance	R_p	500	-	Ω

Notes:

22. All specifications are valid for the signals at the pins of the CS42L56 with the specified load capacitance.
23. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

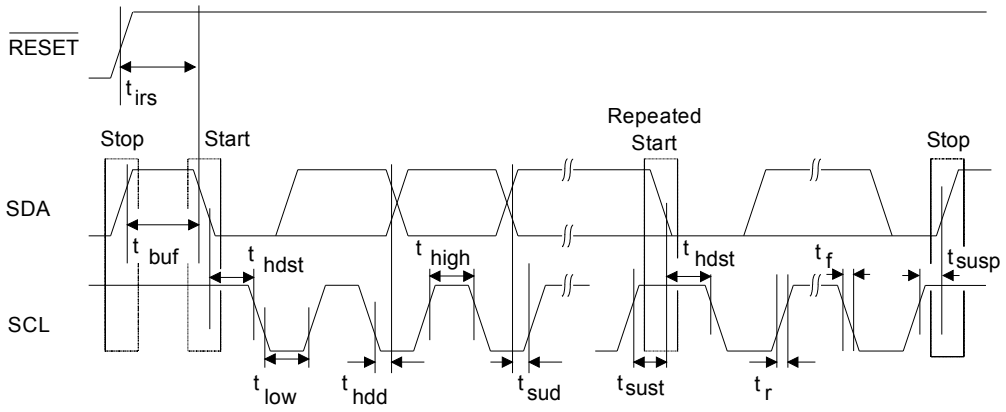


Figure 10. I²C Control Port Timing

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

Inputs: Logic 0 = GND = AGND, Logic 1 = VL, SDA C_L = 30 pF.

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	20	-	ns
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 24)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 25)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 25)	t_{f2}	-	100	ns

Notes:

24. Data must be held for sufficient time to bridge the transition time of CCLK.
25. For f_{sck} <1 MHz.

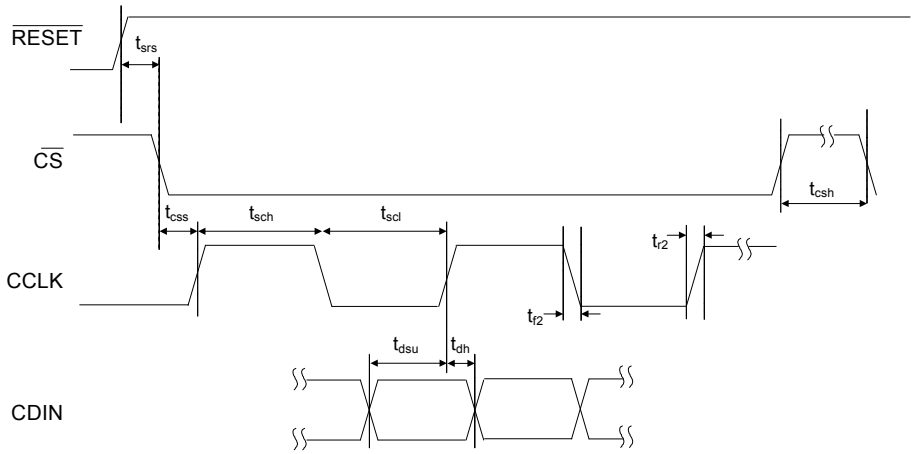


Figure 11. Control Port Timing - SPI Format

ANALOG OUTPUT ATTENUATION CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; GND = AGND = 0 V. Attenuation is referenced to the full-scale voltage for the given output. Test load R_L = 3 kΩ, C_L = 150 pF for a line load, and test load R_L = 16 Ω, C_L = 150 pF for a headphone load (See Figure 6 and Figure 7 on page 21).

Parameters	Power Status		Min	Typ	Max	Units
	Headphone	*Line*				
Headphone Mute Attenuation (HPxMUTE=1) (Note 26)	OFF	OFF	-	90	-	dB
	OFF	ON	-	90	-	dB
	ON	OFF	-	90	-	dB
	ON	ON	-	90	-	dB
Line Mute Attenuation (LINExMUTE=1) (Note 26)	OFF	OFF	-	90	-	dB
	OFF	ON	-	90	-	dB
	ON	OFF	-	90	-	dB
	ON	ON	-	90	-	dB

Notes:

26. Assumes no external impedance on HPREF or LINEREF. External impedance on HPREF or LINEREF will impact the attenuation.

DC CHARACTERISTICS

Test Conditions (unless otherwise specified): Connections to the CS42L56 are shown in the "Typical Connection Diagrams" on page 11; GND = AGND = 0 V; all voltages with respect to ground.

Parameters		Min	Typ	Max	Units
VHPFILT Characteristics (Note 27)					
VCP Mode	+VHPFILT	-	VCP	-	V
	-VHPFILT	-	-VCP	-	V
VCP/2 Mode	+VHPFILT	-	VCP/2	-	V
	-VHPFILT	-	-VCP/2	-	V
MIC BIAS Characteristics					
Nominal Voltage	BIAS_LVL[1:0] = 00	-	0.9•VA	-	V
	BIAS_LVL[1:0] = 01	-	0.8•VA	-	V
	BIAS_LVL[1:0] = 10	-	0.7•VA	-	V
	BIAS_LVL[1:0] = 11	-	0.6•VA	-	V
DC Output Current (Note 28)		-	-	1.22	mA
Power Supply Rejection Ratio (PSRR) @ 1 kHz	BIAS_LVL[1:0] = 00	-	45	-	dB
	BIAS_LVL[1:0] = 01	-	50	-	dB
	BIAS_LVL[1:0] = 10	-	50	-	dB
	BIAS_LVL[1:0] = 11	-	50	-	dB
Misc. DC Filter Characteristics					
	FILT+	-	VA	-	V
	VQ	-	VA/2	-	V
	VDFILT	-	0.9	-	V
Power Supply Rejection Ratio (PSRR) Characteristics					
PSRR with 100 mVpp, 1 kHz signal (Note 29)	PGA to ADC	-	47	-	dB
	PGA (Pseudo Differential) to ADC	-	58	-	dB
	ADC	-	57	-	dB
	PGA to HP & Line Amps	-	44	-	dB
	PGA (Pseudo Differential) to HP & Line Amps	-	54	-	dB
	DAC to HP & Line Amps	-	56	-	dB
PSRR with 100 mVpp, 60 Hz signal (Notes 29, 30)	PGA to ADC	-	35	-	dB
	ADC	-	25	-	dB
	PGA to HP & Line Amps	-	50	-	dB
	DAC to HP & Line Amps	-	60	-	dB

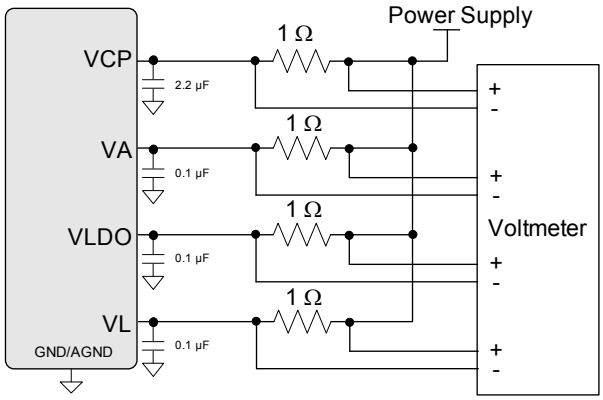
Notes:

27. No load connected to HPOUTx and LINEOUTx.
28. VA = 2.71 V, BIAS_LVL[1:0] = 00, total equivalent external impedance to ground = 2 kΩ.
29. Valid with the recommended capacitor values on FILT+ and VQ, no load on HP and Line. Increasing the capacitance on FILT+ and VQ will also increase the PSRR.
30. The PGA is biased with VQ, created by a resistor divider from the VA supply. Increasing the capacitance on FILT+ and VQ will also increase the PSRR at low frequencies. A 10 µF capacitor on VQ improves the PSRR to 42 dB.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 31)		Symbol	Min	Max	Units
Input Leakage Current		I_{in}	-	±10	µA
Input Capacitance			-	10	pF
1.8 V - 3.3 V Logic					
High-Level Output Voltage (I_{OH} = -100 µA)		V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)		V_{OL}	-	0.2	V
High-Level Input Voltage	VL = 1.65 V VL = 1.8 V VL = 2.0 V VL > 2.0 V	V_{IH}	0.83•VL 0.76•VL 0.68•VL 0.65•VL	- - - -	V
Low-Level Input Voltage		V_{IL}	-	0.30•VL	V
HPDETECT Input					
High-Level Input Voltage		$HPDV_{IH}$	0.65•VA	-	V
Low-Level Input Voltage		$HPDV_{IL}$	-	0.35•VA	V

31. See "I/O Pin Characteristics" on page 10 for serial and control port power rails.



Note: Current is derived from the voltage drop across a 1 Ω resistor in series with each supply input.

Figure 12. Power Consumption Test Configuration

POWER CONSUMPTION - ALL SUPPLIES = 1.8 V

	Operation Test Conditions (unless otherwise specified): All zeros input, slave mode, sample rate = 48 kHz; No load. Refer to Figure 12 on page 28.	**Power Ctl. Registers**								**ADC, Line, HP Sel. Registers**								**Class H Mode page 63**	**Typical Current (mA)**				**Total Power (mW)**
		02h page 58				03h page 59				08h page 74							0Fh page 66		i_{VCP}	i_{VA}	i_{VLDO}	i_{VL}	
		PDN_CHRG	PDN_ADCB	PDN_ADCA	PDN	PDN_HPB[1:0]		PDN_HPA[1:0]		PDN_LINB[1:0]		PDN_LINA[1:0]		ADCBMUX[1:0]	ADCAMUX[1:0]	LINEBMUX	LINEAMUX	HPBMUX	HPAMUX	PDN_DSP					
1	Off (Note 32)	x	x	x	x	x		x		x		x		x	x	x	x	x	x	x	-	0.001	0.001	0.007	0.002	**0.02**
2	Standby (Note 33) MCLKDIS=1	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.001	0.001	0.053	0.007	**0.11**
	MCLKDIS=0	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.001	0.010	0.292	0.007	**0.56**
	(Note 34) MCLKDIS=x	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.001	0.001	0.020	0.001	**0.04**
3	Mono Record (Note 35) ADC	0	1	0	0	11		11		11		11		xx	01	x	x	x	x	x	-	0.001	0.915	0.671	0.018	**2.89**
	PGA to ADC	0	1	0	0	11		11		11		11		xx	00	x	x	x	x	x	-	0.001	1.056	0.672	0.017	**3.14**
4	Stereo Record (Note 35) ADC	0	0	0	0	11		11		11		11		01	01	x	x	x	x	x	-	0.001	1.207	0.824	0.023	**3.70**
	PGA to ADC	0	0	0	0	11		11		11		11		00	00	x	x	x	x	x	-	0.002	1.469	0.826	0.022	**4.17**
5	Mono Play to HP No Effects	1	1	1	0	11		10		11		11		xx	xx	x	x	x	0	1	VCP/2	0.407	1.100	0.718	0.007	**4.02**
																					VCP	0.949	1.107	0.718	0.007	**5.01**
	Effects	1	1	1	0	11		10		11		11		xx	xx	x	x	x	0	0	VCP/2	0.407	1.100	1.050	0.007	**4.62**
																					VCP	0.948	1.107	1.050	0.007	**5.60**
6	Mono Play to Line No Effects	1	1	1	0	11		11		11		10		xx	xx	x	0	x	x	1	VCP/2	0.392	1.101	0.719	0.007	**3.99**
																					VCP	0.844	1.107	0.717	0.007	**4.82**
	Effects	1	1	1	0	11		11		11		10		xx	xx	x	0	x	x	0	VCP/2	0.392	1.101	1.046	0.007	**4.58**
																					VCP	0.844	1.107	1.046	0.007	**5.41**
7	Stereo Play to HP No Effects	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	1	VCP/2	0.604	1.587	0.720	0.007	**5.25**
																					VCP	1.420	1.594	0.717	0.007	**6.73**
	Effects	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	0	VCP/2	0.604	1.587	1.090	0.007	**5.92**
																					VCP	1.419	1.594	1.090	0.007	**7.40**
8	Stereo Play to Line No Effects	1	1	1	0	11		11		10		10		xx	xx	0	0	x	x	1	VCP/2	0.570	1.589	0.718	0.007	**5.19**
																					VCP	1.205	1.597	0.719	0.007	**6.35**
	Effects	1	1	1	0	11		11		10		10		xx	xx	0	0	x	x	0	VCP/2	0.570	1.589	1.089	0.007	**5.86**
																					VCP	1.205	1.597	1.088	0.007	**7.01**
9	Stereo Passthrough to HP	0	1	1	0	10		10		11		11		xx	xx	x	x	1	1	x	VCP/2	0.565	1.180	0.213	0.007	**3.54**
																					VCP	1.198	1.188	0.213	0.007	**4.69**
10	Stereo Passthrough to Line	0	1	1	0	11		11		10		10		xx	xx	1	1	x	x	x	VCP/2	0.571	1.183	0.213	0.007	**3.55**
																					VCP	1.205	1.190	0.213	0.007	**4.71**
11	Mono Rec. & Play No Effects PGA In, HP Out	0	1	0	0	11		10		11		11		xx	00	x	x	x	0	1	VCP/2	0.408	1.921	1.084	0.018	**6.18**
																					VCP	0.950	1.928	1.089	0.018	**7.17**
	Effects	0	1	0	0	11		10		11		11		xx	00	x	x	x	0	0	VCP/2	0.408	1.921	1.415	0.018	**6.77**
																					VCP	0.952	1.928	1.412	0.018	**7.76**
12	Stereo Rec. & Play No Effects PGA In, HP Out	0	0	0	0	10		10		11		11		00	00	x	x	0	0	1	VCP/2	0.604	2.820	1.239	0.023	**8.43**
																					VCP	1.422	2.827	1.240	0.023	**9.92**
	Effects	0	0	0	0	10		10		11		11		00	00	x	x	0	0	0	VCP/2	0.604	2.820	1.613	0.023	**9.11**
																					VCP	1.424	2.827	1.612	0.023	**10.59**
13	Stereo Play to HP No Effects 16 Ω load (Note 36)	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	1	VCP/2	2.725	1.579	0.737	0.008	**9.09**

POWER CONSUMPTION - ALL SUPPLIES = 2.5 V

	Operation Test Conditions (unless otherwise specified): All zeros input, slave mode, sample rate = 48 kHz; No load. Refer to Figure 12 on page 28.	Power Ctl. Registers								MUX Registers							Class H Mode page 63	Typical Current (mA)				Total Power (mW)
		02h page 58				03h page 59				08h page 74						0Fh page 66		i_{VCP}	i_{VA}	i_{VLDO}	i_{VL}	
		PDN_CHRG	PDN_ADCB	PDN_ADCA	PDN	PDN_HPB[1:0]		PDN_HPA[1:0]		PDN_LINB[1:0]		PDN_LINA[1:0]		ADCBMUX[1:0]	ADCAMUX[1:0]	LINEBMUX	LINEAMUX	HPBMUX	HPAMUX	PDN_DSP						
1	Off (Note 32)	x	x	x	x	x		x		x		x		x	x	x	x	x	x	x	-	0.002	0.002	0.013	0.004	**0.05**
2	Standby (Note 33) MCLKDIS=1	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.003	0.003	0.084	0.012	**0.26**
	MCLKDIS=0	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.003	0.017	0.466	0.012	**1.25**
	(Note 34) MCLKDIS=x	x	x	x	1	x		x		x		x		x	x	x	x	x	x	x	-	0.003	0.003	0.032	0.003	**0.10**
3	Mono Record (Note 35) ADC	1	1	0	0	11		11		11		11		xx	01	x	x	x	x	x	-	0.003	0.789	0.744	0.026	**3.91**
	PGA to ADC	1	1	0	0	11		11		11		11		xx	00	x	x	x	x	x	-	0.003	0.963	0.748	0.026	**4.35**
4	Stereo Record (Note 35) ADC	1	0	0	0	11		11		11		11		01	01	x	x	x	x	x	-	0.003	1.089	0.919	0.033	**5.11**
	PGA to ADC	1	0	0	0	11		11		11		11		00	00	x	x	x	x	x	-	0.003	1.419	0.922	0.033	**5.94**
5	Mono Play to HP No Effects	1	1	1	0	11		10		11		11		xx	xx	x	x	x	0	1	VCP/2	0.723	1.469	0.734	0.012	**7.35**
																					VCP	1.984	1.480	0.736	0.012	**10.53**
	Effects	1	1	1	0	11		10		11		11		xx	xx	x	x	x	0	0	VCP/2	0.723	1.468	1.071	0.012	**8.19**
																					VCP	1.982	1.480	1.069	0.012	**11.36**
6	Mono Play to Line No Effects	1	1	1	0	11		11		11		10		xx	xx	x	0	x	x	1	VCP/2	0.693	1.469	0.736	0.012	**7.28**
																					VCP	1.819	1.481	0.732	0.012	**10.11**
	Effects	1	1	1	0	11		11		11		10		xx	xx	x	0	x	x	0	VCP/2	0.693	1.469	1.073	0.012	**8.12**
																					VCP	1.819	1.481	1.069	0.012	**10.95**
7	Stereo Play to HP No Effects	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	1	VCP/2	0.936	2.099	0.737	0.012	**9.46**
																					VCP	2.530	2.113	0.736	0.012	**13.48**
	Effects	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	0	VCP/2	0.934	2.099	1.109	0.012	**10.39**
																					VCP	2.526	2.113	1.109	0.012	**14.40**
8	Stereo Play to Line No Effects	1	1	1	0	11		11		10		10		xx	xx	0	0	x	x	1	VCP/2	0.873	2.102	0.737	0.012	**9.31**
																					VCP	2.197	2.115	0.736	0.012	**12.65**
	Effects	1	1	1	0	11		11		10		10		xx	xx	0	0	x	x	0	VCP/2	0.873	2.102	1.110	0.012	**10.24**
																					VCP	2.196	2.115	1.108	0.012	**13.58**
9	Stereo Passthrough to HP	1	1	1	0	10		10		11		11		xx	xx	x	x	1	1	x	VCP/2	0.870	1.203	0.228	0.012	**5.78**
																					VCP	2.202	1.218	0.228	0.012	**9.15**
10	Stereo Passthrough to Line	1	1	1	0	11		11		10		10		xx	xx	1	1	x	x	x	VCP/2	0.874	1.206	0.228	0.012	**5.80**
																					VCP	2.196	1.220	0.228	0.012	**9.14**
11	Mono Rec. & Play No Effects PGA In, HP Out	1	1	0	0	11		10		11		11		xx	00	x	x	x	0	1	VCP/2	0.723	2.148	1.157	0.026	**10.14**
																					VCP	1.981	2.160	1.162	0.026	**13.32**
	Effects	1	1	0	0	11		10		11		11		xx	00	x	x	x	0	0	VCP/2	0.723	2.148	1.491	0.026	**10.97**
																					VCP	1.983	2.160	1.489	0.027	**14.15**
12	Stereo Rec. & Play No Effects PGA In, HP Out	1	0	0	0	10		10		11		11		00	00	x	x	0	0	1	VCP/2	0.936	3.233	1.335	0.033	**13.84**
																					VCP	2.532	3.247	1.336	0.033	**17.87**
	Effects	1	0	0	0	10		10		11		11		00	00	x	x	0	0	0	VCP/2	0.936	3.233	1.710	0.033	**14.78**
																					VCP	2.534	3.247	1.710	0.033	**18.81**
13	Stereo Play to HP No Effects 16 Ω load (Note 36)	1	1	1	0	10		10		11		11		xx	xx	x	x	0	0	1	VCP/2	3.032	2.081	0.754	0.012	**14.70**

Notes:

32. $\overline{\text{RESET}}$ pin and clock/data lines held LO, PDN=x.
33. $\overline{\text{RESET}}$ pin held HI, PDN=1.
34. Clock/data lines held HI.
35. Either inputs 1 or 2 may be selected. Input 1 is shown for simplicity.
36. In accordance with the JEITA CP-2905B standard, 0.1 mW (per channel) is delivered to the headphone load.

4. APPLICATIONS

4.1 Overview

4.1.1 Basic Architecture

The CS42L56 is a highly integrated, ultra-low power, 24-bit audio CODEC comprised of stereo A/D and D/A converters with pseudo-differential stereo input and output amplifiers. The ADC and DAC are designed using multi-bit delta-sigma techniques; both converters operate at a low oversampling ratio of 64xFs, maximizing power savings while maintaining high performance. The CODEC accepts and is capable of generating serial audio clocks (SCLK, LRCK) derived from a USB or a standard audio input Master Clock (MCLK). Designed with a very low voltage digital core and low voltage Class H amplifiers (powered from an integrated low-dropout regulator and a step-down/inverting charge pump, respectively), the CS42L56 provides significant reduction in overall power consumption.

4.1.2 Line Inputs

The analog input portion of the CODEC allows selection from up to three stereo line-level sources into a Programmable Gain Amplifier (PGA). The optional line pseudo-differential configuration provides common-mode noise rejection for single-ended inputs and is available on AIN1x or AIN2x. If pseudo-differential operation is not required, the pins can also be configured independently as two additional analog inputs (AIN3x).

4.1.3 Line and Headphone Outputs (Class H, Ground-Centered Amplifiers)

The analog output portion of the CODEC includes separate pseudo-differential headphone and line out Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input or one-half the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.

4.1.4 Fixed-function DSP Engine

The fixed function digital signal processing engine processes both the PCM serial input data and ADC output data allowing a mix between the two. Independent volume control, left/right channel swaps, mono mixes, tone control comprise the DSP engine.

4.1.5 Beep Generator

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically or at single time intervals.

4.1.6 Power Management

Several control registers and bits provide independent power down control of the ADC, PGA, DSP, headphone and line outputs, allowing operation in select applications with minimal power consumption.

4.2 Analog Inputs

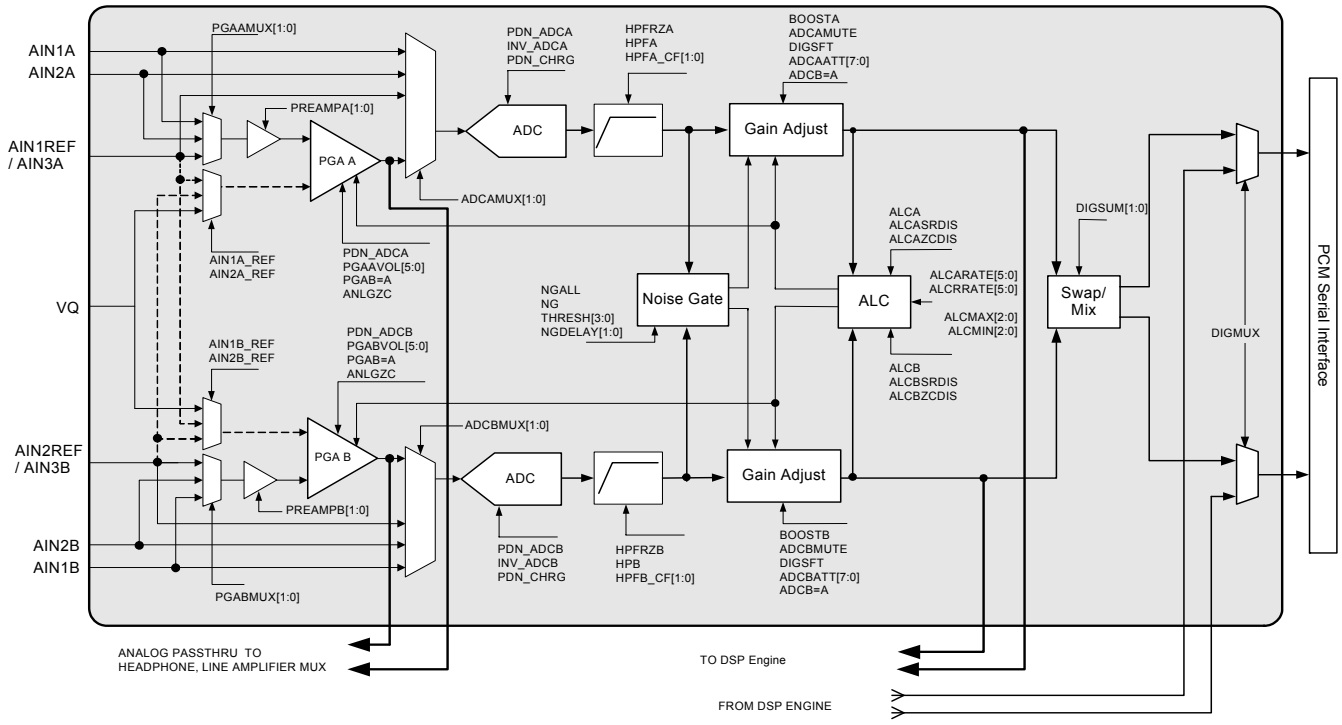


Figure 13. Analog Input Signal Flow

Referenced Control	Register Location
Analog Front End	
AIN1x_REF	"Analog Input 1 x Reference Configuration" on page 74
AIN2x_REF	"Analog Input 2 x Reference Configuration" on page 74
PREAMPx[1:0]	"PGA x Preamplifier Gain" on page 77
PGAxMUX[1:0]	"PGA x Input Select" on page 77
PDN_ADCx	"Power Down ADC x" on page 59
PGAxVOL[5:0]	"PGAx Volume" on page 78
PGAB=A	"PGA Channel B=A" on page 76
ANLGZCx	"Analog Zero Cross" on page 64
ADCxMUX[1:0]	"ADC x Input Select" on page 75
INV_ADCx	"Invert ADC Signal Polarity" on page 76
PDN_CHRG	"Power Down ADC Charge Pump" on page 59
HPFRZx	"ADCx High-Pass Filter Freeze" on page 75
HPFx	"ADCx High-Pass Filter" on page 75
HPFx_CF[1:0]	"HPF x Corner Frequency" on page 75
Digital Volume	
BOOSTx	"Boostx" on page 77
ADCxMUTE	"ADC Mute" on page 76
ADCxATT[7:0]	"ADCx Volume" on page 78
DIGSFT	"Digital Soft Ramp" on page 64
ADCB=A	"ADC Channel B=A" on page 76
ALCx	"ALCx" on page 79
ALCxSRDIS	"ALCx Soft Ramp Disable" on page 82
ALCxZCDIS	"ALCx Zero Cross Disable" on page 82
ALCARATE[5:0]	"ALC Attack Rate" on page 79
ALCRRATE[5:0]	"ALC Release Rate" on page 80
MAX[2:0]	"ALC Maximum Threshold" on page 80
MIN[2:0]	"ALC Minimum Threshold" on page 81
NGALL	"Noise Gate All Channels" on page 81
NG	"Noise Gate Enable" on page 81
THRESH[3:0]	"Noise Gate Threshold and Boost" on page 82
NGDELAY[1:0]	"Noise Gate Delay Timing" on page 82
Miscellaneous	
DIGSUM[1:0]	"Digital Sum" on page 76
DIGMUX	"Digital MUX" on page 63

4.2.1 Pseudo-differential Inputs

The CS42L56 implements a pseudo-differential input stage. The AINxREF inputs are intended to be used as a pseudo-differential reference signal. This feature provides common mode noise rejection with single-ended signals. Figure 14 shows a basic diagram outlining the internal implementation of the pseudo-differential input stage, including a recommended stereo pseudo-differential input topology. If pseudo-differential input functionality is not required, the AINxREF pin should be AC-coupled to GND.

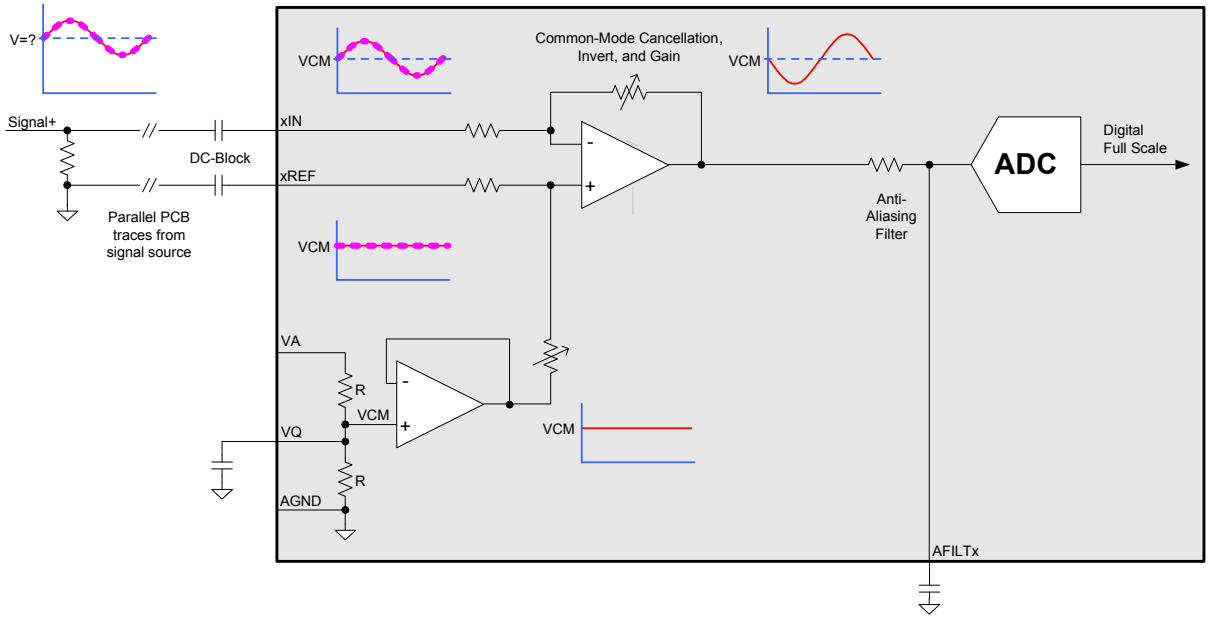


Figure 14. Stereo Pseudo-Differential Input

It should be noted that the AINxREF inputs are intended to be used solely to provide a low-level, pseudo-differential reference signal for the internal input amplifiers when in pseudo-differential mode. Using the analog input pins in a fully differential configuration by providing a large signal on the AINxREF pin is not recommended. The output of the PGA will clip if the voltage difference between AINxx and AINxREF exceeds the full-scale voltage specification (See Note 10 on page 17).

4.2.2 Large-scale Inputs

The CS42L56 allows the user to input signals that would be larger than the ADC full-scale input voltage by using the PGA to attenuate the signal prior to going to the ADC. Table 1 shows the PGA gain setting needed to stay under the maximum ADC input voltage.

Supply Voltage	PGA Gain Setting	Maximum Input Voltage	
(V)	(dB)	(mV_{RMS})	(V_{PP})
1.8	0.0	509	1.44
	-0.5	539	1.52
	-1.0	571	1.62
	-1.5	604	1.71
2.5	0.0	707	2.00
	-0.5	748	2.12
	-1.0	793	2.24
	-1.5	840	2.38

Table 1. Input Voltage PGA Settings

If signals larger than what is shown in Table 1 are needed, an external resistor divider should be used as shown in Table 15. When using an external resistor divider, the PGA must be configured to be in-circuit.

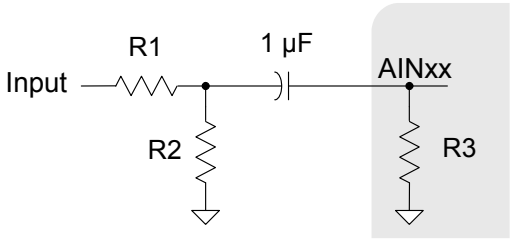


Figure 15. Analog Input Attenuation

Three parameters determine the values of resistors R1 and R2 as shown in Figure 15: source impedance, attenuation, and input impedance. Table 2 shows the design equation used to determine these values.

- **Source Impedance:** Source impedance is defined as the impedance as seen from the PGA looking back into the signal network. The PGA achieves optimal THD+N performance with a source impedance less than 5 kΩ.
- **Attenuation:** The required attenuation factor depends on the magnitude of the input signal. The full-scale input voltage is specified under "Analog Input Characteristics" on page 14. The user should select values for R1 and R2 such that the magnitude of the incoming signal multiplied by the attenuation factor is less than or equal to the full-scale input voltage of the device.
- **Input Impedance:** Input impedance is the impedance from the signal source to the PGA analog input pins, including the PGA. The PGA's input impedance (R3 in Figure 15, Table 2, and Figure 16) is given in the "Analog Input Characteristics" on page 14.

Source Impedance	$\frac{(R1 \times R2)}{(R1 + R2)}$
Attenuation Factor	$\frac{(R2 \times R3)}{(R1 \times R2 + R2 \times R3 + R1 \times R3)}$
Input Impedance	$\frac{(R1 \times R3 + R2 \times R3)}{(R1 + R2 + R3)}$

Table 2. Analog Input Design Parameters

Figure 16 illustrates an example configuration with the PGA in-circuit using one 7.87 kΩ resistor for R1 and one 4.75 kΩ resistor for R2. Based on the discussion above, this circuit provides an optimal interface for both the PGA and the signal source. First, consumer equipment frequently requires an approximate input impedance of 10 kΩ, which the combination of the resistors provide. Second, this circuit will attenuate a typical line level voltage, 2 Vrms, to the full-scale input of the PGA, 0.7 Vrms when VA = 2.5 V. Finally, at approximately 3 kΩ, the source impedance is within the allowable range of the PGA.

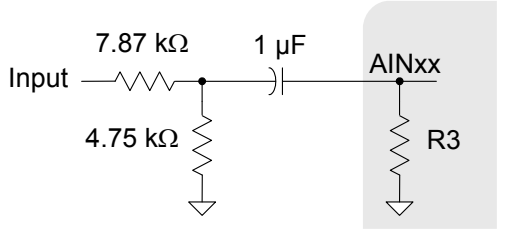


Figure 16. Example Analog Input Attenuation

4.2.3 Microphone Inputs

Any of the line inputs can be configured as a microphone input by using the MICBIAS pin to power the external microphone circuit and by configuring the additional +10 or +20 dB gain in the PGA to properly boost the low-level microphone signal.

4.2.3.1 External Passive Components

The analog inputs are internally biased to VQ. Input signals must be AC coupled using external capacitors with values consistent with the desired high-pass filter design. The analog input resistance may be combined with an external capacitor to achieve the desired cutoff frequency. The equation below gives an example:

$$fc = \frac{1}{2\pi(4\ k\Omega)(1\ \mu F)} = 39.79\ Hz$$

An electrolytic capacitor must be placed such that the positive terminal is positioned relative to the side with the greater bias voltage. The MICBIAS voltage level is controlled by the BIAS_LVL[1:0] bits.

The MICBIAS series resistor must be selected based on the requirements of the particular microphone used.

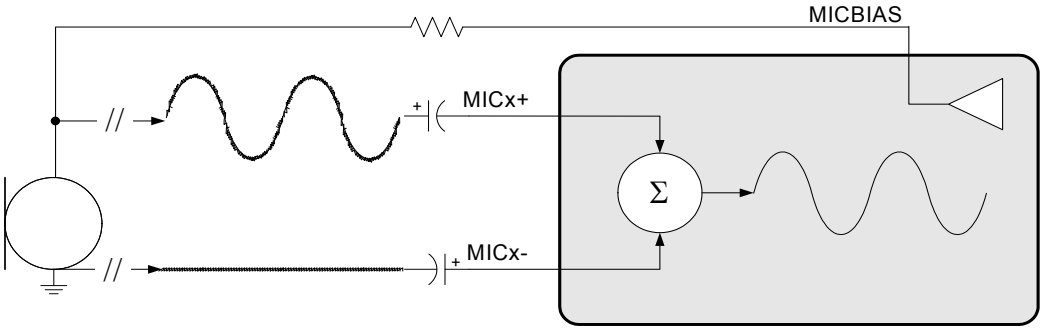


Figure 17. MIC Input Mix w/Common Mode Rejection

Referenced Control	Register Location
BIAS_LVL[1:0]	"Microphone Bias Output Level" on page 77

4.2.4 Optional VCM Buffer

Leaving an analog input pin floating when not being used might inject distortion in the analog input signal path. To prevent this, the analog inputs may be internally biased to VCM by using a weak internal VCM buffer when not being used. The VCM buffer outputs a weakly buffered version of the internal common-mode voltage and biases the chip-side of the analog input AC-coupling capacitor to a constant DC level. This prevents the analog signal from being distorted when that particular channel is not selected by either the PGA or ADC input MUX. If an analog signal is routed to any place other than just the CS42L56, it is recommended to set this bit to 0b. If all analog signals are only routed to the CS42L56, this bit may be left set to 1b.

Referenced Control	Register Location
PDN_VBUF[1:0].....	"Power Down VCM Bias Buffer" on page 58

4.2.5 Automatic Level Control (ALC)

The function of the ALC is to maintain the level of the analog input signal between the maximum and minimum threshold settings programmed in the ALCMAX[2:0] and ALCMIN[2:0] registers. When enabled, the ALC monitors the signal level after the digital volume control block in the input signal path and detects

whenever a threshold violation occurs. It then modifies the signal level by adjusting the gain settings in the PGA and ADC digital volume control accordingly.

As shown in Figure 18, if the input signal level rises above the maximum threshold, the ALC first lowers the PGA gain settings. It then decreases the ADC digital volume at a programmable “attack” rate and maintains the resulting level below the maximum threshold. In contrast, if the input signal level falls below the minimum threshold, the ALC first increases the ADC digital volume settings and then increases the PGA gain settings at a programmable “release” rate. However, once an attack or release operation has been performed on an input signal, the ALC does not change the PGA or the digital volume control settings until the next threshold violation occurs.

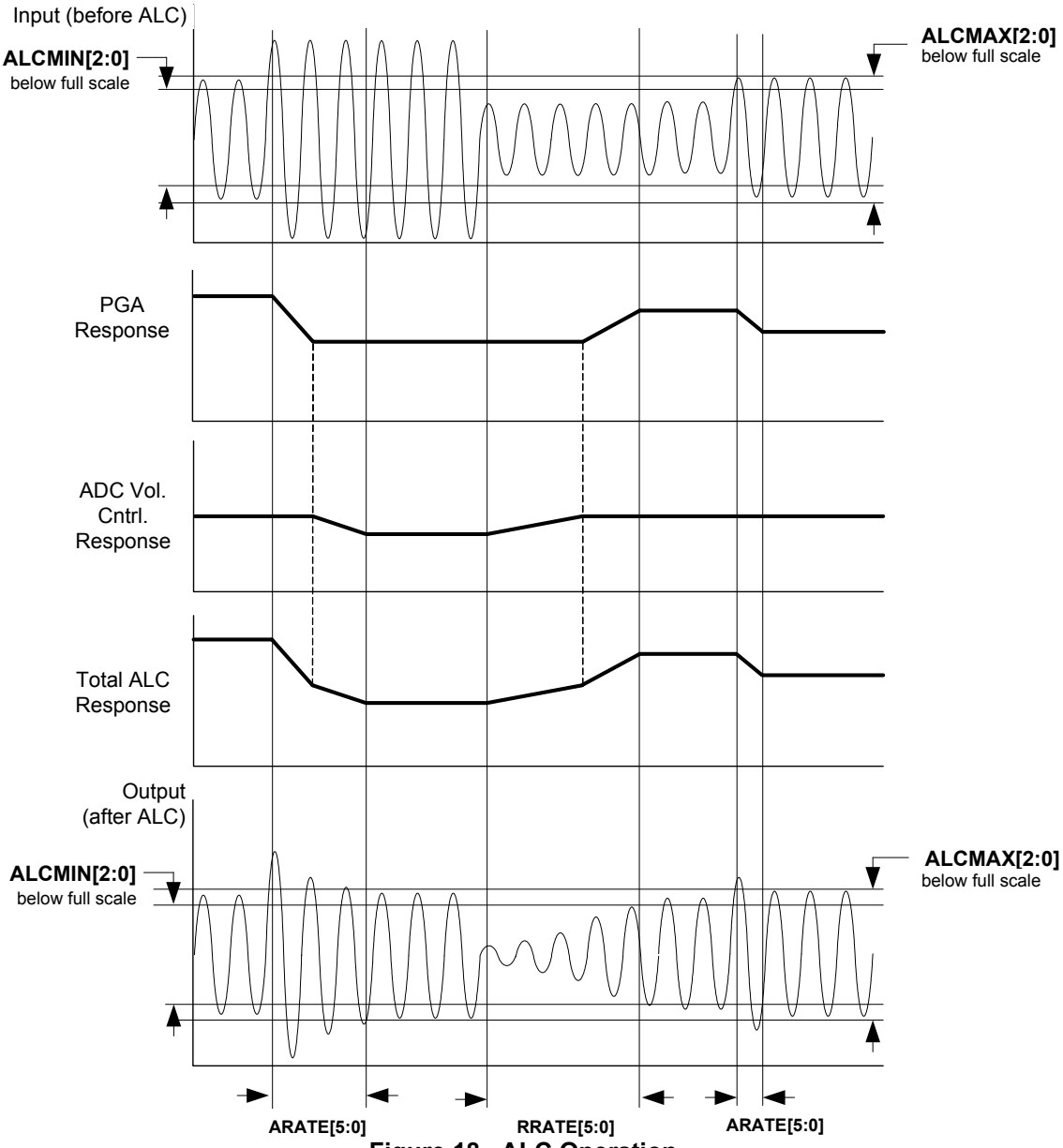


Figure 18. ALC Operation

4.2.5.1 Attack/Release Time Calculations:

The time taken by the ALC to perform an attack or a release operation is a function of the PGA/ADC digital volume control gain settings, ADC soft ramp/zero-cross settings, sample rate (Fs), maximum/minimum threshold settings, attack/release rate settings and the signal level after the digital volume control block. Since the PGA and the ADC digital volume control blocks perform gain increment/decrement steps at different rates, this must be taken into account to get an accurate attack/release time duration calculation. The attack and release rates for each block is determined by the formulas given below:

$$\text{ADC Digital Volume Attack/Release Rate} = \frac{1}{16 \cdot \text{ALCxRATE[5:0]} + 1} \quad \text{dB/LRCK}$$

$$\text{PGA Attack/Release Rate} = \frac{0.5}{16 \cdot \text{ALCxRATE[5:0]} + 1} \quad \text{dB/LRCK}$$

The maximum amount of time that can be taken by the ALC to perform an attack or release operation on a signal with a specific maximum/minimum threshold, PGA gain and ADC digital volume setting is determined by the formulae below:

For attack operations:

$$\text{Maximum Attack Time} = \frac{\text{PGAxVOL[5:0]} - (-6)}{(\text{PGA Attack Rate}) \times \text{Fs}} + \frac{(-\text{ALCMAX[2:0]})}{(\text{ADC Attack Rate}) \times \text{Fs}} \quad \text{s}$$

For release operations:

$$\text{Maximum Release Time} = \frac{\text{ADCxATT[7:0]} - \text{ALCMAX[2:0]}}{(\text{ADC Release Rate}) \times \text{Fs}} + \frac{\text{PGAxVOL[5:0]} - (-6)}{(\text{PGA Release Rate}) \times \text{Fs}} \quad \text{s}$$

Recommended settings: Best level control may be realized with a fast attack and a slow release setting with soft ramp enabled in the control registers.

It should be noted that the ALC can only apply the gain up to the amount set in the PGAxVOL and ADCxATT registers and that the ALC maintains the output signal between the ALCMIN and ALCMAX thresholds. As a result when the input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Referenced Control	Register Location
PGAxVOL[5:0]	"PGAx Volume" on page 78
ADCxATT[7:0]	"ADCx Volume" on page 78
ALCMAX[2:0], ALCMIN[2:0]	"ALC Threshold (Address 24h)" on page 80
ALCARATE[5:0]	"ALC Enable & Attack Rate (Address 22h)" on page 79
ALCRRATE[5:0]	"ALC Release Rate (Address 23h)" on page 79

4.3 Analog In to Analog Out Passthrough

The CS42L56 accommodates analog routing of the analog input signal directly to the headphone and line out amplifiers. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier without digital conversion in the ADC and DAC. This analog passthrough path reduces power consumption and is immune to modulator switching noise that could interfere with some tuners. This path is selected using the Line and/or HP mux bits and powering down the ADC.

Referenced Control	Register Location
PDN_ADCx	"Power Down ADC x" on page 59
HPxMUX	"Headphone Input Select" on page 83
LINExMUX	"Line Input Select" on page 83

4.4 Analog Outputs

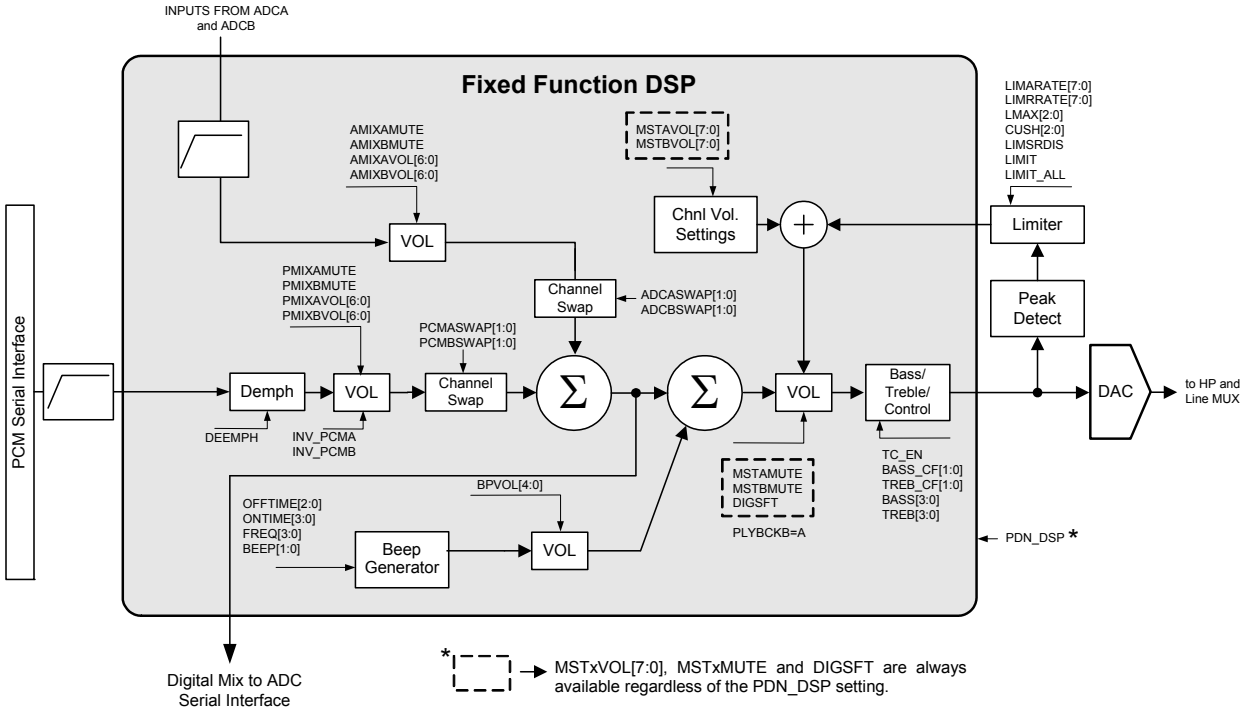


Figure 19. DSP Engine Signal Flow

Referenced Control	Register Location
DSP	
PDN_DSP	“Power Down DSP” on page 66
DEEMPH	“HP/Line De-Emphasis” on page 66
PMIXxMUTE	“PCM Mixer Channel x Mute” on page 67
PMIXxVOL[6:0]	“PCM Mixer Channel x Volume” on page 68
INV_PCMx	“Invert PCM Signal Polarity” on page 66
PCMxSWAP[1:0]	“PCM Mix Channel Swap” on page 74
AMIXxMUTE	“ADC Mixer Channel x Mute” on page 67
AMIXxVOL[6:0]	“ADC Mixer Channel x Volume” on page 67
ADCxSWAP[1:0]	“ADC Mix Channel Swap” on page 74
MSTxVOL[7:0]	“Master Volume Control” on page 70
MSTxMUTE	“Master Playback Mute” on page 67
DIGSFT	“Digital Soft Ramp” on page 64
PLYBCKB=A	“Playback Channels B=A” on page 66
TC_EN	“Tone Control Enable” on page 73
BASS_CF[1:0]	“Bass Corner Frequency” on page 73
TREB_CF[1:0]	“Treble Corner Frequency” on page 72
BASS[3:0]	“Bass Gain” on page 73
TREB[3:0]	“Treble Gain” on page 73
Limiter	
LIMIT	“Peak Detect and Limiter” on page 86
LIMIT_ALL	“Peak Signal Limit All Channels” on page 86
LIMSRDIS	“Limiter Soft Ramp Disable” on page 82
LMAX[2:0]	“Limiter Maximum Threshold” on page 85
CUSH[2:0]	“Limiter Cushion Threshold” on page 85
LIMARATE[7:0]	“Limiter Attack Rate” on page 87
LIMRRATE[7:0]	“Limiter Release Rate” on page 86
Beep Generator	Refer to “Beep Generator” on page 45 for all referenced controls

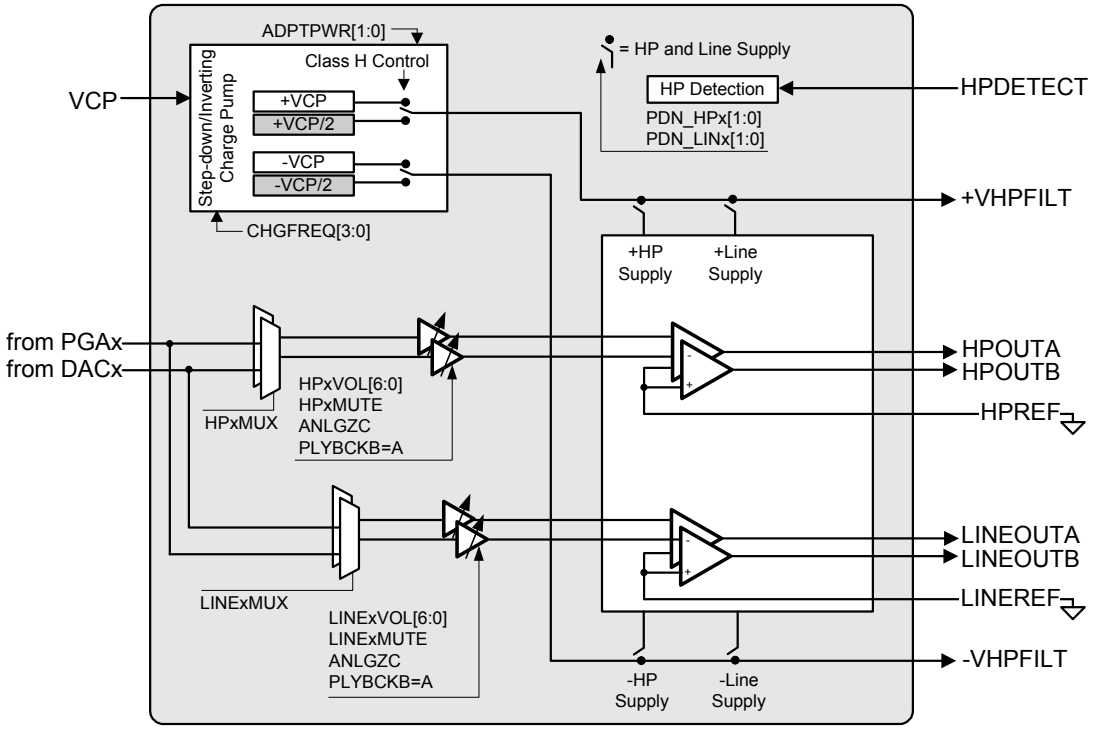


Figure 20. Analog Output Stage

Referenced Control	Register Location
Analog Output	
ADPTPWR[1:0]	"Adaptive Power Adjustment" on page 63
CHGFREQ[3:0]	"Charge Pump Frequency" on page 63
PDN_HPx[1:0]	"Headphone Power Control" on page 59
PDN_LINx[1:0]	"Line Power Control" on page 60
HPxMUTE	"Headphone Channel x Mute" on page 83
HPxVOL[7:0]	"Headphone Volume Control" on page 84
LINExMUTE	"Line Channel x Mute" on page 84
LINExVOL[7:0]	"Line Volume Control" on page 84
ANLGZC	"Analog Zero Cross" on page 64
PLYBCKB=A	"Playback Channels B=A" on page 66
HPxMUX	"Headphone Input Select" on page 83
LINExMUX	"Line Input Select" on page 83

4.5 Class H Amplifier

The CS42L56 headphone and line output amplifiers use a Cirrus Logic patented Bi-Modal Class H technology. This technology maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage that is being amplified. This prevents unnecessarily wasting energy during low power passages of program material or when the program material is played back at a low volume level.

The central component of the Bi-Modal Class H technology found in the CS42L56 is the internal charge pump, which creates the rail voltages for the headphone and line amplifiers of the device. The charge pump receives its input voltage from the voltage present on the VCP pin of the CS42L56. From this input voltage, the charge pump creates the differential rail voltages that are supplied to the amplifier output stages. The charge pump is capable of supplying two sets of differential rail voltages. One set is equal to ± VCP and the other is equal to ± VCP/2.

4.5.1 Power Control Options

The method by which the CS42L56 decides which set of rail voltages is supplied to the amplifier output stages depends on the settings of the Adaptive Power bits (ADPTPWR) found in "Class H Control (Address 08h)" section on page 63. As detailed in this section, there are four possible settings for these bits: standard Class AB mode (settings 01 and 10), adapt to volume mode (setting 00) and adapt to signal (setting 11).

Referenced Control	Register Location
ADPTPWR[1:0].....	"Adaptive Power Adjustment" on page 63

4.5.1.1 Standard Class AB Mode (setting 01 and 10)

When the Adaptive Power bits are set to either 01 or 10, the rail voltages supplied to the amplifiers will be held to ±VCP/2 or ±VCP, respectively. For these two settings, the rail voltages supplied to the output stages are held constant, regardless of the signal level, internal volume settings, or the settings of the AIN and DIN advisory volume registers. In either of these two settings, the amplifiers in the CS42L56 simply operate in a traditional Class AB configuration.

4.5.1.2 Adapt to Volume Mode (setting 00)

When the Adaptive Power bits are set to 00, the Class H controller decides which set of rail voltages to send to the amplifiers based upon the gain and attenuation levels of all active internal processing blocks. The active processing blocks are determined by the signal path configured; the configured path then dictates which volume settings affect the controller. The paths available in the CS42L56 are **(1)** analog-in to analog-out, **(2)** analog-in/digital-mix to analog-out and **(3)** digital-in to analog out.

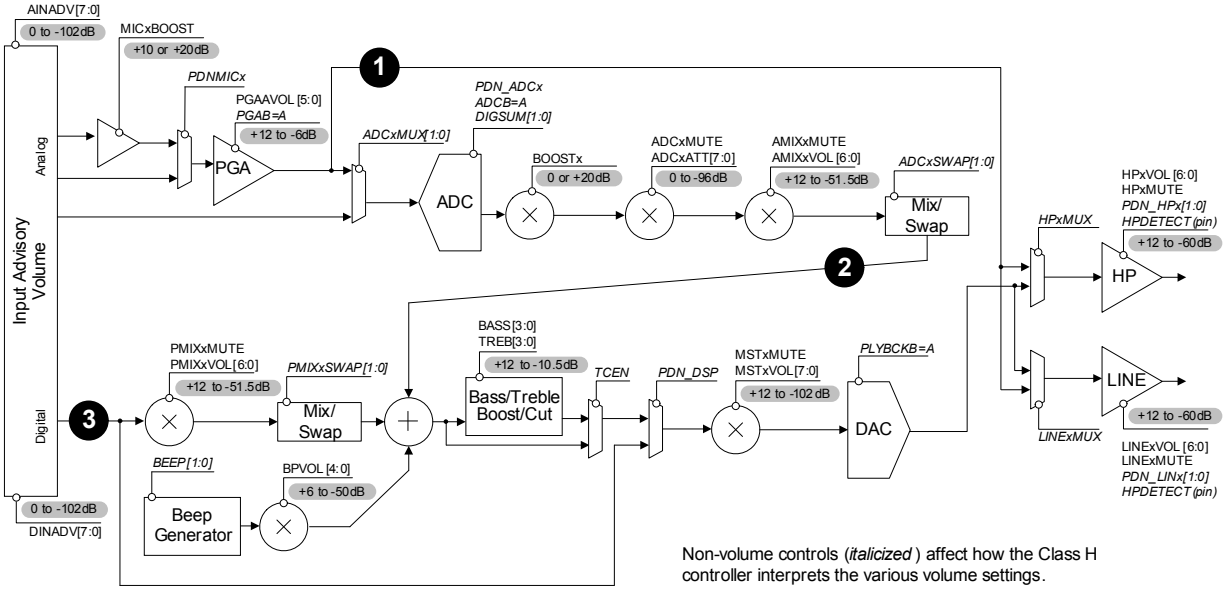


Figure 21. Class H Volume-Adapt Paths

Certain controls for the processing blocks in the signal path (such as B=A, mux, swap, mix and various enables) do not directly affect the controller's total volume sum. These controls do, however, have an indirect effect since they determine how the volume setting of the relevant processing block contributes to the controller's sum. These controls (*italicized* in Figure 21) determine whether or not the associated vol-

ume setting should be factored in with the volume settings of other control blocks in the signal path.

The Class H controller can be affected by the combined effect of all the volume settings in the relevant path or the maximum sum in each channel (A, B) and the maximum sum in each amplifier (HP, Line). To determine the correct rail voltage for the amplifier, the controller assumes the input advisory volume is set correctly and that the signal level in each processing block does not exceed 0 dB.

General Effect of Volume Sum in Signal Path

If the total gain and attenuation set in the volume control registers would cause the amplifiers to clip a full- scale signal when operating from the lower set of rail voltages, the controller instructs the charge pump to supply the higher set of the two rail voltages (±VCP) to the amplifiers (at this threshold, the total gain/attenuation has exceeded -10.5 dB).

If the total gain and attenuation set in the volume control registers would not cause the amplifiers to clip a full-scale signal when operating from the lower set of rail voltages, the controller instructs the charge pump to supply the lower set of rail voltages (±VCP/2) to the amplifiers (at this threshold, the total gain/attenuation is less than or equal to -10.5 dB).

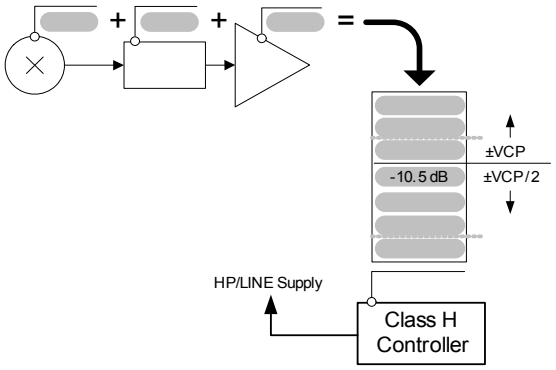


Figure 22. Volume Sum Effects

In order to adjust for external analog (line or microphone sources) or digital (DSP) input volume settings, the Class H controller also takes into account the settings of the AIN and DIN advisory volume registers. These volume settings do not affect the volume of the signal but serves to offset the total volume presented to the Class H controller.

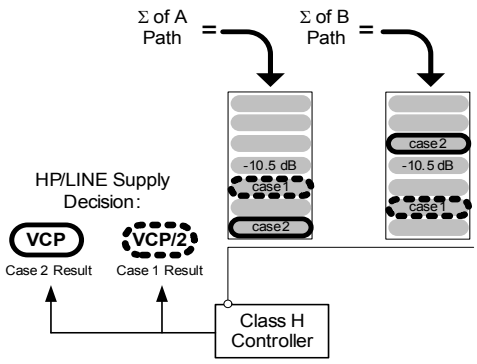


Figure 23. Channel/Amp Effect

Effect of Volume Sum in A or B Path

Since amplifier channels A and B share the same supply, the controller must consider the volume settings in the path of both these channels before supplying the appropriate rail voltage. For any of the three signal paths, the controller will instruct the charge pump to supply ±VCP to the amplifiers when the total gain/attenuation of either channel A *or* B exceeds the -10.5 dB threshold.

Conversely, the charge pump will supply ±VCP/2 only when the total gain/attenuation of both channels A *and* B is less than or equal to -10.5 dB.

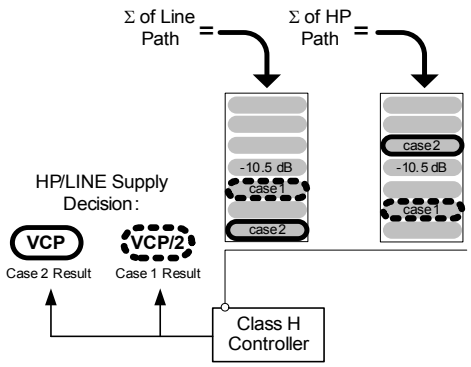


Figure 24. HP/Line Channel Effects

Effect of Volume Sum in HP or Line Paths

Since the HP and the Line amplifiers also share the same supply, the explanation above applies to the total gain/attenuation set in the HP and Line amplifiers. If enabled, the volume settings in the path of both amplifiers are considered before the charge pump supplies the appropriate rail voltage.

Referenced Control	Register Location
AINADV[7:0]	“Analog Input Advisory Volume” on page 69
MICxBOOST	“PGA x Preamplifier Gain” on page 77
PDNMICx	“Power Down MIC Bias” on page 59
PGAxVOL	“PGAx Volume” on page 78
ADCxMUX	“ADC x Input Select” on page 75
ADCxMUTE	“ADC Mute” on page 76
DIGSUM[1:0]	“Digital Sum” on page 76
PDN_DSP	“Power Down DSP” on page 66
HPxVOL[7:0]	“Headphone Volume Control” on page 84
LINExVOL[7:0]	“Line Volume Control” on page 84
MSTxVOL[7:0]	“Master Volume Control” on page 70
MSTxMUTE	“Master Playback Mute” on page 67
AMIXxVOL[6:0]	“ADC Mixer Channel x Volume” on page 67
PMIXxVOL[6:0]	“PCM Mixer Channel x Volume” on page 68
DINADV[7:0]	“Digital Input Advisory Volume” on page 69
ADCxSWP	“ADC Mix Channel Swap” on page 74
PCMxSWP	“PCM Mix Channel Swap” on page 74
HPxMUX	“Headphone Input Select” on page 83
LINExMUX	“Line Input Select” on page 83
HPxMUTE	“Headphone Channel x Mute” on page 83
LINExMUTE	“Line Channel x Mute” on page 84
PDN_HPx	“Headphone Power Control” on page 59
PDN_LINEx	“Line Power Control” on page 60
TREB	“Treble Gain” on page 73
BASS	“Bass Gain” on page 73
TCEN	“Tone Control Enable” on page 73
BEEP	“Beep Configuration” on page 72
BPVOL	“Beep Volume” on page 72
ADCB=A	“ADC Channel B=A” on page 76
PGAB=A	“PGA Channel B=A” on page 76
BOOSTx	“Boostx” on page 77
PLYBCKB=A	“Playback Channels B=A” on page 66

4.5.1.3 Adapt to Output Mode (setting 11)

When the Adaptive Power bits are set to 11, the CS42L56 decides which of the two sets of rail voltages to send to the amplifiers based solely upon the level of the signal being sent to the amplifiers. If the signal that is sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages, the control logic instructs the charge pump to provide the higher set of rail voltages (±VCP) to the amplifiers. If the signal that is sent to the amplifiers would not cause the amplifiers to clip when operating on the lower set of rail voltages, the control logic instructs the charge pump to provide the lower set of rail voltages (±VCP/2) to the amplifiers. This mode of operation eliminates the need to advise the CS42L56 of volume settings external to the device.

Note: Signal detection is implemented using digital circuitry. This mode should, therefore, not be used with analog passthrough (PGA to HP/Line).

4.5.2 Power Supply Transitions

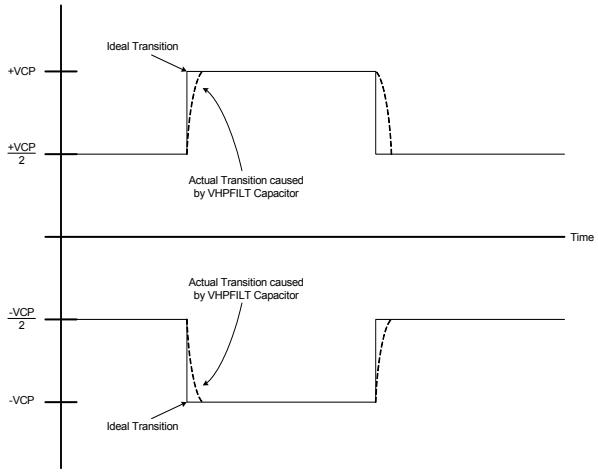


Figure 25. VHPFILT Transitions

Charge pump transitions from the lower set of rail voltages to the higher set of rail voltages occur on the next FLYN/P clock cycle. Despite the fast response time of the system, the capacitive elements on the VHPFILT pins prevent the rail voltages from changing instantaneously. Instead, the rail voltages ramp up from ±VCP/2 to ±VCP based on the time constant created by the output impedance of the charge pump and the capacitor on the VHPFILT pin (the transition time is approximately 20 µs).

This behavior is detailed in Figure 25. During this charging transition, a high dv/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full ±VCP level. This transitory clipping has been found to be inaudible in listening tests.

When the charge pump transitions from the higher set of rail voltages to the lower set, there is a one second delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high level transients in the input signal. The diagram for this transitional behavior is detailed in Figure 26.

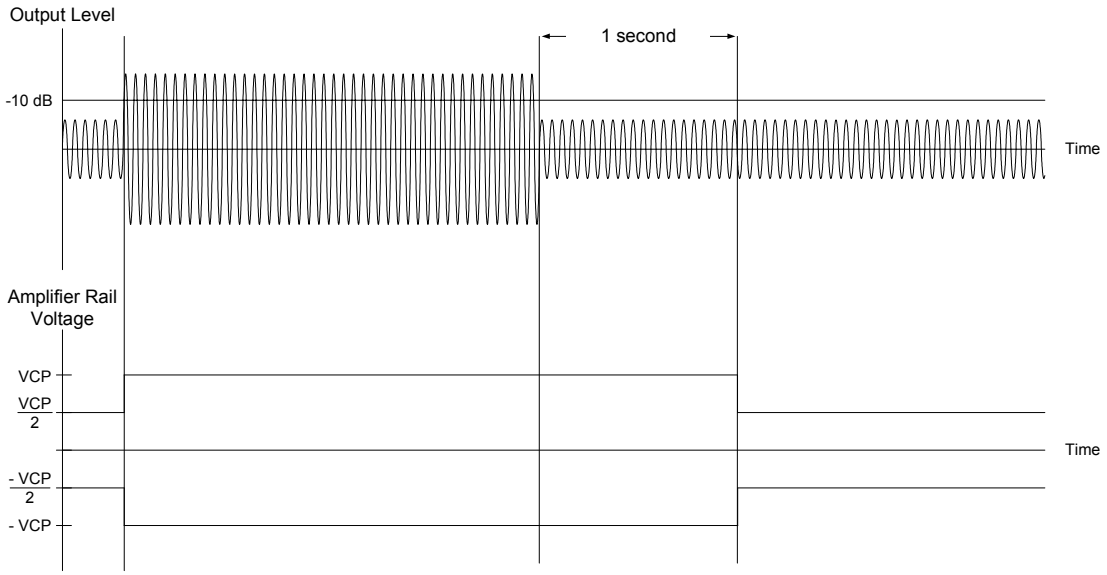


Figure 26. VHPFILT Hysteresis

4.5.3 *Efficiency*

As discussed in previous sections, the amplifiers internal to the CS42L56 operate from one of two sets of rail voltages, based upon the needs of the signal being amplified or the total gain/attenuation settings. The power curves for the two modes of operation are shown in Figure 27 and Figure 28.

This graph details the power supplied to a load versus the power drawn from the supply for each of the three use cases.

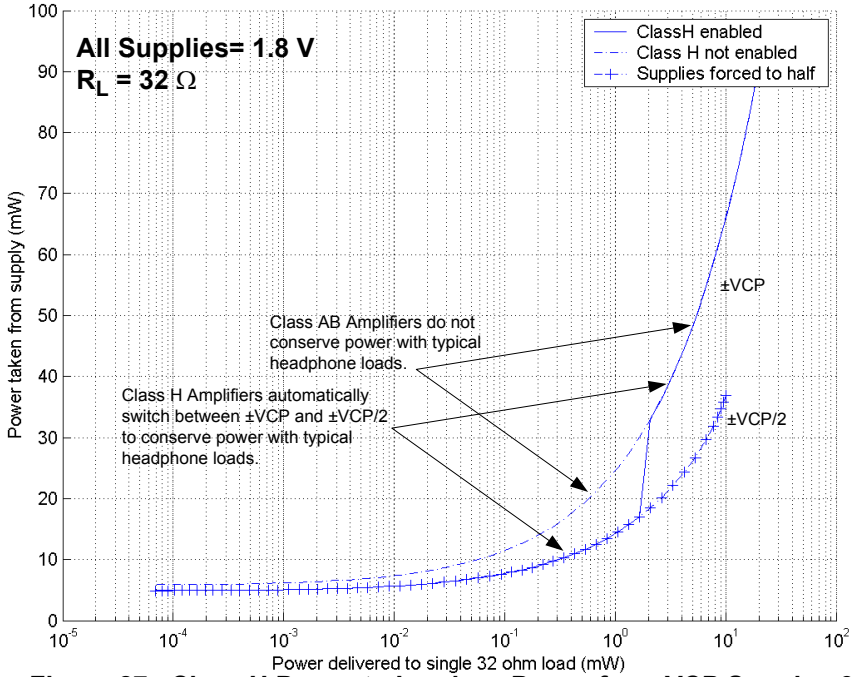


Figure 27. Class H Power to Load vs. Power from VCP Supply - 32 Ω

When the rail voltages are set to VCP, the amplifiers will operate in their least efficient mode. When the rail voltages are held at ±VCP/2, the amplifiers will operate in their most efficient mode, but will be clipped if required to amplify a full-scale signal. Note: The ±VCP/2 curve ends at the point at which the output of the amplifiers reaches 10% THD+N.

The benefit of Bi-Modal Class H is shown in the solid trace on the graph. At lower output levels, the amplifiers operate on the ±VCP/2 curve. At higher output levels, they operate on the ±VCP curve. The duration the amplifiers will operate on either of the two curves (±VCP/2 or ±VCP) depends on both the content and the output level of the program material being amplified. The highest efficiency operation will result from maintaining an output level that is close to, but not exceeding, the clip threshold of the ±VCP/2 curve.

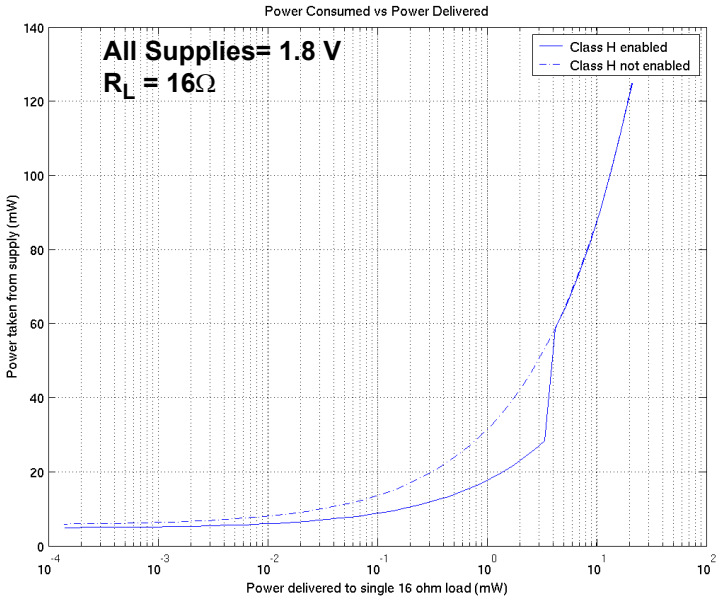


Figure 28. Class H Power to Load vs. Power from VCP Supply - 16 Ω

4.6 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple, and single (one-shot) beeps. Sixteen On and eight Off times are available.

It should be noted that the beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be necessary to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, the DAC volume may alternatively be controlled using the PMIXxVOL[6:0] bits.

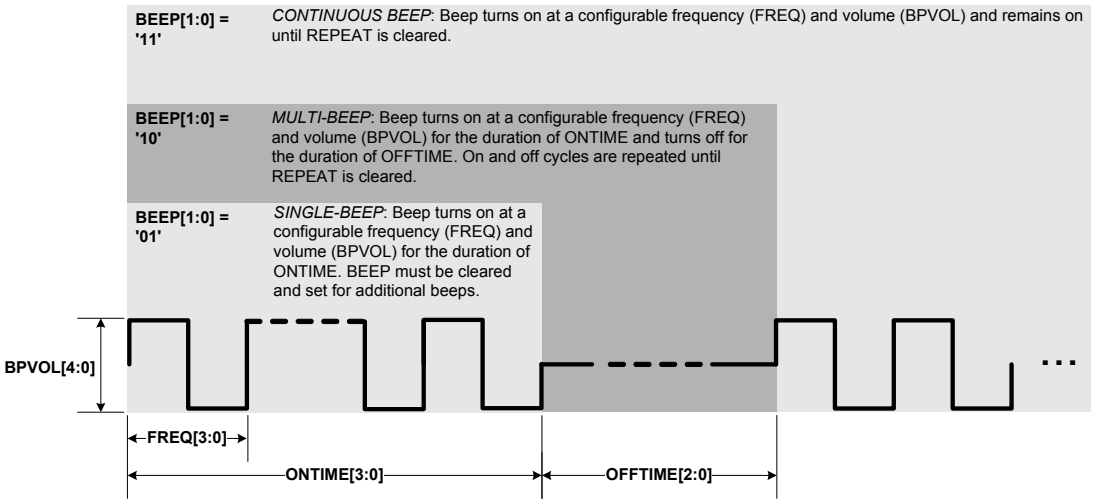


Figure 29. Beep Configuration Options

Referenced Control	Register Location
MSTxVOL[7:0]	"Master Volume Control: MSTA (Address 13h) & MSTB (Address 14h)" on page 70
PMIXxVOL[6:0]	"PCMx Mixer Volume: PCMA (Address 0Fh) & PCMB (Address 10h)" on page 68
OFFTIME[2:0]	"Beep Off Time" on page 71
ONTIME[3:0]	"Beep On Time" on page 71
FREQ[3:0]	"Beep Frequency" on page 70
BEEP[1:0]	"Beep Configuration" on page 72
BPVOL[4:0]	"Beep Volume" on page 72

4.7 Limiter

When enabled, the limiter monitors the digital input signal before the DAC modulators, detects when levels exceed the maximum threshold settings and lowers the master volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Master Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp settings and sample rate, Fs. Limiter soft ramp dependency may be independently enabled/disabled using the LIMSRDIS.

It should be noted that the Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds

Recommended settings: Best limiting performance may be realized with a fast attack and a slow release setting with soft ramp enabled in the control registers. The CUSH bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.

Referenced Control	Register Location
Limiter Rates	"Limiter Release Rate" on page 86, "Limiter Attack Rate" on page 87
Limiter Thresholds	"Limiter Maximum Threshold" on page 85, "Limiter Cushion Threshold" on page 85
LIMSRDIS	"Limiter Soft Ramp Disable" on page 82
Master Volume Control	"Master Volume Control: MSTA (Address 13h) & MSTB (Address 14h)" on page 70

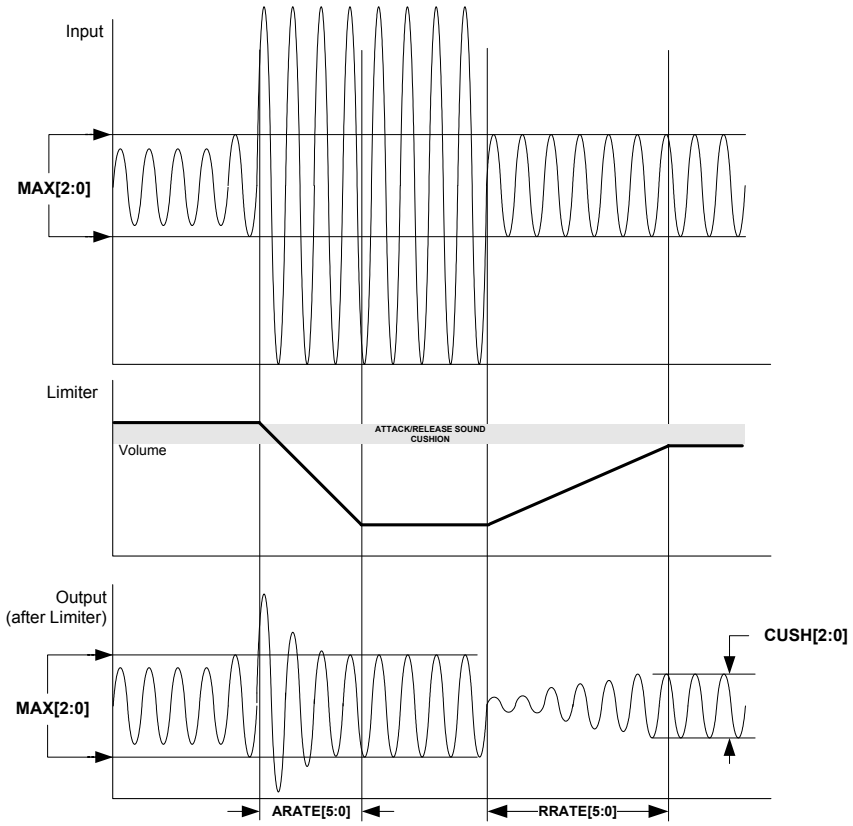


Figure 30. Peak Detect & Limiter

4.8 Serial Port Clocking

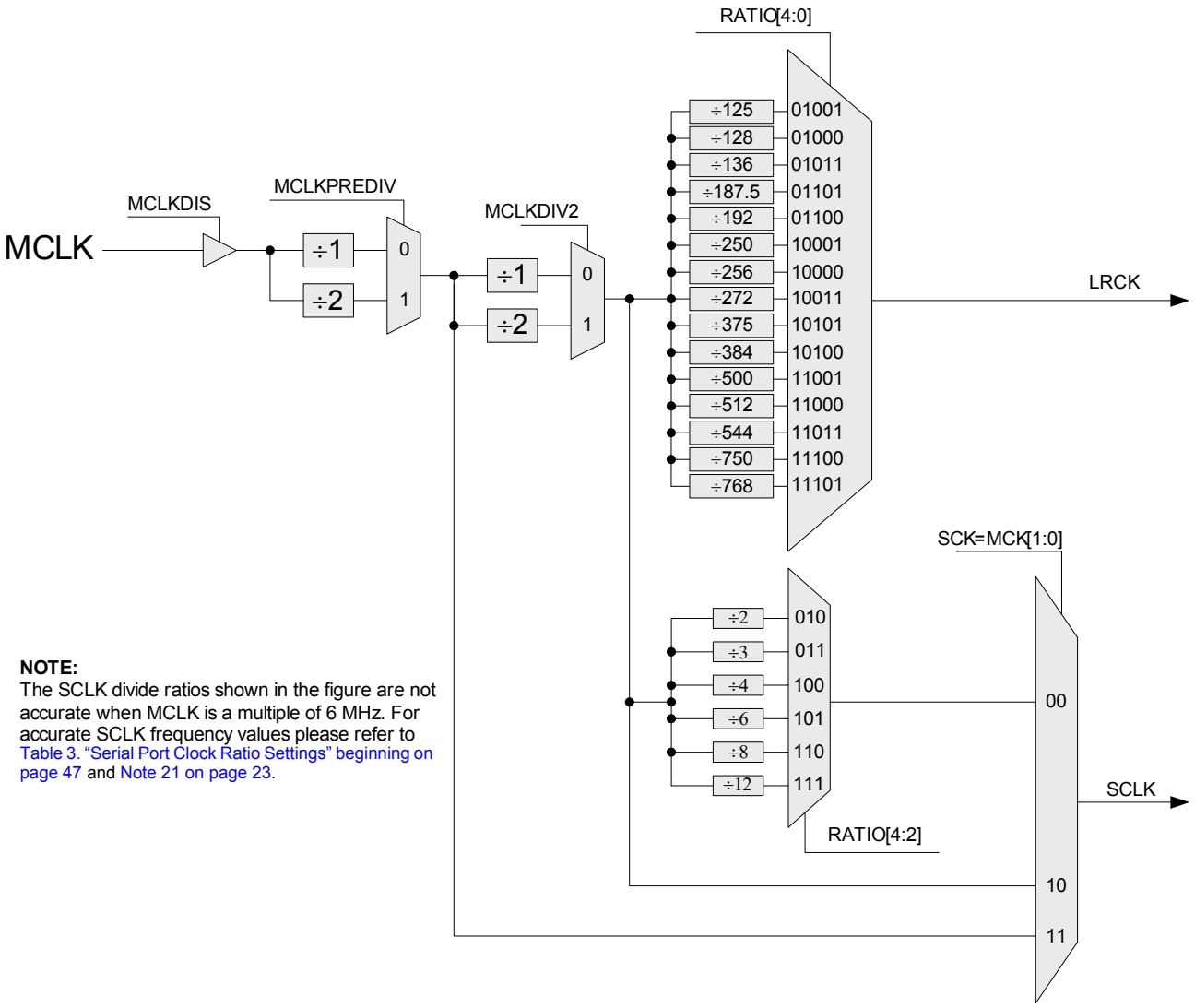
The CODEC serial audio interface port operates either as a slave or master. It accepts externally generated clocks in Slave Mode (M/$\overline{S}$ = 0b) and will generate synchronous clocks derived from an input master clock (MCLK) in Master Mode (M/$\overline{S}$ = 1b). The RATIO[4:0] bits need to be set appropriately according to the clocks being used in the system for correct device functionality. Table 3. "Serial Port Clock Ratio Settings" beginning on page 47 shows possible clock frequencies achievable by the CS42L56 serial port and provides a reference on how the RATIO[4:0] bits need to be configured for different clock ratios. Figure 31 shows how SCLK and LRCK are internally derived in Master Mode.

MCLK (MHz)	LRCK (kHz)	MCLK/ LRCK Clock Ratio	SCLK (MHz)	MCLK/SCLK Clock Ratio	RATIO[4:0]
22.5792 (MKPREDIV=1b) (MCLKDIV2=1b)	11.0250	2048	0.7056	32	11000
	22.0500	1024	1.4112	16	10000
	44.1000	512	2.8224	8	01000
11.2896 (MKPREDIV=0b) (MCLKDIV2=1b)	11.0250	1024	0.7056	16	11000
	22.0500	512	1.4112	8	10000
	44.1000	256	2.8224	4	01000
5.6448 (MKPREDIV=0b) (MCLKDIV2=0b)	11.0250	512	0.7056	8	11000
	22.0500	256	1.4112	4	10000
	44.1000	128	2.8224	2	01000

Table 3. Serial Port Clock Ratio Settings

MCLK (MHz)	LRCK (kHz)	MCLK/ LRCK Clock Ratio	SCLK (MHz)	MCLK/SCLK Clock Ratio	RATIO[4:0]
24.0000 (MKPREDIV=1b) (MCLKDIV2=1b)	8.0000	3000	0.496	~48	11101
	11.0294	2176	0.75	32	11011
	12.0000	2000	0.744	~32	11001
	16.0000	1500	0.992	~24	10101
	22.0588	1088	1.500	16	10011
	24.0000	1000	1.488	~16	10001
	32.0000	750	1.984	~12	01101
	44.1180	544	3.000	8	01011
	48.0000	500	2.976	~8	01001
12.0000 (MKPREDIV=0b) (MCLKDIV2=1b)	8.0000	1500	0.496	~24	11101
	11.0294	1088	0.75	16	11011
	12.0000	1000	0.744	~16	11001
	16.0000	750	0.992	~12	10101
	22.0588	544	1.500	8	10011
	24.0000	500	1.488	~8	10001
	32.0000	375	1.984	~6	01101
	44.1180	272	3.000	4	01011
	48.0000	250	2.976	~4	01001
6.0000 (MKPREDIV=0b) (MCLKDIV2=0b)	8.0000	750	0.496	~12	11101
	11.0294	544	0.75	8	11011
	12.0000	500	0.744	~8	11001
	16.0000	375	0.992	~6	10101
	22.0588	272	1.500	4	10011
	24.0000	250	1.488	~4	10001
	32.0000	187.5	1.984	~3	01101
	44.1180	136	3.000	2	01011
	48.0000	125	2.976	~2	01001
24.5760 (MKPREDIV=1b) (MCLKDIV2=1b)	8.0000	3072	0.512	48	11100
	12.0000	2048	0.768	32	11000
	16.0000	1536	1.024	24	10100
	24.0000	1024	1.536	16	10000
	32.0000	768	2.048	12	01100
	48.0000	512	3.072	8	01000
12.2880 (MKPREDIV=0b) (MCLKDIV2=1b)	8.0000	1536	0.512	24	11100
	12.0000	1024	0.768	16	11000
	16.0000	768	1.024	12	10100
	24.0000	512	1.536	8	10000
	32.0000	384	2.048	6	01100
	48.0000	256	3.072	4	01000
6.1440 (MKPREDIV=0b) (MCLKDIV2=0b)	8.0000	768	0.512	12	11100
	12.0000	512	0.768	8	11000
	16.0000	384	1.024	6	10100
	24.0000	256	1.536	4	10000
	32.0000	192	2.048	3	01100
	48.0000	128	3.072	2	01000

Table 3. Serial Port Clock Ratio Settings (Continued)



NOTE:
The SCLK divide ratios shown in the figure are not accurate when MCLK is a multiple of 6 MHz. For accurate SCLK frequency values please refer to Table 3. "Serial Port Clock Ratio Settings" beginning on page 47 and Note 21 on page 23.

Figure 31. Serial Port Timing in Master Mode

Referenced Control	Register Location
SCK=MCK[1:0]	"SCLK Equals MCLK" on page 60
MKPREDIV	"MCLK Pre-Divide" on page 60
MCLKDIV2	"MCLK Divide" on page 61
MCLKDIS	"MCLK Disable" on page 61
RATIO[4:0]	"Clock Ratio" on page 62

4.9 Digital Interface Format

The serial port operates in standard I²S or Left-Justified digital interface formats with varying bit depths from 16 to 24. Data is clocked out of the ADC or into the DAC on the rising edge of SCLK. Figures 32-33 illustrate the general structure of each format. Refer to "Switching Specifications - Serial Port" on page 23 for exact timing relationship between clocks and data.

For additional information, application note AN282 presents a tutorial of the 2-channel serial audio interface. AN282 can be downloaded from the Cirrus Logic web site at http://www.cirrus.com.

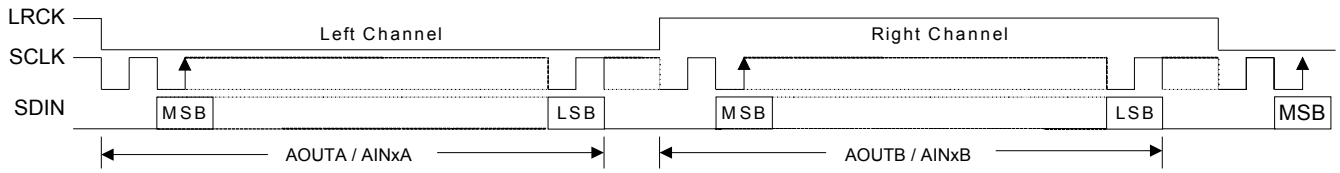


Figure 32. I²S Format

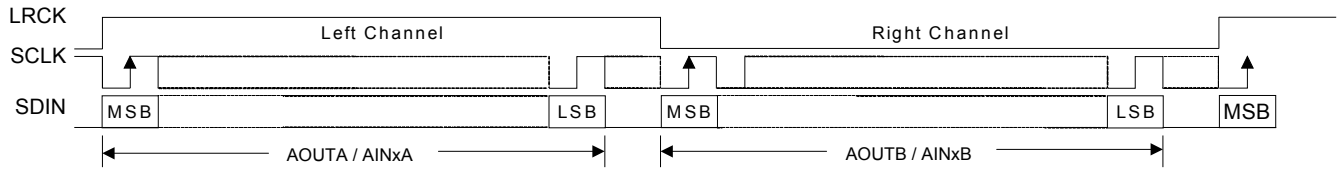


Figure 33. Left-Justified Format

4.10 Initialization

The CODEC enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The charge pump, LDO, internal voltage reference and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in the "Register Description" on page 58.

After the PDN bit is released and MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. MCLK occurrences are counted over one LRCK period to determine a valid MCLK/LRCK ratio and normal operation begins.

4.11 Recommended DAC to HP or Line Power Sequence

4.11.1 Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable. **Note:** VA must be applied prior to VCP to maintain the relationship specified in "Recommended Operating Conditions" on page 14. $\overline{\text{RESET}}$ should be held low for a minimum of 1 ms after power supplies are stable.
2. Apply MCLK at the appropriate frequency, as discussed in Section 4.8. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
3. Bring $\overline{\text{RESET}}$ high.

4. Wait a minimum of 500 ns before writing to the control port.
5. The default state of the master power down bit, PDN, is 1b. Load the following register settings while keeping the PDN bit set to 1b.
6. Configure the headphone and line power down controls for ON, OFF, or HPDETECT operation.
   Register Controls: **PDN_HPx[1:0], PDN_LINx[1:0]**
7. Configure the serial port I/O control for master or slave operation.
   Register Controls: **M/S**
8. Configure the master clock (MCLK) and bit clock (SCLK) I/O control as desired. Refer to 4.8 “Serial Port Clocking” on page 47 for the required configuration for a given master clock.
   Register Controls: MKPREDIV, **MCLKDIV2, SCLK=MCLK**
9. Configure the sample rate (LRCK) controls for the desired sample rate. Refer to 4.8 “Serial Port Clocking” on page 47 for the required configuration for a given sample rate.
   Register Controls: **See Register 05h**
10. The default state of the DSP engine’s power down bit, PDN_DSP, is 0b. It is not necessary to power down the DSP before changing the various DSP functions. The DSP may be powered down for additional power savings.
11. To minimize pops on the headphone or line amplifier, each respective analog volume control must first be muted and set to maximum attenuation.
    Register Controls: **HPxMUTE, LINExMUTE, HPxVOL[6:0], LINExVOL[6:0]**
12. After muting the headphone or line amplifiers, set the PDN bit to 0b.
13. Wait 75 ms for the headphone or line amplifier to power up.
14. Un-mute and ramp the volume for the headphone or line amplifiers to the desired level.
15. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Power Up Sequence	Register Location
Step 5, 12	“Power Down” on page 59
Step 6	“Power Control 2 (Address 04h)” on page 59
Steps 7-8	“Clocking Control 1 (Address 05h)” on page 60
Step 9	“Clocking Control 2 (Address 06h)” on page 61
Step 10	“Power Down DSP” on page 66
Step 11a,14a	“Headphone Channel x Mute” on page 83, “Line Channel x Mute” on page 84
Step 11b,14b	“Headphone Volume Control” on page 84, “Line Volume Control” on page 84

4.11.2 Power-Down Sequence

1. To minimize pops during volume transitions, mute the master volume with soft ramp enabled.
   Register Controls: **MSTxMUTE, DIGSFT**
2. The required wait time for muting the master volume as described in 1 above depends on the soft ramp rate, initial master volume setting and sample rate. For example, if the master volume is set to 0 dB and the sample rate is 48 kHz, the required wait time is at least:
   8 [soft ramp rate is 1/8 dB per LRCK] **x 102** [volume must transition from 0 dB to -102 dB] x 21 µs [period of 48 kHz LRCK] **= 17 ms**. Wait at least [the delay required according to the details in this step].
3. To minimize pops on the headphone or line amplifier, each respective analog volume control must first be muted and set to maximum attenuation.
   Register Controls: **HPxMUTE, LINExMUTE, HPxVOL[6:0], LINExVOL[6:0]**
4. Disable soft ramp and zero cross volume transitions.
   Register Controls: **ANLGSFT, ANLGZC, DIGSFT**
5. Set the PDN bit to ‘1’b.
6. Wait at least 100 µs.

The CODEC will be fully powered down after this 100 µs delay. Prior to the removal of the master clock (MCLK), this delay of at least 100 µs must be implemented after step 5 to avoid premature disruption of the CODEC's power down sequence. A disruption in the CODEC's power down sequence may abruptly stop the charge pump, causing the headphone and/or line amplifiers to drive the outputs up to the VCP supply. Such disruption may also cause clicks and pops on the output of the DAC's.

7. Optionally, MCLK may be removed at this time.
8. To achieve the lowest operating quiescent current, bring $\overline{\text{RESET}}$ low. All control port registers will be reset to their default state.
9. Power Supply Removal (Option 1): Switch power supplies to a high impedance state. **Note:** VCP must be removed prior to VA to maintain the relationship specified in "Recommended Operating Conditions" on page 14.
10. Power Supply Removal (Option2): To minimize pops when the power supplies are pulled to ground, a discharge resistor must be added in parallel with the capacitor on the FILT+ pin. With a 1 MΩ resistor and a 2.2 µF capacitor on FILT+, FILT+ will ramp to ground in approximately 5 seconds.

    After step 5, wait the required time for FILT+ to ramp to ground before pulling VA to ground. **Note:** VCP must be pulled to ground prior to VA to maintain the relationship specified in "Recommended Operating Conditions" on page 14.

Power Down Sequence	Register Location
Step 1a	"Headphone Volume Control" on page 84, "Line Volume Control" on page 84
Step 1b	"Headphone Channel x Mute" on page 83, "Line Channel x Mute" on page 84
Step 4	"Analog Soft Ramp" on page 64, "Analog Zero Cross" on page 64, "Digital Soft Ramp" on page 64
Step 5	"Power Down" on page 59

4.12 Recommended PGA to HP or Line Power Sequence (Analog Passthrough)

4.12.1 Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable. **Note:** VA must be applied prior to VCP to maintain the relationship specified in "Recommended Operating Conditions" on page 14. $\overline{\text{RESET}}$ should be held low for a minimum of 1 ms after power supplies are stable.
2. Apply MCLK at the appropriate frequency.
3. Bring $\overline{\text{RESET}}$ high.
4. Wait a minimum of 500 ns before writing to the control port.
5. The default state of the master power down bit, PDN, is '1'b. Load the following register settings while keeping the PDN bit set to '1'b.
6. Configure the headphone and line power down controls for ON, OFF, or HPDETECT operation.
   Register Controls: **PDN_HPx[1:0], PDN_LINx[1:0]**
7. Configure the HP and/or Line amplifiers to receive the analog output from the PGA.
   Register Controls: **LINExMUX, HPxMUX**
8. Power down the DSP engine.
   Register Controls: **PDN_DSP**
9. To minimize pops on the headphone or line amplifier, each respective analog volume control must first be muted and set to maximum attenuation.
   Register Controls: **HPxMUTE, LINExMUTE, HPxVOL[6:0], LINExVOL[6:0]**
10. After muting the headphone and/or line amplifiers, set the PDN bit to '0'b.
11. Wait 75 ms for the headphone or line amplifier to power up.
12. Un-mute and ramp the volume for the headphone or line amplifiers to the desired level.

13. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Power Up Sequence	Register Location
Step 5, 10	"Power Down" on page 59
Step 6	"Power Control 2 (Address 04h)" on page 59
Steps 7	"AIN Reference Configuration, ADC MUX (Address 1Ah)" on page 74
Step 8	"Power Down DSP" on page 66
Step 9a,12a	"Headphone Channel x Mute" on page 83, "Line Channel x Mute" on page 84
Step 9b,12b	"Headphone Volume Control" on page 84, "Line Volume Control" on page 84

4.12.2 Power-Down Sequence

1. To minimize pops on the headphone and/or line amplifier, each respective analog volume control must first be muted and set to maximum attenuation. To reduce the volume transition delay while minimizing pops, enable the analog zero cross function and disable the analog soft ramp function.
   Register Controls: **HPxMUTE, LINExMUTE, HPxVOL[6:0], LINExVOL[6:0], ANLGSFT, ANLGZC**
2. The required wait time for muting the analog volume as described in 1 above depends on the worst case zero cross timeout of 150 ms in passthrough mode. Wait at least 150 ms.
3. Disable soft ramp and zero cross volume transitions.
   Register Controls: **ANLGZC, DIGSFT**
4. Set the PDN bit to '1'b.
5. Wait at least 100 µs.
   The CODEC will be fully powered down after this 100 µs delay. Prior to the removal of the master clock (MCLK), this delay of at least 100 µs must be implemented after step 4 to avoid premature disruption of the CODEC's power down sequence. A disruption in the CODEC's power down sequence may abruptly stop the charge pump, causing the headphone and/or line amplifiers to drive the outputs up to the VCP supply. Such disruption may also cause clicks and pops on the output of the DAC's.
6. Optionally, MCLK may be removed at this time.
7. To achieve the lowest operating quiescent current, bring $\overline{\text{RESET}}$ low. All control port registers will be reset to their default state.
8. Power Supply Removal (Option 1): Switch power supplies to a high impedance state. **Note:** VCP must be removed prior to VA to maintain the relationship specified in "Recommended Operating Conditions" on page 14.
9. Power Supply Removal (Option 2): To minimize pops when the power supplies are pulled to ground, a discharge resistor must be added in parallel with the capacitor on the FILT+ pin. With a 1 MΩ resistor and a 2.2 µF capacitor on FILT+, FILT+ will ramp to ground in approximately 5 seconds.

   After step 5, wait the required time for FILT+ to ramp to ground before pulling VA to ground. **Note:** VCP must be pulled to ground prior to VA to maintain the relationship specified in "Recommended Operating Conditions" on page 14.

Power Down Sequence	**Register Location**
Step 1a	"Analog Soft Ramp" on page 64, "Analog Zero Cross" on page 64
Step 1b	"Headphone Volume Control" on page 84, "Line Volume Control" on page 84
Step 1c	"Headphone Channel x Mute" on page 83, "Line Channel x Mute" on page 84
Step 3	, "Analog Zero Cross" on page 64, "Digital Soft Ramp" on page 64
Step 4	"Power Down" on page 59

4.13 Control Port Operation

The control port is used to access the registers allowing the CODEC to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The device enters software mode only after a successful write command using one of two software protocols: SPI or I²C, with the device acting as a slave. The SPI protocol is permanently selected whenever there is a high-to-low transition on the AD0/CS pin after reset. If using the I²C protocol, pin AD0/CS should be permanently connected to either VL or GND; this option allows the user to slightly alter the chip address as desired.

4.13.1 SPI Control

In Software Mode, $\overline{CS}$ is the CS42L56 chip-select signal, CCLK is the control port bit clock (input into the CS42L56 from the microcontroller), CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The CODEC will only support write operations. Read request will be ignored.

Figure 34 shows the operation of the control port in Software Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001010. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

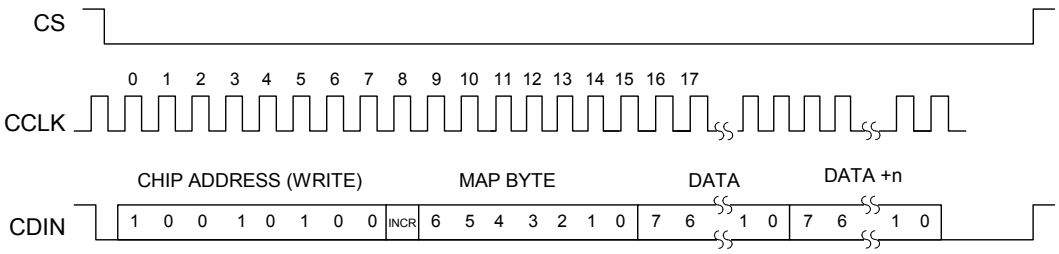


Figure 34. Control Port Timing in SPI Mode

4.13.2 I²C Control

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. The signal timings for a read and write cycle are shown in Figure 35 and Figure 36. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42L56 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write).

The upper 6 bits of the address field are fixed at 100101. Pin ADO forms the least significant bit of the chip address and should be connected to VL or DGND as desired. To communicate with the CS42L56, the chip address field, which is the first byte sent to the CS42L56, should match 100101+AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP); the MAP selects the register to be read or written. If the operation is a read, the contents of the

register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42L56 after each input byte is read and is input to the CS42L56 from the microcontroller after each transmitted byte.

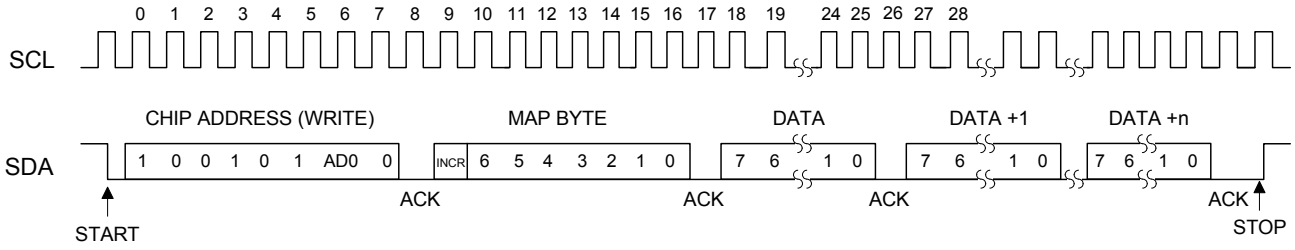


Figure 35. Control Port Timing, I²C Write

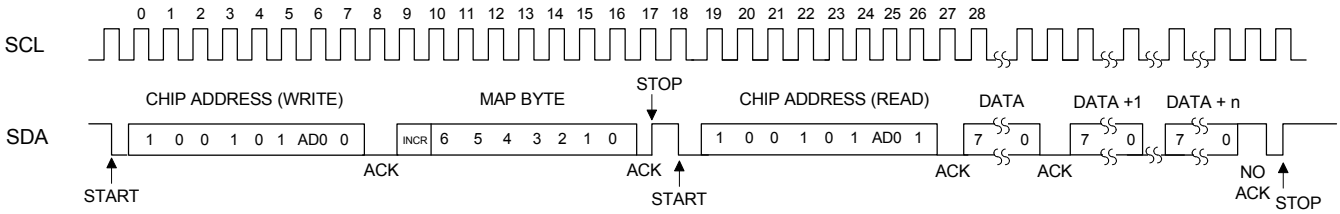


Figure 36. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 36, the write operation is aborted (after the acknowledge for the MAP byte) by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 10010100 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto-increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010101 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.13.3 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.13.3.1 Map Increment (INCR)

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

5. REGISTER QUICK REFERENCE

Default values are shown below the bit names. Unless otherwise specified, all “Reserved” bits must maintain their default value.

Adr.	Function	7	6	5	4	3	2	1	0
01h p 58	ID 1 *(Read Only)*	DEVID7 x	DEVID6 x	DEVID5 x	DEVID4 x	DEVID3 x	DEVID2 x	DEVID1 x	DEVID0 x
02h p 58	ID 2 *(Read Only)*	Reserved x	Reserved x	Reserved x	AREVID2 x	AREVID1 x	AREVID0 x	MTLREVID1 x	MTLREVID0 x
03h p 58	Power Ctl 1	Reserved 1	Reserved 1	PDN_VBUF 1	PDN_BIAS 1	PDN_CHRG 1	PDN_ADCB 1	PDN_ADCA 1	PDN 1
04h p 59	Power Ctl 2	PDN_HPB1 1	PDN_HPB0 1	PDN_HPA1 1	PDN_HPA0 1	PDN_LINB1 1	PDN_LINB0 1	PDN_LINA1 1	PDN_LINA0 1
05h p 60	Clocking Ctl 1	Reserved 0	M/S 0	INV_SCLK 0	SCK=MCK1 0	SCK=MCK0 0	MKPREDIV 0	MCLKDIV2 0	MCLKDIS 0
06h p 61	Clocking Ctl 2	Reserved 0	Reserved 0	AUTO 0	RATIO4 0	RATIO3 1	RATIO2 0	RATIO1 1	RATIO0 1
07h p 62	Serial Format	Reserved 0	Reserved 0	Reserved 0	Reserved 0	DIF 0	Reserved 0	Reserved 0	Reserved 0
08h p 63	Class H Ctl	ADPTPWR1 0	ADPTPWR0 0	Reserved 0	Reserved 0	CHGFREQ3 0	CHGFREQ2 1	CHGFREQ1 0	CHGFREQ0 1
09h p 63	Misc. Ctl	DIGMUX 0	Reserved 0	Reserved 0	ANLGSFT 0	ANLGZC 1	DIGSFT 1	Reserved 0	FREEZE 0
0Ah p 65	Status *(Read Only)*	HPDETECT 0	SPCLKERR 0	DSPBOVFL 0	DSPAOVFL 0	MIXBOVFL 0	MIXAOVFL 0	ADCBOVFL 0	ADCAOVFL 0
0Bh p 66	Playback Ctl	PDN_DSP 0	DEEMPH 0	Reserved 0	PLYBCKB=A 0	INV_PCMB 0	INV_PCMA 0	Reserved 0	Reserved 0
0Ch p 67	DSP Mute Ctl	AMIXBMUTE 1	AMIXAMUTE 1	PMIXBMUTE 0	PMIXAMUTE 0	Reserved 0	Reserved 0	MSTBMUTE 0	MSTAMUTE 0
0Dh p 67	ADCMIXA Vol	AMIXAVOL7 0	AMIXAVOL6 0	AMIXAVOL5 0	AMIXAVOL4 0	AMIXAVOL3 0	AMIXAVOL2 0	AMIXAVOL1 0	AMIXAVOL0 0
0Eh p 67	ADCMIXB Vol	AMIXBVOL7 0	AMIXBVOL6 0	AMIXBVOL5 0	AMIXBVOL4 0	AMIXBVOL3 0	AMIXBVOL2 0	AMIXBVOL1 0	AMIXBVOL0 0
0Fh p 68	PCMMIXA Vol	PMIXAVOL7 0	PMIXAVOL6 0	PMIXAVOL5 0	PMIXAVOL4 0	PMIXAVOL3 0	PMIXAVOL2 0	PMIXAVOL1 0	PMIXAVOL0 0
10h p 68	PCMMIXB Vol	PMIXBVOL7 0	PMIXBVOL6 0	PMIXBVOL5 0	PMIXBVOL4 0	PMIXBVOL3 0	PMIXBVOL2 0	PMIXBVOL1 0	PMIXBVOL0 0
11h p 69	Analog Input Advisory Vol	AINADV7 0	AINADV6 0	AINADV5 0	AINADV4 0	AINADV3 0	AINADV2 0	AINADV1 0	AINADV0 0
12h p 69	Digital Input Advisory Vol	DINADV7 0	DINADV6 0	DINADV5 0	DINADV4 0	DINADV3 0	DINADV2 0	DINADV1 0	DINADV0 0
13h p 70	Master A Vol	MSTAVOL7 0	MSTAVOL6 0	MSTAVOL5 0	MSTAVOL4 0	MSTAVOL3 0	MSTAVOL2 0	MSTAVOL1 0	MSTAVOL0 0
14h p 70	Master B Vol	MSTBVOL7 0	MSTBVOL6 0	MSTBVOL5 0	MSTBVOL4 0	MSTBVOL3 0	MSTBVOL2 0	MSTBVOL1 0	MSTBVOL0 0
15h p 70	BEEP Freq, On Time	FREQ3 0	FREQ2 0	FREQ1 0	FREQ0 0	ONTIME3 0	ONTIME2 0	ONTIME1 0	ONTIME0 0
16h p 71	BEEP Vol, Off Time	OFFTIME2 0	OFFTIME1 0	OFFTIME0 0	BPVOL4 0	BPVOL3 0	BPVOL2 0	BPVOL1 0	BPVOL0 0
17h p 72	BEEP, Tone Cfg.	BEEP1 0	BEEP0 0	Reserved 0	TREB_CF1 0	TREB_CF0 0	BASS_CF1 0	BASS_CF0 0	TC_EN 0
18h p 73	Tone Ctl	TREB3 1	TREB2 0	TREB1 0	TREB0 0	BASS3 1	BASS2 0	BASS1 0	BASS0 0
19h p 74	Channel Mixer & Swap	PCMBSWP1 0	PCMBSWP0 0	PCMASWP1 0	PCMASWP0 0	ADCBSWP1 0	ADCBSWP0 0	ADCASWP1 0	ADCASWP0 0
1Ah p 74	AIN Ref Config, ADC MUX	AIN2B_REF 0	AIN2A_REF 0	AIN1B_REF 0	AIN1A_REF 0	ADCBMUX1 0	ADCBMUX0 0	ADCAMUX1 0	ADCAMUX0 0

Adr.	Function	7	6	5	4	3	2	1	0
1Bh p 75	HPF Ctl	HPFB 1	HPFRZB 0	HPFA 1	HPFRZA 0	HPFB_CF1 0	HPFB_CF0 0	HPFA_CF1 0	HPFA_CF0 0
1Ch p 76	Misc. ADC Ctl	ADCB=A 0	PGAB=A 0	DIGSUM1 0	DIGSUM0 0	INV_ADCB 0	INV_ADCA 0	ADCBMUTE 0	ADCAMUTE 0
1Dh p 77	Gain & Bias Ctl	PREAMPB1 0	PREAMPB0 0	PREAMPA1 0	PREAMPA0 0	BOOSTB 0	BOOSTA 0	BIAS_LVL1 0	BIAS_LVL0 0
1Eh p 77	PGAA MUX, Vol	PGAAMUX1 0	PGAAMUX0 0	PGAAVOL5 0	PGAAVOL4 0	PGAAVOL3 0	PGAAVOL2 0	PGAAVOL1 0	PGAAVOL0 0
1Fh p 77	PGAB MUX, Vol	PGABMUX1 0	PGABMUX0 0	PGABVOL5 0	PGABVOL4 0	PGABVOL3 0	PGABVOL2 0	PGABVOL1 0	PGABVOL0 0
20h p 78	ADCA Attenu-ator	ADCAATT7 0	ADCAATT6 0	ADCAATT5 0	ADCAATT4 0	ADCAATT3 0	ADCAATT2 0	ADCAATT1 0	ADCAATT0 0
21h p 78	ADCB Attenu-ator	ADCBATT7 0	ADCBATT6 0	ADCBATT5 0	ADCBATT4 0	ADCBATT3 0	ADCBATT2 0	ADCBATT1 0	ADCBATT0 0
22h p 79	ALC Enable, Attack Rate	ALCB 0	ALCA 0	ALCARATE5 0	AALCRATE4 0	ALCARATE3 0	ALCARATE2 0	ALCARATE1 0	ALCARATE0 0
23h p 79	ALC Release Rate	ALC_ALL 1	Reserved 0	ALCRRATE5 1	ALCRRATE4 1	ALCRRATE3 1	ALCRRATE2 1	ALCRRATE1 1	ALCRRATE0 1
24h p 80	ALC Thresh-olds	ALCMAX2 0	ALCMAX1 0	ALCMAX0 0	ALCMIN2 0	ALCMIN1 0	ALCMIN0 0	Reserved 0	Reserved 0
25h p 81	Noise Gate Ctl	NGALL 0	NG 0	NGBOOST 0	THRESH2 0	THRESH1 0	THRESH0 0	NGDELAY1 0	NGDELAY0 0
26h p 82	ALC, Limiter SFT, ZC	ALCASRDIS 0	ALCAZCDIS 0	ALCBSRDIS 0	ALCBZCDIS 0	LIMSRDIS 0	Reserved 0	Reserved 0	Reserved 0
27h p 83	AMUTE, Line & HP MUX	AMUTE 0	Reserved 0	Reserved 0	Reserved 0	LINEBMUX 0	LINEAMUX 0	HPBMUX 0	HPAMUX 0
28h p 83	Headphone A Volume	HPAMUTE 0	HPAVOL6 0	HPAVOL5 0	HPAVOL4 0	HPAVOL3 0	HPAVOL2 0	HPAVOL1 0	HPAVOL0 0
29h p 83	Headphone B Volume	HPBMUTE 0	HPBVOL6 0	HPBVOL5 0	HPBVOL4 0	HPBVOL3 0	HPBVOL2 0	HPBVOL1 0	HPBVOL0 0
2Ah p 84	Line A Volume	LINEAMUTE 0	LINEAVOL6 0	LINEAVOL5 0	LINEAVOL4 0	LINEAVOL3 0	LINEAVOL2 0	LINEAVOL1 0	LINEAVOL0 0
2Bh p 84	Line B Volume	LINEBMUTE 0	LINEBVOL6 0	LINEBVOL5 0	LINEBVOL4 0	LINEBVOL3 0	LINEBVOL2 0	LINEBVOL1 0	LINEBVOL0 0
2Ch p 85	Limit Thresh-olds Control	LMAX2 0	LMAX1 0	LMAX0 0	CUSH2 0	CUSH1 0	CUSH0 0	Reserved 0	Reserved 0
2Dh p 86	Limit Ctl, Release Rate	LIMIT 0	LIMIT_ALL 1	LIMRRATE5 1	LIMRRATE4 1	LIMRRATE3 1	LIMRRATE2 1	LIMRRATE1 1	LIMRRATE0 1
2Eh p 87	Limiter Attack Rate	Reserved 0	Reserved 0	LIMARATE5 0	LIMARATE4 0	LIMARATE3 0	LIMARATE2 0	LIMARATE1 0	LIMARATE0 0

6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and revision register and the status register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description. Unless otherwise specified, all “Reserved” bits must maintain their default value.

I²C Address: 1001010[R/$\overline{W}$]

6.1 Device I.D. Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
DEVID7	DEVID6	DEVID5	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0

6.1.1 Device I.D. (Read Only)

Device I.D. code for the CS42L56.

DEVID[7:0]	Part Number
01010110	CS42L56

6.2 Device Revision Register (Address 02h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	AREVID2	AREVID1	AREVID0	MTLREVID1	MTLREVID0

6.2.1 Alpha Revision (Read Only)

CS42L56 alpha revision level.

AREVID[2:0]	Alpha Revision Level
000	A

6.2.2 Numeric Revision (Read Only)

CS42L56 numeric revision level.

MTLREVID[1:0]	Metal Revision Level
00	0

6.3 Power Control 1 (Address 03h)

7	6	5	4	3	2	1	0
Reserved	Reserved	PDN_VBUF	PDN_BIAS	PDN_CHRG	PDN_ADCB	PDN_ADCA	PDN

6.3.1 Power Down VCM Bias Buffer

Configures the power state of the weak internal VCM buffer.

PDN_VBUF	Weak VCM Status
0	All weak VCM buffers for the AINx inputs that are not selected (either through ADCxMUX[1:0] or PGAx-MUX[1:0]) are powered up. The weak VCM buffers for the AINx inputs that are selected are powered down.
1	All weak VCM buffers are powered down.
Application:	“Optional VCM Buffer” on page 35

6.3.2 Power Down MIC Bias

Configures the power state of the microphone bias output.

PDN_BIAS	MIC Bias Status
0	Powered Up
1	Powered Down

6.3.3 Power Down ADC Charge Pump

Configures the power state of the ADC charge pump. For optimal ADC performance and power consumption, set to 1b when VA > 2.1 V and set to 0b when VA < 2.1 V.

PDN_CHRG	ADC Charge Pump Status
0	Powered Up
1	Powered Down

6.3.4 Power Down ADC x

Configures the power state of ADC channel x.

PDN_ADCx	ADC Status
0	Powered Up
1	Powered Down

6.3.5 Power Down

Configures the power state of the entire CODEC.

PDN	CODEC Status
0	Powered Up
1	Powered Down

6.4 Power Control 2 (Address 04h)

7	6	5	4	3	2	1	0
PDN_HPB1	PDN_HPB0	PDN_HPA1	PDN_HPA0	PDN_LINB1	PDN_LINB0	PDN_LINA1	PDN_LINA0

6.4.1 Headphone Power Control

Configures how the HPDETECT pin, controls the power for the headphone amplifier.

PDN_HPx[1:0]	Headphone Status
00	Headphone channel is ON when the HPDETECT pin, is LO. Headphone channel is OFF when the HPDETECT pin, is HI.
01	Headphone channel is ON when the HPDETECT pin, is HI. Headphone channel is OFF when the HPDETECT pin, is LO.
10	Headphone channel is always ON.
11	Headphone channel is always OFF.

6.4.2 Line Power Control

Configures how the HPDETECT pin, 29, controls the power for the line amplifier.

PDN_LINx[1:0]	Line Status
00	Line channel is ON when the HPDETECT pin, is LO. Line channel is OFF when the HPDETECT pin, is HI.
01	Line channel is ON when the HPDETECT pin, is HI. Line channel is OFF when the HPDETECT pin, is LO.
10	Line channel is always ON.
11	Line channel is always OFF.

6.5 Clocking Control 1 (Address 05h)

7	6	5	4	3	2	1	0
Reserved	M/S	INV_SCLK	SCK=MCK1	SCK=MCK0	MKPREDIV	MCLKDIV2	MCLKDIS

6.5.1 Master/Slave Mode

Configures the serial port I/O clocking.

M/S	Serial Port Clocks
0	Slave (Input ONLY)
1	Master (Output ONLY)
Application:	"Serial Port Clocking" on page 47

6.5.2 SCLK Polarity

Configures the polarity of the SCLK signal.

INV_SCLK	SCLK Polarity
0	Not Inverted
1	Inverted

6.5.3 SCLK Equals MCLK

Configures the SCLK signal source and speed for master mode.

SCK=MCK[1:0]	Output SCLK
00	Re-timed, bursted signal with minimal speed needed to clock the required data samples
01	Reserved
10	MCLK signal *after* the MCLK divide by 2 (MCLKDIV2) circuit
11	MCLK signal *before* the MCLK divide by 2 (MCLKDIV2) circuit

Note: The SCK=MCK[1:0] bits must be set to "00" when the device is in slave mode.

6.5.4 MCLK Pre-Divide

Configures a divide of the input MCLK prior to all internal circuitry.

MKPREDIV	MCLK signal into CODEC
0	No divide
1	Divided by 2
Application:	"Serial Port Clocking" on page 47

6.5.5 MCLK Divide

Configures a divide of the MCLK after the MCLK pre-divide.

MCLKDIV2	MCLK signal into CODEC
0	No divide
1	Divided by 2
Application:	"Serial Port Clocking" on page 47

6.5.6 MCLK Disable

Configures the MCLK signal prior to all internal circuitry.

MCLKDIS	MCLK signal into CODEC
0	On
1	Off; Disables the clock tree to save power when the CODEC is powered down.

Note: This function should be enabled during power down (PDN=1) ONLY.

6.6 Clocking Control 2 (Address 06h)

7	6	5	4	3	2	1	0
Reserved	Reserved	AUTO	RATIO4	RATIO3	RATIO2	RATIO1	RATIO0

6.6.1 Clock Ratio Auto-Detect

Configures the power status of the Auto-Detect circuitry. When enabled, the Auto-Detect circuitry detects when the LRCK changes and automatically adjusts internal clock divide-ratios eliminating the need of a register write to account for the change. It should be noted that the Auto-detect circuitry can only detect when the LRCK changes by a factor of two while the MCLK stays the same (for instance, Mclk = 6.000 MHz; LRCK changes from 48 kHz to 24 kHz). Any other major clock frequency changes must be accounted for by appropriate control port writes.

AUTO	Auto-detection of Clock Ratio
0	Disabled
1	Enabled
Application:	"Serial Port Clocking" on page 47

Note: When AUTO is enabled, the MCLK/LRCK ratio must be implemented according to Table 3 on page 47.

6.6.2 Clock Ratio

Configures the appropriate internal MCLK divide ratio for LRCK and SCLK.

RATIO[4:0]	MCLK/LRCK Ratio	MCLK/SCLK Ratio
01000	128	2
01001	125	2
01011	136	2
01100	192	3
01101	187.5	3
10000	256	4
10001	250	4
10011	272	4
10100	384	6
10101	375	6
11000	512	8
11001	500	8
11011	544	8
11100	750	12
11101	768	12
Application:	"Serial Port Clocking" on page 47	

Notes:

1. Register settings not shown in the table are reserved. Use Table 3. "Serial Port Clock Ratio Settings" beginning on page 47 for determining the register settings based on the system master clock (MCLK), bit clock (SCLK) and frame clock (LRCK) frequencies.

6.7 Serial Format (Address 07h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DIF	Reserved	Reserved	Reserved

6.7.1 CODEC Digital Interface Format

Configures the digital interface format for data on SDOUT and SDIN.

DIF	CODEC Interface Format
0	I²S
1	Left Justified
Application:	

6.8 Class H Control (Address 08h)

7	6	5	4	3	2	1	0
ADPTPWR1	ADPTPWR0	Reserved	Reserved	CHGFREQ3	CHGFREQ2	CHGFREQ1	CHGFREQ0

6.8.1 Adaptive Power Adjustment

Configures how the power to the headphone and line amplifiers adapts to the output signal level.

ADPTPWR[1:0]	Power Supply
00	Adapted to volume setting; Voltage level is determined by the sum of the relevant volume settings
01	Fixed - Headphone and Line Amp supply = ±VCP/2
10	Fixed - Headphone and Line Amp supply = ±VCP
11	Adapted to Signal; Voltage level is dynamically determined by the output signal
Application:	"Class H Amplifier" on page 39

6.8.2 Charge Pump Frequency

Sets the charge pump frequency on FLYN and FLYP.

CHGFREQ[3:0]	N
0000	0
...	
0101	5
...	
1111	15
Formula:	Frequency = $\frac{f_{MCLK}}{4 \cdot (N + 2)}$; where f_{MCLK} is the frequency of the MCLK signal after the MCLKDIV2 circuit.

Notes:

1. The output THD+N performance improves at higher frequencies; power consumption increases at higher frequencies.

6.9 Misc. Control (Address 09h)

7	6	5	4	3	2	1	0
DIGMUX	Reserved	Reserved	ANLGSFT	ANLGZC	DIGSFT	Reserved	FREEZE

6.9.1 Digital MUX

Selects the signal source for the ADC serial port.

DIGMUX	SDOUT Signal Source
0	ADC
1	DSP Mix

6.9.2 Analog Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

ANLGSFT	Volume Changes	Affected Analog Volume Controls
0	Do not occur with a soft ramp	PGAx_VOL[5:0] ("PGAx Volume" on page 78) HPxMUTE ("Headphone Channel x Mute" on page 83) HPxVOL[6:0] ("Headphone Volume Control" on page 84) LINExMUTE ("Line Channel x Mute" on page 84) LINExVOL[6:0] ("Line Volume Control" on page 84)
1	Occur with a soft ramp	
Ramp Rate:	1/8 dB every LRCK cycle	

6.9.3 Analog Zero Cross

Configures when the signal level changes occur for the analog volume controls.

ANLGZCx	Volume Changes	Affected Analog Volume Controls
0	Do not occur on a zero crossing	PGAx_VOL[5:0] ("PGAx Volume" on page 78) HPxMUTE ("Headphone Channel x Mute" on page 83) HPxVOL[6:0] ("Headphone Volume Control" on page 84) LINExMUTE ("Line Channel x Mute" on page 84) LINExVOL[6:0] ("Line Volume Control" on page 84)
1	Occur on a zero crossing	

Note: If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period between 1024 and 1536 sample periods (approximately 21.3 ms to 32 ms at 48 kHz sample rate).

6.9.4 Digital Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

DIGSFT	Volume Changes	Affected Digital Volume Controls
0	Do not occur with a soft ramp	ADCxMUTE ("ADC Mute" on page 76) ADCxATT[7:0] ("ADCx Volume" on page 78) AMIXxMUTE ("ADC Mixer Channel x Mute" on page 67) AMIXxVOL[6:0] ("ADC Mixer Channel x Volume" on page 67) PMIXxMUTE ("PCM Mixer Channel x Mute" on page 67) PMIXxVOL[6:0] ("PCM Mixer Channel x Volume" on page 68) MSTxMUTE ("Master Playback Mute" on page 67) MSTxVOL[7:0] ("Master Volume Control" on page 70)
1	Occur with a soft ramp	
Ramp Rate:	1/8 dB every LRCK cycle	

6.9.5 Freeze Registers

Configures a hold on all register settings.

FREEZE	Control Port Status
0	Register changes take effect immediately
1	Modifications may be made to all control port registers without the changes taking effect until after the FREEZE is disabled.

Notes:

1. This bit should only be used to synchronize run-time controls, such as volume and mute, during normal operation. Using this bit before the relevant circuitry begins normal operation could cause the change to take effect immediately, ignoring the FREEZE bit.

6.10 Status (Address 0Ah) (Read Only)

Bits [6:0] in this register are “sticky”. 1b means the associated error condition has occurred at least once since the register was last read. 0b means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets these bits to 0. Bit 7 is not “sticky” and will always indicate current status when the register is read.

7	6	5	4	3	2	1	0
HPDETECT	SPCLKERR	DSPBOVFL	DSPAOVFL	MIXBOVFL	MIXAOVFL	ADCBOVFL	ADCAOVFL

6.10.1 HPDETECT Pin Status (Read Only)

Indicates the status of the HPDETECT pin.

HPDETECT	Pin State
0	Low
1	High

6.10.2 Serial Port Clock Error (Read Only)

Indicates the status of the MCLK to LRCK ratio.

SPCLKERR	Serial Port Clock Status:
0	MCLK/LRCK ratio is valid.
1	MCLK/LRCK ratio is not valid.
Application:	“Serial Port Clocking” on page 47

Note: On initial power up and application of clocks, this bit will report 1b as the serial port re-synchronizes.

6.10.3 DSP Engine Overflow (Read Only)

Indicates the over-range status in the DSP data path.

DSPxOVFL	DSP Overflow Status:
0	No digital clipping has occurred in the data path after the DSP.
1	Digital clipping has occurred in the data path after the DSP.

6.10.4 MIXx Overflow (Read Only)

Indicates the over-range status in the PCM mix data path.

MIXxOVFL	PCM Overflow Status:
0	No digital clipping has occurred in the data path of the ADC and PCM mix of the DSP.
1	Digital clipping has occurred in the data path of the ADC and PCM mix of the DSP.

6.10.5 ADCx Overflow (Read Only)

Indicates the over-range status in the ADC signal path.

ADCxOVFL	ADC Overflow Status:
0	No clipping has occurred anywhere in the ADC signal path.
1	Clipping has occurred in the ADC signal path.

6.11 Playback Control (Address 0Bh)

7	6	5	4	3	2	1	0
PDN_DSP	DEEMPH	Reserved	PLYBCKB=A	INV_PCMB	INV_PCMA	Reserved	Reserved

6.11.1 Power Down DSP

Configures the power state of the DSP Engine.

PDNDSP	DSP Status	DSP Engine Controls/Blocks
0	Powered Up	AMIXxMUTE ("ADC Mixer Channel x Mute" on page 67) AMIXxVOL[6:0] ("ADC Mixer Channel x Volume" on page 67) PMIXxMUTE ("PCM Mixer Channel x Mute" on page 67) PMIXxVOL[6:0] ("PCM Mixer Channel x Volume" on page 68) Beep Generator, Tone Control, De-Emphasis
1	Powered Down	

6.11.2 HP/Line De-Emphasis

Configures a 15µs/50µs (when Fs = 44.1 kHz) digital de-emphasis filter response on the headphone and line outputs.

DEEMPH	De-Emphasis Status
0	Disabled
1	Enabled

6.11.3 Playback Channels B=A

Configures independent or ganged volume and mute control of all playback channels. When enabled, the channel B settings are ignored and the channel A settings control channel A and channel B.

PLYBCKB=A	Single Volume Control for all Playback Channels	Affected Volume Controls
0	Disabled; Independent channel control.	AMIXxMUTE ("ADC Mixer Channel x Mute" on page 67) AMIXxVOL[6:0] ("ADC Mixer Channel x Volume" on page 67) PMIXxMUTE ("PCM Mixer Channel x Mute" on page 67) PMIXxVOL[6:0] ("PCM Mixer Channel x Volume" on page 68) MSTxVOL[7:0] ("Master Volume Control" on page 70) HPxMUTE ("Headphone Channel x Mute" on page 83) HPxVOL[7:0] ("Headphone Volume Control" on page 84 LINExMUTE[7:0] ("Line Channel x Mute" on page 84) LINExVOL[7:0] ("Line Volume Control" on page 84)
1	Enabled; Ganged channel control. Channel A volume control controls channel B volume.	

6.11.4 Invert PCM Signal Polarity

Configures the polarity of the digital input signal.

INV_PCMx	PCM Signal Polarity
0	Not Inverted
1	Inverted

6.12 DSP Mute Controls (Address 0Ch)

7	6	5	4	3	2	1	0
AMIXBMUTE	AMIXAMUTE	PMIXBMUTE	PMIXAMUTE	Reserved	Reserved	MSTBMUTE	MSTAMUTE

6.12.1 ADC Mixer Channel x Mute

Configures a digital mute on the ADC mix in the DSP Engine.

AMIXxMUTE	ADC Mixer Mute
0	Disabled
1	Enabled

6.12.2 PCM Mixer Channel x Mute

Configures a digital mute on the PCM mix from the serial data input (SDIN) to the DSP Engine.

PMIXxMUTE	PCM Mixer Mute
0	Disabled
1	Enabled

6.12.3 Master Playback Mute

Configures a digital mute on the master volume control for channel x.

MSTxMUTE	Master Mute
0	Not muted.
1	Muted

6.13 ADCx Mixer Volume: ADCA (Address 0Dh) & ADCB (Address 0Eh)

7	6	5	4	3	2	1	0
AMIXxVOL7	AMIXxVOL6	AMIXxVOL5	AMIXxVOL4	AMIXxVOL3	AMIXxVOL2	AMIXxVOL1	AMIXxVOL0

6.13.1 ADC Mixer Channel x Volume

Sets the volume/gain of the ADC mix in the DSP Engine.

AMIXxVOL[7:0]	Volume
0111 1111	+12 dB
...	...
0001 1000	+12 dB
...	...
0000 0001	+0.5 dB
0000 0000	0 dB
1111 1111	-0.5 dB
...	...
1000 1000	-60.0 dB
1000 0111	Mute
...	...
1000 0000	Mute
Step Size:	0.5 dB

6.14 PCMx Mixer Volume: PCMA (Address 0Fh) & PCMB (Address 10h)

7	6	5	4	3	2	1	0
PMIXxVOL7	PMIXxVOL6	PMIXxVOL5	PMIXxVOL4	PMIXxVOL3	PMIXxVOL2	PMIXxVOL1	PMIXxVOL0

6.14.1 PCM Mixer Channel x Volume

Sets the volume/gain of the PCM mix from the serial data input (SDIN) to the DSP Engine.

PMIXxVOL[7:0]	**Volume**
0111 1111	+12 dB
...	...
0001 1000	+12 dB
...	...
0000 0001	+0.5 dB
0000 0000	0 dB
1111 1111	-0.5 dB
...	...
1000 1000	-60.0 dB
1000 0111	Mute
...	...
1000 0000	Mute
Step Size:	0.5 dB

6.15 Analog Input Advisory Volume (Address 11h)

7	6	5	4	3	2	1	0
AINADV7	AINADV6	AINADV5	AINADV4	AINADV3	AINADV2	AINADV1	AINADV0

6.15.1 Analog Input Advisory Volume

Defines the maximum analog input volume level used by the class H controller to determine the appropriate supply for the HP and Line amplifiers.

AINADV[7:0]	Defined Input Volume
0001 1000	Reserved
…	…
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
…	…
0011 0100	-102 dB
…	…
0001 1001	-102 dB
Step Size:	0.5 dB

6.16 Digital Input Advisory Volume (Address 12h)

7	6	5	4	3	2	1	0
DINADV7	DINADV6	DINADV5	DINADV4	DINADV3	DINADV2	DINADV1	DINADV0

6.16.1 Digital Input Advisory Volume

Defines the maximum digital input volume level used by the class H controller to determine the appropriate supply for the HP and Line amplifiers.

DINADV[7:0]	Defined Input Volume
0001 1000	Reserved
…	…
0000 0001	Reserved
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
…	…
0011 0100	-102 dB
…	…
0001 1001	-102 dB
Step Size:	0.5 dB

Note: Between the headphone and line, the final output voltage from the charge pump is dictated by the highest required advisory volume. When any respective amplifier is powered down, the charge pump's voltage automatically adjusts to the appropriate level.

6.17 Master Volume Control: MSTA (Address 13h) & MSTB (Address 14h)

7	6	5	4	3	2	1	0
MSTxVOL7	MSTxVOL6	MSTxVOL5	MSTxVOL4	MSTxVOL3	MSTxVOL2	MSTxVOL1	MSTxVOL0

6.17.1 Master Volume Control

Sets the volume of the signal out the DSP.

MSTxVOL[7:0]	Master Volume
0001 1000	+12.0 dB
…	…
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
…	…
0011 0100	-102 dB
0011 0011	Mute
…	…
0001 1001	Mute
Step Size:	0.5 dB

6.18 Beep Frequency & On Time (Address 15h)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

6.18.1 Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	Frequency *(Fs = 12, 24, 48 or 96 kHz)*	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	“Beep Generator” on page 45	

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep frequency will scale directly with sample rate, Fs.

6.18.2 Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	On Time *(Fs = 12, 24 or 48 kHz)*
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 45

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep on time will scale inversely with sample rate, Fs.

6.19 Beep Volume & Off Time (Address 16h)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

6.19.1 Beep Off Time

Sets the off duration of the beep signal.

OFFTIME[2:0]	Off Time *(Fs = 12, 24 or 48 kHz)*
000	~1.23 s
001	~2.58 s
010	~3.90 s
011	~5.20 s
100	~6.60 s
101	~8.05 s
110	~9.35 s
111	~10.80 s
Application:	"Beep Generator" on page 45

Notes:

1. This setting must not change when BEEP and/or REPEAT is enabled.
2. Beep off time will scale inversely with sample rate, Fs.

6.19.2 Beep Volume

Sets the volume of the beep signal.

BPVOL[4:0]	Gain
00110	+6.0 dB
…	…
00000	0 dB
11111	-2 dB
11110	-4 dB
…	…
00111	-50 dB
Step Size:	2 dB
Application:	"Beep Generator" on page 45

6.20 Beep & Tone Configuration (Address 17h)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	Reserved	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

6.20.1 Beep Configuration

Configures a beep mixed with the HP and Line output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 45

Notes:

1. When used in analog pass through mode, the output alternates between the signal from the PGA and the beep signal. The beep signal does not mix with the analog signal from the PGA.
2. Re-engaging the beep before it has completed its initial cycle may cause the beep signal to remain ON for the maximum ONTIME duration.

6.20.2 Treble Corner Frequency

Sets the corner frequency for the treble shelving filter.

TREBCF[1:0]	Treble Corner Frequency Setting
00	5 kHz
01	7 kHz
10	10 kHz
11	15 kHz

6.20.3 Bass Corner Frequency

Sets the corner frequency for the bass shelving filter.

BASSCF[1:0]	Bass Corner Frequency Setting
00	50 Hz
01	100 Hz
10	200 Hz
11	250 Hz

6.20.4 Tone Control Enable

Configures the treble and bass activation.

TCEN	Bass and Treble Control
0	Disabled
1	Enabled

6.21 Tone Control (Address 18h)

7	6	5	4	3	2	1	0
TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0

6.21.1 Treble Gain

Sets the gain of the treble shelving filter.

TREB[3:0]	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB
Step Size:	1.5 dB

6.21.2 Bass Gain

Sets the gain of the bass shelving filter.

BASS[3:0]	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB
Step Size:	1.5 dB

6.22 ADC & PCM Channel Mixer (Address 19h)

7	6	5	4	3	2	1	0
PCMBSWP1	PCMBSWP0	PCMASWP1	PCMASWP0	ADCBSWP1	ADCBSWP0	ADCASWP1	ADCASWP0

6.22.1 PCM Mix Channel Swap

Configures a mix/swap of the PCM Mix to the headphone/line outputs.

PCMxSWP[1:0]	PCM Mix to HP/LINEOUTA	PCM Mix to HP/LINEOUTB
00	Left	Right
01	(Left + Right)/2	(Left + Right)/2
10		
11	Right	Left

6.22.2 ADC Mix Channel Swap

Configures a mix/swap of the ADC Mix to the headphone/line outputs.

ADCxSWP[1:0]	ADC Mix to HP/LINEOUTA Channel	ADC Mix to HP/LINEOUTB Channel
00	Left	Right
01	(Left + Right)/2	(Left + Right)/2
10		
11	Right	Left

6.23 AIN Reference Configuration, ADC MUX (Address 1Ah)

7	6	5	4	3	2	1	0
AIN2B_REF	AIN2A_REF	AIN1B_REF	AIN1A_REF	ADCBMUX1	ADCBMUX0	ADCAMUX1	ADCAMUX0

6.23.1 Analog Input 2 x Reference Configuration

Configures the analog input 2 x reference.

AIN2x_REF	Analog Input Configuration
0	AIN2x is configured as a single-ended input, referenced to the internal ADC common-mode voltage. If both AIN2 channels are configured as single-ended, AIN2REF/AIN3B can be used as an additional single-ended input, referenced to the internal ADC common-mode voltage.
1	AIN2x is configured as a pseudo-differential input, referenced to AIN2REF/AIN3B.

6.23.2 Analog Input 1 x Reference Configuration

Configures the analog input 1 x reference.

AIN1x_REF	Analog Input Configuration
0	AIN1x is configured as a single-ended input, referenced to the internal ADC common-mode voltage. If both AIN1 channels are configured as single-ended, AIN1REF/AIN3A can be used as an additional single-ended input, referenced to the internal ADC common-mode voltage.
1	AIN1x is configured as a pseudo-differential input, referenced to AIN1REF/AIN3A.

6.23.3 ADC x Input Select

Selects the specified analog input signal into ADCx.

ADCxMUX[1:0]	Selected Input to ADCx
00	PGAx - Use PGAxMUX bit ("PGA x Input Select" on page 77) to select an input channel.
01	AIN1x; PGA is bypassed.
10	AIN2x; PGA is bypassed.
11	AIN3x; PGA is bypassed.

Note: Pseudo-differential inputs are not available when the PGA is bypassed. Use the AINx_REF bits (Analog Input 1 x Reference Configuration and "Analog Input 1 x Reference Configuration" on page 74) to properly configure the input channel.

6.24 HPF Control (Address 1Bh)

7	6	5	4	3	2	1	0
HPFB	HPFRZB	HPFA	HPFRZA	HPFB_CF1	HPFB_CF0	HPFA_CF1	HPFA_CF0

6.24.1 ADCx High-Pass Filter

Configures the internal high-pass filter after ADCx.

HPFx	High Pass Filter Status
0	Disabled
1	Enabled

6.24.2 ADCx High-Pass Filter Freeze

Configures the high pass filter's digital DC subtraction and/or calibration after ADCx.

HPFRZx	High Pass Filter Digital Subtraction
0	Continuous DC Subtraction
1	Frozen DC Subtraction

6.24.3 HPF x Corner Frequency

Sets the corner frequency (-3 dB point) for the internal High-Pass Filter (HPF).

HPFx_CF[1:0]	HPF Corner Frequency Setting *(Fs=48 kHz)*
00	1.8 Hz
01	119 Hz
10	236 Hz
11	464 Hz

6.25 Misc. ADC Control (Address 1Ch)

7	6	5	4	3	2	1	0
ADCB=A	PGAB=A	DIGSUM1	DIGSUM0	INV_ADCB	INV_ADCA	ADCBMUTE	ADCAMUTE

6.25.1 ADC Channel B=A

Configures independent or ganged volume and mute control of the ADC. When enabled, the channel B settings are ignored and the channel A settings control channel A and channel B.

ADCB=A	Single Volume Control	Affected Volume Controls
0	Disabled; Independent channel control.	ADCxMUTE (“ADC Mute” on page 76) ADCxVOL[6:0] (“ADCx Volume” on page 78)
1	Enabled; Ganged channel control. Channel A volume control controls channel B volume.	

6.25.2 PGA Channel B=A

Configures independent or ganged volume control of the PGA. When enabled, the channel B settings are ignored and the channel A settings control channel A and channel B. Affected register bits include PGAx-VOL[5:0].

PGAB=A	Single Volume Control	Affected Volume Controls
0	Disabled; Independent channel control.	PGAxVOL[5:0] (“PGAx Volume” on page 78)
1	Enabled; Ganged channel control. Channel A volume control controls channel B volume.	

6.25.3 Digital Sum

Configures a mix/swap of ADCA and ADCB.

DIGSUM[1:0]	Serial Output Signal	
	Left Channel	Right Channel
00	ADCA	ADCB
01	(ADCA + ADCB)/2	(ADCA + ADCB)/2
10	(ADCA - ADCB)/2	(ADCA - ADCB)/2
11	ADCB	ADCA

6.25.4 Invert ADC Signal Polarity

Configures the polarity of the ADC signal.

INV_ADCx	ADC Signal Polarity
0	Not Inverted
1	Inverted

6.25.5 ADC Mute

Configures a digital mute on ADC channel x.

ADCxMUTE	ADC Mute
0	Not muted.
1	Muted

6.26 Gain & Bias Control (Address 1Dh)

7	6	5	4	3	2	1	0
PREAMPB1	PREAMPB0	PREAMPA1	PREAMPA0	BOOSTB	BOOSTA	BIAS_LVL1	BIAS_LVL0

6.26.1 PGA x Preamplifier Gain

Configures the gain of the PGA x preamp.

PREAMPx[1:0]	PGA x Preamp Gain
00	0 dB
01	+10 dB
10	+20 dB
11	Reserved

6.26.2 Boostx

Configures a +20 dB digital boost on ADC channel x.

BOOSTx	+20 dB Boost
0	No boost applied
1	+20 dB digital boost applied

6.26.3 Microphone Bias Output Level

Configures the voltage level of the microphone bias output.

BIAS_LVL[1:0]	MIC Bias Output Level
00	0.9xVA
01	0.8xVA
10	0.7xVA
11	0.6xVA

6.27 PGA x MUX, Volume: PGA A (Address 1Eh) & PGA B (Address 1Fh)

7	6	5	4	3	2	1	0
PGAxMUX1	PGAxMUX0	PGAxVOL5	PGAxVOL4	PGAxVOL3	PGAxVOL2	PGAxVOL1	PGAxVOL0

6.27.1 PGA x Input Select

Selects the specified analog input signal into PGA channel x.

PGAxMUX[1:0]	Selected Input to PGAx
00	AIN1x.
01	AIN2x.
10	AIN3x.
11	Reserved

Note: For pseudo-differential inputs, the CODEC automatically chooses the respective pseudo-ground (AIN1REF or AIN2REF) for each input selection.

Use the AINx_REF bits (Analog Input 1 x Reference Configuration and “Analog Input 1 x Reference Configuration” on page 74) to properly configure the input channel.

6.27.2 PGAx Volume

Sets the volume/gain of the Programmable Gain Amplifier (PGA).

PGAxVOL[5:0]	Volume
01 1111	+12 dB
...	...
01 1000	+12 dB
...	...
00 0001	+0.5 dB
00 0000	0 dB
11 1111	-0.5 dB
...	...
11 0100	-6.0 dB
...	...
10 0000	-6.0 dB
Step Size:	0.5 dB

Notes:

1. Refer to Figure 37 and Figure 38 on page 89 for differential and integral nonlinearity (DNL and INL).

6.28 ADCx Attenuator Control: ADCAATT (Address 20h) & ADCBATT (Address 21h)

7	6	5	4	3	2	1	0
ADCxATT7	ADCxATT6	ADCxATT5	ADCxATT4	ADCxATT3	ADCxATT2	ADCxATT1	ADCxATT0

6.28.1 ADCx Volume

Sets the volume of the ADC signal.

ADCxATT[7:0]	Volume
0111 1111	0 dB
...	...
0000 0000	0 dB
1111 1111	-1.0 dB
1111 1110	-2.0 dB
...	...
1010 0000	-96.0 dB
1001 1111	Mute
...	...
1000 0000	Mute
Step Size:	1.0 dB

6.29 ALC Enable & Attack Rate (Address 22h)

7	6	5	4	3	2	1	0
ALCB	ALCA	ALCARATE5	AALCRATE4	ALCARATE3	ALCARATE2	ALCARATE1	ALCARATE0

6.29.1 ALCx

Configures the automatic level controller (ALC).

ALC	ALC Status
0	Disabled
1	Enabled
Application:	"Automatic Level Control (ALC)" on page 35

Notes:

1. The ALC should only be configured while the power down bit ("Power Down" on page 59) is enabled.
2. The ALC is not available in passthrough mode.

6.29.2 ALC Attack Rate

Sets the rate at which the ALC applies analog and/or digital attenuation from levels above the AMAX[2:0] threshold ("ALC Maximum Threshold" on page 80).

ALCARATE[5:0]	Attack Time
00 0000	Fastest Attack
…	…
11 1111	Slowest Attack
Application:	"Automatic Level Control (ALC)" on page 35

Note: The ALC attack rate is user-selectable but is also a function of the sampling frequency, Fs, the ANLGZCx ("Analog Zero Cross" on page 64) and the DIGSFT ("Digital Soft Ramp" on page 64) setting unless the respective disable bit ("ALCx Soft Ramp Disable" on page 82 or "ALCx Zero Cross Disable" on page 82) is enabled.

6.30 ALC Release Rate (Address 23h)

7	6	5	4	3	2	1	0
ALC_ALL	Reserved	ALCRRATE5	ALCRRATE4	ALCRRATE3	ALCRRATE2	ALCRRATE1	ALCRRATE0

6.30.1 ALC Limit All Channels

Sets how channels are attenuated when the ALC is enabled.

ALC_ALL	ALC action:
0	Apply the necessary attenuation on a specific channel only when the signal amplitudes on *that* specific channel rises above ALCMAX[2:0]. Remove attenuation on a specific channel only when the signal amplitude on *that* specific channel falls below ALCMIN[2:0].
1	Apply the necessary attenuation on BOTH channels when the signal amplitudes on any ONE channel rises above ALCMAX[2:0]. Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below ALCMIN[2:0].
Application:	"Automatic Level Control (ALC)" on page 35

Note: This function should only be used when the ALC for both channels is enabled.

6.30.2 ALC Release Rate

Sets the rate at which the ALC releases the analog and/or digital attenuation from levels below the MIN[2:0] threshold (“Limiter Cushion Threshold” on page 85) and returns the signal level to the PGAx-VOL[5:0] (“PGAx Volume” on page 78) and ADCxVOL[7:0] (“ADCx Volume” on page 78) setting.

ALCRRATE[5:0]	Release Time
00 0000	Fastest Release
…	…
11 1111	Slowest Release
Application:	“Automatic Level Control (ALC)” on page 35

Notes:

1. The ALC release rate is user-selectable but is also a function of the sampling frequency, Fs, and the DIGSFT (“Digital Soft Ramp” on page 64) and ANLGZCx (“Analog Zero Cross” on page 64) setting.
2. It is recommended that the Release Rate setting be slower than the Attack Rate.

6.31 ALC Threshold (Address 24h)

7	6	5	4	3	2	1	0
ALCMAX2	ALCMAX1	ALCMAX0	ALCMIN2	ALCMIN1	ALCMIN0	Reserved	Reserved

6.31.1 ALC Maximum Threshold

Sets the maximum level, below full scale, at which to limit and attenuate the input signal at the attack rate (ALCARATE - “ALC Attack Rate” on page 79).

MAX[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	“Automatic Level Control (ALC)” on page 35

6.31.2 ALC Minimum Threshold

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at the release rate (ALCRRATE - "ALC Release Rate" on page 80) until levels lie between the ALCMAX and ALCMIN thresholds.

ALCMIN[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	"Automatic Level Control (ALC)" on page 35

Note: This setting is usually set slightly below the ALCMAX threshold.

6.32 Noise Gate Control (Address 25h)

7	6	5	4	3	2	1	0
NGALL	NG	NG_BOOST	THRESH2	THRESH1	THRESH0	NGDELAY1	NGDELAY0

6.32.1 Noise Gate All Channels

Sets which channels are attenuated when clipping on any single channel occurs.

NGALL	Noise Gate triggered by:
0	Individual channel; Any channel that falls below the threshold setting triggers the noise gate attenuation for ONLY that channel.
1	Both channels A & B; Both channels must fall below the threshold setting for the noise gate attenuation to take effect.

6.32.2 Noise Gate Enable

Configures the noise gate.

NG	Noise Gate Status
0	Disabled
1	Enabled

6.32.3 Noise Gate Threshold and Boost

THRESH sets the threshold level of the noise gate. Input signals below the threshold level will be attenuated to -96 dB. NG_BOOST configures a +30 dB boost to the threshold settings.

THRESH[2:0]	**Minimum Setting** (NG_BOOST = 0b)	**Minimum Setting** (NG_BOOST = 1b)
000	-64 dB	-34 dB
001	-67 dB	-36 dB
010	-70 dB	-40 dB
011	-73 dB	-43 dB
100	-76 dB	-46 dB
101	-82 dB	-52 dB
110	Reserved	-58 dB
111	Reserved	-64 dB

6.32.4 Noise Gate Delay Timing

Sets the delay time before the noise gate attacks.

NGDELAY[1:0]	**Delay Setting**
00	50 ms
01	100 ms
10	150 ms
11	200 ms

Note: The Noise Gate attack rate is a function of the sampling frequency, Fs, and the DIGSFT ("Digital Soft Ramp" on page 64) setting.

6.33 ALC and Limiter Soft Ramp, Zero Cross Disables (Address 26h)

7	6	5	4	3	2	1	0
ALCASRDIS	ALCAZCDIS	ALCBSRDIS	ALCBZCDIS	LIMSRDIS	Reserved	Reserved	Reserved

6.33.1 ALCx Soft Ramp Disable

Configures an override of the analog soft ramp setting.

ALCxSRDIS	**ALC Soft Ramp Disable**
0	OFF; ALC Attack Rate is dictated by the DIGSFT ("Digital Soft Ramp" on page 64) setting
1	ON; ALC volume changes take effect in one step, regardless of the DIGSFT setting.

6.33.2 ALCx Zero Cross Disable

Configures an override of the analog zero cross setting.

ALCxZCDIS	**ALC Zero Cross Disable**
0	OFF; ALC Attack Rate is dictated by the ANLGZC ("Analog Zero Cross" on page 64) setting
1	ON; ALC volume changes take effect at any time, regardless of the ANLGZC setting.

6.33.3 Limiter Soft Ramp Disable

Configures an override of the digital soft ramp setting.

LIMSRDIS	**Limiter Soft Ramp Disable**
0	OFF; Limiter Attack Rate is dictated by the DIGSFT ("Digital Soft Ramp" on page 64) setting
1	ON; Limiter volume changes take effect in one step, regardless of the DIGSFT setting.

6.34 Automute, Line & HP MUX (Address 27h)

7	6	5	4	3	2	1	0
AMUTE	Reserved	Reserved	Reserved	LINEBMUX	LINEAMUX	HPBMUX	HPAMUX

6.34.1 Auto Mute

Configures the state of the auto mute feature. When enabled, the analog outputs will mute after 4096 consecutive zeros or ones from SDIN.

AMUTE	Auto Mute Configuration
0	Auto Mute Disabled
1	Auto Mute Enabled. The analog outputs will mute after 4096 consecutive words of all zeros or ones from SDIN.

6.34.2 Line Input Select

Selects the specified analog input signal into line amplifier x.

LINExMUX	Selected Input to Line Amplifier Ch. x
0	DACx
1	PGAx - Use PGAxMUX bit ("PGA x Input Select" on page 77) to select an input channel.

Note: The PGA path must not be selected while the Line Amplifier is powered down.

6.34.3 Headphone Input Select

Selects the specified analog input signal into headphone amplifier x.

HPxMUX	Selected Input to HP Amplifier Ch. x
0	DACx
1	PGAx - Use PGAxMUX bit ("PGA x Input Select" on page 77) to select an input channel.

Note: The PGA path must not be selected while the Headphone Amplifier is powered down.

6.35 Headphone Volume Control: HPA (Address 28h) & HPB (Address 29h)

7	6	5	4	3	2	1	0
HPxMUTE	HPxVOL6	HPxVOL5	HPxVOL4	HPxVOL3	HPxVOL2	HPxVOL1	HPxVOL0

6.35.1 Headphone Channel x Mute

Configures an analog mute on the headphone amplifier.

HPxMUTE	HP Amp Mute
0	Disabled
1	Enabled

6.35.2 Headphone Volume Control

Sets the volume of the signal out of the headphone amplifier.

HPxVOL[6:0]	Heaphone Volume
0111111	+12 dB
...	...
0001100	+12 dB
...	...
0000001	+1.0 dB
0000000	0 dB
1111111	-1.0 dB
...	...
1000100	-60.0 dB (Nominal Level (Note 1))
1000011	Mute
...	...
1000000	Mute (Note 2)
Step Size:	1.0 dB

Notes:

1. The step size may deviate from 1.0 dB. Refer to Figure 39 and Figure 40 on page 89.
2. See section "Analog Output Attenuation Characteristics" on page 26 for actual Mute Attenuation.

6.36 Line Volume Control: LINEA (Address 2Ah) & LINEB (Address 2Bh)

7	6	5	4	3	2	1	0
LINExMUTE	LINExVOL6	LINExVOL5	LINExVOL4	LINExVOL3	LINExVOL2	LINExVOL1	LINExVOL0

6.36.1 Line Channel x Mute

Configures an analog mute on the line amplifier.

LINExMUTE	HP Amp Mute
0	Disabled
1	Enabled

6.36.2 Line Volume Control

Sets the volume of the signal out of the line amplifier.

LINExVOL[6:0]	Line Volume
0111111	+12 dB
...	...
0001100	+12 dB
...	...
0000001	+1.0 dB
0000000	0 dB
1111111	-1.0 dB
...	...
1000100	-60.0 dB (Nominal Level (Note 1))
1000011	Mute (Note 2)
...	...
Step Size:	1.0 dB

Notes:

1. The step size may deviate from 1.0 dB. Refer to Figure 39 on page 89 and Figure 40 on page 89.
2. See section "Analog Output Attenuation Characteristics" on page 26 for actual Mute Attenuation.

6.37 Limiter Min/Max Thresholds (Address 2Ch)

7	6	5	4	3	2	1	0
LMAX2	LMAX1	LMAX0	CUSH2	CUSH1	CUSH0	Reserved	Reserved

6.37.1 Limiter Maximum Threshold

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate (LIMARATE - "Limiter Release Rate" on page 86).

LMAX[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	"Limiter" on page 46

Note: Bass, Treble and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

6.37.2 Limiter Cushion Threshold

Sets the minimum level at which to disengage the Limiter's attenuation at the release rate (LIMRRATE - "Limiter Release Rate" on page 86) until levels lie between the LMAX and CUSH thresholds.

CUSH[2:0]	Threshold Setting
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-18 dB
110	-24 dB
111	-30 dB
Application:	"Limiter" on page 46

Note: This setting is usually set slightly below the LMAX threshold.

6.38 Limiter Control, Release Rate (Address 2Dh)

7	6	5	4	3	2	1	0
LIMIT	LIMIT_ALL	LIMRRATE5	LIMRRATE4	LIMRRATE3	LIMRRATE2	LIMRRATE1	LIMRRATE0

6.38.1 Peak Detect and Limiter

Configures the peak detect and limiter circuitry.

LIMIT	Limiter Status
0	Disabled
1	Enabled
Application:	"Limiter" on page 46

Note: The Limiter should only be configured while the power down bit ("Power Down" on page 59) is enabled.

6.38.2 Peak Signal Limit All Channels

Sets how channels are attenuated when the limiter is enabled.

LIMIT_ALL	Limiter action:
0	Apply the necessary attenuation on a specific channel only when the signal amplitudes on *that* specific channel rises above LMAX. Remove attenuation on a specific channel only when the signal amplitude on *that* specific channel falls below CUSH.
1	Apply the necessary attenuation on BOTH channels when the signal amplitudes on any ONE channel rises above LMAX. Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below CUSH.
Application:	"Limiter" on page 46

6.38.3 Limiter Release Rate

Sets the rate at which the limiter releases the digital attenuation from levels below the CUSH[2:0] threshold ("Limiter Cushion Threshold" on page 85) and returns the analog output level to the MSTxVOL[7:0] ("Master Volume Control" on page 70) setting.

LIMRRATE[5:0]	Release Time
00 0000	Fastest Release
…	…
11 1111	Slowest Release
Application:	"Limiter" on page 46

Note: The limiter release rate is user-selectable but is also a function of the sampling frequency, Fs, and the DIGSFT ("Digital Soft Ramp" on page 64) setting unless the disable bit ("Limiter Soft Ramp Disable" on page 82) is enabled.

6.39 Limiter Attack Rate (Address 2Eh)

7	6	5	4	3	2	1	0
Reserved	Reserved	LIMARATE5	LIMARATE4	LIMARATE3	LIMARATE2	LIMARATE1	LIMARATE0

6.39.1 Limiter Attack Rate

Sets the rate at which the limiter applies digital attenuation from levels above the MAX[2:0] threshold ("Limiter Maximum Threshold" on page 85).

LIMARATE[5:0]	Attack Time
00 0000	Fastest Attack
…	…
11 1111	Slowest Attack
Application:	"Limiter" on page 46

Note: The limiter attack rate is user-selectable but is also a function of the sampling frequency, Fs, and the DIGSFT ("Digital Soft Ramp" on page 64) setting unless the disable bit ("Limiter Soft Ramp Disable" on page 82) is enabled.

7. PCB LAYOUT CONSIDERATIONS

7.1 Power Supply

As with any high-resolution converter, the CS42L56 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 11 shows the recommended power arrangements, with VA and VCP connected to clean supplies. VLDO, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VLDO may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VLDO.

7.2 Grounding

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS42L56 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS42L56 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+, VQ, +VHPFILT and -VHPFILT capacitors must be positioned to minimize the electrical path from each respective pin to AGND. The CDB42L56 evaluation board demonstrates the optimum layout and power supply arrangements.

7.3 QFN Thermal Pad

The CS42L56 comes in a compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CDB42L56 evaluation board demonstrates the optimum thermal pad and via configuration.

8. ANALOG VOLUME NON-LINEARITY (DNL & INL)

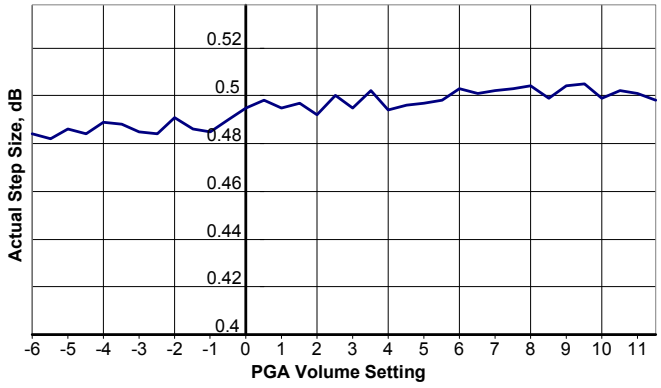


Figure 37. PGA Step Size vs. Volume Setting

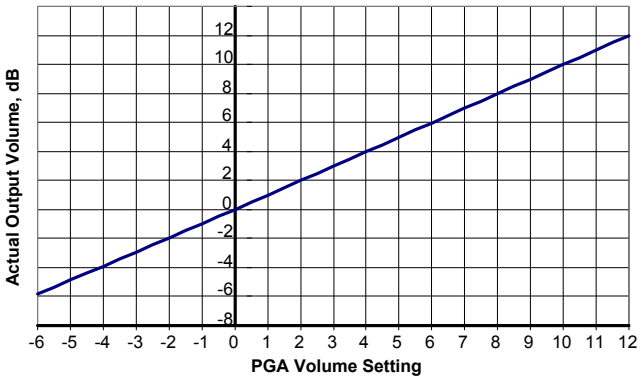


Figure 38. PGA Output Volume vs. Volume Setting

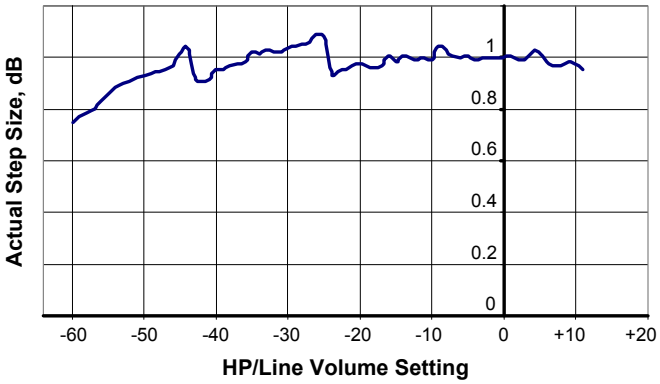


Figure 39. HP/Line Step Size vs. Volume Setting

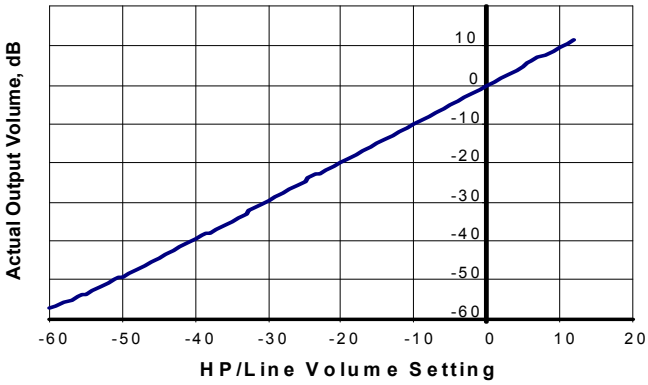


Figure 40. HP/Line Output Volume vs. Volume Setting

9. ADC & DAC DIGITAL FILTERS

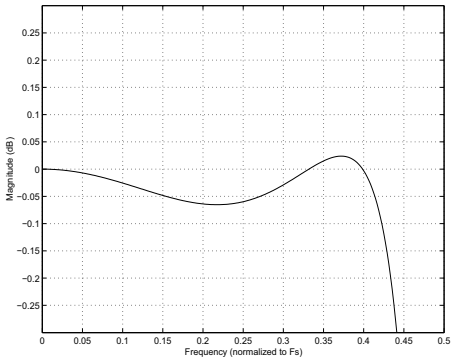


Figure 41. ADC Frequency Response

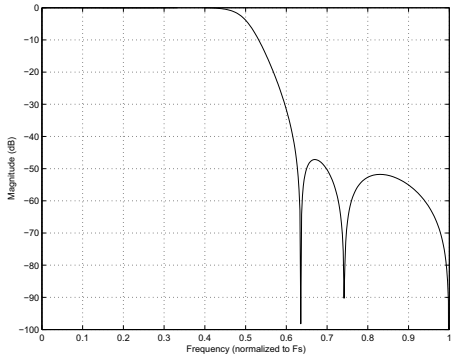


Figure 42. ADC Stopband Rejection

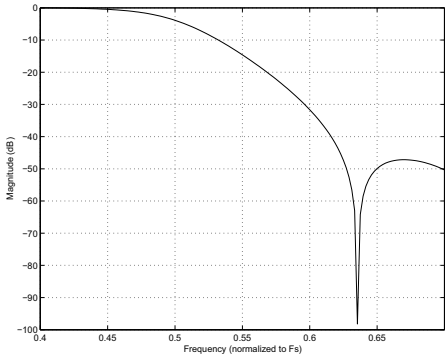


Figure 43. ADC Transition Band

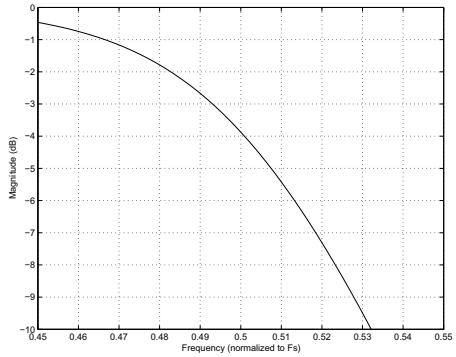


Figure 44. ADC Transition Band Detail

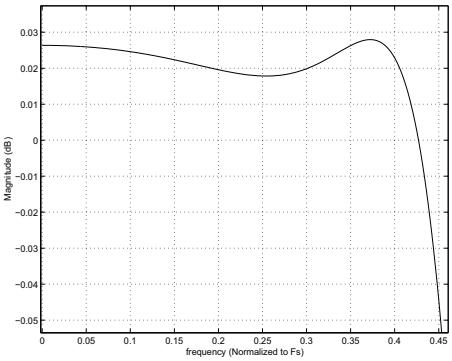


Figure 45. DAC Frequency Response

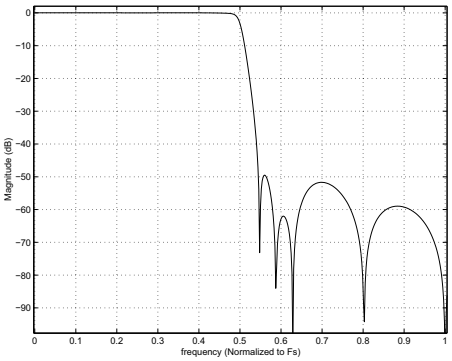


Figure 46. DAC Stopband

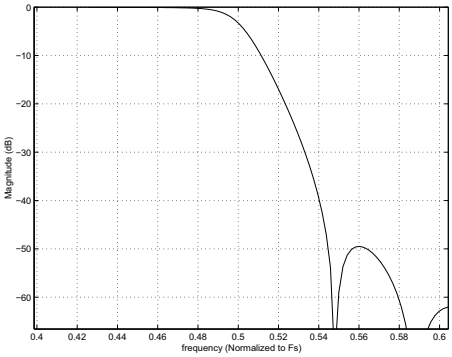


Figure 47. DAC Transition Band

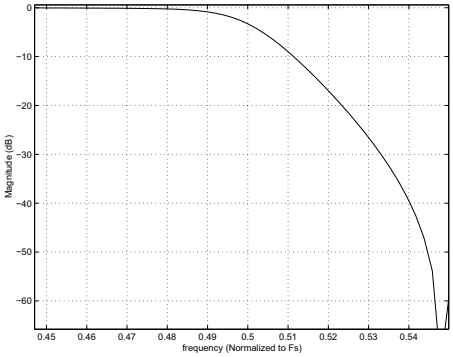


Figure 48. DAC Transition Band (Detail)

10.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dB signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 dBFS and -20 dBFS for the analog input and 0 dB and -20 dB for the analog output as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

HP to ADC Isolation

A measure of crosstalk between the headphone amplifier and the ADC inputs. Measured for each channel at the ADC's output with no signal to the input and a full-scale signal applied to the headphone amplifier with a 16 Ω or 10 kΩ load. Units in decibels.

Output Offset Voltage

Describes the DC offset voltage present at the amplifier's output. When measuring the offset out the line amplifier, the line amplifier is ON while the headphone amplifier is OFF; when measuring the offset out the headphone amplifier, the headphone amplifier is ON while the line amplifier is OFF.

AC Load Resistance and Capacitance

R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

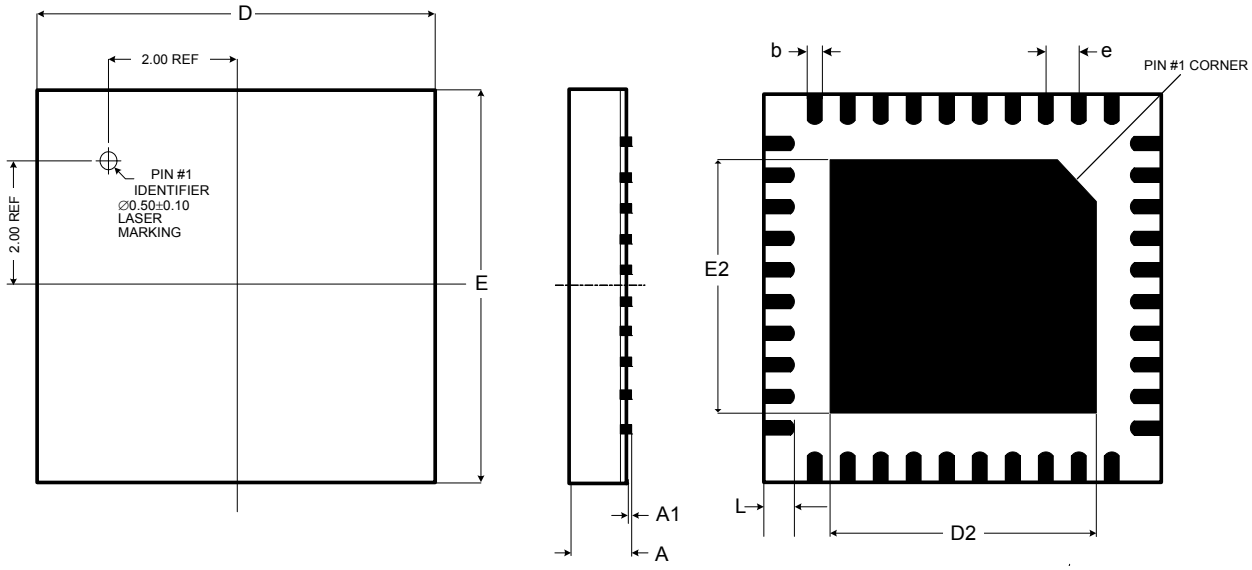
Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal.

11.PACKAGE DIMENSIONS

(Unless otherwise specified, linear tolerance is ±0.05 mm, and angular tolerance is ±2 deg.)

40L QFN (5 X 5 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
Dim	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.01575	0.01772	0.01969	0.40	0.45	0.50	1,2
A1	0.00000	-	0.00197	0.00	-	0.05	1,2
b	0.00591	0.00787	0.00984	0.15	0.20	0.25	1,2,3
e	0.01575 BSC			0.40 BSC			1,2
D	0.19685 BSC			5.00 BSC			1,2
E	0.19685 BSC			5.00 BSC			1,2
D2	0.13583	0.13780	0.13976	3.45	3.50	3.55	1,2
E2	0.13583	0.13780	0.13976	3.45	3.50	3.55	1,2
L	0.01181	0.01378	0.01575	0.30	0.35	0.40	1,2

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y 14.5M-1994.
3. Dimension lead width applies to the plated terminal and is measured 0.25 mm and 0.30 mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	68	-	°C/Watt
	4 Layer Board	θ_{JA}	-	28	-	°C/Watt

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L56	Ultralow Power, Stereo Codec with Class H Headphone Amp	40L-QFN	YES	Commercial	-40°C to +85°C	Rail	CS42L56-CNZ
						Tape & Reel	CS42L56-CNZR
CDB42L56	CS42L56 Evaluation Board	-	-	-	-	-	CDB42L56

13.REFERENCES

1. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000. http://www.semiconductors.philips.com

14.REVISION HISTORY

Release	Changes
F1	Final Release.
F2	Updated "ADC Digital Filter Characteristics" section on page 18. Updated dither specified in Note 15 on page 20. Updated "Combined DAC Interpolation & On-Chip Analog FIlter Response" section on page 22. Updated Figure 14. "Stereo Pseudo-Differential Input" on page 33. Updated the Class H section, "Adapt to Volume Mode (setting 00)" on page 40. Updated Section 4.11 "Recommended DAC to HP or Line Power Sequence" on page 50. Updated Section 4.12 "Recommended PGA to HP or Line Power Sequence (Analog Passthrough)" on page 52. Updated the first paragraph in "Register Quick Reference" on page 56 and "Register Description" on page 58 to allow data sheet-specified control-writes to reserved registers. Removed I²C address heading row from "Register Quick Reference" on page 56. Added Note 1 in "Freeze Registers" on page 64. Corrected BEEP volume settings to reflect level relative to DAC's full scale in "Beep Volume" on page 72 Updated "PGA x Preamplifier Gain" section on page 77. Corrected the E2 scale in the package drawing in "Package Dimensions" on page 92.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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