

General Description

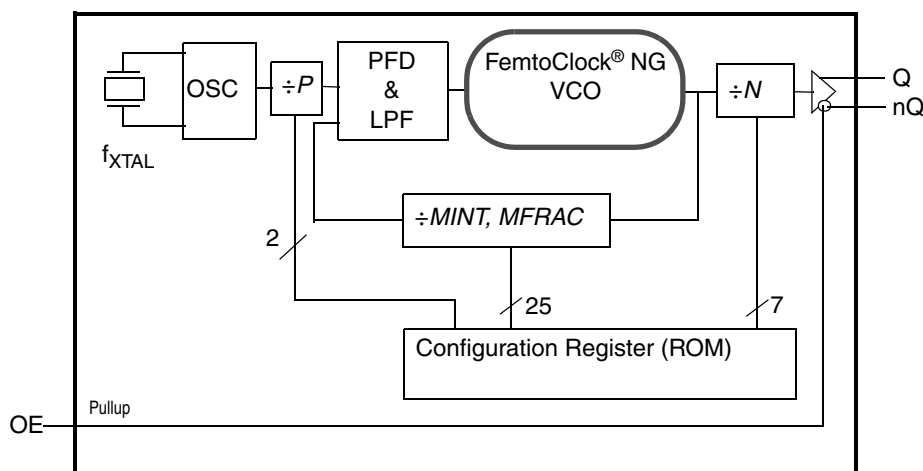
The IDT8N4S270 is a Factory Frequency-Programmable Crystal Oscillator with very flexible frequency programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory programmed to any in the range from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz and supports a very high degree of frequency precision of 218Hz or better. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

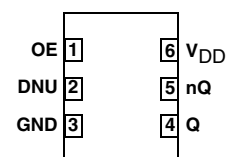
Features

- Fourth generation FemtoClock® NG technology
- Factory-programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Frequency programming resolution is 218Hz and better
- One 2.5V, 3.3V LVDS clock output
- Output enable control (positive polarity), LVCMOS/LVTTL compatible
- RMS phase jitter @ 231.25MHz (12kHz - 20MHz): 0.48ps (typical), integer PLL feedback configuration
- RMS phase jitter @ 231.25MHz (1kHz - 40MHz): 0.50ps (typical), integer PLL feedback configuration
- 2.5V or 3.3V supply
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) 6-pin ceramic package

Block Diagram



Pin Assignment



IDT8N4S270
6-lead ceramic 5mm x 7mm x 1.55mm
package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
2	DNU			Do not use (factory use only).
3	GND	Power		Power supply ground.
4, 5	Q, nQ	Output		Differential clock output pair. LVDS interface levels.
6	V _{DD}	Power		Power supply pin.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			5.5		pF
R _{PULLUP}	Input Pullup Resistor			50		kΩ

Function Tables

Table 3A. OE Configuration

Input	Output Enable
OE	
0	Outputs Q, nQ are in high-impedance state
1 (default)	Outputs Q, nQ are enabled

NOTE: OE is an asynchronous control.

Principles of Operation

The block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock f_{XTAL} of either 114.285MHz or 100MHz. The PLL includes the FemtoClock NG VCO along with the Pre-divider (P), the feedback divider (M) and the post divider (N). The P , M , and N dividers determine the output frequency based on the f_{XTAL} reference. The feedback divider is fractional supporting a huge number of output frequencies. The configuration of the feedback divider to integer-only values results in an improved output phase noise characteristics at the expense of the range of output frequencies. Internal registers are used to hold one factory pre-set P , M , and N configuration setting. The P , M , and N frequency configuration supports an output frequency range from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator.

The output frequency is determined by the 2-bit pre-divider (P), the feedback divider (M) and the 7-bit post divider (N). The feedback divider (M) consists of both a 7-bit integer portion ($MINT$) and an 18-bit fractional portion ($MFRAC$) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right]$$

Frequency Configuration

An order code is assigned to each frequency configuration programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information on programming capabilities of the device for custom frequency and pull-range configurations, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide*.

Table 3B. Output Frequency Range¹

15.476MHz to 866.67MHz
975MHz to 1,300MHz

1. Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC*

Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, θ_{JA}	49.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			134	160	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			129	155	mA

Table 4C. LVCMOS/LVTTL DC Characteristic, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE	$V_{DD} = 3.3V$		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	OE	$V_{DD} = 3.3V$		0.8	V
			$V_{DD} = 2.5V$		0.7	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		10	μA
I_{IL}	Input Low Current	OE	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150		μA

Table 4D. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	370	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.22	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4E. LVDS DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	360	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.21	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		15.476		866.67	MHz
			975		1,300	MHz
f_I	Initial Accuracy	Measured @ $25^\circ C$			± 10	ppm
f_S	Temperature Stability	Option code = A or B			± 100	ppm
		Option code = E or F			± 50	ppm
		Option code = K or L			± 20	ppm
f_A	Aging	Frequency drift over 10 year life			± 3	ppm
		Frequency drift over 15 year life			± 5	ppm
f_T	Total Stability	Option code A, B (10 year life)			± 113	ppm
		Option code E, F (10 year life)			± 63	ppm
		Option code K, L (10 year life)			± 33	ppm
$\bar{f}_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 1				20	ps
$\bar{f}_{jit}(per)$	RMS Period Jitter; NOTE 1			3	5	ps
$\bar{f}_{jit}(\emptyset)$	RMS Phase Jitter (Random); Fractional PLL feedback and $f_{XTAL}=100.000MHz$ (2xxx order codes), NOTE 2, 3	$17MHz \leq f_{OUT} \leq 1300MHz$, Integration Range: 12kHz-20MHz		0.497	0.882	ps
	RMS Phase Jitter (Random); Integer PLL feedback and $f_{XTAL}=100.00MHz$ (1xxx order codes), NOTE 2, 3	$500MHz \leq f_{OUT} \leq 1300MHz$, Integration Range: 12kHz-20MHz		0.232	0.322	ps
		$125MHz \leq f_{OUT} < 500MHz$, Integration Range: 12kHz-20MHz		0.250	0.450	ps
		$17MHz \leq f_{OUT} < 125MHz$, Integration Range: 12kHz-20MHz		0.275	0.405	ps
		$f_{OUT} = 156.25MHz$, Integration Range: 12kHz-20MHz		0.242	0.311	ps
		$f_{OUT} = 231.25MHz$, Integration Range: 12kHz-20MHz		0.476	0.680	ps
		$f_{OUT} = 156.25MHz$, Integration Range: 1kHz-40MHz		0.275	0.359	ps
		$f_{OUT} = 231.25MHz$, Integration Range: 1kHz-40MHz		0.504	0.700	ps
	RMS Phase Jitter (Random) Fractional PLL feedback and $f_{XTAL}=114.285MHz$ (0xxx order codes), NOTE 2, 3	$17MHz \leq f_{OUT} \leq 1300 MHz$, Integration Range: 12kHz-20MHz		0.474	0.986	ps
$\Phi_N(100)$	Single-side Band Phase Noise, 100Hz from Carrier	231.25MHz		-88		dBc/Hz
$\Phi_N(1k)$	Single-side Band Phase Noise, 1kHz from Carrier	231.25MHz		-110		dBc/Hz
$\Phi_N(10k)$	Single-side Band Phase Noise, 10kHz from Carrier	231.25MHz		-123		dBc/Hz
$\Phi_N(100k)$	Single-side Band Phase Noise, 100kHz from Carrier	231.25MHz		-125		dBc/Hz
$\Phi_N(1M)$	Single-side Band Phase Noise, 1MHz from Carrier	231.25MHz		-137		dBc/Hz

Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(10M)$	Single-side band phase noise, 10MHz from Carrier	231.25MHz		-141		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		450	ps
odc	Output Duty Cycle		47		53	%
$t_{STARTUP}$	Device Startup Time After Power Up				20	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

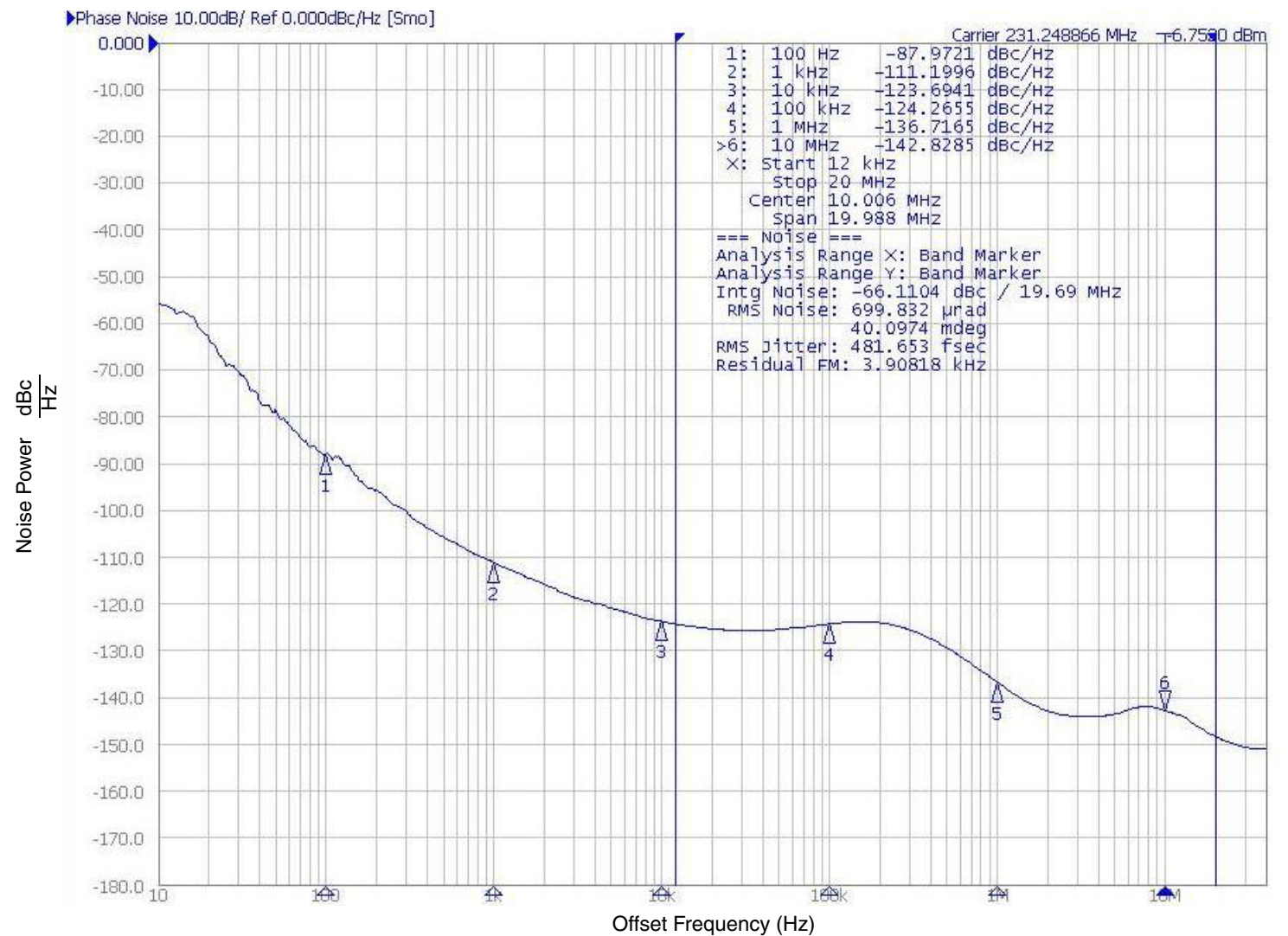
NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.

NOTE 1: This parameter is defined in accordance with JEDEC standard 65.

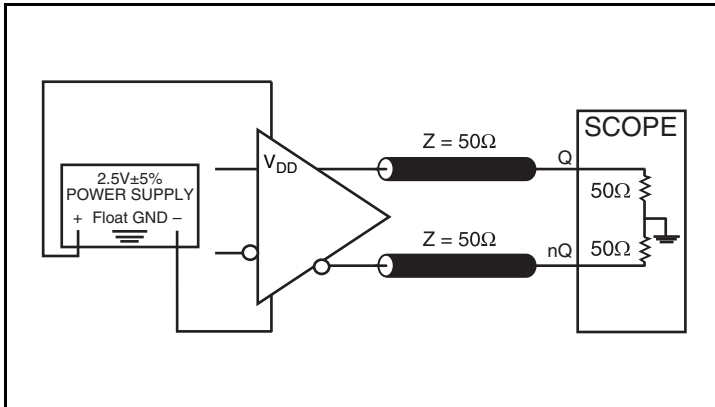
NOTE 2: Please refer to the phase noise plot.

NOTE 3: Please see the FemtoClock NG Ceramic 5x7 Modules Programming guide for more information on PLL feedback modes and the optimum configuration for phase noise. Integer PLL feedback is the default operation for the dddd = 1xxx order codes.

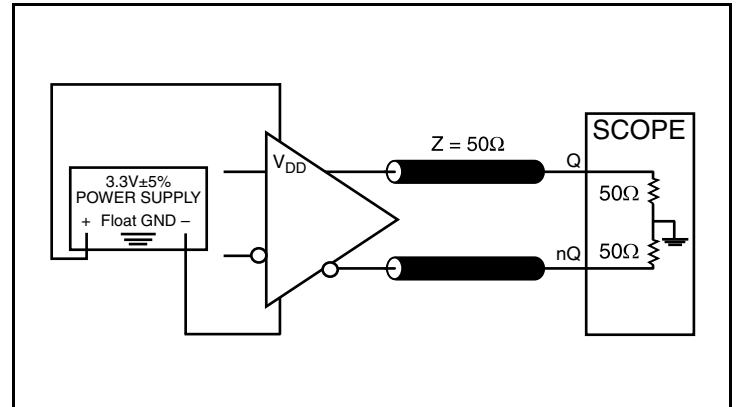
Typical Phase Noise at 231.25MHz (12kHz - 20MHz)



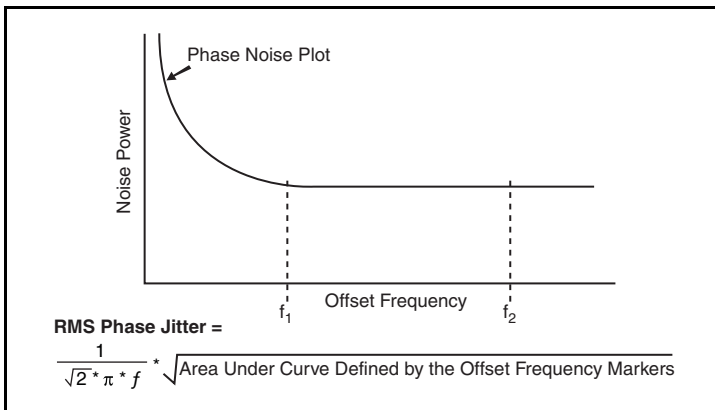
Parameter Measurement Information



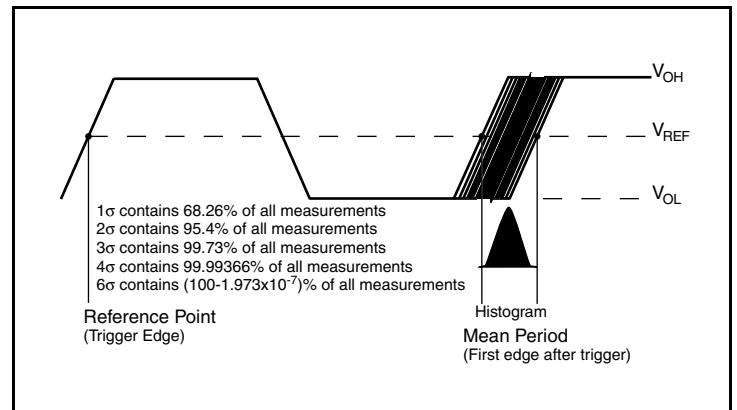
2.5V LVDS Output Load AC Test Circuit



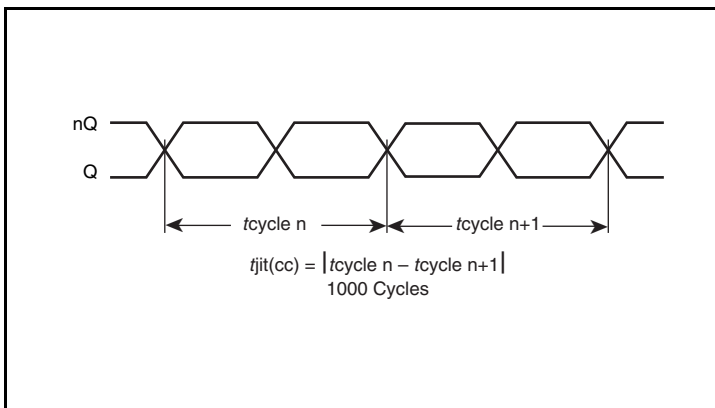
3.3V LVDS Output Load AC Test Circuit



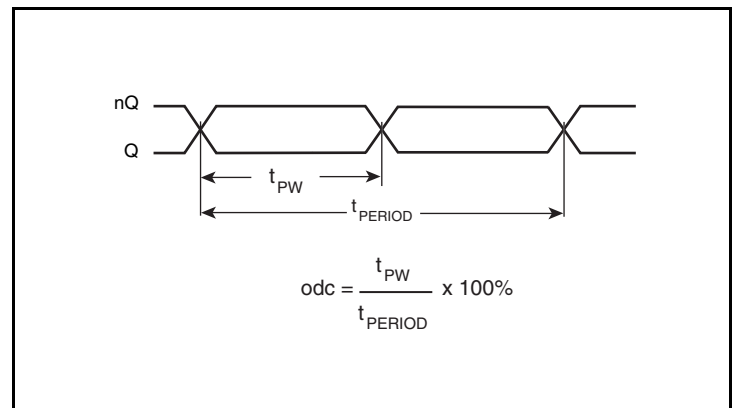
RMS Phase Jitter



RMS Period Jitter

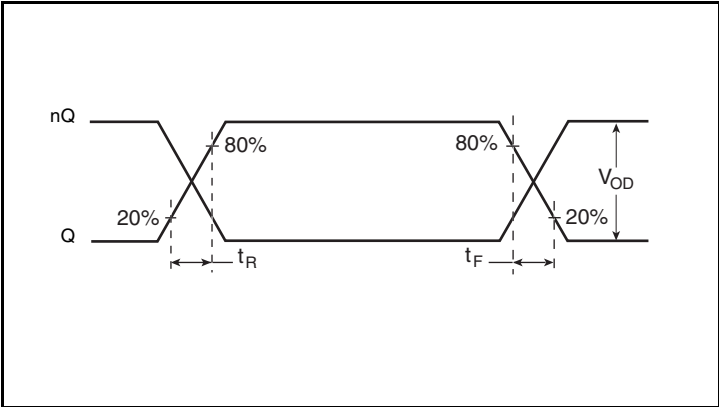


Cycle-to-Cycle Jitter

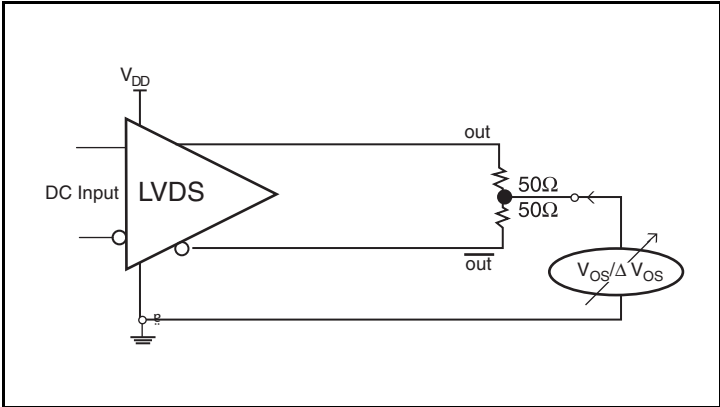


Output Duty Cycle/Pulse Width/Period

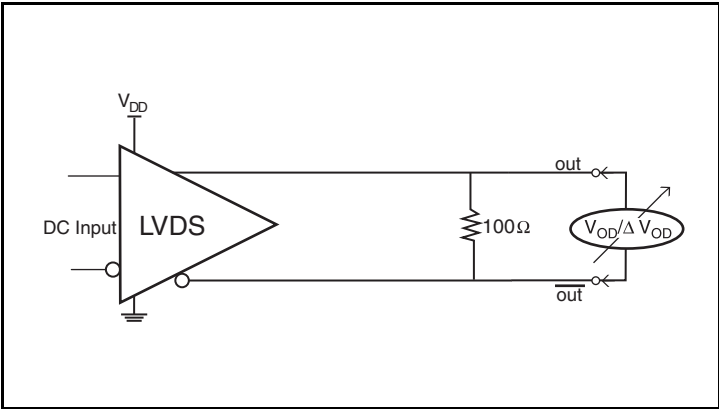
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



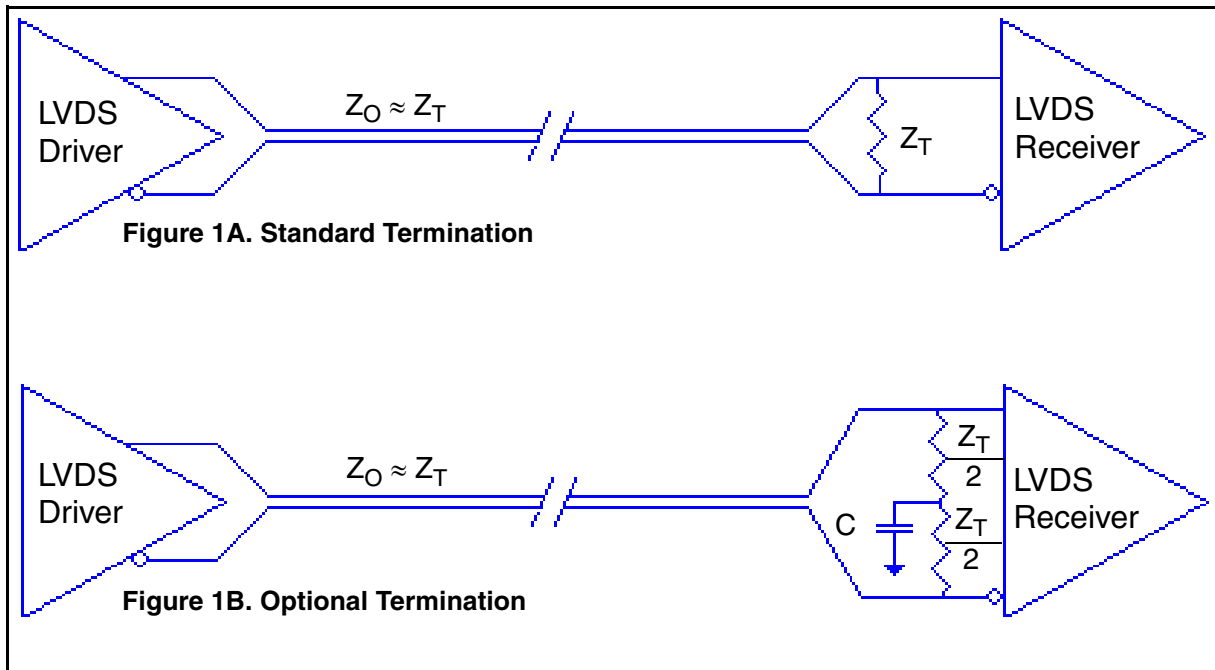
Differential Output Voltage Setup

Applications Information

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 1A* can be used with either type of output structure. *Figure 1B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



Schematic Layout

Figure 2 shows an example IDT8N4S270 application schematic. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE and FSEL can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{DD} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the $0.1\mu\text{F}$

capacitor on the V_{DD} pin must be placed on the device side with direct return to the ground plane through vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

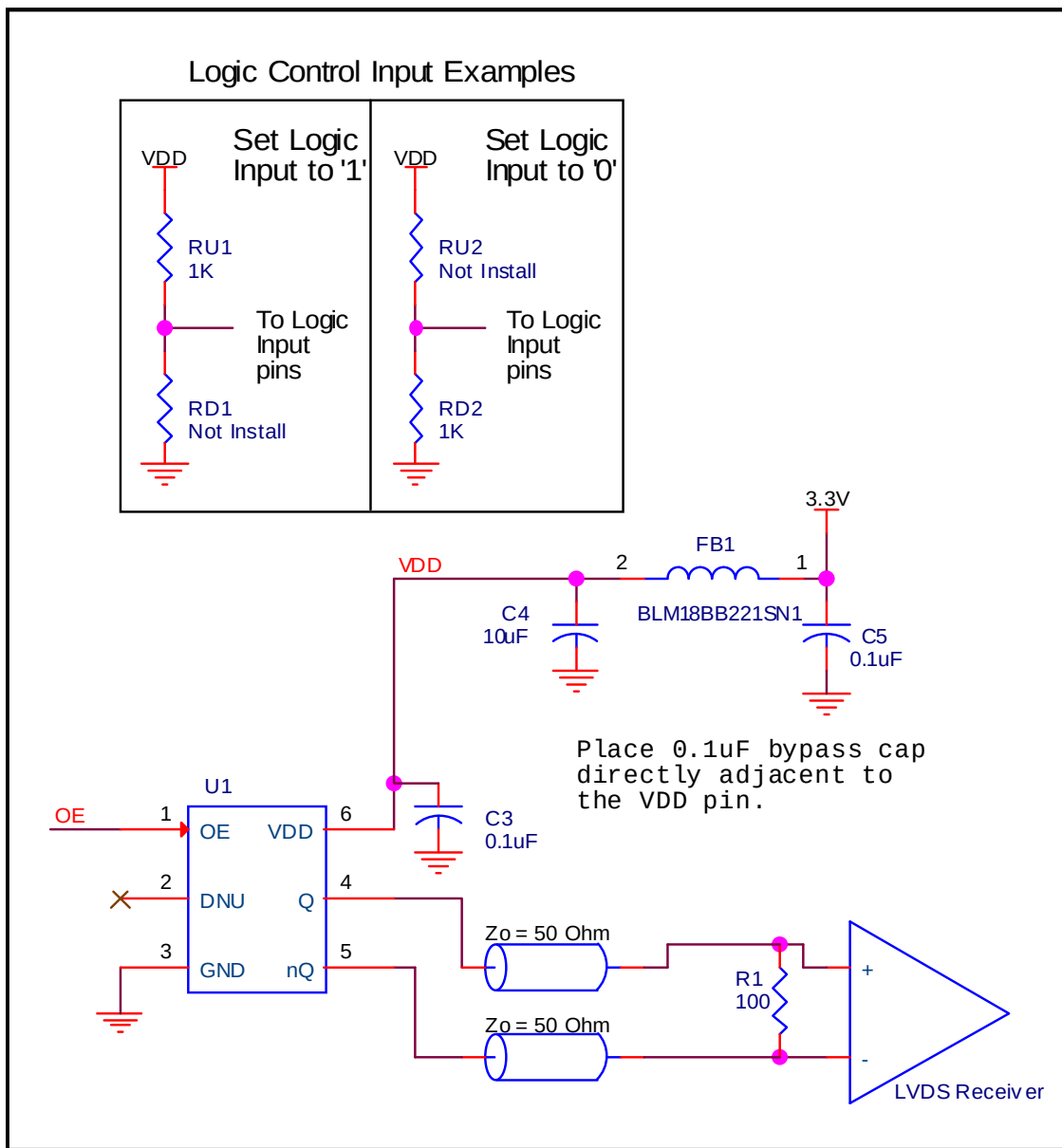


Figure 2. IDT8N4S270 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N4S270. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N4S270 is the sum of the core power plus the power dissipated due to the load. The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 160mA = \mathbf{554.4mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.554W * 49.4^\circ\text{C/W} = 112.4^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 6 Lead Ceramic 5mm x 7mm Package, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Reliability Information

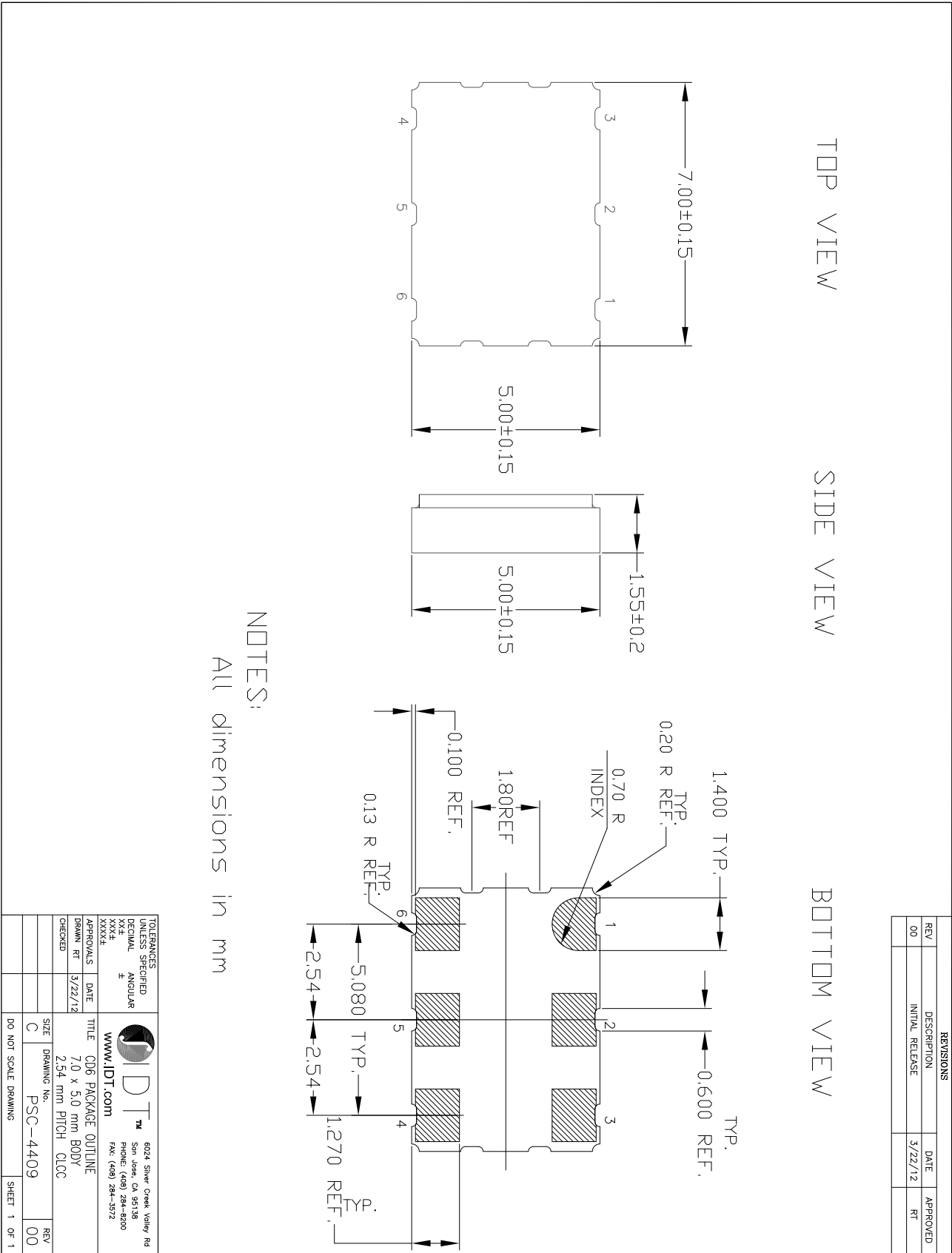
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Transistor Count

The transistor count for IDT8N4S270 is: 47,511

Package Outline and Package Dimensions

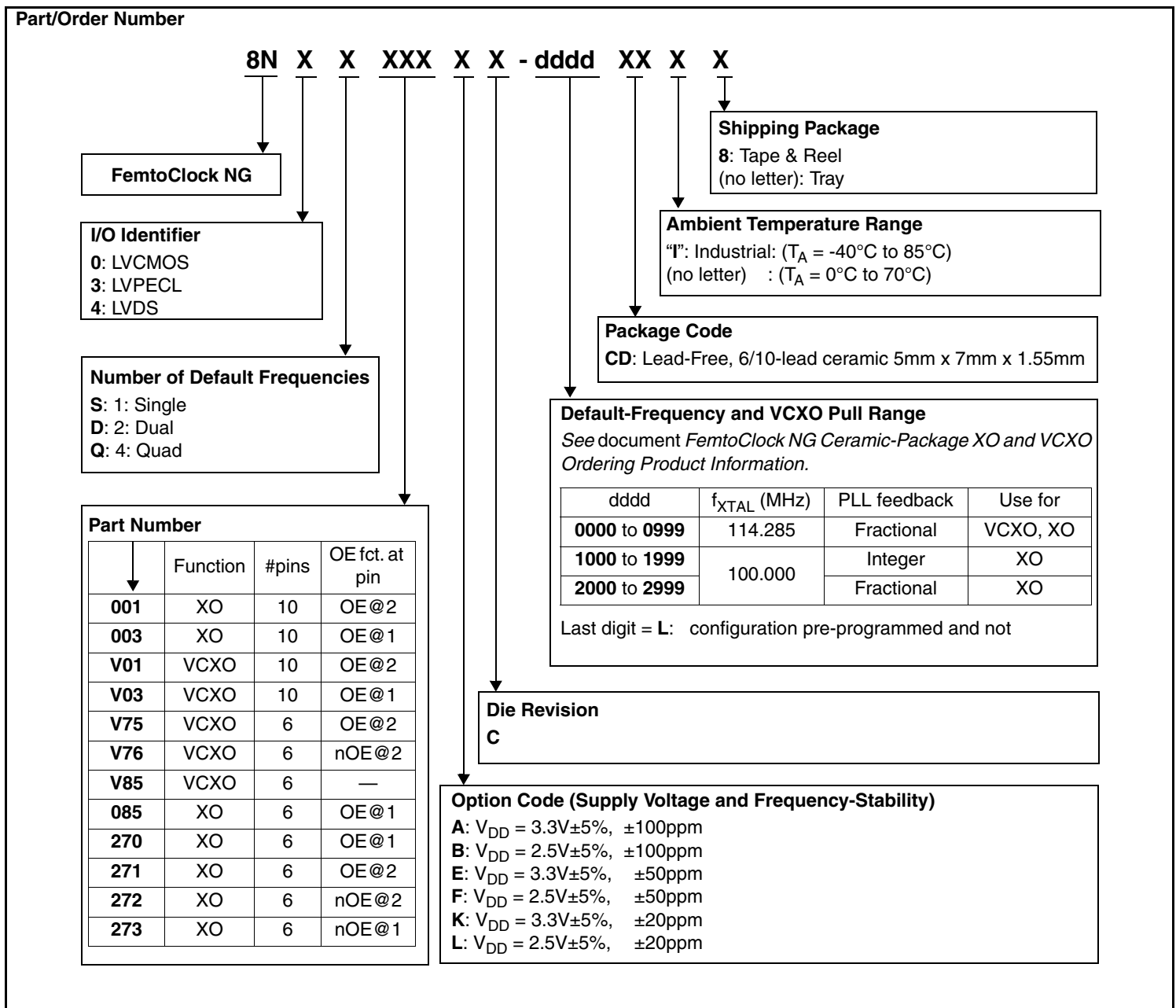


Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of device options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. The table below specifies the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N3QV01FG-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ± 50 ppm crystal frequency accuracy,

contains a 114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of minimum ± 100 ppm.

Other default frequencies and order codes are available from IDT on request. For more information on available default frequencies, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.



NOTE: For order information, also see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

Table 8. Device Marking

Marking	Industrial Temperature Range (T _A = -40°C to 85°C)	Commercial Temperature Range (T _A = 0°C to 70°C)
	IDT8N4S270yC- ddddCDI	IDT8N4S270yC- ddddCD
	y = Option Code, dddd=Default-Frequency and VCXO Pull Range	

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