

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT428 (DPAK) surface mountable plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

## 3. Applications

- Electronic thermostats
- General purpose motor controls

## 4. Quick reference data

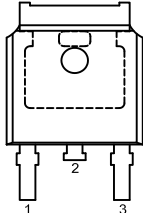
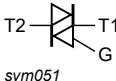
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 102\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	8	A
$I_{\text{TSM}}$	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	65	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 16.7\text{ ms}$	-	-	72	A
$T_{\text{j}}$	junction temperature		-	-	125	°C
<b>Static characteristics</b>						
$I_{\text{GT}}$	gate trigger current	$V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G+; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G-; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	-	15	mA
$V_T$	on-state voltage	$I_T = 10\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	-	1.65	V
Dynamic characteristics						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$ ; gate open circuit	6	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit; <a href="#">Fig. 12</a>	2	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 DPAK (SOT428)	 sym051
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BTA208S-600D	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DRM</sub>	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>mb</sub> ≤ 102 °C; Fig. 1; Fig. 2; Fig. 3	-	8	A
I <sub>TSM</sub>	non-repetitive peak on-state current	full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 20 ms; Fig. 4; Fig. 5	-	65	A
		full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 16.7 ms	-	72	A
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	21	A <sup>2</sup> s
di <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 10 mA	-	100	A/μs
I <sub>GM</sub>	peak gate current		-	2	A
P <sub>GM</sub>	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
T <sub>j</sub>	junction temperature		-	125	°C

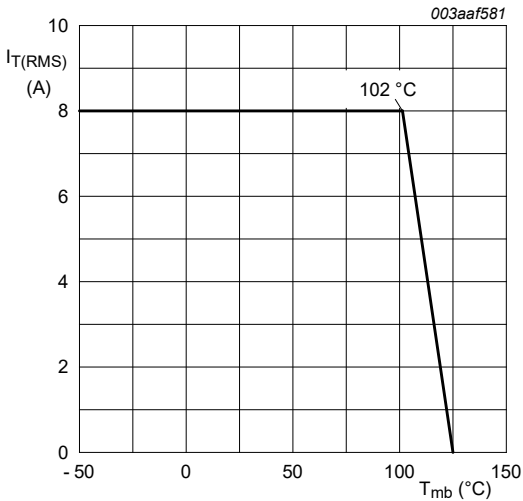


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

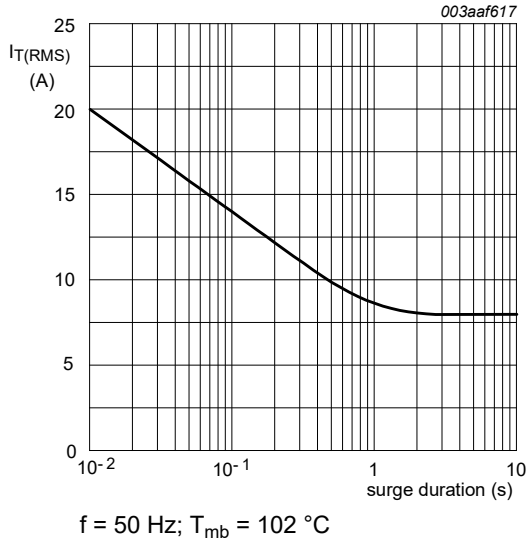


Fig. 2. RMS on-state current as a function of surge duration; maximum values





8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	2	K/W
		half cycle; Fig. 6		-	-	2.4	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted		-	75	-	K/W

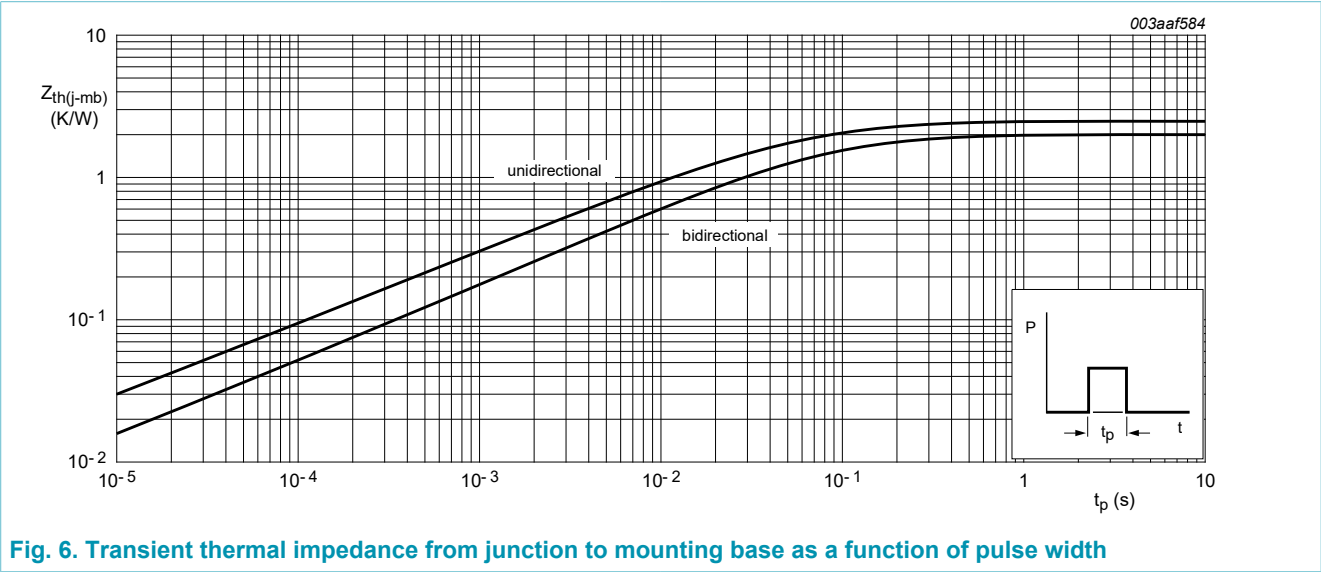


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	15	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	25	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	25	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	-	15	mA
$V_T$	on-state voltage	$I_T = 10\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	-	1.65	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$	-	-	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$ ; gate open circuit	6	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit; <a href="#">Fig. 12</a>	2	-	-	A/ms



Fig. 7. Normalized gate trigger current as a function of junction temperature

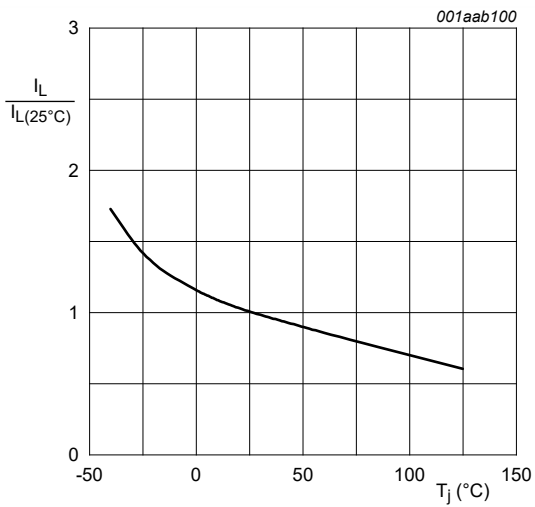


Fig. 8. Normalized latching current as a function of junction temperature

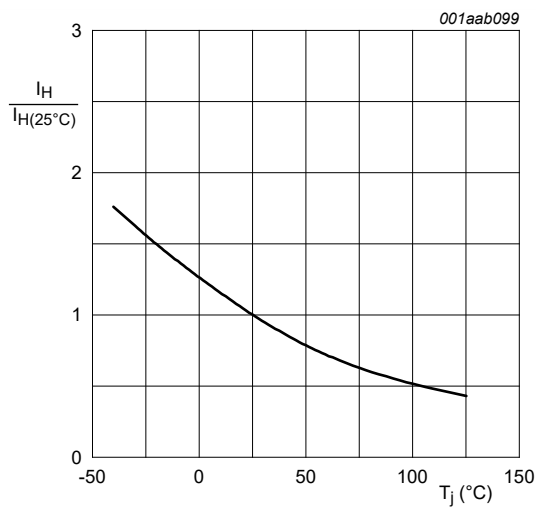


Fig. 9. Normalized holding current as a function of junction temperature

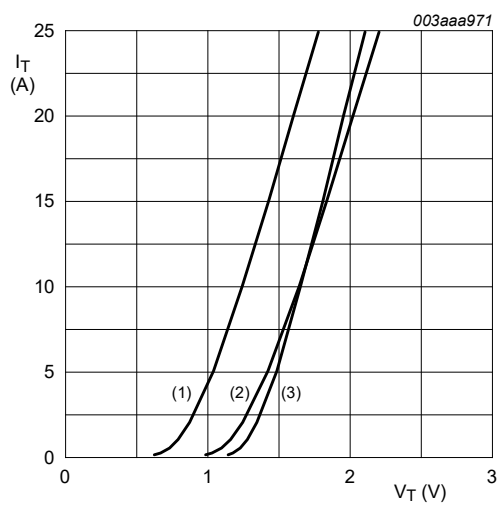
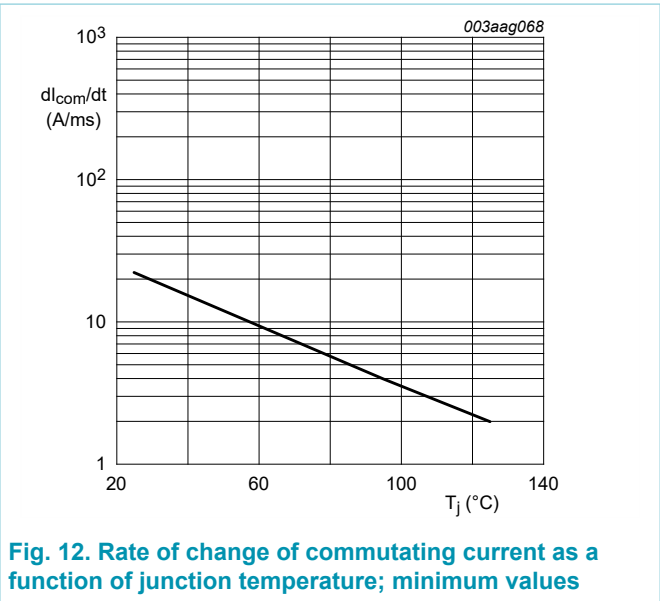
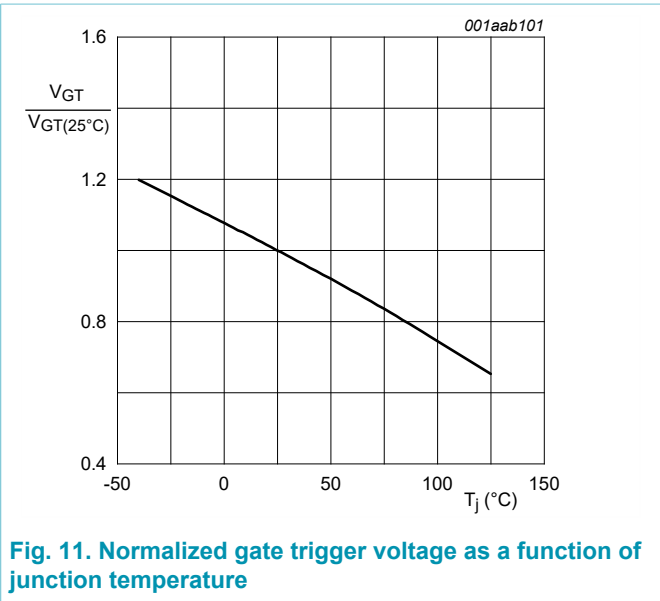


Fig. 10. On-state current as a function of on-state voltage





10. Package outline

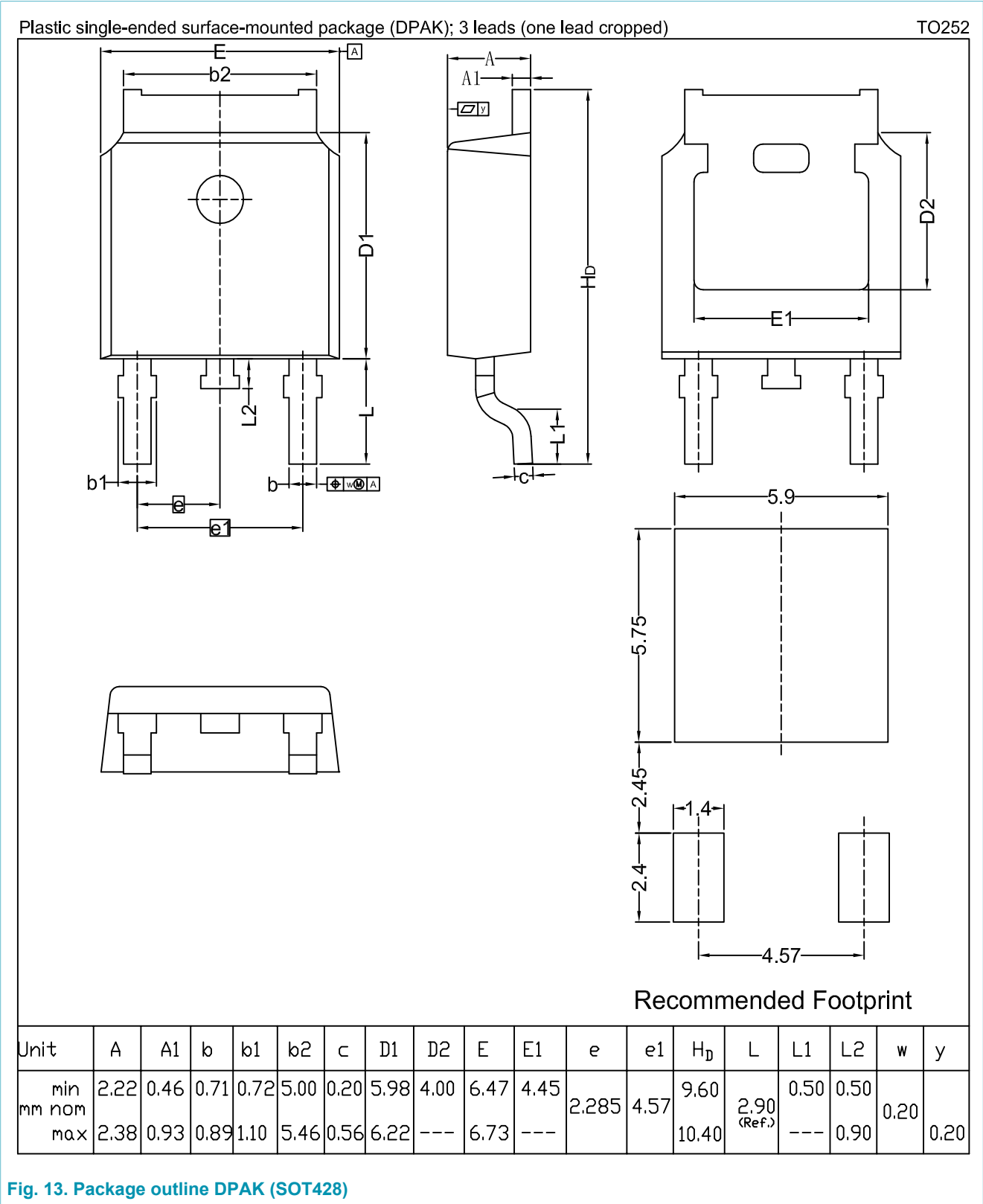


Fig. 13. Package outline DPAK (SOT428)

## 11. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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