



#### **General Description**

The MAX17020 is a dual Quick-PWM™ step-down power-supply (SMPS) controller with synchronous rectification, intended for main 5V/3.3V or I/O 1.5V/1.05V power generation in battery-powered systems. Lowside MOSFET sensing provides a simple low-cost, highly efficient current sense for valley current-limit protection. Combined with the output overvoltage and undervoltage protection features, this current limit ensures robust output supplies.

The 5V/3.3V or 1.5V/1.05V SMPS outputs can save power by operating in pulse-skipping mode or in ultrasonic mode to avoid audible noise. Ultrasonic mode forces the controller to maintain switching frequencies greater than 20kHz at light loads.

An internal 100mA linear regulator can be used to either generate the 5V bias needed for power-up or other lower power "always-on" suspend supplies. An independent bypass input allows automatic bypassing of the linear regulator when the SMPS is active.

This main controller also includes a secondary feedback input that triggers an ultrasonic pulse (DL1 turned on) if the SECFB voltage drops below its threshold voltage. This refreshes an external charge pump driven by DL1 without overcharging the output voltage.

The device includes independent shutdown controls to simplify power-up and power-down sequencing. To prevent current surges at startup, the internal voltage target is slowly ramped up from zero to the final target over a 1ms period. To prevent the output from ringing below ground in shutdown, the internal voltage target is ramped down from its previous value to zero over a 1ms period. Two independent power-good outputs simplify the interface with external controllers.

The MAX17020 is a pin-for-pin replacement of the MAX8778.

#### **Applications**

**Notebook Computers** 

Main System Supply (5V and 3.3V Supplies)

I/O System Supply (1.5V and 1.05V Supplies)

Graphic Cards

DDR1, DDR2, DDR3 Power Supplies

Game Consoles

Low-Power I/O and Chipset Supplies

Two-to-Four Li+ Cell Battery-Powered Devices

PDAs and Mobile Communicators

**Telecommunication** 

#### Features

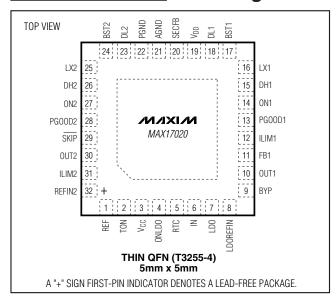
- **♦ Dual Quick-PWM**
- ♦ Internal 100mA 5V or Adjustable Linear Regulator
- ♦ Independent LDO Bypass Input
- ♦ Internal Boost Diodes
- ♦ Secondary Feedback Input Maintains Charge Pump
- ♦ 3.3V 5mA RTC Power (Always On)
- ♦ OUT1: 5V or 1.5V Fixed or 0.7V Adjustable **Feedback**
- ♦ OUT2: 3.3V or 1.05V Fixed or Dynamic Adjustable
- ♦ Dynamic 0V to 2V REFIN2 Input on Second SMPS
- ♦ 2V ±1% 50µA Reference
- ♦ 6V to 24V Input Range (28V max)
- **♦ Ultrasonic Mode**
- ♦ Independent SMPS and LDO Enable Controls
- ♦ Independent SMPS Power-Good Outputs
- **♦** Minimal Component Count

#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX17020ETJ+	-40°C to +85°C	32 TQFN

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

#### Pin Configuration



Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Maxim Integrated Products 1

<sup>\*</sup>EP = Exposed pad.

#### **ABSOLUTE MAXIMUM RATINGS**

IN, ONLDO to GND	
	0.3V to +28V

BST1 to LX1	0.3V to (V <sub>BST2</sub> + 0.3V) 0.3V to +6V Momentary
LDO Current (Internal Regulator)	
Continuous	+100mA
LDO Current (Switched Over) Continuou	us+200mA
Continuous Power Dissipation ( $T_A = +70$	O°C)
32-Pin 5mm x 5mm TQFN	
(derate 34.5mW/°C above +70°C)	2.76W
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN,  $ON1 = ON2 = V_{CC}$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS
INPUT SUPPLIES						
IN Standby Supply Current	I <sub>IN(STBY)</sub>	V <sub>IN</sub> = 6V to 24V, ON1 = ON2 = GND, ONLDO = V <sub>CC</sub>		85	175	μА
IN Shutdown Supply Current	IN(SHDN)	V <sub>IN</sub> = 4.5V to 24V, ON1 = ON2 = ONLDO = GND		50	70	μA
IN Supply Current	I <sub>IN</sub>	ON1 = ON2 = REFIN2 = V <sub>CC</sub> , SKIP = FB1 = GND, V <sub>OUT2</sub> = 3.5V, V <sub>OUT1</sub> = 5.3V		0.1	0.2	mA
V <sub>CC</sub> Supply Current	Icc			1.0	1.5	mA
PWM CONTROLLERS						
	V0.7	5V preset output: FB1 = GND, V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	4.95	5.00	5.05	
OUT1 Output Voltage Accuracy (Note 1)	VOUT1	1.5V preset output: FB1 = V <sub>CC</sub> (5V), V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	1.485	1.50	1.515	V
	V <sub>FB1</sub>	Adjustable feedback output, V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	0.693	0.700	0.707	
OUT1 Voltage Adjust Range			0.7		5.5	V
FB1 Dual-Mode™ Threshold		Low	0.04		0.110	
Voltage Levels		High	V <sub>CC</sub> - 1.6V		V <sub>CC</sub> - 0.7V	V
FB1 Input Bias Current	I <sub>FB1</sub>	V <sub>FB1</sub> = 0.8V, T <sub>A</sub> = +25°C	-0.2		+0.2	μΑ

Dual Mode is a trademark of Maxim Integrated Products, Inc.

#### **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN}$  = 12V,  $V_{DD}$  =  $V_{CC}$  =  $V_{SECFB}$  = 5V,  $V_{REFIN2}$  = 1.0V, BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $T_A$  = 0°C to +85°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Note 3)

PARAMETER	SYMBOL	CON	NDITIONS	MIN	TYP	MAX	UNITS
		3.3V preset output: I V <sub>IN</sub> = 12V, SKIP = V		3.267	3.30	3.333	
OUT2 Output Voltage Accuracy (Note 1)	V <sub>OUT2</sub>	1.05V preset output: V <sub>IN</sub> = 12V, SKIP = V	REFIN2 = RTC (3.3V),	1.040	1.050	1.060	V
		Tracking output: V <sub>RI</sub> V <sub>IN</sub> = 12V, SKIP = V		0.995	1.00	1.005	
OUT2 Voltage-Adjust Range				0		2	V
REFIN2 Voltage-Adjust Range				0		2	V
DEEING Input Biog Current	le seu in	VREFIN2 = 2.2V, TA =	= +25°C	-0.1		+0.1	
REFIN2 Input Bias Current	IREFIN2	$V_{REFIN2} = 0, T_A = +3$	25°C	-0.5		+0.1	μA
REFIN2 Dual-Mode Threshold		Low (REFIN2 = RTC	:)	2.2		3.0	
Voltage Levels		High (REFIN2 = V <sub>CC</sub>	s)	V <sub>CC</sub> - 1.0V		V <sub>CC</sub> - 0.4V	V
		Either SMPS, SKIP =	VCC, ILOAD = 0 to 5A		-0.1		
Load Regulation Error		Either SMPS, SKIP =	REF, I <sub>LOAD</sub> = 0 to 5A		-1.7		%
		Either SMPS, SKIP =	GND, I <sub>LOAD</sub> = 0 to 5A		-1.5		]
Line Regulation Error		Either SMPS, V <sub>IN</sub> = 6	6V to 24V		0.005		%N
DH1 On-Time	ton1	V <sub>IN</sub> = 12V, V <sub>OUT1</sub> = 5.0V	TON = GND or REF (400kHz)	895	1052	1209	ns
		(Note 2)	$TON = V_{CC} (200kHz)$	1895	2105	2315	
		V <sub>IN</sub> = 12V,	TON = GND (500kHz)	475	555	635	
DH2 On-Time	t <sub>ON2</sub>	V <sub>OUT2</sub> = 3.3V (Note 2)	TON = REF or V <sub>CC</sub> (300kHz)	833	925	1017	ns
Minimum Off-Time	toff(MIN)	(Note 2)	•		250	400	ns
Soft-Start/Stop Slew Rate	tss	Rising/falling edge	on ON1 or ON2 (preset)		1		ms
Soft-Start/Stop Slew Rate	tss	Rising/falling edge	on ON2 (REFIN2 ADJ)		1		mV/µs
Dynamic REFIN2 Slew Rate	t <sub>DYN</sub>	Rising edge on REF	IN2		8		mV/μs
Ultrasonic Operating Frequency	fsw(usonic)	SKIP = open (REF)		20	27		kHz
SECFB Threshold Voltage	VSECFB			1.94	2.0	2.06	V
SECFB Input Bias Current	ISECFB	VSECFB = 2.2V, TA =	+25°C	-0.2		+0.2	μΑ
LINEAR REGULATOR (LDO)							
		V <sub>IN</sub> = 24V, LDOREFI 0mA < I <sub>LDO</sub> < 100m		4.90	5.0	5.10	
LDO Output-Voltage Accuracy	V <sub>LDO</sub>	V <sub>IN</sub> = 24V, LDOREFIN = V <sub>CC</sub> , BYP = GND, 0mA < I <sub>LDO</sub> < 100mA		3.23	3.3	3.37	V
		V <sub>IN</sub> = 24V, BYP = GND, V <sub>LDOREFIN</sub> = 0.5V, 0mA < I <sub>LDO</sub> < 100mA		0.960	1.0	1.040	
LDOREFIN Input Range	VLDOREFIN	VLDO = 2 x VLDOREFIN		0.3		2.0	V
LDOREFIN Leakage Current	ILDOREFIN	VLDOREFIN = 0 or 2V	′, T <sub>A</sub> = +25°C	-0.5		+0.5	μΑ
LDOREFIN Dual-Mode		LDOREFIN low thres	shold	0.1	0.15	0.20	1 1
Threshold Voltage		LDOREFIN high thre	eshold	V <sub>CC</sub> -	V <sub>CC</sub> - 1.5V	V <sub>CC</sub> - 0.9V	V

#### **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $T_A = 0^{\circ}C$  to +85°C, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS
LDO Short-Circuit Current	lilim(LDO)	LDO = GND	100		260	mA
LDO Regulation Reduction/ Bypass Switchover Threshold		With respect to the LDO voltage, falling edge of BYP		-8.5	-6.0	%
LDO Bypass Switchover Threshold		With respect to the LDO voltage, rising edge of BYP		-6.5		%
LDO Bypass Switchover Startup Timeout	t <sub>BYP</sub>	Rising edge of BYP to bypass gate pulled low		500		μs
LDO Bypass Switch Resistance		LDO to BYP, V <sub>BYP</sub> = 5V (Note 4)		1.2	4.5	Ω
V <sub>CC</sub> Undervoltage-Lockout (UVLO) Threshold	V <sub>UV</sub> LO(VCC)	Falling edge of V <sub>CC</sub> , PWM disabled below this threshold	3.8	4.0	4.3	V
(OVEO) Triconold		Rising edge of V <sub>CC</sub>		4.2		
Thermal-Shutdown Threshold	TSHDN	Hysteresis = 10°C		+160		°C
3.3V ALWAYS-ON LINEAR REG	ULATOR (RT	(C)				
RTC Output-Voltage Accuracy	\/DT0	ON1 = ON2 = GND, $V_{IN}$ = 6V to 24V, $0 < I_{RTC} < 5mA$	3.23	3.33	3.43	V
The Output-Voltage Accuracy	VRTC	ON1 = ON2 = ONLDO = GND, V <sub>IN</sub> = 6V to 24V, 0 < I <sub>RTC</sub> < 5mA	3.19 3.		3.47	V
RTC Short-Circuit Current	IILIM(RTC)	RTC = GND	5		30	mA
REFERENCE (REF)						
Reference Voltage	V <sub>REF</sub>	V <sub>CC</sub> = 4.5V to 5.5V, I <sub>REF</sub> = 0	1.980	2.00	2.020	V
Reference Load-Regulation Error	$\Delta V_{REF}$	I <sub>REF</sub> = -20μA to 50μA	-10		+10	mV
REF Lockout Voltage	V <sub>REF</sub> (UVLO)	Rising edge, 350mV (typ) hysteresis		1.95		V
OUT1 FAULT DETECTION						
OUT1 Overvoltage Trip Threshold	VovP(out1)	With respect to error-comparator threshold	13	16	19	%
OUT1 Overvoltage Fault- Propagation Delay	tovp	FB1 forced 50mV above trip threshold		10		μs
OUT1 Undervoltage-Protection Trip Threshold	VuvP(OUT1)	With respect to error-comparator threshold	65	70	75	%
OUT1 Output-Undervoltage Fault-Propagation Delay	tuvp			10		μs
PGOOD1 Lower Trip Threshold		With respect to error-comparator threshold, falling edge, hysteresis = 1%	-19	-16	-13	%
PGOOD1 Propagation Delay	tPGOOD1	FB1 forced 50mV beyond PGOOD1 trip threshold, falling edge		10		μs
PGOOD1 Output Low Voltage		V <sub>FB1</sub> = 0.56V (PGOOD1 low impedance), I <sub>SINK</sub> = 4mA			0.3	V
PGOOD1 Leakage Current	IPGOOD1	V <sub>FB1</sub> = 0.70V (PGOOD1 high impedance), PGOOD1 forced to 5.5V, T <sub>A</sub> = +25°C			1	μΑ

\_\_\_ /VIXI/VI

#### **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $T_A = 0^{\circ}C$  to +85°C, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			TYP	MAX	UNITS
OUT2 FAULT DETECTION							
		Preset mode (REFIN2 respect to error-comp	2 = RTC or V <sub>CC</sub> ): with parator threshold	13	16	19	%
OUT2 Overvoltage Trip Threshold	Vovp(out2)	Dynamic transition,  SKIP = REF or V <sub>CC</sub> a	nd OUT2 > REFIN2		V <sub>REF</sub> + 0.20		V
		Tracking mode: with re	espect to REFIN2 voltage	170	200	230	mV
		Minimum overvoltage	e threshold		0.7		V
OUT2 Overvoltage Fault-Propagation Delay	tovp	OUT2 forced 50mV a	bove trip threshold		10		μs
OUT2 Undervoltage-Protection Trip Threshold	Vuvp(out2)	Preset mode: with reservor-comparator three	•	65	70	75	%
Trip Threshold		Tracking mode: with re	espect to REFIN2 voltage	-250	-300	-350	mV
OUT2 Overvoltage Fault-Propagation Delay	tovp	OUT2 forced 50mV a	bove trip threshold		10		μs
OUT2 Output Undervoltage Fault-Propagation Delay	tuvp	OUT2 forced 50mV b	elow trip threshold		10		μs
Dynamic REFIN2 Transition PGOOD Blanking Threshold		Blanking initiated; REFIN2 deviation from the internal target voltage (error-comparator threshold); hysteresis = 5mV			±25		mV
PGOOD2 Lower Trip Threshold			Preset mode: with respect to error-comparator threshold, falling edge, hysteresis = 1%		-16	-13	%
T GOODZ Lower Trip Trireshold		Tracking mode: with voltage, falling edge,		-175	-150	-125	mV
PGOOD2 Propagation Delay	tpGOOD2	OUT2 forced 50mV b threshold, falling edg			10		μs
PGOOD2 Output-Low Voltage		VOUT2 = VREFIN2 - 15 impedance), ISINK =				0.3	V
PGOOD2 Leakage Current	IPGOOD2	OUT2 = REFIN2 (PG/ PGOOD2 forced to 5	OOD2 high impedance), .5V, T <sub>A</sub> = +25°C			1	μΑ
CURRENT LIMIT							
ILIM_ Adjustment Range	VILIM			0.2		2.0	V
ILIM_ Current	I <sub>ILIM</sub>				5		μΑ
Valley Current-Limit Threshold			$R_{ILIM} = 100k\Omega$	44	50	56	
(Adjustable)	VVALLEY	VAGND - VLX_	$R_{ILIM} = 200k\Omega$	90	100	110	mV
			$R_{ILIM} = 400k\Omega$	180	200	220	
Current-Limit Threshold (Negative)	VNEG	With respect to valley current-limit threshold, SKIP = VCC			-120		%
Ultrasonic Current-Limit Threshold	VNEG(US)	VOUT1 = VOUT2 = VFB1	$= 0.77V$ , $V_{REFIN2} = 0.70V$		25		mV
Current-Limit Threshold (Zero Crossing)	V <sub>Z</sub> X	VAGND - VLX_, SKIP =	V <sub>AGND</sub> - V <sub>LX</sub> , <del>SKIP</del> = GND or OPEN/REF				mV

#### **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $T_A = 0^{\circ}C$  to +85°C, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 3)

PARAMETER	SYMBOL	CON	DITIONS	MIN	TYP	MAX	UNITS
GATE DRIVERS	•			•			•
DH_ Gate Driver On-Resistance	RDH	BST1 - LX1 and BST2	2 - LX2 forced to 5V		1.5	3.5	Ω
DL_ Gate Driver On-Resistance	R <sub>DL</sub>	DL1, DL2; high state			2.2	4.5	Ω
DL_ date briver off-resistance	LIDE	DL1, DL2; low state			0.6	1.5	52
DH_ Gate Driver Source/Sink Current	I <sub>DH</sub>	DH1, DH2 forced to 2 BST1 - LX1 and BST2			2		А
DL_ Gate Driver Source Current	I <sub>DL</sub> (SOURCE)	DL1, DL2 forced to 2	.5V		1.7		А
DL_ Gate Driver Sink Current	IDL (SINK)	DL1, DL2 forced to 2	.5V		3.3		А
Internal BST_ Switch On-Resistance	R <sub>BST</sub>	I <sub>BST</sub> = 10mA, V <sub>DD</sub> =	= 5V		5		Ω
BST_ Leakage Current	I <sub>BST</sub>	V <sub>BST</sub> = 26V, T <sub>A</sub> = +25°C, OUT2 and FB1 above regulation threshold			0.1	5	μА
INPUTS AND OUTPUTS							
		High REF or open		V <sub>CC</sub> - 0.4V			
TON Input Logic Levels				1.6		3.0	\ \
		Low			0.4		
		High (forced-PWM)		V <sub>CC</sub> - 0.4V			
SKIP Input Logic Levels		Open (ultrasonic)		1.6		3.0	V
		Low (skip)				0.4	
SKIP, TON Leakage Current	ISKIP, ITON	$V_{\overline{SKIP}} = V_{TON} = 0$ or	5V, T <sub>A</sub> = +25°C	-2		+2	μA
ON Input Logic Levels		68mV hysteresis	High (SMPS on)	2.4			V
ON_ Input Logic Levels		Contractive trysteresis	Low (SMPS off)			0.8	v
ON_ Leakage Current	I <sub>ON</sub> _	V <sub>ON1</sub> = V <sub>ON2</sub> = 0 or 5V, T <sub>A</sub> = +25°C		-2		+2	μΑ
ONLDO Input Logic Levels		68mV hysteresis	High (SMPS on)	2.4			V
ONEDO Input Logic Levels		Low (SMPS off)				0.8	\ \ \
ONLDO Leakage Current	IONLDO	V <sub>ONLDO</sub> = 0 or 24V, T <sub>A</sub> = +25°C		-1		+1	μA

#### **ELECTRICAL CHARACTERISTICS**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN}$  = 12V,  $V_{DD}$  =  $V_{CC}$  =  $V_{SECFB}$  = 5V,  $V_{REFIN2}$  = 1.0V, BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $V_{CC}$ 

PARAMETER	SYMBOL	CONDI	MIN	TYP	MAX	UNITS		
INPUT SUPPLIES								
IN Standby Supply Current	IIN(STBY)	V <sub>IN</sub> = 6V to 24V, ON1 = ONLDO = V <sub>CC</sub>			200	μА		
IN Shutdown Supply Current	IN(SHDN)	V <sub>IN</sub> = 4.5V to 24V, ON1 =	: ON2 = ONLDO = GND			70	μΑ	
IN Supply Current	I <sub>IN</sub>	ON1 = ON2 = REFIN2 : SKIP = FB1 = GND, V <sub>OU</sub>				0.2	mA	
V <sub>CC</sub> Supply Current	Icc	ON1 = ON2 = REFIN2 : SKIP = FB1 = GND, V <sub>OU</sub>				1.5	mA	
PWM CONTROLLERS								
	V	5V preset output: FB1 = V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	= GND,	4.90		5.10		
OUT1 Output-Voltage Accuracy (Note 1)	VouT1	1.5V preset output: FB1 V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	= V <sub>CC</sub> (5V),	1.47		1.53	V	
	VFB1	Adjustable feedback of VIN = 12V, SKIP = VCC	utput,	0.685		0.715		
OUT1 Voltage-Adjust Range				0.7		5.5	V	
FB1 Dual-Mode Threshold		Low		0.040		0.125		
Voltage		High		V <sub>CC</sub> - 1.6V		V <sub>CC</sub> - 0.7V	V	
		3.3V preset output: REF V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	$FIN2 = V_{CC} (5V),$	3.234		3.366	71 V	
OUT2 Output-Voltage Accuracy (Note 1)	V <sub>OUT2</sub>	1.05V preset output: RE V <sub>IN</sub> = 1.2V, SKIP = V <sub>CC</sub>		1.029		1.071		
		Tracking output: V <sub>REFIN</sub> V <sub>IN</sub> = 12V, SKIP = V <sub>CC</sub>	y <sub>2</sub> = 1.0V,	0.985		1.015		
OUT2 Voltage-Adjust Range				0		2	V	
REFIN2 Voltage-Adjust Range				0		2	V	
REFIN2 Dual-Mode Threshold		Low (REFIN2 = RTC)		2.2		3.0		
Voltage		High (REFIN2 = V <sub>CC</sub> )		V <sub>CC</sub> - 1.2V		V <sub>CC</sub> - 0.4V	V	
DH1 On-Time	t <sub>ON1</sub>	V <sub>IN</sub> = 12V, V <sub>OUT1</sub> = 5.0V (Note 2)	TON = GND or REF (400kHz)	895		1209	ns	
		VOUT1 = 5.0V (Note 2)	TON = V <sub>CC</sub> (200kHz)	1895		2315		
		V <sub>IN</sub> = 12V.	TON = GND (500kHz)	475		635		
DH2 On-Time	t <sub>ON2</sub>	$V_{OUT2} = 3.3V \text{ (Note 2)}$	TON = REF or V <sub>CC</sub> (300kHz)	833		1017	ns	
Minimum Off-Time	toff(MIN)	(Note 2)				425	ns	
Ultrasonic Operating Frequency	fsw(usonic)	SKIP = open (REF)	18			kHz		
SECFB Threshold Voltage	VSECFB		1.92		2.08	V		

#### **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $V_{CC}$ , V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (LDO)						•
		V <sub>IN</sub> = 24V, LDOREFIN = BYP = GND, 0mA < I <sub>LDO</sub> < 100mA	4.85		5.15	
LDO Output-Voltage Accuracy	V <sub>LDO</sub>	$V_{IN} = 24V$ , LDOREFIN = $V_{CC}$ , BYP = GND, 0mA < $I_{LDO}$ < 100mA	3.20		3.40	V
		V <sub>IN</sub> = 24V, BYP = GND, V <sub>LDOREFIN</sub> = 0.5V, 0mA < I <sub>LDO</sub> < 100mA	0.960		1.040	
LDOREFIN Input Range	VLDOREFIN	V <sub>LDO</sub> = 2x V <sub>LDOREFIN</sub>	0.3		2.0	V
LDODEEN DO LAM		LDOREFIN low threshold	0.10		0.25	
LDOREFIN Dual-Mode Threshold Voltage		LDOREFIN high threshold	V <sub>CC</sub> -		V <sub>CC</sub> - 0.9V	V
LDO Short-Circuit Current	lilim(LDO)	LDO = GND			260	mA
LDO Regulation Reduction/ Bypass Switchover Threshold		Falling edge of BYP	-12		-5	%
V <sub>CC</sub> Undervoltage-Lockout Threshold	V <sub>UVLO(VCC)</sub>	Falling edge of V <sub>CC</sub> , PWM disabled below this threshold	3.8		4.3	V
3.3V ALWAYS-ON LINEAR REG	ULATOR (RT	C)				
DTO O	\/==0	ON1 = ON2 = GND, V <sub>IN</sub> = 6V to 24V, 0 < I <sub>RTC</sub> < 5mA	3.18		3.45	V
RTC Output-Voltage Accuracy	VRTC	ON1 = ON2 = ONLDO = GND, V <sub>IN</sub> = 6V to 24V, 0 < I <sub>RTC</sub> < 5mA	3.16		3.50	v
RTC Short-Circuit Current	ILIM(RTC)	RTC = GND	5		30	mA
REFERENCE (REF)						
Reference Voltage	V <sub>REF</sub>	V <sub>CC</sub> = 4.5V to 5.5V, I <sub>REF</sub> = 0	1.975		2.025	V
Reference Load-Regulation Error	V <sub>REF</sub>	I <sub>REF</sub> = -20μA to 50μA	-10		+10	mV
OUT1 FAULT DETECTION						
OUT1 Overvoltage Trip Threshold	VovP(OUT1)	With respect to error-comparator threshold	12		20	%
OUT1 Undervoltage-Protection Trip Threshold	VUVP(OUT1)	With respect to error-comparator threshold	63		77	%
PGOOD1 Lower Trip Threshold		With respect to error-comparator threshold, falling edge, hysteresis = 1%	-20		-12	%
PGOOD1 Output-Low Voltage		V <sub>FB1</sub> = 0.56V (PGOOD1 low impedance), I <sub>SINK</sub> = 4mA			0.4	V
OUT2 FAULT DETECTION						•
OUT2 Overvoltage Trip	Vovp(out2)	Preset mode (REFIN2 = RTC or V <sub>CC</sub> ): with respect to error-comparator threshold	12		20	%
Threshold	()	Tracking mode: with respect to REFIN2 voltage	160		240	mV

· \_\_\_\_\_ NIXIM

#### **ELECTRICAL CHARACTERISTICS (continued)**

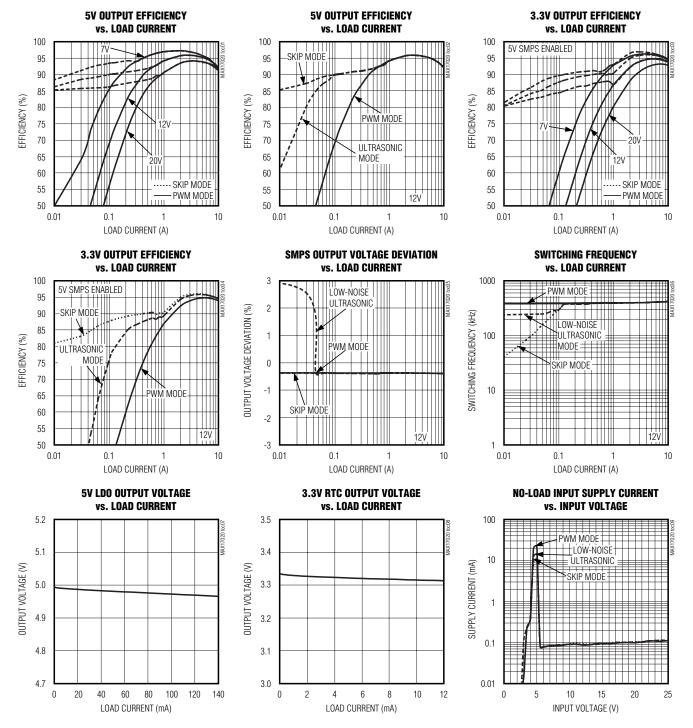
(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = V_{SECFB} = 5V$ ,  $V_{REFIN2} = 1.0V$ , BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 =  $V_{CC}$ ,  $V_{CC}$ ,  $V_{CC}$ ,  $V_{CC}$ , unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	co	ONDITIONS	MIN	TYP	MAX	UNITS	
OUT2 Undervoltage-Protection Trip Threshold	V <sub>UVP(OUT2)</sub>	Preset mode: with r threshold	espect to error-comparator	63		77	%	
rrip i rriesnoia	,	Tracking mode: with	respect to REFIN2 voltage	-230		-370	mV	
DCCCDC Louise Trip Threehold			respect to error-comparator dge, hysteresis = 1%	-20		-12	%	
PGOOD2 Lower Trip Threshold			h respect to REFIN2 e, hysteresis = 12mV	-185		-115	mV	
PGOOD2 Output-Low Voltage		V <sub>OUT2</sub> = V <sub>REFIN2</sub> - impedance), I <sub>SINK</sub>	150mV (PGOOD2 low = 4mA			0.4	V	
CURRENT LIMIT	· U	•		I.				
ILIM_ Adjustment Range	VILIM			0.2		2.0	V	
			$R_{ILIM} = 100k\Omega$	40		60		
Valley Current-Limit Threshold (Adjustable)	VVALLEY	VAGND - VLX_	$R_{ILIM} = 200k\Omega$	85		115	mV	
(Adjustable)			$R_{ILIM} = 400k\Omega$	164		236		
GATE DRIVERS								
DH_ Gate Driver On-Resistance	R <sub>DH</sub>	BST1 - LX1 and BS	T2 - LX2 forced to 5V			3.5	Ω	
DL_ Gate Driver On-Resistance	R <sub>DL</sub>	DL1, DL2; high state				4.5	Ω	
DL_ Gate Driver On-nesistance	חטר	DL1, DL2; low state	)			1.5	52	
INPUTS AND OUTPUTS								
		High		V <sub>CC</sub> - 0.4V				
TON Input Logic Levels		REF or open		1.6		3.0	V	
		Low				0.4		
		High (forced-PWM)		V <sub>CC</sub> - 0.4V				
SKIP Input Logic Levels		Open (ultrasonic)		1.6		3.0	V	
		Low (skip)				0.4		
		High (SMPS on)					V	
ON_ Input Logic Levels		Low (SMPS off)			0.8	V		
ONI DO Input Logio Lovelo		High (LDO on)		2.4			V	
ONLDO Input Logic Levels		Low (LDO off)			0.8	V		

- Note 1: DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17020 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction (I<sub>OUT</sub> < I<sub>LOAD(SKIP)</sub>), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.
- **Note 2:** On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = PGND, VBST = 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.
- Note 3: Limits are 100% production tested at T<sub>A</sub> = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.
- Note 4: Specifications increased by  $1\Omega$  to account for test measurement error.

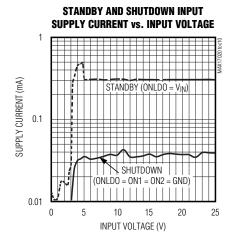
#### Typical Operating Characteristics

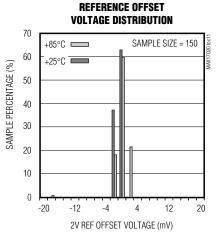
(Circuit of Figure 1, V<sub>IN</sub> = 12V, V<sub>DD</sub> = V<sub>CC</sub> = 5V, TON = REF, T<sub>A</sub> = +25°C, unless otherwise noted.)

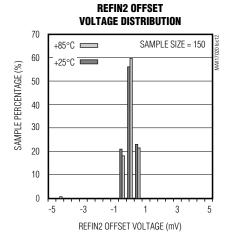


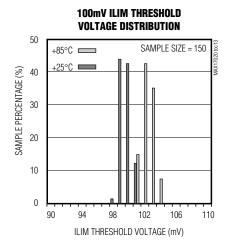
#### Typical Operating Characteristics (continued)

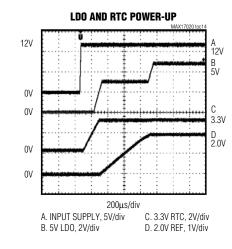
(Circuit of Figure 1,  $V_{IN}$  = 12V,  $V_{DD}$  =  $V_{CC}$  = 5V, TON = REF,  $T_A$  = +25°C, unless otherwise noted.)

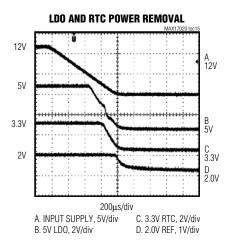






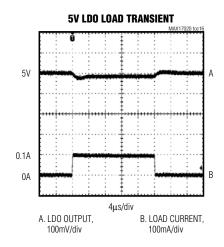


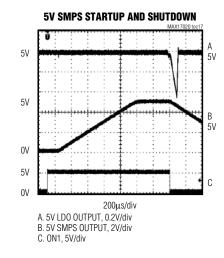


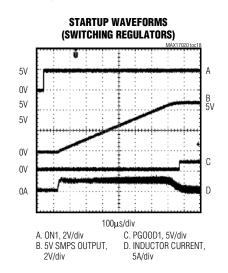


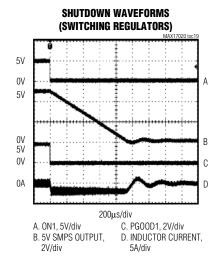
#### **Typical Operating Characteristics (continued)**

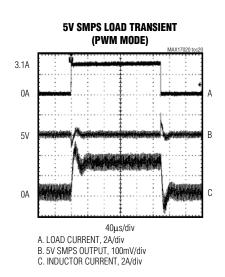
(Circuit of Figure 1,  $V_{IN}$  = 12V,  $V_{DD}$  =  $V_{CC}$  = 5V, TON = REF,  $T_A$  = +25°C, unless otherwise noted.)





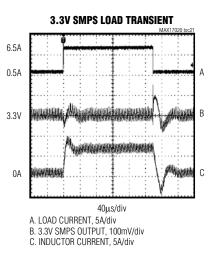


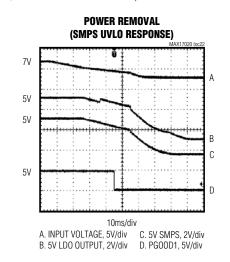




#### Typical Operating Characteristics (continued)

(Circuit of Figure 1,  $V_{IN}$  = 12V,  $V_{DD}$  =  $V_{CC}$  = 5V, TON = REF,  $T_A$  = +25°C, unless otherwise noted.)





#### **Pin Description**

PIN	NAME	FUNCTION
1	REF	2V Reference-Voltage Output. Bypass REF to AGND with a 0.1μF or greater ceramic capacitor. The reference can source up to 50μA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error. The reference shuts down when ON1, ON2, and ONLDO are all pulled low.
2	TON	Switching-Frequency Setting Input. Select the OUT1/OUT2 switching frequencies by connecting TON as follows for:  High (Vcc) = 200kHz/300kHz  Open (REF) = 400kHz/300kHz  GND = 400kHz/500kHz
3	Vcc	Analog Supply Voltage Input. Connect $V_{CC}$ to the system supply voltage with a series $50\Omega$ resistor, and bypass to analog ground using a $1\mu F$ or greater ceramic capacitor.
4	ONLDO	Enable Input for LDO. Drive ONLDO high to enable the linear regulator (LDO) output. Drive ONLDO low to shut down the linear regulator output.
5	RTC	3.3V Always-On Linear Regulator Output for RTC Power. Bypass RTC with a 1µF or greater ceramic capacitor to analog ground. RTC can source at least 5mA for external load support. RTC power-up is required for controller operation.
6	IN	Power-Input Supply. IN powers the linear regulators (RTC and LDO) and senses the input voltage for the Quick-PWM on-time one-shot timers. The high-side MOSFET's on-time is inversely proportional to the input voltage. Bypass IN with a 0.1µF or greater ceramic capacitor to PGND close to the MAX17020.
7	LDO	Linear Regulator Output. Bypass LDO with a 4.7µF or greater ceramic capacitor. LDO can source at least 100mA for external load support. LDO is powered from IN and its regulation threshold is set by LDOREFIN. For preset 5V operation, connect LDOREFIN directly to GND. For preset 3.3V operation, connect LDOREFIN directly to V <sub>CC</sub> . When LDO is used for 5V operation, LDO must supply V <sub>CC</sub> and V <sub>DD</sub> .

#### Pin Description (continued)

PIN	NAME	FUNCTION
8	External Reference Input for the Linear Regulator. LDOREFIN sets the LDO regulation voltage (V <sub>LDO</sub> V <sub>LDOREFIN</sub> ) for a 0.3V to 2V LDOREFIN range. Connect LDOREFIN to GND for a fixed 5V linear-regulator output voltage, or connect LDOREFIN to V <sub>CC</sub> for a fixed 3.3V linear-regulator output voltage. When L to 5V and is enabled, LDO must supply V <sub>CC</sub> and V <sub>DD</sub> .	
9 BYP bypasses the LDO output to the BYP input. The bypass switch is disabled if the LDO voltage drop		Linear Regulator Bypass Input. When BYP voltage exceeds 93.5% of the LDO voltage, the controller bypasses the LDO output to the BYP input. The bypass switch is disabled if the LDO voltage drops by 8.5% from its nominal regulation threshold. When not being used, connect BYP to GND.
10	OUT1	Output Voltage-Sense Input for SMPS1. OUT1 is an input to the Quick-PWM on-time one-shot timer. OUT1 also serves as the feedback input for the preset 5V (FB1 = GND) and 1.5V (FB1 = $V_{CC}$ ) output voltage settings.
11	FB1	Adjustable Feedback Voltage-Sense Connection for SMPS1. Connect FB1 to GND for fixed 5V operation. Connect FB1 to V <sub>CC</sub> for fixed 1.5V operation. Connect FB1 to an external resistive voltage-divider from OUT1 to analog ground to adjust the output voltage between 0.7V and 5.5V.
12	ILIM1	Valley Current-Limit Adjustment for SMPS1. The GND - LX1 current-limit threshold is 1/10 the voltage present on ILIM1 over a 0.2V to 2V range. An internal 5µA current source allows this voltage to be set with a single resistor between ILIM1 and analog ground.
13 PGOOD1 the nominal regulation threshold, during soft-start, in shutdown, and after		Open-Drain Power-Good Output for SMPS1. PGOOD1 is low when the output voltage is more than 16% (typ) below the nominal regulation threshold, during soft-start, in shutdown, and after the fault latch has been tripped. After the soft-start circuit has terminated, PGOOD1 becomes high impedance if the output is in regulation.
14	ON1	Enable Input for SMPS1. Drive ON1 high to enable SMPS1. Drive ON1 low to shut down SMPS1.
15	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1.
16	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 is the lower supply rail for the DH1 high-side gate driver.
17	BST1	Boost Flying-Capacitor Connection for SMPS1. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST1 allows the DH1 turn-on current to be adjusted.
18	DL1	Low-Side Gate-Driver Output for SMPS1. DL1 swings from PGND to V <sub>DD</sub> .
19	V <sub>DD</sub>	Supply-Voltage Input for the DL_ Gate Drivers. Connect to a 5V supply. Also connect to the drain of the BST diode switch.
20 SECFB		Secondary Feedback Input. The secondary feedback input forces the SMPS1 output into ultrasonic mode when the SECFB voltage drops below its 2V threshold voltage. This forces DL1 and DH1 to switch, allowing the system to refresh an external low-power charge pump being driven by DL1 (see Figure 1). Connect SECFB to V <sub>CC</sub> to the 5V bias supply to disable secondary feedback.
21 AGND Analog Ground. Connect the backside exposed pad to AGND.		Analog Ground. Connect the backside exposed pad to AGND.
22	PGND	Power Ground
23	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V <sub>DD</sub> .
24	BST2	Boost Flying-Capacitor Connection for SMPS2. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST2 allows the DH2 turn-on current to be adjusted.
25 LX2 Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower s for the DH2 high-side gate driver.		Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower supply rail for the DH2 high-side gate driver.

### Pin Description (continued)

PIN	NAME	FUNCTION	
26	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2.	
27	ON2	Enable Input for SMPS2. Drive ON2 high to enable SMPS2. Drive ON2 low to shut down SMPS2.	
28	PGOOD2	Open-Drain Power-Good Output for SMPS2. PGOOD2 is low when the output voltage is more than 150mV (typ) below the REFIN2 voltage or more than 16% below the preset voltage, during soft-start, in shutdown, and when the fault latch has been tripped. After the soft-start circuit has terminated, PGOOD2 becomes high impedance if the output is in regulation. PGOOD2 is blanked—forced high-impedance state—when a dynamic REFIN transition is detected.	
29	SKIP	Pulse-skipping Control Input. This three-level input determines the operating mode for the switching regulators:  High (V <sub>CC</sub> ) = Forced-PWM operation  Open/REF (2V) = Ultrasonic mode  GND = Pulse-skipping mode	
30	OUT2	Output Voltage-Sense Input for SMPS2. OUT2 is an input to the Quick-PWM on-time one-shot timer. OUT2 also serves as the feedback input for the preset 3.3V (REFIN2 = V <sub>CC</sub> ) and 1.05V (REFIN2 = RTC).	
		Valley Current-Limit Adjustment for SMPS2. The GND - LX2 current-limit threshold is 1/10 the voltage present on ILIM2 over a 0.2V to 2V range. An internal 5µA current source allows this voltage to be set with a single resistor between ILIM2 and analog ground.	
32	REFIN2	External Reference Input for SMPS2. REFIN2 sets the feedback-regulation voltage (V <sub>OUT2</sub> = V <sub>REFIN2</sub> ). The MAX17020 includes an internal window comparator to detect when the REFIN2 voltage changes, allowing the controller to blank PGOOD2 and the fault protection. Connect REFIN2 to RTC for fixed 1.05V operation. Connect REFIN2 to V <sub>CC</sub> for fixed 3.3V operation.	
_	EP	Exposed Pad. Connect the backside exposed pad to AGND.	

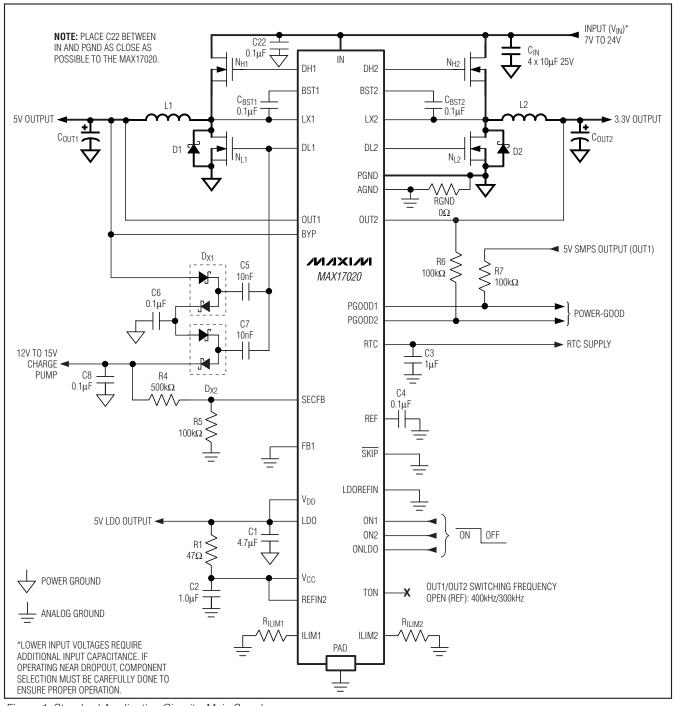


Figure 1. Standard Application Circuit—Main Supply

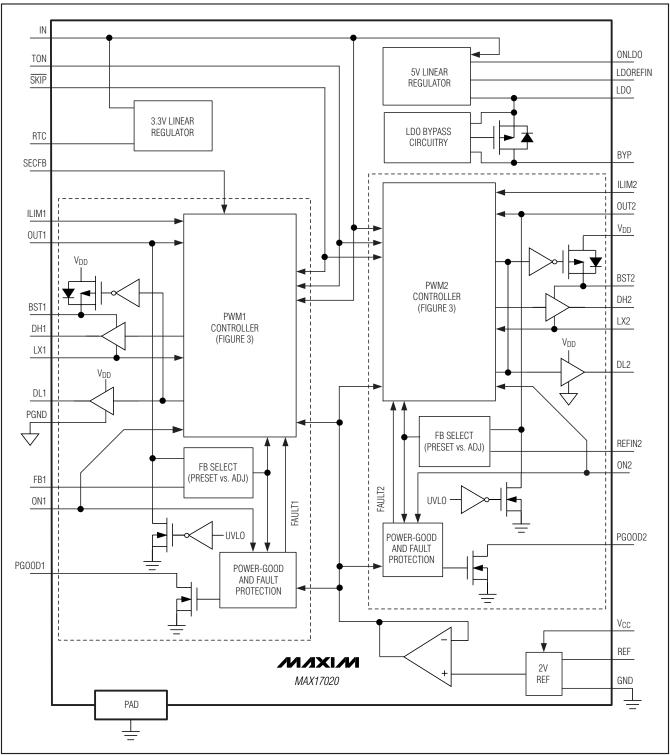


Figure 2. Functional Diagram Overview

**Table 1. Component Selection for Standard Applications** 

COMPONENT	400kHz/300kHz SMPS 1: 5V AT 5A SMPS 2: 3.3V AT 8A	400kHz/500kHz SMPS 1: 5V AT 3A SMPS 2: 3.3V AT 5A	400kHz/300kHz SMPS 1: 1.5V AT 8A SMPS 2: 1.05V AT 5A
Input Voltage	V <sub>IN</sub> = 7V to 24V	V <sub>IN</sub> = 7V to 24V	V <sub>IN</sub> = 7V to 24V
Input Capacitor (C <sub>IN</sub> )	(4x) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2x) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(4x) 10µF, 25V Taiyo Yuden TMK432BJ106KM
SMPS 1			
Output Capacitor (C <sub>OUT1</sub> )	$330\mu\text{F}$ , $6\text{V}$ , $18\text{m}\Omega$ SANYO 6TPE330MIL	330μF, 6V, 18mΩ SANYO 6TPE330MIL	(2x) 330μF, 2V, 7mΩ SANYO 2TPF330M7
Inductor (L1)	4.3μH, 11.4m $\Omega$ , 11A Sumida CEP125U	4.7μH, 9.8mΩ, 7A Sumida CDRH10D68	1.5μH, 12A, 7mΩ NEC/Tokin MPLC1040L1R5
High-Side MOSFET (N <sub>H1</sub> )	Fairchild Semiconductor FDS6612A 26mΩ/30mΩ, 30V	Vishay Siliconix Si4814DY Dual 30V MOSFET	Fairchild Semiconductor FDS8690 8.6m $\Omega$ /11.4m $\Omega$ , 30V
Low-Side MOSFET (N <sub>L1</sub> )	Fairchild Semiconductor FDS6670S $9m\Omega/11.5m\Omega$ , 30V	High side: $19$ mΩ/ $23$ mΩ Low side: $18$ mΩ/ $22$ mΩ	Fairchild Semiconductor FDMS8660S 2.6m $\Omega$ /3.5m $\Omega$ , 30V
Current-Limit Resistor (R <sub>ILIM1</sub> )	200kΩ	150kΩ	49.9kΩ
SMPS 2	•		
Output Capacitor (C <sub>OUT2</sub> )	$470\mu\text{F}$ , $4\text{V}$ , $15\text{m}\Omega$ SANYO $4\text{TPE}470\text{MFL}$	330μF, 6V, 18mΩ SANYO 6TPE330MIL	330μF, 2V, 7mΩ SANYO 2TPF330M7
Inductor (L2)	4.3μH, 11.4mΩ, 11A Sumida CEP125U	4.7μH, 9.8mΩ, 7A Sumida CDRH10D68	1.5μH, 12A, 7mΩ NEC/Tokin MPLC1040L1R5
High-Side MOSFET (N <sub>H2</sub> )	Fairchild Semiconductor FDS8690 8.6m $\Omega$ /11.4m $\Omega$ , 30V	Vishay Siliconix Si4814DY Dual 30V MOSFET	Fairchild Semiconductor FDS8690 8.6m $\Omega$ /11.4m $\Omega$ , 30V
Low-Side MOSFET (N <sub>L2</sub> )	Fairchild Semiconductor FDMS8660S 2.6m $\Omega$ /3.5m $\Omega$ , 30V	High side: $19\text{m}\Omega/23\text{m}\Omega$ Low side: $18\text{m}\Omega/22\text{m}\Omega$	Fairchild Semiconductor FDMS8660S 2.6m $\Omega$ /3.5m $\Omega$ , 30V
Current-Limit Resistor (R <sub>ILIM2</sub> )	200kΩ	200kΩ	49.9kΩ

#### **Table 2. Component Suppliers**

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp	www.kemet.com
NEC/Tokin America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
Philips/nxp Semiconductor	www.semiconductors.philips.com
Pulse Engineering	www.pulseeng.com

SUPPLIER	WEBSITE
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com
Würth Elektronik GmbH & Co. KG	www.we-online.com

\_\_ /N/1XI/N

#### **Detailed Description**

The MAX17020 step-down controller is ideal for high-voltage, low-power supplies for notebook computers. Maxim's Quick-PWM pulse-width modulator in the MAX17020 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. Figure 2 is a functional diagram overview. Figure 3 is the functional diagram—Quick-PWM core.

The MAX17020 includes several features for multipurpose notebook functionality, allowing this controller to be used two or three times in a single notebook—main, I/O chipset, and graphics. The MAX17020 includes a 100mA LDO that can be configured for preset 5V operation-ideal for initial power-up of the notebook and main supply—or can be adjusted for lower voltage operation—ideal for low-power I/O or graphics supply requirements. Additionally, the MAX17020 includes a 3.3V, 5mA RTC supply that remains always enabled. which can be used to power the RTC supply and system pullups when the notebook shuts down. The MAX17020 also includes an optional secondary feedback input that allows an unregulated charge pump or secondary winding to be included on a supply-ideal for generating the low-power 12V to 15V load switch supply. Finally, the MAX17020 includes a reference input on SMPS 2 that allows dynamic voltage transitions when driven by an adjustable resistive voltage-divider or DAC—ideal for the dynamic graphics core requirements.

#### 3.3V RTC Power

The MAX17020 includes a low-current (5mA) linear regulator that remains active as long as the input supply (IN) exceeds 2V (typ). The main purpose of this "always-enabled" linear regulator is to power the real-time clock (RTC) when all other notebook regulators are disabled. RTC also serves as the main bias supply of the MAX17020 so it powers up before the LDO and switching regulators. The RTC regulator sources at least 5mA for external loads.

#### Adjustable 100mA Linear Regulator

The MAX17020 includes a high-current (100mA) linear regulator that can be configured for preset 5V or 3.3V operation or adjusted between 0.6V to 4V. When the MAX17020 is configured as a main supply, this LDO is required to generate the 5V bias supply necessary to power up the switching regulators. Once the switching regulators are enabled, the LDO can be bypassed using the dedicated BYP input. The adjustable linear regulator allows generation of the 3.3V suspend supply or buffered low-power chipset and GPU reference supplies. The MAX17020 LDO sources at least 100mA of supply current.

#### **Bypass Switch**

The MAX17020 includes an independent LDO bypass input that allows the LDO to be bypassed by either switching regulator output or from a different regulator all together. When the bypass voltage (BYP) exceeds 93.5% of the LDO output voltage for 500µs, the MAX17020 reduces the LDO regulation threshold and turns on an internal p-channel MOSFET to short BYP to LDO. Instead of disabling the LDO when the MAX17020 enables the bypass switch, the controller reduces the LDO regulation voltage, which effectively places the linear regulator in a standby state while switched over, yet allows a fast recovery if the bypass supply drops.

Connect BYP to GND when not used to avoid unintentional conduction through the body diode (BYP to LDO) of the p-channel MOSFET.

#### 5V Bias Supply (VCC/VDD)

The MAX17020 requires an external 5V bias supply (V<sub>DD</sub> and V<sub>CC</sub>) in addition to the battery. Typically, this 5V bias supply is generated by either the internal 100mA LDO (when configured for a main supply) or from the notebook's 95%-efficient 5V main supply (when configured for an I/O chipset, DDR, or graphics). Keeping these bias supply inputs independent improves the overall efficiency and allows the internal linear regulator to be used for other applications as well.

The  $V_{DD}$  bias supply input powers the internal gate drivers and the  $V_{CC}$  bias supply input powers the analog control blocks. The maximum current required is dominated by the switching losses of the drivers and can be estimated as follows:

 $IBIAS(MAX) = ICC(MAX) + fSWQG \approx 30mA \text{ to 60mA (typ)}$ 

### Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

#### **On-Time One-Shot**

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as sensed by the IN input, and proportional to the output voltage:

On-Time = K (Vout/VIN)

where K (switching period) is set by the tri-level TON input (see the *Pin Description* section). High-frequency (400kHz/500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz/300kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V<sub>DROP1</sub> is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V<sub>DROP2</sub> is the sum of the voltage drops in the charging path, including the high-side switch, inductor, and PCB resistances; and t<sub>ON</sub> is the on-time calculated by the MAX17020.

**Table 3. Approximate K-Factor Errors** 

SWITCHING REGULATOR	TON SETTING (kHz)	TYPICAL K-FACTOR (μs)	K-FACTOR ERROR (%)	COMMENTS
SMPS 1	200kHz TON = V <sub>CC</sub>	5.0	±10	Use for absolute best efficiency.
SIVIFS I	400kHz TON = REF or GND	2.5	±12.5	Useful in 3-cell systems for lighter loads than the CPU core or where size is key.
SMPS 2	I ION = REF or Vcc	3.3	±10	Considered mainstream by current standards.
SIVIFO 2	500kHz TON = GND	2.0	±12.5	Good operating point for compound buck designs or desktop circuits.

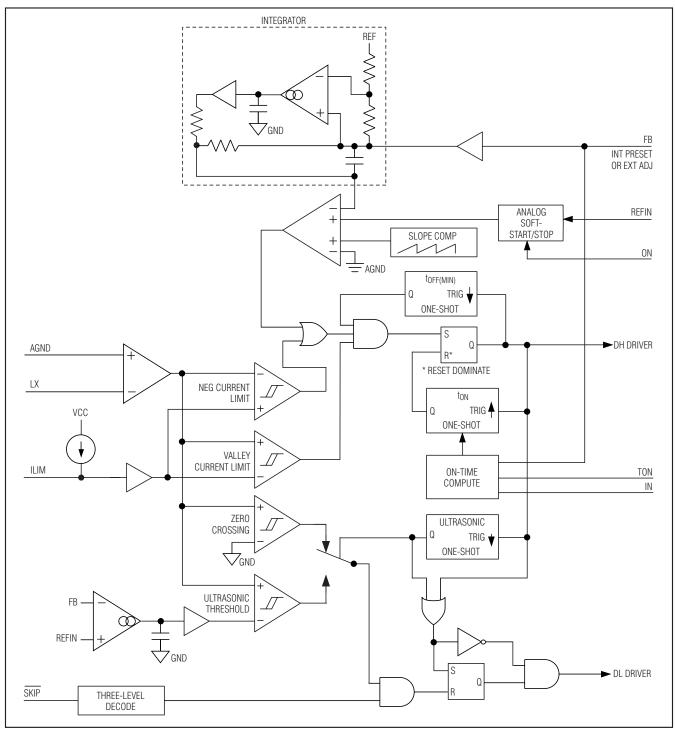


Figure 3. Functional Diagram—Quick-PWM Core

#### **Modes of Operation**

#### Forced-PWM Mode (SKIP = Vcc)

The low-noise forced-PWM mode (SKIP = V<sub>CC</sub>) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of V<sub>OUT</sub>/V<sub>IN</sub>. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 20mA to 60mA depending on the switching frequency and MOSFET selection.

The MAX17020 automatically uses forced-PWM operation during all transitions—dynamic REFIN, startup, and shutdown—regardless of the SKIP configuration.

#### Automatic Pulse-Skipping Mode (SKIP = GND)

In skip mode (SKIP = GND), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across LX and AGND.

DC output-accuracy specifications refer to the integrated threshold of the error comparator. When the inductor is in continuous conduction, the MAX17020 regulates the valley of the output ripple and the internal integrator removes the actual DC output-voltage error caused by the output-ripple voltage and internal slope compensation. In discontinuous conduction (SKIP = GND and IOUT < ILOAD(SKIP)), the integrator cannot correct for the low-frequency output ripple error, so the output voltage has a DC regulation level higher than the error comparator threshold by approximately 1.5% due to slope compensation and output ripple voltage.

#### Ultrasonic Mode (SKIP = Open or REF)

Leaving SKIP unconnected or connecting SKIP to REF (2V) activates a unique pulse-skipping mode with a guaranteed minimum switching frequency of 20kHz. This ultrasonic pulse-skipping mode eliminates audiofrequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point (ILOAD(SKIP)) that occurs when normally pulse skipping.

An ultrasonic pulse occurs (Figure 4) when the controller detects that no switching has occurred within the last 37µs or when SECFB drops below its feedback threshold. Once triggered, the ultrasonic circuitry pulls

DL high, turning on the low-side MOSFET to induce a negative inductor current. After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the inductor current drops below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equation:

where  $V_{NOM}$  is the nominal feedback-regulation voltage, and  $V_{FB}$  is the actual feedback voltage ( $V_{FB} > V_{NOM}$ ), and  $R_{CS}$  is the current-sense resistance seen across LX to AGND.

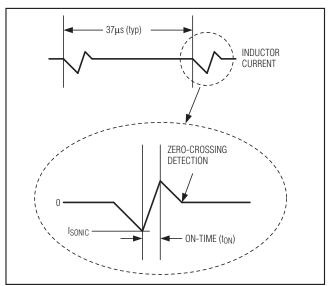


Figure 4. Ultrasonic Waveforms

#### Secondary Feedback: SECFB—OUT1 ONLY

When the controller skips pulses ( $\overline{\text{SKIP}} = \text{GND}$  or REF), the long time between pulses (especially if the output is sinking current) allows the external charge-pump voltage or transformer secondary winding voltage to drop. When the SECFB voltage drops below its 2V feedback threshold, the MAX17020 issues an ultrasonic pulse (regardless of the ultrasonic one-shot state). This forces a switching cycle, allowing the external unregulated charge pump (or transformer secondary winding) to be refreshed. See the *Ultrasonic Mode* ( $\overline{SKIP} = Open\ or\ REF$ ) section for switching cycle sequence/specifications.

#### **Dynamic Output Voltage—OUT2 Only**

The MAX17020 regulates OUT2 to the voltage set at REFIN2, so the MAX17020 supports applications that require dynamic output-voltage changes between two set points by adjusting the REFIN2 voltage. For a stepvoltage change at REFIN2, the rate of change of the output voltage is limited either by the internal slew-rate circuit, by the REFIN2 slew rate, or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is the slowest. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate. Additional load current slows down the output voltage change during a positive REFIN2 voltage change, and speeds up the output voltage change during a negative REFIN2 voltage change. Figure 5 is the dynamic REFIN transition.

#### **Automatic Fault Blanking**

When the MAX17020 automatically detects that the internal target and REFIN2 are more than ±25mV (typ) apart, the controller automatically blanks PGOOD2, blanks the UVP protection, and sets the OVP threshold to REF + 200mV. The blanking remains until 1) the internal target and REFIN2 are within ±20mV of each other and 2) an edge is detected on the error amplifier signifying that the output is in regulation. This prevents the system or internal fault protection from shutting down the controller during transitions.

#### **Valley Current-Limit Protection**

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current through the low-side MOSFET—across LX to AGND. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX17020 also implements a negative current limit to prevent excessive reverse inductor currents when V<sub>OUT</sub> is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

#### POR, UVLO

When  $V_{CC}$  rises above the power-on reset (POR) threshold, the MAX17020 clears the fault latches, forces the low-side MOSFET to turn on (DL high), and resets the soft-start circuit, preparing the controller for power-up. However, the  $V_{CC}$  undervoltage lockout (UVLO) circuitry inhibits switching until  $V_{CC}$  reaches 4.2V (typ). When  $V_{CC}$  rises above 4.2V and the controller has been enabled (ON\_ pulled high), the controller activates the enabled PWM controllers and initializes soft-start.

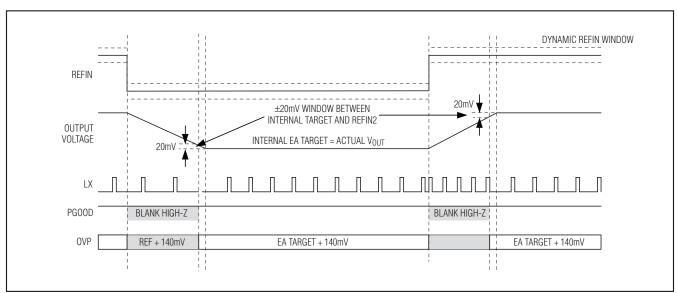


Figure 5. Dynamic REFIN Transition

When VCC drops below the UVLO threshold (falling edge), the controller stops switching, and DH and DL are pulled low and a  $10\Omega$  switch discharges the outputs. When the 2V POR falling-edge threshold is reached, the DL state no longer matters since there is not enough voltage to force the switching MOSFETs into a low on-resistance state, so the controller pulls DL high, allowing a soft discharge of the output capacitors (damped response). However, if the VCC recovers before reaching the falling POR threshold, DL remains low until the error comparator has been properly powered up and triggers an on-time. Only one enable input needs to be toggled to clear the fault latches and activate both outputs.

#### **Soft-Start and Soft-Shutdown**

The MAX17020 includes voltage soft-start and soft-shutdown—slowly ramping up and down the target voltage. During startup, the slew-rate control softly slews the preset/fixed target voltage over a 1ms startup period or its tracking voltage (REFIN2 < 2V) with a 1mV/µs slew rate. This long startup period reduces the inrush current during startup.

When ON1 or ON2 is pulled low or the output undervoltage fault latch is set, the respective output automatically enters soft-shutdown—the regulator enters PWM mode and ramps down its preset/fixed output voltage over a 1ms period or its tracking voltage (REFIN2 < 2V) with a 1mV/µs slew rate. After the output voltage drops below 0.1V, the MAX17020 pulls DL high, clamping the output and LX switching node to ground, preventing leakage currents from pulling up the output and minimizing the negative output voltage undershoot during shutdown.

#### **Output Voltage**

DC output-accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold. When the inductor continuously conducts, the MAX17020 regulates the valley of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM} + \left(\frac{V_{RIPPLE}}{2A_{CCV}}\right)$$

where  $V_{NOM}$  is the nominal feedback voltage,  $A_{CCV}$  is the integrator's gain, and  $V_{RIPPLE}$  is the output ripple voltage ( $V_{RIPPLE} = ESR \times \Delta I_{INDUCTOR}$ , as described in the *Output Capacitor Selection* section).

In discontinuous conduction (I<sub>OUT</sub> < I<sub>LOAD(SKIP)</sub>), the longer off-times allow the slope compensation to increase the threshold voltage by as much as 1%, so

the output voltage regulates slightly higher than it would in PWM operation.

#### Internal Integrator

The internal integrator improves the output accuracy by removing any output accuracy errors caused by the slope compensation, output ripple voltage, and erroramplifier offset. Therefore, the DC accuracy (in forced-PWM mode) depends on the integrator's gain, the integrator's offset, and the accuracy of the integrator's reference input.

#### Adjustable/Fixed Output Voltages

Connect FB1 to GND for fixed 5V operation. Connect FB1 to V<sub>CC</sub> for fixed 1.5V operation. Connect FB1 to an external resistive voltage-divider from OUT1 to analog ground to adjust the output voltage between 0.7V and 5.5V. During soft-shutdown, application circuits configured for adjustable feedback briefly switch modes when FB1 drops below the 110mV dual-mode threshold.

Choose R<sub>FBL</sub> (resistance from FB1 to AGND) to be approximately 49.9k $\Omega$  and solve for R<sub>FBH</sub> (resistance from OUT1 to FB1) using the following equation:

$$R_{FBH} = R_{FBL} \times \left( \frac{V_{OUT1}}{0.7V} - 1 \right)$$

Connect REFIN2 to  $V_{CC}$  for fixed 3.3V operation. Connect REFIN2 to RTC (3.3V) for fixed 1.05V operation. Connect REFIN2 to an external resistive voltage-divider from REF to analog ground to adjust the output voltage between 0V and 2V.

Choose RREFINL (resistance from REFIN2 to GND) to be approximately 49.9k $\Omega$  and solve for RREFINH (resistance from REF to REFIN2) using the equation:

$$R_{REFINH} = R_{REFINL} \times \left( \frac{V_{REF}}{V_{OUT2}} - 1 \right)$$

### Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and overvoltage conditions. PGOOD\_ is actively held low in shutdown (ON\_ = GND), during soft-start or soft-shutdown. Approximately 20µs (typ) after the soft-start terminates, PGOOD\_ becomes high impedance as long as the feedback voltage exceeds 85% of the nominal fixed-regulation voltage or within 150mV of the REFIN2 input voltage. PGOOD\_ goes low if the feedback voltage drops 16% below the fixed target voltage, or if the output voltage drops 150mV below the dynamic REFIN2 voltage, or if the SMPS controller is shut down. For a

MIXIM

logic-level PGOOD\_ output voltage, connect an external pullup resistor between PGOOD\_ and  $V_{DD}$ . A  $100k\Omega$  pullup resistor works well in most applications.

#### Overvoltage Protection (OVP)

When the output voltage rises 16% above the fixed-regulation voltage or has risen 200mV above the dynamic REFIN2 input voltage, the controller immediately pulls the respective PGOOD\_ low, sets the overvoltage fault latch, and immediately pulls the respective DL\_ high—clamping the output to GND. Toggle either ON1 or ON2 input, or cycle VCC power below its POR threshold to clear the fault latch and restart the controller.

#### Undervoltage Protection (UVP)

When the output voltage drops 30% below the fixed-regulation voltage or has dropped 300mV below the dynamic REFIN2 input voltage, the controller immediately pulls the respective PGOOD\_ low, sets the undervoltage fault latch, and begins the shutdown sequence. After the output voltage drops below 0.1V, the synchronous rectifier turns on, clamping the output to GND. Toggle either ON1 or ON2 input, or cycle VCC power below its POR threshold to clear the fault latch and restart the controller.

#### Thermal-Fault Protection (TSHDN)

The MAX17020 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD1 and PGOOD2 low, enables the 10 $\Omega$  discharge circuit, and disables the controller—DH and DL are pulled low. Toggle ONLDO or cycle IN power to reactivate the controller after the junction temperature cools by 15°C.

#### Design Procedure

Firmly establish the input-voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary

design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- Input Voltage Range: The maximum value (VIN(MAX)) must accommodate the worst-case, high AC-adapter voltage. The minimum value (VIN(MIN)) must account for the lowest battery voltage after drops due to connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- Maximum Load Current: There are two values to consider. The peak load current (I<sub>LOAD(MAX)</sub>) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I<sub>LOAD</sub>) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V<sub>IN</sub><sup>2</sup>. The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- Inductor Operating Point: This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values

Table 4. Fault Protection and Shutdown Operation Table

MODE	CONTROLLER STATE	DRIVER STATE
Shutdown (ON_ = High to Low); Output UVP (Latched)	Voltage soft-shutdown initiated. Internal error-amplifier target slowly ramped down to GND and output actively discharged (automatically enters forced-PWM mode).	DL driven high and DH pulled low after soft-shutdown completed (output < 0.1V).
Output OVP (Latched)	Controller shuts down and EA target internally slewed down. Controller remains off until ON_ toggled or VCC power cycled.	DL <b>immediately</b> driven high, DH pulled low.
V <sub>CC</sub> UVLO Falling-Edge Thermal Fault (Latched)	SMPS controller disabled (assuming ON_ pulled high), $10\Omega$ output discharge active.	DL and DH pulled low.
V <sub>CC</sub> UVLO Rising Edge	SMPS controller enabled (assuming ON_ pulled high).	DL driven high, DH pulled low.
V <sub>CC</sub> POR	SMPS inactive, $10\Omega$ output discharge active.	DL driven high, DH pulled low.

lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping (SKIP low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

#### **Inductor Selection**

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{RIPPLE} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

For example:  $I_{LOAD(MAX)} = 4A$ ,  $V_{IN} = 12V$ ,  $V_{OUT2} = 2.5V$ ,  $f_{SW} = 355kHz$ , 30% ripple current or LIR = 0.3:

$$L = \frac{2.5V \times (12V - 2.5V)}{12V \times 355kHz \times 4A \times 0.3} = 4.65\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (IPFAK):

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

#### **Transient Response**

The inductor ripple current also impacts transient-response performance, especially at low  $V_{\text{IN}}$  -  $V_{\text{OUT}}$  differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the ontime and minimum off-time:

$$V_{SAG} = \frac{L \times \left(\Delta I_{LOAD(MAX)}\right)^{2} \times \left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2 \times C_{OUT} \times V_{OUT}\left[\left(\frac{\left(V_{IN} - V_{OUT}\right) \times K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where toff(MIN) is the minimum off-time (see the *Electrical Characteristics* table) and K is from Table 3.

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

#### **Setting the Current Limit**

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at ILOAD(MAX) minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)} \times LIR}{2}\right)$$

where  $I_{LIM(VAL)}$  equals the minimum valley current-limit threshold voltage divided by the current-sense resistance (RSENSE). When using a  $100k\Omega$  ILIM resistor, the minimum valley current-limit threshold is 40mV.

Connect a resistor between ILIM\_ and analog ground (AGND) to set the adjustable current-limit threshold. The valley current-limit threshold is approximately 1/10 the ILIM voltage formed by the external resistance and internal 5µA current source. The 40k $\Omega$  to 400k $\Omega$  adjustment range corresponds to a 20mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors to prevent significant inaccuracy in the valley current-limit tolerance.

#### **Output Capacitor Selection**

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a stepdown controller equals the total inductor ripple current

multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)} \times LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent VSAG and VSOAR from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the VSAG and VSOAR equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that could affect the overall stability (see the *Output Capacitor Stability Considerations* section).

#### **Output Capacitor Stability Considerations**

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$fESR \le \frac{fSW}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mVp-p ripple is  $25\text{mV}/1.2\text{A} = 20.8\text{m}\Omega$ . One  $220\mu\text{F/4V}$  SANYO polymer (TPE) capacitor provides  $15\text{m}\Omega$  (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of

inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related, but distinctly different ways: double-pulsing and fast-feed-back loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability results in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

#### **Input Capacitor Selection**

The input capacitor must meet the ripple current requirement (IRMS) imposed by the switching currents:

$$I_{RMS} = I_{LOAD} \times \left( \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \right)$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX17020 is operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

#### **Power-MOSFET Selection**

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N<sub>H</sub>) must be able to dissipate the resistive losses plus the switching losses at both  $V_{IN(MIN)}$  and  $V_{IN(MAX)}$ . Ideally, the losses at  $V_{IN(MAX)}$ , with lower losses in between. If the losses at  $V_{IN(MIN)}$  are

significantly higher, consider increasing the size of N<sub>H</sub>. Conversely, if the losses at  $V_{IN(MAX)}$  are significantly higher, consider reducing the size of N<sub>H</sub>. If  $V_{IN}$  does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N<sub>H</sub>) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (NL) that has the lowest possible on-resistance (R<sub>DS(ON)</sub>), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D²PAK), and is reasonably priced. Ensure that the MAX17020 DL\_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

#### **Power-MOSFET Dissipation**

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N<sub>H</sub>), the worst-case power dissipation due to resistance occurs at minimum input voltage:

PD (N<sub>H</sub> Resistive) = 
$$\left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(I_{LOAD}\right)^2 \times R_{DS(ON)}$$

Generally, use a small, high-side MOSFET to reduce switching losses at high input voltages. However, the RDS(ON) required to stay within package power-dissipation often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction (RDS(ON)) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N<sub>H</sub>) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N<sub>H</sub>:

$$\begin{split} \text{PD(N}_{H} \text{ Switching)} = & \left( \frac{V_{(MAX)} \times I_{LOAD} \times f_{SW} \times Q_{G(SW)}}{I_{GATE}} \right) + \\ & \left( \frac{V_{IN}^2 \times C_{OSS} \times f_{SW}}{2} \right) \end{split}$$

where COSS is the high-side MOSFET's output capacitance, QG(SW) is the charge needed to turn on the high-side MOSFET, and IGATE is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation provided above. If the high-side MOSFET chosen for adequate RDS(ON) at low battery voltages becomes extraordinarily hot when subjected to VIN(MAX), consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N<sub>L</sub>), the worst-case power dissipation always occurs at maximum battery voltage:

PD(N<sub>L</sub> Resistive) = 
$$\left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] \left(I_{LOAD}\right)^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than I<sub>LOAD(MAX)</sub>, but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} \approx I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} \times LIR}{2}\right)$$

where IVALLEY(MAX) is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode ( $D_L$ ) with a forward voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

#### Applications Information

### Step-Down Converter Dropout Performance

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3).

Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the VSAG equation in the *Transient Response* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time ( $\Delta I_{DOWN}$ ) as much as it ramps up during the on-time ( $\Delta I_{UP}$ ). The ratio  $h = \Delta I_{UP}/\Delta I_{DOWN}$  indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and  $V_{SAG}$  greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V<sub>SAG</sub>, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{CHG}}{1 - \left(\frac{h \times t_{OFF(MIN)}}{K}\right)}$$

where  $V_{CHG}$  is the parasitic voltage drop in the charge path (see the *On-Time One-Shot* section),  $t_{OFF(MIN)}$  is from the *Electrical Characteristics* table, and K (1/fsw) is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated  $V_{IN(MIN)}$  is greater than the required minimum input voltage, operating frequency must be reduced or output capacitance added to obtain an acceptable  $V_{SAG}$ . If operation near dropout is anticipated, calculate  $V_{SAG}$  to be sure of adequate transient response.

#### **Dropout Design Example:**

 $V_{OUT2} = 2.5V$ 

fsw = 355kHz

 $K = 3.0\mu s$ , worst-case  $K_{MIN} = 3.3\mu s$ 

tOFF(MIN) = 500ns

 $V_{CHG} = 100 \text{mV}$ 

h = 1.5:

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 500 \text{ns}}{3.0 \text{µs}}\right)} = 3.47V$$

Calculating again with h = 1 and the typical K-factor value ( $K = 3.3\mu$ s) gives the absolute limit of dropout:

$$V_{IN(MIN)} = \frac{2.5V + 0.1V}{1 - \left(\frac{1 \times 500 \text{ns}}{3.3 \mu \text{s}}\right)} = 3.06V$$

Therefore, V<sub>IN</sub> must be greater than 3.06V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.47V.

### Dynamic Output Voltage Settings (OUT2 Only)

The second output (OUT2) of the MAX17020 works with applications that require multiple dynamic output voltages, easily supporting two to four output voltages with external resistors selected by control FETs or REFIN2 can be driven by a DAC for tight voltage control.

Figure 6 shows an application circuit providing four voltage levels using discrete components. Switching resistors in and out of the resistor network changes the voltage at REFIN2. The reference input automatically detects large input voltage transitions and blanks the fault and PGOOD2 comparators, allowing the system to perform the transition without tripping the fault protection.

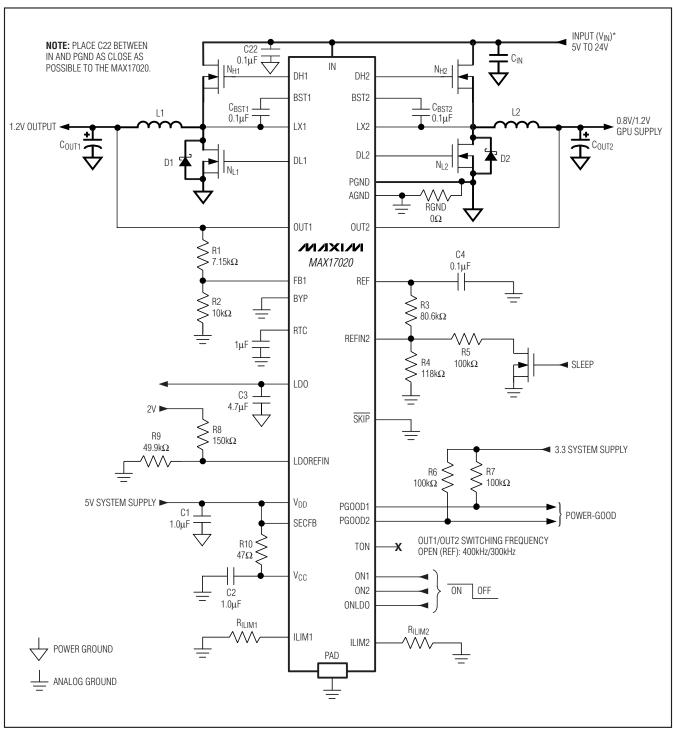


Figure 6. Dynamic Output Application Circuit—Graphics Supply

#### **PCB Layout Guidelines**

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short.
   This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting LX\_ directly to the drain of the low-side MOSFET.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the lowside MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST\_, LX\_, DH\_, and DL\_) away from sensitive analog areas (REF, FB\_, and OUT\_).

A sample layout is available in the MAX17020 evaluation kit data sheet.

#### Layout Procedure

- Place the power components first, with ground terminals adjacent (N<sub>L</sub> source, C<sub>IN</sub>, C<sub>OUT</sub>, and D<sub>L</sub> anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
- 2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite N<sub>L</sub> and N<sub>H</sub> to keep LX\_, GND, DH\_, and the DL\_ gatedrive lines short and wide. The DL\_ and DH\_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
- 3) Group the gate-drive components (BST\_ capacitor, VDD bypass capacitor) together near the controller IC.
- 4) Make the DC-DC controller ground connections as shown in Figures 1 and 6. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
- 5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

#### Table 5. MAX17020 vs. MAX8778 Design Differences

MAX17020	MAX8778	
RTC power-up required for controller operation.	LDO and switching regulators independent of RTC operation.	

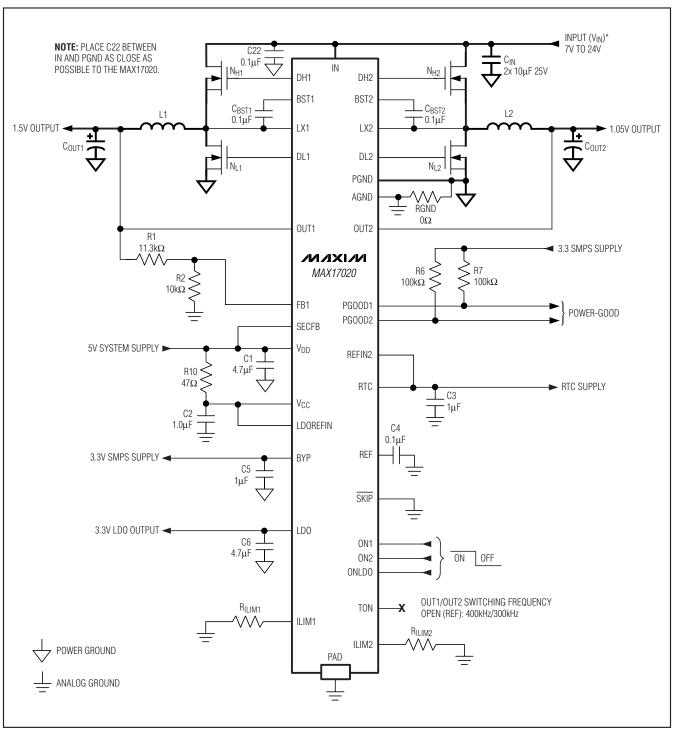


Figure 7. Standard Output Application Circuit—Chipset Supply

# **MAX17020**

### Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

\_\_Chip Information

**Package Information** 

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN	T3255-3	<u>21-0140</u>

PROCESS: BiCMOS

#### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	_
1	9/08	Added three new TOCs, various changes throughout	3, 8, 12–15, 24, 25, 26, 33
2	2/09	Minor edits to EC table and text additions	1, 5, 7, 14, 15, 23

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

#### **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

### Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

#### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

#### Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9