HFBR-57E5APZ

Multimode Small Form-Factor Pluggable Transceivers with LC connector and DMI for ATM, FDDI, Fast Ethernet and SONET OC-3/SDH STM-1

Data Sheet

Description

The HFBR-57E5APZ Small Form-Factor Pluggable LC transceiver gives the system designer a product to implement FDDI/Fast Ethernet network with DMI and SONET OC-3 (SDH STM-1) physical layers for ATM and other services.

As an enhancement to the conventional SFP interface defined in SFF-8074i, the HFBR-57E5APZ is compatible to SFF-8472 (digital diagnostic interface for optical transceivers). Using the 2-wire serial interface defined in the SFF-8472 MSA, the HFBR-57E5APZ provides real-time information on temperature, LED bias current, LED average output power and receiver average input power. The interface also adds the ability to monitor the Receiver Loss of Signal (RX_LOS).

Transmitter

The transmitter contains a 1310 nm InGaAsP LED. The LED is packaged in the optical subassembly of the transmitter. It is driven by an integrated circuit which converts differential PECL logic signals into an analog LED drive current. This current is monitored by the digital diagnostic interface. The transmitter light output power is inferred from this information.

Receiver

The receiver utilizes an InGaAs PIN photodiode coupled to a transimpedance preamplifier IC. It is packaged in the optical subassembly of the receiver. The PIN/preamplifier combination is connected to a quantizer IC which provides the final pulse shaping for data output. The data output is differential LVPECL. The quantizer IC has a loss of signal (LOS) detection circuit and has an open collector logic high output signal in the absence of a usable input optical signal. This LOS output is +3.3 V TTL as per SFF-8074i.

The PIN photodiode average current is monitored by the digital diagnostic interface as a measure for input optical power.

Features

- RoHS compliant
- Compatible with ATM Forum UNI SONET OC-3 multimode fiber physical layer specification
- Lead free
- Industry Standard Small Form Pluggable (SFP) package
- LC duplex connector optical interface
- Operates with 50/125 μm and 62.5/125 μm multimode fiber
- Compatible with 100Base-FX version of IEEE802.3u
- Single +3.3 V power supply
- +3.3 V TTL LOS output
- Receiver outputs are squelch enabled
- Manufactured in an ISO 9001 certified facility
- -40° C to 85° C temperature range
- Bail de-latch
- Hot plug capability

Applications

- Factory automation at Fast Ethernet speeds
- Fast Ethernet networking over multimode fiber
- OC-3 SFP transceivers are designed for ATM LAN and WAN applications such as:
  - ATM switches and routers
  - SONET/SDH switch infrastructure
- Multimode fiber ATM backbone links

Loss of Signal

The Loss of Signal (LOS) output indicates that the optical input signal to the receiver does not meet the minimum detectable level for FDDI and OC-3 compliance. When LOS is high, it indicates a link failure such as a disconnected or broken fiber connection or a malfunctioning transmitter.

Module package

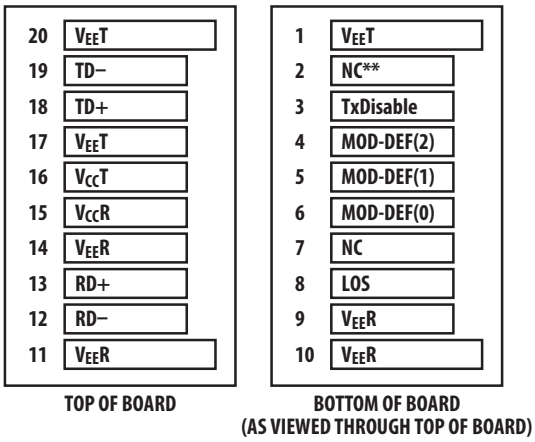
The transceiver package is compliant with the Small Form Pluggable (SFP) MSA with the LC duplex connector option. The hot-pluggable capability of the SFP package allows the module to be installed at any time – even with the host system operating and on-line. This permits the system to be configured or maintained without system downtime. The HFBR-57E5APZ requires a 3.3 V DC power supply for optimal performance.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-57E5APZ. The connection diagram of the module is shown in Figure 2. Figures 5 and 7 depict the external configuration and dimensions of the module.

Installation

The HFBR-57E5APZ can be installed in or removed from any MultiSource Agreement (MSA) compliant Small Form Pluggable port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical interface first, under finger pressure. Controlled hot-plugging is ensured by design and by 3-stage pin sequencing at the electrical interface. The module housing makes initial contact with the host board EMI shield mitigating potential damage due to Electro-Static Discharge (ESD). The 3-stage pin contact sequencing involves (1) Ground, (2) Power, and then (3) Signal pins making contact with the host board surface mount connector in that order. This printed circuit board card edge connector is depicted in Figure 2.



** Connect to Internal Ground

Figure 2. Connection diagram of module printed circuit board.

Digital Diagnostic Interface and Serial Identification

The 2-wire serial interface is based on the ATMEL AT24C01A series EEPROM protocol. Conventional EEPROM memory (bytes 0-255 at memory address 0xA0) is organized in compliance with SFF-8074i. As an enhancement the HFBR-57E5APZ is also compatible to SFF-8472. This enhancement offers digital diagnostic information at bytes 0-255 at memory address 0xA2.

In addition to monitoring of the LED drive current and photodiode current, the interface also monitors the transmitter supply voltage and temperature. The transmitter voltage supply must be provided for the digital diagnostic interface to operate.

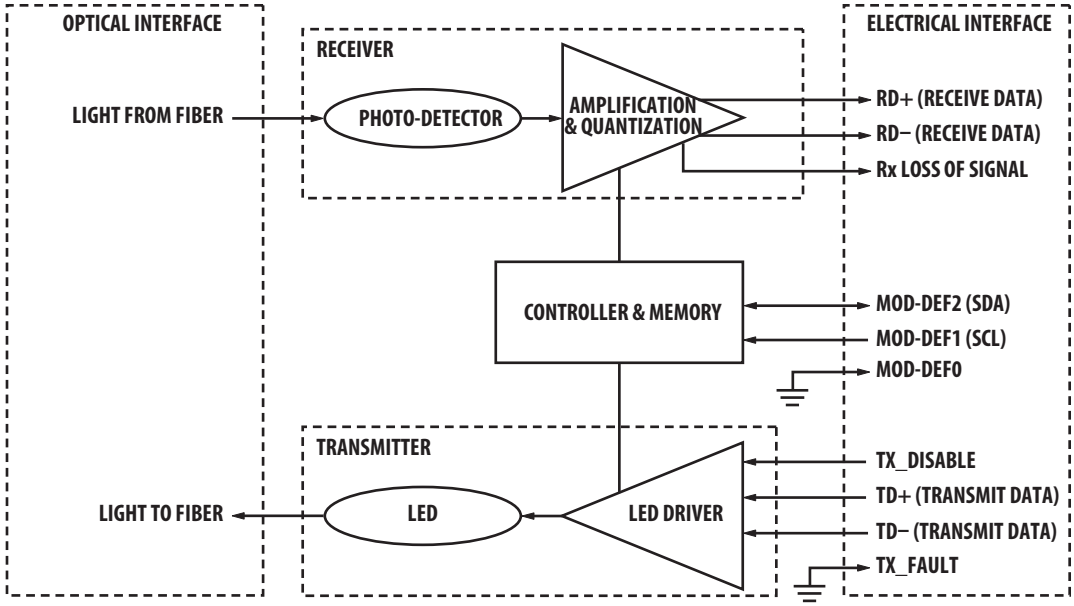


Figure 1. Transceiver functional diagram

Functional Data I/O

The HFBR-57E5APZ fiber-optic transceiver is designed to accept industry standard differential signals. The transceiver provides an AC-coupled, internally terminated data interface. Coupling capacitors have been included within the module to reduce the number of components on the customer's board. Figure 3 depicts the recommended interface circuitry.

Regulator Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions where immunity to ESD damage is important. Table 1 documents our immunity to both these conditions.

The first condition is static discharge to the transceiver when handling it. For example when the transceiver is inserted into the transceiver port. To protect the transceiver, it is important to use normal ESD handling procedures. These precautions include grounded wrist straps, workbenches, and floor maps in ESD controlled areas. The ESD sensitivity of the HFBR-57E5APZ is compatible with typical industry production environments.

The second condition is static discharge to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD events. The ESD performance of HFBR-57E5APZ exceeds typical industry standards.

Immunity

Equipment hosting the HFBR-57E5APZ will be subjected to radio-frequency electromagnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of CENELEC EN55022.

The metal housing design and shielded design of the HFBR-57E5APZ transceiver minimize the EMI challenge facing the host equipment designer. The transceivers provide superior EMI performance.

Eye Safety

These transceivers provide Class 1 eye safety by design. Avago has tested the transceiver design for compliance with the requirements listed in Table 1 under normal operating conditions and under a single fault condition.

Flammability

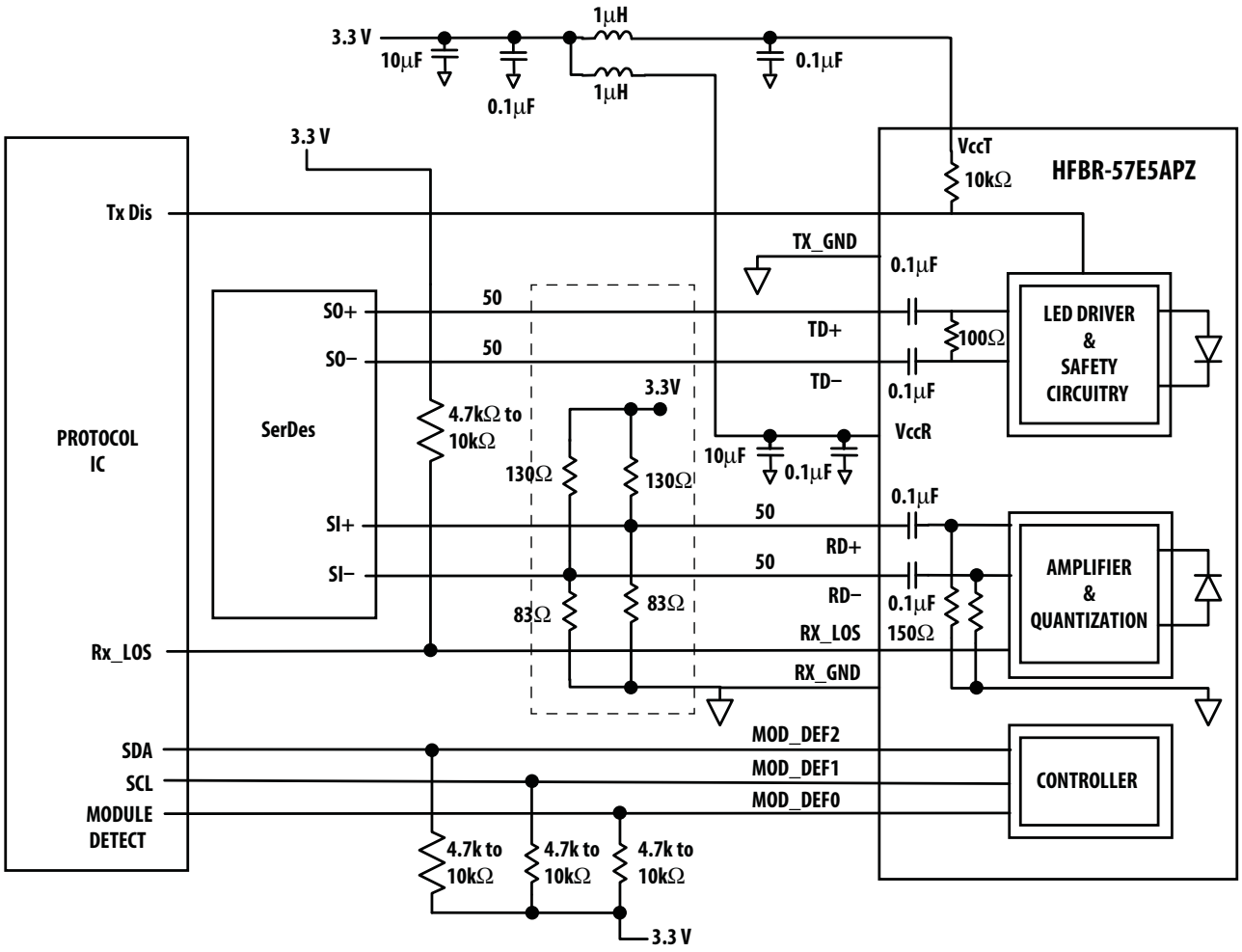
The HFBR-57E5APZ transceiver housing is made of metal and high strength, heat resistant, chemically resistant and UL-94V-0 flame retardant plastic.

Shipping Container

10 transceivers are packaged in one shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

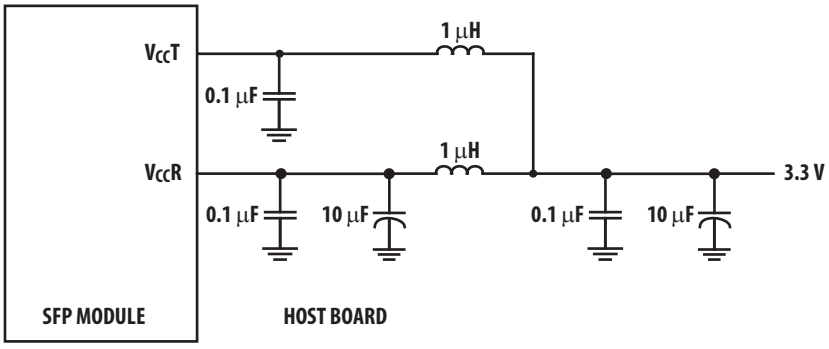
Table 1. Regulator Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C	HBM 2 kV
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the LC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	CENELEC CEN55022 Class B	System margins are dependant on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 450 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	AEL Class 1 EN60825-1 (+A11)	Compliant per Avago testing under single fault conditions.
RoHS Compliance		Reference to EU RoHS Directive 2002/95/EC



Note: Please refer to the PHY or SerDes supplier´s recommendation regarding the interface between HFBR-57E5APZ and SerDes. (Components in dotted line box show LVPECL-termination at Vcc=3.3V for Rx only)

Figure 3. Recommended connection circuitry



Note: Inductors must have less than 1 ohm series resistance per MSA.

Figure 4. MSA required power supply filter

Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}T$	Transmitter Ground	
2	NC	NC	1
3	Tx Disable	Transmitter Disable – Module disables on high or open	
4	MOD-DEF2	Module Definition 2 – Two wire serial ID interface	2
5	MOD-DEF1	Module Definition 1 – Two wire serial ID interface	2
6	MOD-DEF0	Module Definition 0 – grounded in module	2
7	NC	NC	
8	LOS	Loss of Signal – high indicates loss of signal	3
9	$V_{EE}R$	Receiver Ground	
10	$V_{EE}R$	Receiver Ground	4
11	$V_{EE}R$	Receiver Ground	4
12	RD-	Inverse Received Data Out	
13	RD+	Received Data Out	
14	$V_{EE}R$	Receiver Ground	
15	$V_{CC}R$	Receiver Power 3.3 V ± 10%	5
16	$V_{CC}T$	Transmitter Power 3.3 V ± 10%	5
17	$V_{EE}T$	Transmitter Ground	
18	TD+	Transmitter Data In	6
19	TD-	Inverse Transmitter Data In	6
20	$V_{EE}T$	Transmitter Ground	

Notes:

1. Pin 2 is connected to internal ground.
2. Mod-Def 0, 1, 2 are the module definition pins. They should be pulled up with a 4.7 kΩ to 10 kΩ resistor on the host board to a supply less than $V_{CC}T$ + 0.3 V or $V_{CC}R$ + 0.3 V. In order to use this interface, supply 3.3 V to $V_{CC}T$.
   Mod-Def 0 is grounded by the module to indicate that the module is present.
   Mod-Def 1 is the clock line of the two-wire serial interface.
   Mod-Def 2 is the data line of the two-wire serial interface.
3. LOS (Loss Of Signal) is an open collector/drain output which should be pulled up with an externally with a 4.7 kΩ to 10 kΩ resistor on the host board to a supply less than $V_{CC}T$, R + 0.3 V. When high, this output indicates that the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). In the low state, the output will be pulled to a voltage less than 0.8 V.
4. RD-/+: These are the differential receiver outputs. They are AC-coupled to 100 Ω differential lines which should be terminated with 100 Ω differential at the SERDES. AC-coupling is present inside the module and is thus not required on the host board.
5. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 2.97 V to 3.63 V at the SFP connector pin.
6. TD-/+: These are the differential transmitter inputs. They are AC-coupled differential lines with 100 Ω differential termination inside the module. AC-coupling is present inside the module and is thus not required on the host board.

Table 3. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_s	-40	+100	°C	
Supply Voltage	V_{cc}	-0.5	3.63	V	
Data Input Voltage	V_i	-0.5	Vcc	V	

Table 4. Recommended Operating Conditions

All the data in this specification refers to the operating conditions above and over lifetime unless otherwise stated.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case Operating Temperature	T_c	-40		+85	°C	Note 1, 2
Supply Voltage	V_{cc}	3.0	3.30	3.6	V	
Data Output Load	R_L		100		Ω	differential
Signalling Rate (Fast Ethernet)	B		125		MBd	4B/5B. Note 3
Singalling Rate (OC-3)	B		155.52		MBd	

Notes:
1. The case temperature is measured at the surface of the topside (see figure 5 Module drawing) using a thermocouple connected to the housing.
2. Electrical and optical specifications of the product are guaranteed across recommended case operating temperature range only.
3. Ethernet auto-negotiation pulses are not supported.

Table 5. Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Current	I_{cc}		60	140	mA	Note 5
Power Dissipation	P_{DISS}		200	500	mW	
Differential Input Voltage	V_{DIFF}	0.5	0.8	1.8	V	Peak-to-peak
Input Differential Impedance	R_{in}		100		Ω	Note 6
Transmitter Disable (TX Disable) High	V_{IH}	2.0		3.5	V	
Transmitter Disable (TX Disable) Low	V_{IL}	0		0.8	V	

Notes:
5. Typical value is valid for room temperature and 3.3 V.
6. Connected directly to TX data input pins. AC coupling from pins into driver IC.

Table 6. Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Current	I_{CC}		67	100	mA	
Power Dissipation	P_{DISS}		220	360	mW	
Data Output: Receiver Differential Output Voltage (RD+/-)	$\|V_{OH}-V_{OL}\|$	0.4		2.0	V	Notes 7, 8
Data Output Rise Time (10%-90%)	t_r			2.20	ns	
Data Output Fall Time (10%-90%)	t_f			2.20	ns	
Loss of Signal Output Voltage – Low	$LOSV_{OL}$			0.8	V	
Loss of Signal Output Voltage – High	$LOSV_{OH}$	2.0			V	

Notes:
7. Differential output voltage is internally AC-coupled but requires an external load termination (100 Ω differential). The low and high voltages are measured under this load condition.
8. Data and Data-bar outputs are squelched at LOS assert levels.

Table 7. Transmitter Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Optical Power 62.5/125 μm NA = 0.275 Fiber	Po	-20.0	-17.0	-14.0	dBm	Average power, Note 1
Output Optical Power 50/125 μm NA = 0.20 Fiber	Po	-23.5	-20.0	-14.0	dBm	Average power, Note 1
Extinction Ratio	ER	10			dB	
Central Wavelength	λ_c	1270	1308	1380	nm	
Spectral Width – FWHM	$\Delta\lambda$		147		nm	
Optical Rise Time (10%-90%)	t_r	0.6	1.0	3.0	ns	
Optical Fall Time (10%-90%)	t_f	0.6	1.0	3.0	ns	
Duty Cycle Distortion Contributed by the Transmitter	DCD			0.60	ns	Note 2, 3
Data Dependent Jitter Contributed by the Transmitter	DDJ			0.60	ns	Note 3
Random Jitter Contributed by the Transmitter	RJ			0.69	ns	Note 3, Peak-to-peak
			0.1	0.52	ns	Note 4, Peak-to-peak, OC-3
Systematic Jitter Contributed by the Transmitter OC-3	SJ		0.25	1.2	ns	Note 5, Peak-to-peak, OC-3
Transmitter Disable (High)	PO(off)			-45	dBm	

Notes:
1. These optical power values are measured over the specified operating voltage and temperature ranges. The average power value can be converted to a peak power value by adding 3 dB.
2. Duty Cycle Distortion contributed by the transmitter is measured at the 50% threshold of the optical output signal.
3. Characterized with PRBS2^7-1 pattern.
4. Random Jitter contributed by the transmitter is specified with a 155.52 MBd (77.76 MHz square-wave) input signal.
5. Systematic Jitter contributed by the transmitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. It's measured with 50% threshold using 2^23-1 PRBS input pattern at 155.52 MBd.

Table 8. Receiver Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Optical Input Power	P_{IN}	-31.0		-14.0	dBm	Note 6, Average power
		-31.0		-14.0		Note 6, 9, Average power, OC-3
Operating Wavelength	λ_R	1270		1380	nm	
Duty Cycle Distortion Contributed by the Receiver	DCD			0.4	ns	Note 7, 8
Data Dependent Jitter Contributed by the Receiver	DDJ			1.0	ns	Note 8
Random Jitter Contributed by the Receiver	RJ		0.1	2.14	ns	Note 8, Peak-to-peak
			0.1	1.91	ns	Note 10, Peak-to-peak, OC-3
Systematic Jitter Contributed by the Receiver OC-3	SJ		0.16	1.2	ns	Note 11, Peak-to-peak, OC-3
Loss of Signal – De-asserted	P_D			-32.0	dBm	Average
Loss of Signal – Asserted	P_A	-45			dBm	Average
Loss of Signal – Hysteresis	$P_A - P_D$	0.5	1.8		dB	

Notes:
6. This specification is intended to indicate the performance of the receiver section of the transceiver when Optical Input Power signal characteristics are present per the following definitions:
   - Over the specified operating temperature and voltage ranges
   - Bit Error Rate (BER) is better than or equal to 1 x 10^{-10}
   - Transmitter is operating to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
   - Fiber: 62.5/125 μm, NA = 0.275; or 50/125 μm, NA = 0.20
7. Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold of the electrical output signal.
8. Characterized with PRBS2^7-1 pattern.
9. Measured per 50/125 μm (NA = 0.2) fiber with a 155.52 MBd (77.76 MHz square-wave) input pattern.
10. Random Jitter contributed by the Receiver is specified with a 155.52 MBd (77.76 MHz square-wave) input signal.
11. Systematic Jitter contributed by the receiver is definied as the combination of Duty Cycle Distortion and Data Dependent Jitter. It's measured with 50% threshold using 2^23-1 PRBS input pattern at 155.52 MBd.

Table 9. Transceiver diagnostics timing characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Hardware TXDIS Assert Time	t_off		10	µs	Note 1, Figure 8
Hardware TXDIS De-Assert Time	t_on		10	µs	Note 2, Figure 8
Time to Initialize	t_init		300	ms	Note 3, Figure 8
Hardware LOS Assert Time	t_sd_on		100	µs	Note 4
Hardware LOS De-Assert Time	t_sd_off		350	µs	Note 5
Software TX_DISABLE Assert Time	t_off_soft		100	ms	Note 6
Software TX_DISABLE De-Assert Time	t_on_soft		100	ms	Note 7
Software RX_LOS Assert Time	t_loss_on_soft		100	ms	Note 8
Software RX_LOS De-Assert Time	t_loss_off_soft		100	ms	Note 9
Analog Parameter Data Ready	t_data		1000	ms	Note 10
Serial Hardware Ready	t_serial		300	ms	Note 11
Write Cycle Time	t_write		10	ms	Note 12
Serial ID clock Rate	f_serial_clock		400	kHz	

Notes:
1. Time from rising edge of TXDIS to when the optical output falls below 10% of nominal.
2. Time from falling edge of TXDIS to when the modulated optical output rises above 90% of nominal.
3. Time from Power on or falling edge of TXDIS to when the modulated optical output rises above 90% of nominal.
4. Time from valid optical signal to SD assertion.
5. Time from loss of optical signal to SD de-assertion.
6. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
7. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the modulated optical output rises above 90% of nominal.
8. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
9. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
10. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
11. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
12. Time from stop bit to completion of a 1-8 byte write command.

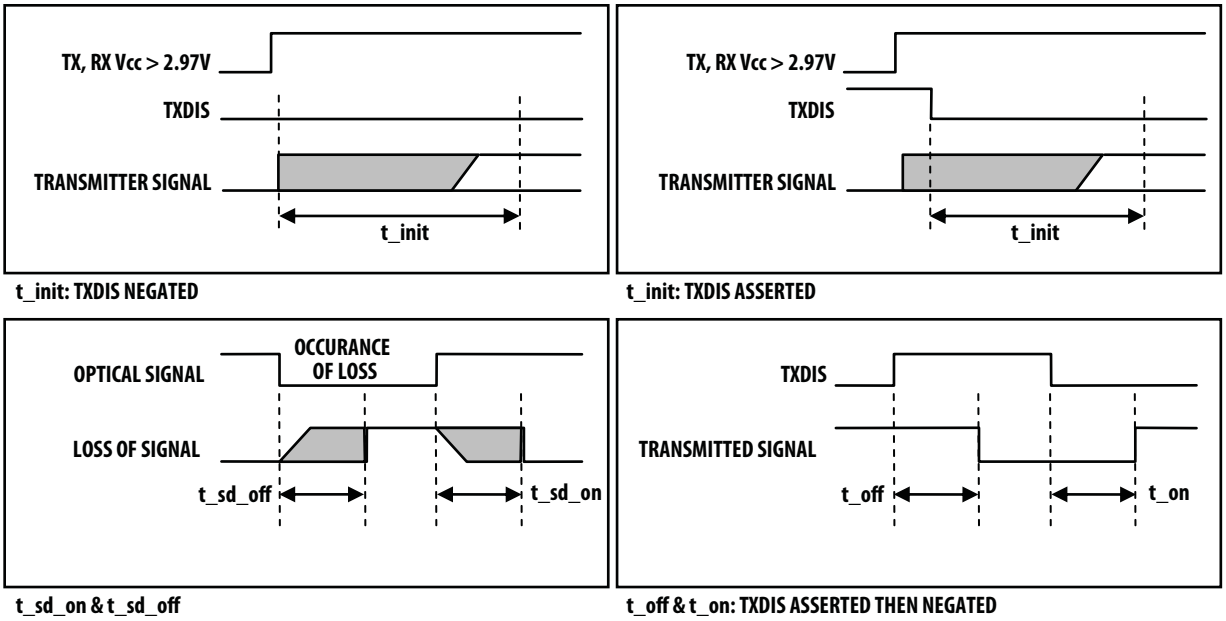


Figure 5. Timing diagrams

Table 10. Transceiver Digital Diagnostic Monitor (Read Time Sense) Characteristics.

Parameter	Symbol	Max	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±3.0	°C	Temperature is measured internal to the transceiver. Valid from -40°C to +85°C case temperature. The temperature reference point is located in the center of the module and is typically 5 to 10 degrees hotter than the module case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	±0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP VCC pin. Valid over 3.3 V ±10%.
Transmitter LED DC Bias Current Accuracy	I_{INT}	±10	%	I_{INT} is better than ±10% value.
Transmitter Average Optical Power Accuracy	P_T	±3.0	dB	Transmitter power is inferred from the LED bias current.
Received Average Optical Input Power Accuracy	P_R	±3.0	dB	Coupled from a 62.5/125 μm fiber.

Table 11. EEPROM Serial ID Memory Contents – Address A0h

Byte # Decimal	Hex	ASCII	Description	Byte # Decimal	Hex	ASCII	Description
0	03		SFP transceiver	37	00		
1	04			38	17		
2	07		LC connector	39	6A		
3	00			40	48	H	
4	00			41	46	F	
5	01		OC3	42	42	B	
6	20		100Base-FX compliance	43	52	R	
7	00			44	2D	-	
8	00			45	35	5	
9	00			46	37	7	
10	00			47	45	E	
11	02		4B/5B Encoding [1]	48	35	5	
12	01		100Mbits/s [2]	49	41	A	
13	00			50	50	P	
14	00			51	5A	Z	
15	00			52	20		
16	C8			53	20		
17	C8			54	20		
18	00			55	20		
19	00			56	20		
20	41	A		57	20		
21	56	V		58	20		
22	41	A		59	20		
23	47	G		60	05		Note 3
24	4F	O		61	1E		Note 3
25	20			62	00		
26	20			63			Note 4
27	20			64	00		
28	20			65	12		TX Disable and LOS implemented.
29	20			66	00		
30	20			67	00		
31	20			68 - 83			Note 5
32	20			84 - 91			Note 6
33	20			92	68		Digital diagnostics implemented. Internally calibrated. Average RX Power.
34	20			93	D0		Alarm warnings, SoftTX_Disable and Soft RX_LOS implemented.
35	20			94	03		Includes functionality described in Rev 10.2 of SFF-8472.
36	00			95			Note 4
				96 - 127	00		Note 7

Notes:
1. Also supports Sonet OC3 encoding code.
2. Also supports 155 MBaud for Sonet OC3.
3. LED wavelength is represented in 16 unsigned bits. The hex representation of 1310 (nm) is 0x051E.
4. Address 63 is the checksum for bytes 0-62 and address 95 is the checksum for bytes 64-94. They are calculated (per SFF-8472) and stored prior to product shipment.
5. Address 68-83 specify a unique module serial number.
6. Address 84-91 specify the date code.
7. Address 96-127 is vendor specific.

Table 12. EEPROM Serial ID Memory Contents - Enhanced Features (Address A2h)

Byte # Decimal	Notes	Byte # Decimal	Notes	Byte # Decimal	Notes
0	Temp H Alarm MSB [1]	26	Tx Power L Alarm MSB [4]	104	Real Time Rx Power MSB [5]
1	Temp H Alarm LSB [1]	27	Tx Power L Alarm LSB [4]	105	Real Time Rx Power LSB [5]
2	Temp L Alarm MSB [1]	28	Tx Power H Warning MSB [4]	106	Reserved
3	Temp L Alarm LSB [1]	29	Tx Power H Warning LSB [4]	107	Reserved
4	Temp H Warning MSB [1]	30	Tx Power L Warning MSB [4]	108	Reserved
5	Temp H Warning LSB [1]	31	Tx Power L Warning LSB [4]	109	Reserved
6	Temp L Warning MSB [1]	32	Rx Power H Alarm MSB [5]	110	Status/Control – See Table
7	Temp L Warning LSB [1]	33	Rx Power H Alarm LSB [5]	111	Reserved
8	Vcc H Alarm MSB [2]	34	Rx Power L Alarm MSB [5]	112	Flag Bits – See Table
9	Vcc H Alarm LSB [2]	35	Rx Power L Alarm LSB [5]	113	Flag Bits – See Table
10	Vcc L Alarm MSB [2]	36	Rx Power H Warning MSB [5]	114	Reserved
11	Vcc L Alarm LSB [2]	37	Rx Power H Warning LSB [5]	115	Reserved
12	Vcc H Warning MSB [2]	38	Rx Power L Warning MSB [5]	116	Flag Bits – See Table
13	Vcc H Warning LSB [2]	39	Rx Power L Warning LSB [5]	117	Flag Bits – See Table
14	Vcc L Warning MSB [2]	40-55	Reserved	118-127	Reserved
15	Vcc L Warning LSB [2]	56-94	External Calibration Constants [6]	128-247	Customer Writable
16	Tx Bias H Alarm MSB [3]	95	Checksum for Bytes 0-94 [7]	248-255	Vendor Specific
17	Tx Bias H Alarm LSB [3]	96	Real Time Temperature MSB [1]		
18	Tx Bias L Alarm MSB [3]	97	Real Time Temperature LSB [1]		
19	Tx Bias L Alarm LSB [3]	98	Real Time Vcc MSB [2]		
20	Tx Bias H Warning MSB [3]	99	Real Time Vcc LSB [2]		
21	Tx Bias H Warning LSB [3]	100	Real Time Tx Bias MSB [3]		
22	Tx Bias L Warning MSB [3]	101	Real Time Tx Bias LSB [3]		
23	Tx Bias L Warning LSB [3]	102	Real Time Tx Power MSB [4]		
24	Tx Power H Alarm MSB [4]	103	Real Time Tx Power LSB [4]		
25	Tx Power H Alarm LSB [4]				

Notes:
1. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256°C.
2. Supply Voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 μV.
3. Tx bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 μA.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
6. Bytes 56-94 are not intended for use with HFBR-57E5APZ, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

Table 13. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110).

Bit #	Status/Control Name	Description	Notes
7	TX_DISABLE State	Digital state of Soft TX_DISABLE	
6	Soft TX_DISABLE	Read/write bit for changing digital state of TX_DISABLE function	
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	RX_LOS State	Digital state of SFP RX_LOS Output Pin (1 = RX_LOS asserted)	
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = ready)	

Table 14. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold.
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold.
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold.
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold.
	3	Tx Bias High Alarm	Set when transceiver LED bias exceeds high alarm threshold.
	2	Tx Bias Low Alarm	Set when transceiver LED bias exceeds low alarm threshold.
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold.
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold.
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold.
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold.
	0-5	Reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold.
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold.
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold.
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold.
	3	Tx Bias High Warning	Set when transceiver LED bias exceeds high warning threshold.
	2	Tx Bias Low Warning	Set when transceiver LED bias exceeds low warning threshold.
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold.
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold.
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold.
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold.
	0-5	Reserved	

Table 15. Settings of Alarm and Warning Thresholds

	Tx power [dBm]	Rx power [dBm]	Transceiver Temperature [°C]	Supply voltage [V]	Tx bias current [mA]
High Alarm	-10	-10	110	3.6	120
Low Alarm	-23	-33	-45	2.8	10
High Warning	-12	-12	95	3.5	110
Low Warning	-22	-32	-42	3	15

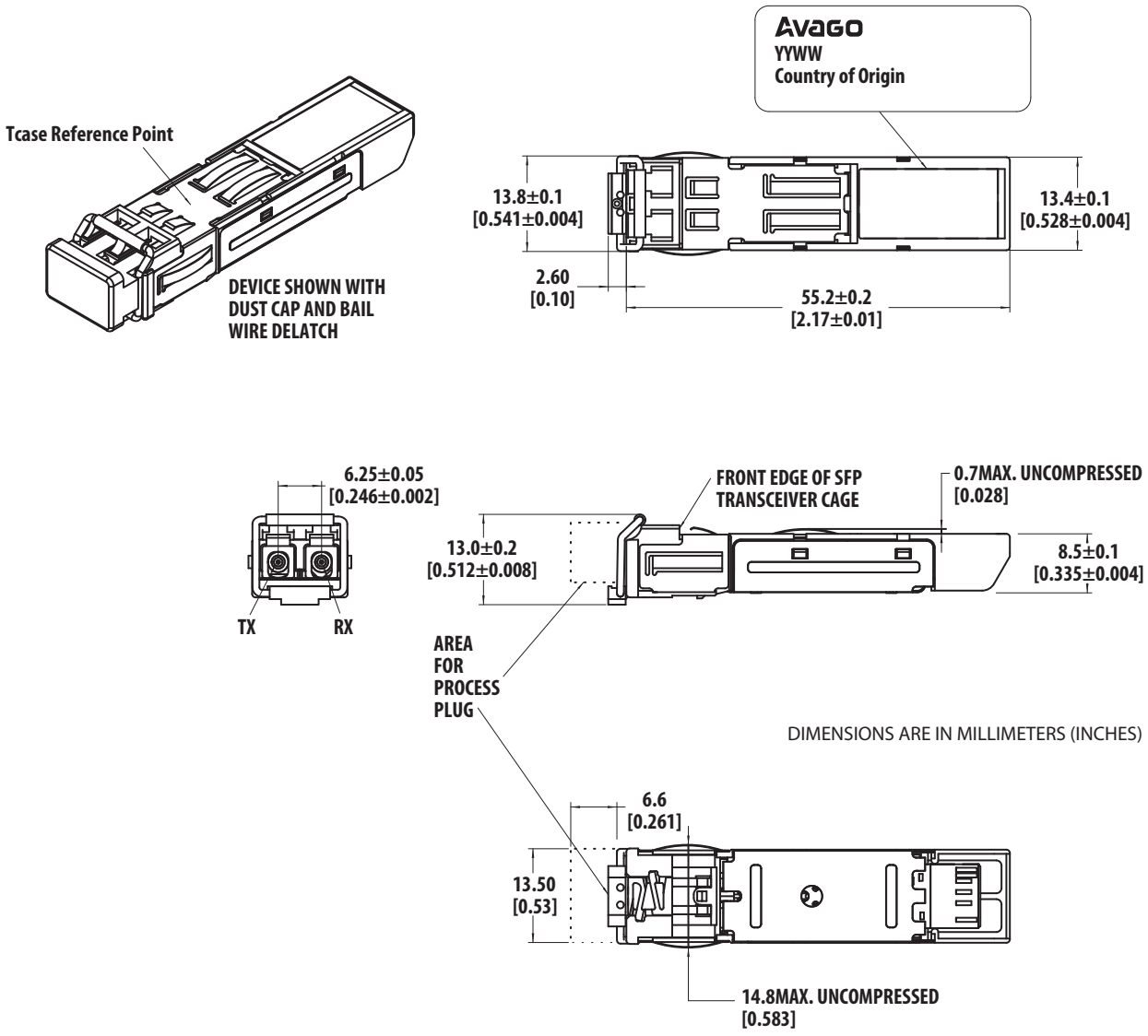
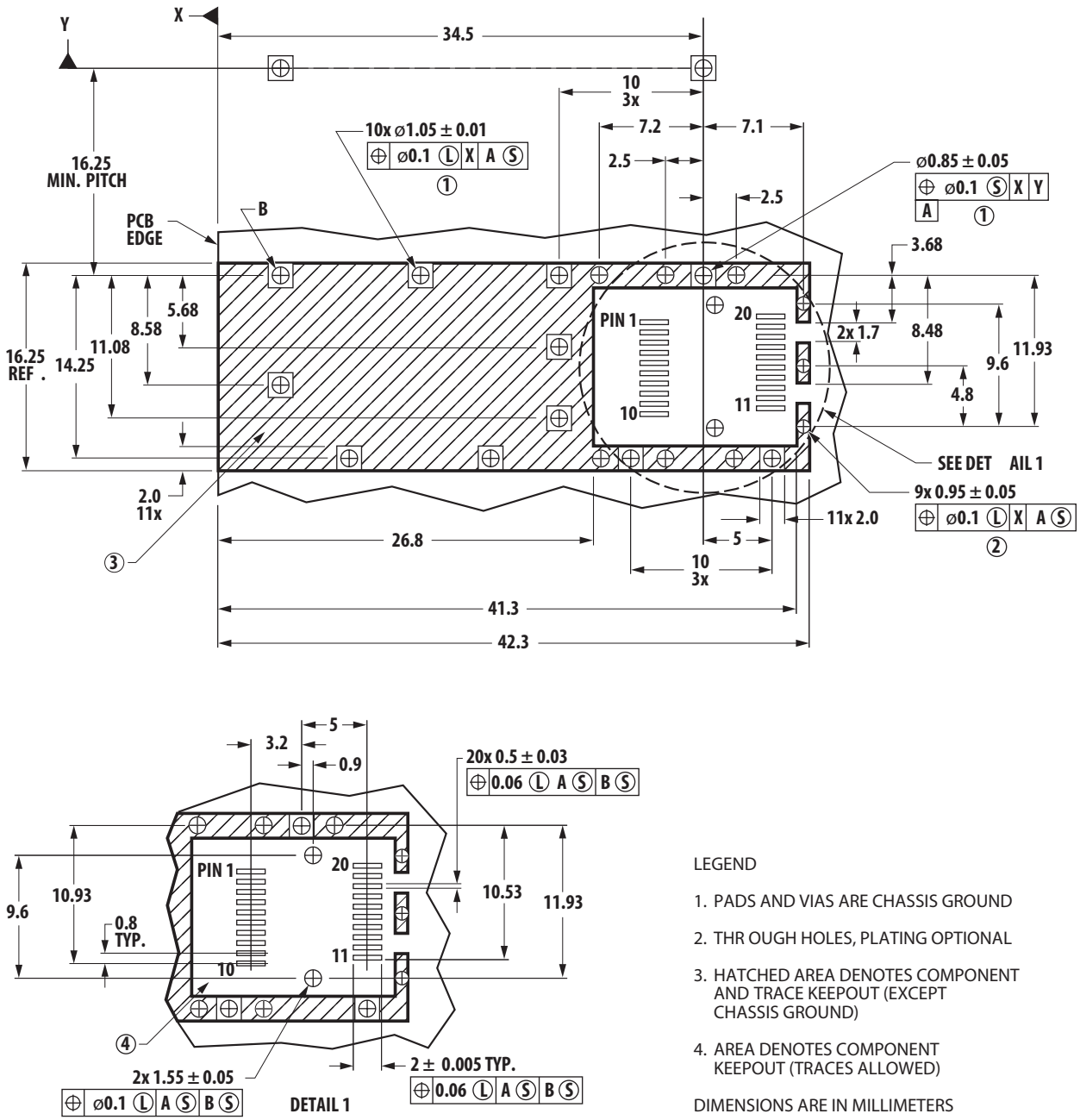


Figure 6. Module Drawing

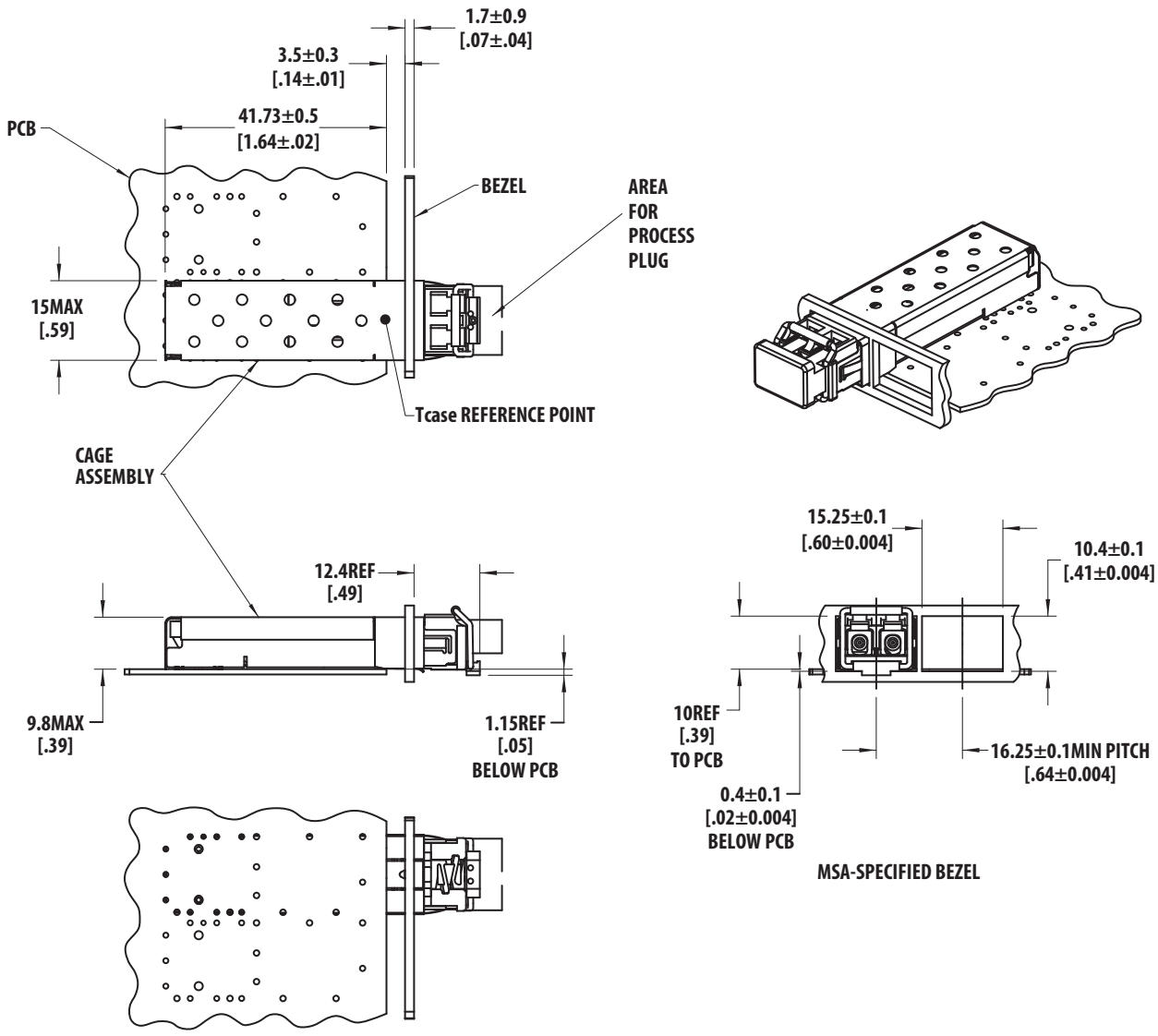


LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
2. THR OUGH HOLES, PLATING OPTIONAL
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)

DIMENSIONS ARE IN MILLIMETERS

Figure 7. SFP Host Board Mechanical Layout



DIMENSIONS ARE IN MILLIMETERS [INCHES].

Figure 8. SFP Assembly Drawing

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9