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June 2000 Revised April 2005

FSTD16211 24-Bit Bus Switch with Level Shifting

Ordering Code:

exists between the A and B Ports.

5V inputs and 3.3V outputs.

FAIRCHILD

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General Description

FSTD16211

Order Number	Package Number	Package Description				
FSTD16211G (Note 1)(Note 2)		54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]				
FSTD16211MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide				
Note 1: Ordering code "G" indicates Trays.						

Features

■ Low I_{CC}

(FBGA)

■ Voltage level shifting

 \blacksquare 4 Ω switch connection between two ports

Control inputs compatible with TTL level

■ Zero bounce in flow-through mode

Minimal propagation delay through the switch

■ Also packaged in plastic Fine-Pitch Ball Grid Array

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

24-Bit Bus Switch with Level Shifting

The Fairchild Switch FSTD16211 provides 24-bits of high-

speed CMOS TTL-compatible bus switching. The low On

Resistance of the switch allows inputs to be connected to

outputs without adding propagation delay or generating

additional ground bounce noise. A diode to V_{CC} has been

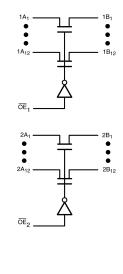
integrated into the circuit to allow for level shifting between

The device is organized as a 12-bit or 24-bit bus switch.

When \overline{OE}_1 is LOW, the switch is ON and Port 1A is con-

nected to Port 1B. When $\overline{\text{OE}}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{\text{OE}}_{1/2}$ is HIGH, a high impedance state

Logic Diagram



FSTD16211

Connection Diagrams

Pin Assignment for TSSOP								
NC -		56	- OE,					
1A1 -	2	55						
1A2 -	3	54	- 1B1					
1A3 —	4	53	- 1B ₂					
1A4 —	5	52	— 1B ₃					
1A ₅ —	6	51	— 1B ₄					
1A ₆ —	7	50	— 1B ₅					
GND —	8	49	- GND					
1A7 —	9	48	— 1B ₆					
1A ₈ —	10	47	— 1B ₇					
1A ₉ —	11	46	— 1B ₈					
1A ₁₀ -	12	45	— 1B ₉					
1A ₁₁ —	13	44	— 1B ₁₀					
1A ₁₂ -	14	43	— 1B ₁₁					
2A1-	15	42	- 1B ₁₂					
2A2-	16	41	— 2B1					
V _{CC}	17	40	- 2B ₂					
2A3-	18	39	— 2B ₃					
GND-	19	38	- GND					
2A4-	20	37	— 2B ₄					
2A5-	21	36	— 2B ₅					
2A ₆ —	22	35	— 2B ₆					
2A7-	23	34	— 2B ₇					
2A ₈ —	24	33	— 2B ₈					
2A ₉ —	25	32	— 2B ₉					
2A ₁₀ —	26	31	- 2B ₁₀					
2A ₁₁ —	27	30	— 2B ₁₁					
2A ₁₂ —	28	29	- 2B ₁₂					

Pin Assignment for FBGA

	1	2	3	4	5	6
A	0	0	0	0	0	0
В	Ιõ	õ	õ	õ	õ	õ
υ	Õ	Õ	Õ	Õ	Õ	Õ
D	Ó	Ó	Ò	0	0	Ó
ш	Ó	Ó	Ò	0	0	Ó
ч	0	0	0	0	0	0
G	0	0	0	0	0	0
н	0	0	0	0	0	0
ſ	0	0	0	0	0	0

(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

Pin Assignment for FBGA

	1	2	3	4	5	6
Α	1A ₂	1A ₁	NC	OE ₂	1B ₁	1B ₂
В	1A ₄	1A ₃	1A ₇	OE ₁	1B ₃	1B ₄
С	1A ₆	1A ₅	GND	1B ₇	1B ₅	1B ₆
D	1A ₁₀	1A ₉	1A ₈	1B ₈	1B ₉	1B ₁₀
E	1A ₁₂	1A ₁₁	2A ₁	2B ₁	1B ₁₁	1B ₁₂
F	2A ₄	2A ₃	2A ₂	2B ₂	2B ₃	2B ₄
G	2A ₆	2A ₅	V _{CC}	GND	2B ₅	2B ₆
н	2A ₈	2A ₇	2A ₉	2B ₉	2B ₇	2B ₈
J	2A ₁₂	2A ₁₁	2A ₁₀	2B ₁₀	2B ₁₁	2B ₁₂

Truth Table

Inp	uts	Inputs/Outputs		
OE ₁	OE ₂	1A, 1B	2A, 2B	
L	L	1A = 1B	2A = 2B	
L	н	1A = 1B	Z	
н	L	Z	2A = 2B	
н	Н	Z	Z	

Absolute Maximum Ratings(Note 3)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Switch Voltage (V _S) (Note 4)	-0.5V to +7.0V
DC Input Control Pin Voltage (VIN)(Note 5)	-0.5V to +7.0V
DC Input Diode Current (I _{IK}) $V_{IN} < 0V$	–50 mA
DC Output (I _{OUT})	128 mA
DC V _{CC} /GND Current (I _{CC} /I _{GND})	+/- 100 mA
Storage Temperature Range (T _{STG})	–65°C to +150 °C

Recommended Operating

Conditions (Note 6)	
Power Supply Operating $(V_{CC)}$	4.5V to 5.5V
Input Voltage (V _{IN})	0V to 5.5V
Output Voltage (V _{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T _A)	-40 °C to +85 °C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

		V _{CC}	T _A =	-40 °C to +	85 °C		
Symbol	Parameter	(V)	Min	Typ (Note 7)	Мах	Units	Conditions
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18 \text{ mA}$
V _{IH}	HIGH Level Input Voltage	4.5-5.5	2.0			V	
VIL	LOW Level Input Voltage	4.5-5.5			0.8	V	
V _{OH}	HIGH Level	4.5-5.5		See Figure 3	3	V	
II.	Input Leakage Current	5.5			±1.0	μA	$0 \le V_{IN} \le 5.5 V$
		0			10	μA	$V_{IN} = 5.5V$
I _{OZ}	OFF-STATE Leakage Current	5.5			±1.0	μA	$0 \le A, B \le V_{CC}$
R _{ON}	Switch On Resistance	4.5		4	7	Ω	V _{IN} = 0V, I _{IN} = 64 mA
	(Note 8)	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 30 \text{ mA}$
		4.5		35	50	Ω	$V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$
I _{CC}	Quiescent Supply Current	5.5			1.5	mA	$OE_1 = OE_2 = GND$
							$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
					10	μA	$OE_1 = OE_2 = V_{CC}$
							$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
I _{CCT}	Increase in I _{CC} per Control Input	5.5			2.5	mA	One Control Input at 3.4V
							Other Control Inputs at V_{CC} or GND

Note 7: Typical values are at V_{CC} = 5.0V and $T_A{=}\ {+}25^{\circ}C$

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

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AC Electrical Characteristics

Symbol	Parameter	$\label{eq:T_A} \begin{split} & \textbf{T}_{\textbf{A}} = -40 ~^\circ \textbf{C} ~ \textbf{to} ~ +85 ~^\circ \textbf{C}, \\ & \textbf{C}_{\textbf{L}} = 50 \textbf{pF}, ~ \textbf{RU} = \textbf{RD} = 500 \Omega \\ & \textbf{V}_{\textbf{CC}} = 4.5 - 5.5 \textbf{V} \end{split}$		Units	Conditions	Figure Number	
		Min	Max				
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 9)		0.25	ns	V _I = OPEN	Figures 1, 2	
t _{PZH} , t _{PZL}	Output Enable Time	1.5	5.5	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figures 1, 2	
t _{PHZ} , t _{PLZ}	Output Disable Time	1.5	6.5	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figures 1, 2	

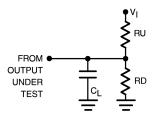
Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	3.5		pF	$V_{CC} = 5.0V$
C _{I/O}	Input/Output Capacitance	5.5		pF	$V_{CC}, \overline{OE} = 5.0V$

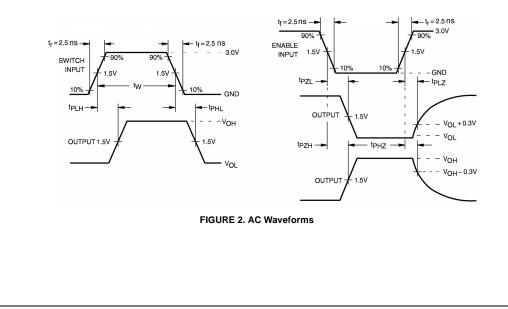
Note 10: $T_A = +25 \,^{\circ}C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



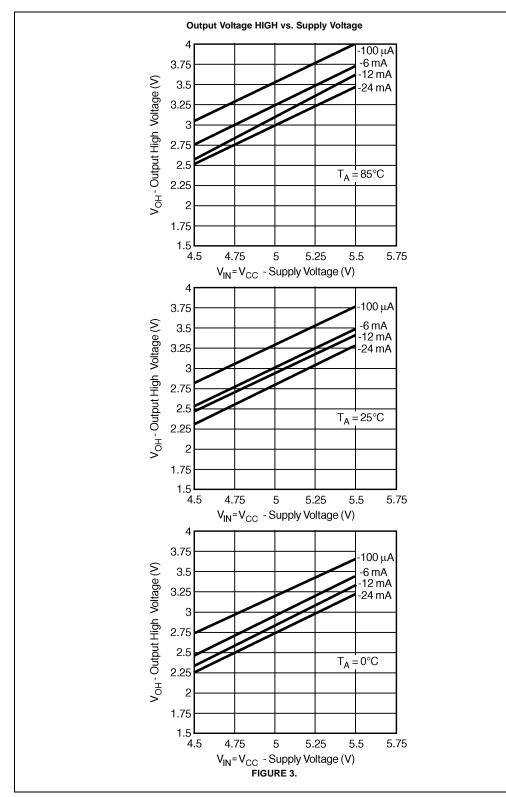
Note: Input driven by 50Ω source terminated in 50Ω Note: CL includes load and stray capacitance Note: Input PRR = 1.0 MHz, $t_W = 500$ ns

FIGURE 1. AC Test Circuit

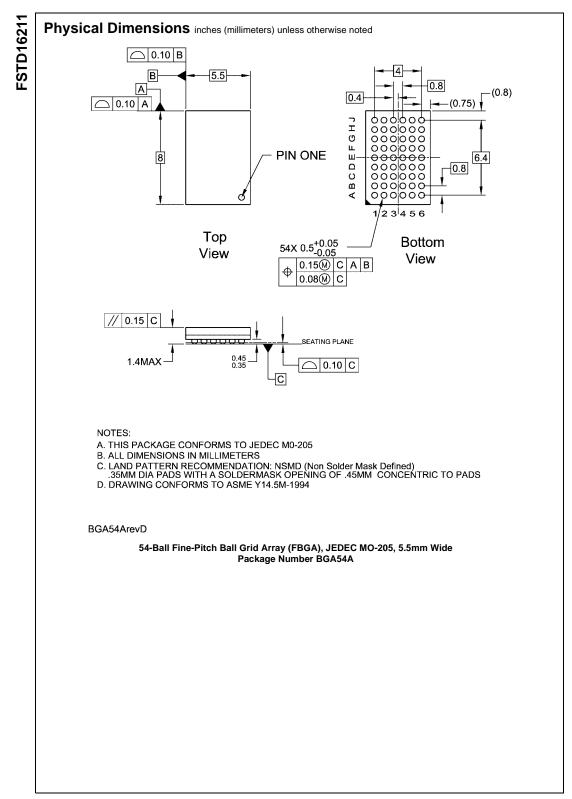


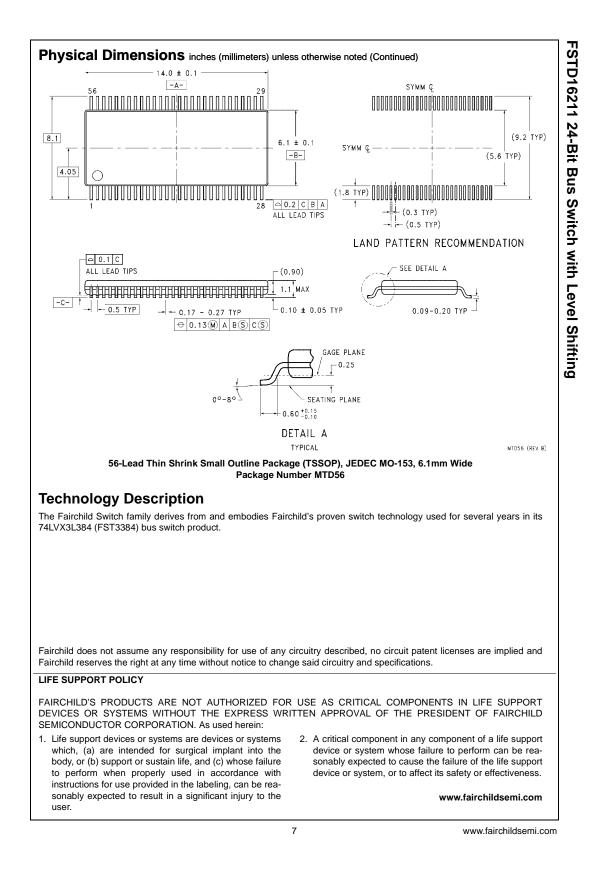
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