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April 1st, 2010
Renesas Electronics Corporation

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R8C/10 Group
SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0035-0160
Rev.1.60
Jan 27, 2006

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	62.5 ns (f(X$_{IN}$) = 16 MHz, V$_{CC}$ = 3.0 to 5.5 V)
		100 ns (f(X$_{IN}$) = 10 MHz, V$_{CC}$ = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 "Product List"
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel,
		Timer Z: 8 bits x 1 channel
		(Each timer equipped with 8-bit prescaler)
		Timer C: 16 bits x 1 channel
		(Input capture circuit)
	Serial interface	•1 channel
		Clock synchronous, UART
		•1 channel
		UART
	A/D converter	10-bit A/D converter: 1 circuit, 8 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	Internal: 9 factors, External: 5 factors,
		Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits
		•Main clock generation circuit (Equipped with a built-in
		feedback resistor)
		•On-chip oscillator
	Oscillation stop detection function	Main clock oscillation stop detection function
Electrical characteristics	Supply voltage	V$_{CC}$ = 3.0 to 5.5 V (f(X$_{IN}$) = 16 MHz)
		V$_{CC}$ = 2.7 to 5.5 V (f(X$_{IN}$) = 10 MHz)
	Power consumption	Typ. 8mA (V$_{CC}$ = 5.0 V, (f(X$_{IN}$) = 16MHz)
		Typ. 5mA (V$_{CC}$ = 3.0 V, (f(X$_{IN}$) = 10MHz)
		Typ. 35μA (V$_{CC}$ = 3.0 V, Wait mode, Peripheral clock off)
		Typ. 0.7μA (V$_{CC}$ = 3.0 V, Stop mode)
Flash memory	Program/erase supply voltage	V$_{CC}$ = 2.7 to 5.5 V
	Program/erase endurance	100 times
Operating ambient temperature		-20 to 85 °C
		-40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

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1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

Figure 1.1 Block Diagram

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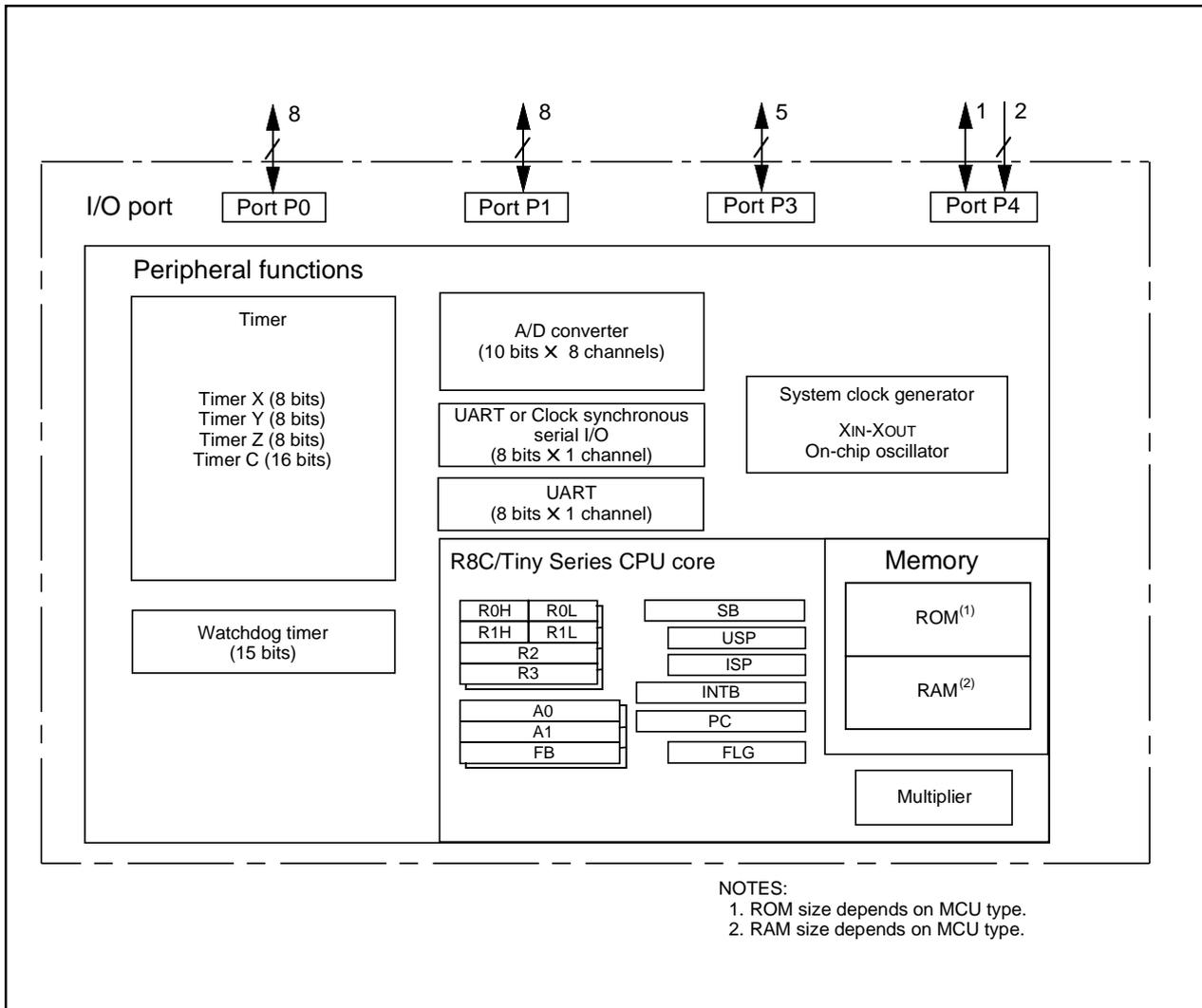
1.4 Product Information

Table 1.2 lists the product inforamation.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21102FP	8K bytes	512 bytes	PLQP0032GB-A	Flash memory version
R5F21103FP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104FP	16K bytes	1K bytes	PLQP0032GB-A	
R5F21102DFP	8K bytes	512 bytes	PLQP0032GB-A	D version
R5F21103DFP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104DFP	16K bytes	1K bytes	PLQP0032GB-A	

Type No. R 5 F 21 10 4 D FP

- Package type:
  FP : PLQP0032GB-A

- Classification:
  D: Operating ambient temperature −40 °C to 85 °C
  No symbol: Operating ambient temperature −20 °C to 85 °C

- ROM capacity:
  2 : 8 KBytes.
  3 : 12 KBytes.
  4 : 16 KBytes.

- R8C/10 group

- R8C/Tiny series

- Memory type:
  F: Flash memory version

- Renesas MCU

- Renesas semiconductors

Figure 1.2 Type No., Memory Size, and Package

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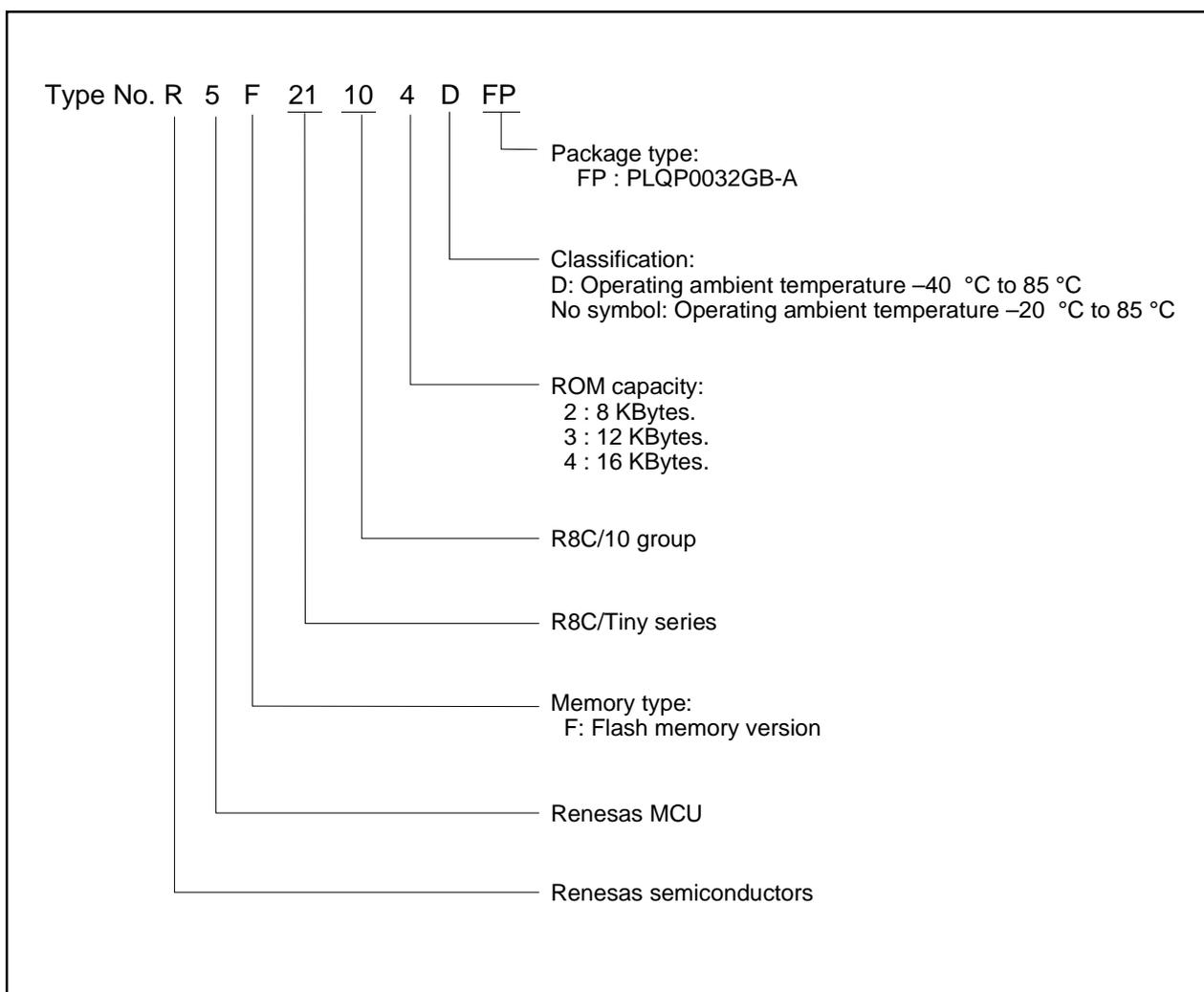
1.5 Pin Assignment

Figure 1.3 shows the pin Assignments (top view).

PIN CONFIGURATION (top view)

R8C/10 Group

Top pins (left to right): 24 23 22 21 20 19 18 17
- 24 P07/AN0
- 23 IVcc
- 22 P30/CNTR0
- 21 AVss
- 20 P31/TZout
- 19 AVcc/Vref
- 18 P32/INT2/CNTR1
- 17 P33/INT3/TCin

Left pins:
- 25 P06/AN1
- 26 P05/AN2
- 27 P04/AN3
- 28 MODE
- 29 P03/AN4
- 30 P02/AN5
- 31 P01/AN6
- 32 P00/AN7/TxD11

Right pins:
- 16 P45/INT0
- 15 P10/KI0
- 14 P11/KI1
- 13 P12/KI2
- 12 P13/KI3
- 11 P14/TxD0
- 10 P15/RxD0
- 9 P16/CLK0

Bottom pins (left to right): 1 2 3 4 5 6 7 8
- 1 P37/TxD10/RxD1
- 2 CNVss
- 3 RESET
- 4 Xout/P47 (1)
- 5 Vss
- 6 Xin/P46
- 7 Vcc
- 8 P17/INT1/CNTR0

NOTES:
1. P47 functions only as an input port.
2. When using On-chip debugger, do not use pins P00/AN7/TxD11 and P37/TxD10/RxD1.
3. Do not connect IVcc to Vcc.

Package: PLQP0032GB-A (32P6U-A)

Figure 1.3 Pin Assignments (Top View)

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1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μF). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	X_{IN}	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the X_{IN} and X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
Main clock output	X_{OUT}	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT}}_0$ to $\overline{\text{INT}}_3$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI}}_0$ to $\overline{\text{KI}}_3$	I	Key input interrupt pins.
Timer X	$CNTR_0$	I/O	Timer X I/O pin
	$\overline{CNTR_0}$	O	Timer X output pin
Timer Y	$CNTR_1$	I/O	Timer Y I/O pin
Timer Z	TZ_{OUT}	O	Timer Z output pin
Timer C	TC_{IN}	I	Timer C input pin
Serial interface	CLK_0	I/O	Transfer clock I/O pin.
	RxD_0, RxD_1	I	Serial data input pins.
	TxD_0, TxD_{10}, TxD_{11}	O	Serial data output pins.
Reference voltage input	V_{REF}	I	Reference voltage input pin for A/D converter. Connect the V_{REF} pin to Vcc.
A/D converter	AN_0 to AN_7	I	Analog input pins for A/D converter
I/O port	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P3_0$ to $P3_3$, $P3_7$, $P4_5$	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. $P1_0$ to $P1_7$ also function as LED drive ports.
Input port	$P4_6$, $P4_7$	I	Port for input-only.

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2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.
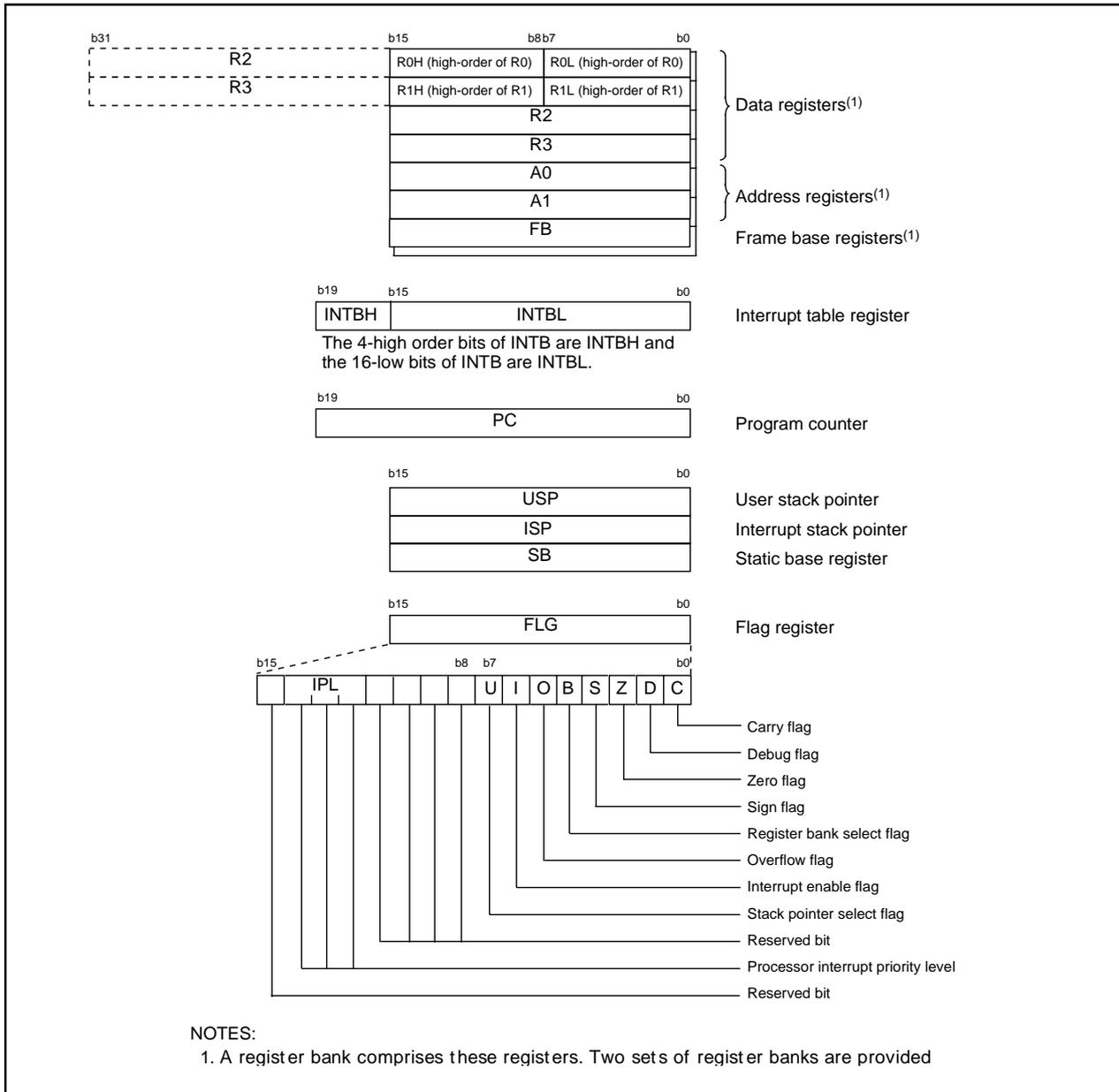
Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

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2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

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3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated lower addresses beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated addresses $0FFDC_{16}$ to $0FFFF_{16}$. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated addresses 00400_{16} to $007FF_{16}$. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000_{16} to $002FF_{16}$. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

NOTES :
1. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address $0YYYY_{16}$	Size	Address $0XXXX_{16}$
R5F21104FP, R5F21104DFP	16K bytes	$0C000_{16}$	1K bytes	$007FF_{16}$
R5F21103FP, R5F21103DFP	12K bytes	$0D000_{16}$	768 bytes	$006FF_{16}$
R5F21102FP, R5F21102DFP	8K bytes	$0E000_{16}$	512 bytes	$005FF_{16}$
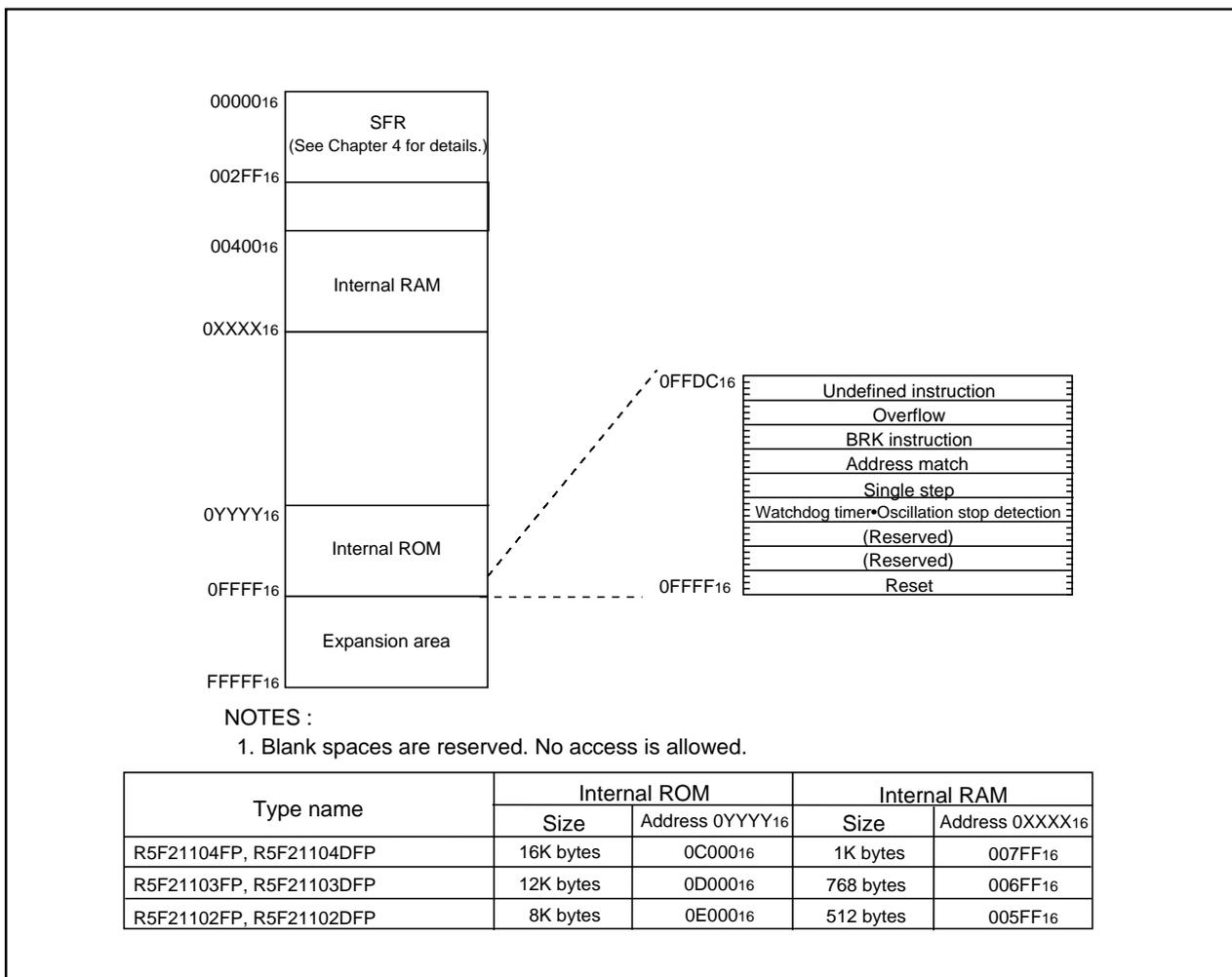
Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	$XXXX0X00_2$
0005_{16}	Processor mode register 1	PM1	$00XXX0X0_2$
0006_{16}	System clock control register 0	CM0	01101000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$00XXX000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register	OCD	00000100_2
$000D_{16}$	Watchdog timer reset register	WDTR	XX_{16}
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	00011111_2
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	$\overline{INT0}$ input filter select register	INT0F	$XXXXX000_2$
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

NOTES:
 1. Blank spaces are reserved. No access is allowed.
X : Undefined

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Table 4.2 SFR Information(2)[1]

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E₁₆	AD conversion interrupt control register	ADIC	XXXXX0002
004F₁₆			
0050₁₆			
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C₁₆			
005D₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

NOTES :
  1. Blank spaces are reserved. No access is allowed.

X : Undefined

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Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
0080_{16}	Timer Y, Z mode register	TYZMR	00_{16}
0081_{16}	Prescaler Y register	PREY	FF_{16}
0082_{16}	Timer Y secondary register	TYSC	FF_{16}
0083_{16}	Timer Y primary register	TYPR	FF_{16}
0084_{16}	Timer Y, Z waveform output control register	PUM	00_{16}
0085_{16}	Prescaler Z register	PREZ	FF_{16}
0086_{16}	Timer Z secondary register	TZSC	FF_{16}
0087_{16}	Timer Z primary register	TZPR	FF_{16}
0088_{16}			
0089_{16}			
$008A_{16}$	Timer Y, Z output control register	TYZOC	00_{16}
$008B_{16}$	Timer X mode register	TXMR	00_{16}
$008C_{16}$	Prescaler X register	PREX	FF_{16}
$008D_{16}$	Timer X register	TX	FF_{16}
$008E_{16}$	Count source set register	TCSS	00_{16}
$008F_{16}$			
0090_{16}	Timer C register	TC	00_{16}
0091_{16}			00_{16}
0092_{16}			
0093_{16}			
0094_{16}			
0095_{16}			
0096_{16}	External input enable register	INTEN	00_{16}
0097_{16}			
0098_{16}	Key input enable register	KIEN	00_{16}
0099_{16}			
$009A_{16}$	Timer C control register 0	TCC0	00_{16}
$009B_{16}$	Timer C control register 1	TCC1	00_{16}
$009C_{16}$	Capture register	TM0	00_{16}
$009D_{16}$			00_{16}
$009E_{16}$			
$009F_{16}$			
$00A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$00A1_{16}$	UART0 bit rate generator	U0BRG	XX_{16}
$00A2_{16}$	UART0 transmit buffer register	U0TB	XX_{16}
$00A3_{16}$			XX_{16}
$00A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$00A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$00A6_{16}$	UART0 receive buffer register	U0RB	XX_{16}
$00A7_{16}$			XX_{16}
$00A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$00A9_{16}$	UART1 bit rate generator	U1BRG	XX_{16}
$00AA_{16}$	UART1 transmit buffer register	U1TB	XX_{16}
$00AB_{16}$			XX_{16}
$00AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$00AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$00AE_{16}$	UART1 receive buffer register	U1RB	XX_{16}
$00AF_{16}$			XX_{16}
$00B0_{16}$	UART transmit/receive control register 2	UCON	00_{16}
$00B1_{16}$			
$00B2_{16}$			
$00B3_{16}$			
$00B4_{16}$			
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$			
$00B9_{16}$			
$00BA_{16}$			
$00BB_{16}$			
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

NOTES:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

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Table 4.4 SFR Information(4)[1]

Address	Register	Symbol	After reset
$00C0_{16}$	AD register	AD	$XXXXXXXX_2$
$00C1_{16}$			$XXXXXXXX_2$
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	AD control register 2	ADCON2	00_{16}
$00D5_{16}$			
$00D6_{16}$	AD control register 0	ADCON0	$00000XXX_2$
$00D7_{16}$	AD control register 1	ADCON1	00_{16}
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	XX_{16}
$00E1_{16}$	Port P1 register	P1	XX_{16}
$00E2_{16}$	Port P0 direction register	PD0	00_{16}
$00E3_{16}$	Port P1 direction register	PD1	00_{16}
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	XX_{16}
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	00_{16}
$00E8_{16}$	Port P4 register	P4	XX_{16}
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	00_{16}
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	$00XX0000_2$
$00FD_{16}$	Pull-up control register 1	PUR1	$XXXXXX0X_2$
$00FE_{16}$	Port P1 drive capacity control register	DRR	00_{16}
$00FF_{16}$			
$01B3_{16}$	Flash memory control register 4	FMR4	01000000_2
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	$0100XX0X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	00000001_2

NOTES:
  1. Blank columns, 0100_{16} to $01B2_{16}$ and $01B8_{16}$ to $02FF_{16}$ are all reserved. No access is allowed.

X : Undefined

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5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr}=25 $^\circ$C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	$^\circ$C
T_{stg}	Storage temperature		-65 to 150	$^\circ$C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	——	5.5	V
AV_{CC}	Analog supply voltage			——	V_{CC}(3)	——	V
V_{SS}	Supply voltage			——	0	——	V
AV_{SS}	Analog supply voltage			——	0	——	V
V_{IH}	"H" input voltage			0.8V_{CC}	——	V_{CC}	V
V_{IL}	"L" input voltage			0	——	0.2V_{CC}	V
$I_{OH (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		——	——	-60.0	mA
$I_{OH (peak)}$	"H" peak output current			——	——	-10.0	mA
$I_{OH (avg)}$	"H" average output current			——	——	-5.0	mA
$I_{OL (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		——	——	60	mA
$I_{OL (peak)}$	"L" peak output current	Except P1$_0$ to P1$_7$		——	——	10	mA
		P1$_0$ to P1$_7$	Drive capacity HIGH	——	——	30	mA
			Drive capacity LOW	——	——	10	mA
$I_{OL (avg)}$	"L" average output current	Except P1$_0$ to P1$_7$		——	——	5	mA
		P1$_0$ to P1$_7$	Drive capacity HIGH	——	——	15	mA
			Drive capacity LOW	——	——	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	——	16	MHz
			2.7V ≤ Vcc < 3.0V	0	——	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC}=AV_{CC}.

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Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		Vref =Vcc	—	—	10	Bit
_	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]	—	—	±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]		—	±2	LSB
R_{LADDER}	Ladder resistance		$V_{REF}=V_{CC}$	10	—	40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	—	—	µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8	—	—	µs
V_{REF}	Reference voltage			—	Vcc[4]	—	V
V_{IA}	Analog input voltage			0	—	Vref	V
_	A/D operating clock frequency[2]	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:
 1. Vcc=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
 2. If fAD exceeds 10 MHz, divide the fAD and hold A/D operating clock frequency (ØAD) 10 MHz or below.
 3. If the AVcc is less than 4.2V, divide the fAD and hold A/D operating clock frequency (ØAD) fAD/2 or below.
 4. Hold Vcc=Vref.

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/erase endurance		100	—	—	times
–	Byte program time		—	50	400	µs
–	Block erase time		—	0.4	9	s
$t_{d(SR-ES)}$	Time delay from suspend request until erase suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase voltage		2.7	—	5.5	V
–	Read voltage		2.7	—	5.5	V
–	Program, Erase temperature		0	—	60	°C
–	Data hold time[2]	Ambient temperature=55 °C	20	—	—	year

NOTES:
 1. Vcc1=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C, unless otherwise specified.
 2. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on[2]		1	—	2000	µs
td(R-S)	STOP release time[3]		—	—	150	µs

NOTES:
 1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
 2. This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.
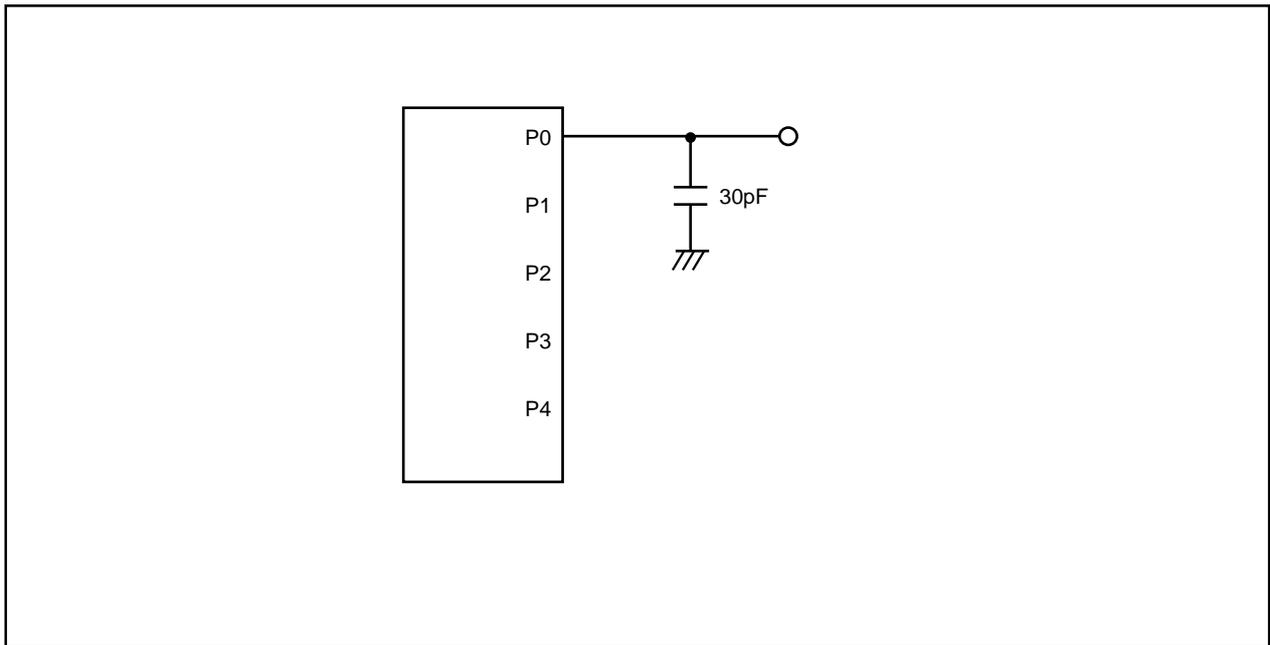 3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

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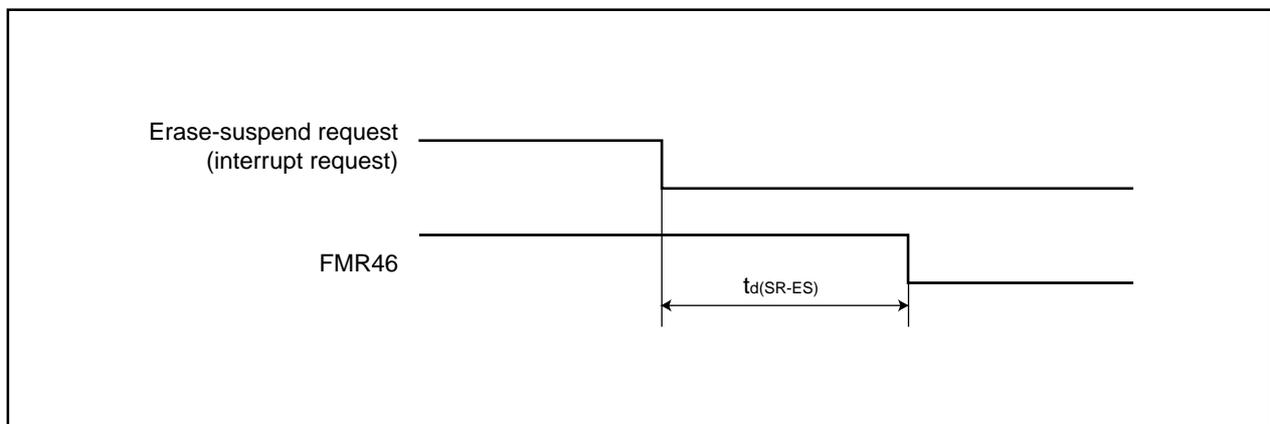**Figure 5.1 Port P0 to P4 measurement circuit**

Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Electrical Characteristics (1)   [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V$_{OH}$	"H" output voltage	Except X$_{OUT}$	I$_{OH}$=-5mA		Vcc-2.0		Vcc	V
			I$_{OH}$=-200µA		Vcc-0.3		Vcc	V
		X$_{OUT}$	Drive capacity HIGH	I$_{OH}$=-1 mA	Vcc-2.0		Vcc	V
			Drive capacity LOW	I$_{OH}$=-500µA	Vcc-2.0		Vcc	V
V$_{OL}$	"L" output voltage	Except P10 to P17, X$_{OUT}$	I$_{OL}$= 5 mA				2.0	V
			I$_{OL}$= 200 µA				0.45	V
		P10 to P17	Drive capacity HIGH	I$_{OL}$= 15 mA			2.0	V
			Drive capacity LOW	I$_{OL}$= 5 mA			2.0	V
			Drive capacity LOW	I$_{OL}$= 200 µA			0.45	V
		X$_{OUT}$	Drive capacity HIGH	I$_{OL}$= 1 mA			2.0	V
			Drive capacity LOW	I$_{OL}$=500µA			2.0	V
V$_{T+}$-V$_{T-}$	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TC$_{IN}$, RxD0, RxD1, P45			0.2		1.0	V
		RESET			0.2		2.2	V
I$_{IH}$	"H" input current		V$_{I}$=5V				5.0	µA
I$_{IL}$	"L" input current		V$_{I}$=0V				-5.0	µA
R$_{PULLUP}$	Pull-up resistance		V$_{I}$=0V		30	50	167	kΩ
R$_{fXIN}$	Feedback resistance	X$_{IN}$				1.0		MΩ
f$_{RING}$	On-chip oscillator frequency				40	125	250	kHz
V$_{RAM}$	RAM retention voltage		At stop mode		2.0			V

NOTES:
  1. Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X$_{IN}$)=20MHz unless otherwise specified.

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Table 5.7 Electrical Characteristics (2)   [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss		High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
				X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
			On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	µA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[1] Peripheral clock operation	—	40	80	µA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[1] Peripheral clock off	—	38	76	µA
			Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at Topr = 25 °C) [V_{CC}=5V]

Table 5.8 X_{IN} input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(X_{IN})$	X_{IN} input cycle time	62.5	–	ns
$t_{WH}(X_{IN})$	X_{IN} input HIGH pulse width	30	–	ns
$t_{WL}(X_{IN})$	X_{IN} input LOW pulse width	30	–	ns

Table 5.9 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	CNTR0 input cycle time	100	–	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	40	–	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	40	–	ns

Table 5.10 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	TCIN input cycle time	400[1]	–	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	200[2]	–	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	200[2]	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.11 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CK)$	CLKi input cycle time	200	–	ns
$t_W(CKH)$	CLKi input HIGH pulse width	100	–	ns
$t_W(CKL)$	CLKi input LOW pulse width	100	–	ns
$t_d(C-Q)$	TxDi output delay time	–	80	ns
$t_h(C-Q)$	TxDi hold time	0	–	ns
$t_{su}(D-C)$	RxDi input setup time	35	–	ns
$t_h(C-D)$	RxDi input hold time	90	–	ns

Table 5.12 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_W(INH)$	$\overline{INT0}$ input HIGH pulse width	250[1]	–	ns
$t_W(INL)$	$\overline{INT0}$ input LOW pulse width	250[2]	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
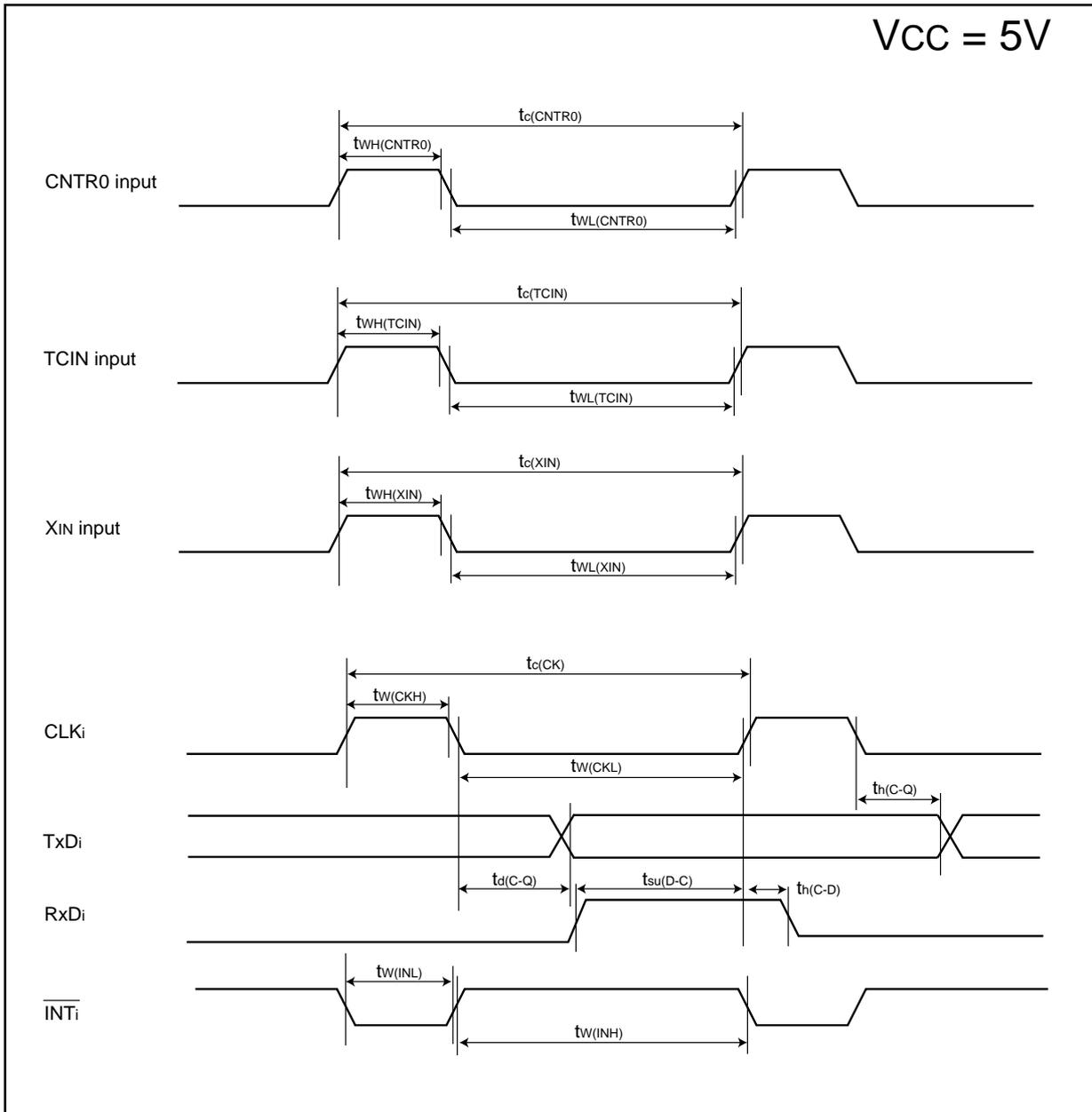2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

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Figure 5.3 Vcc=5V timing diagram

Table 5.13 Electrical Characteristics (3)   [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		V_{CC}-0.5	—	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	V_{CC}-0.5	—	V_{CC}	V
			Drive capacity LOW	I_{OH}=-50 μA	V_{CC}-0.5	—	V_{CC}	V
V_{OL}	"L" output voltage	Except P10 to P17, X_{OUT}	I_{OL}= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 2 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}= 1 mA	—	—	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}=50 μA	—	—	0.5	V
$V_{T+}-V_{T-}$	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		$\overline{RESET}$			0.2	—	1.8	V
I_{IH}	"H" input current		V_I=3V		—	—	4.0	μA
I_{IL}	"L" input current		V_I=0V		—	—	-4.0	μA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	3.0	—	MΩ
f_{RING}	On-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:
1. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

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Table 5.14 Electrical Characteristics (4)   [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	⎯	7	12	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	⎯	5	⎯	mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	⎯	2.5	⎯	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	⎯	1.6	⎯	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	⎯	420	800	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[1] Peripheral clock operation	⎯	37	74	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[1] Peripheral clock off	⎯	35	70	µA
		Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	⎯	0.7	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, $f(X_{IN})$=10MHz unless otherwise specified.

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Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc=3V]

Table 5.15 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100	–	ns
tWH(XIN)	XIN input HIGH pulse width	40	–	ns
tWL(XIN)	XIN input LOW pulse width	40	–	ns

Table 5.16 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300	–	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120	–	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120	–	ns

Table 5.17 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200[1]	–	ns
tWH(TCIN)	TCIN input HIGH pulse width	600[2]	–	ns
tWL(TCIN)	TCIN input LOW pulse width	600[2]	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300	–	ns
tW(CKH)	CLKi input HIGH pulse width	150	–	ns
tW(CKL)	CLKi input LOW pulse width	150	–	ns
td(C-Q)	TxDi output delay time	–	160	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	55	–	ns
th(C-D)	RxDi input hold time	90	–	ns

Table 5.19 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380[1]	–	ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
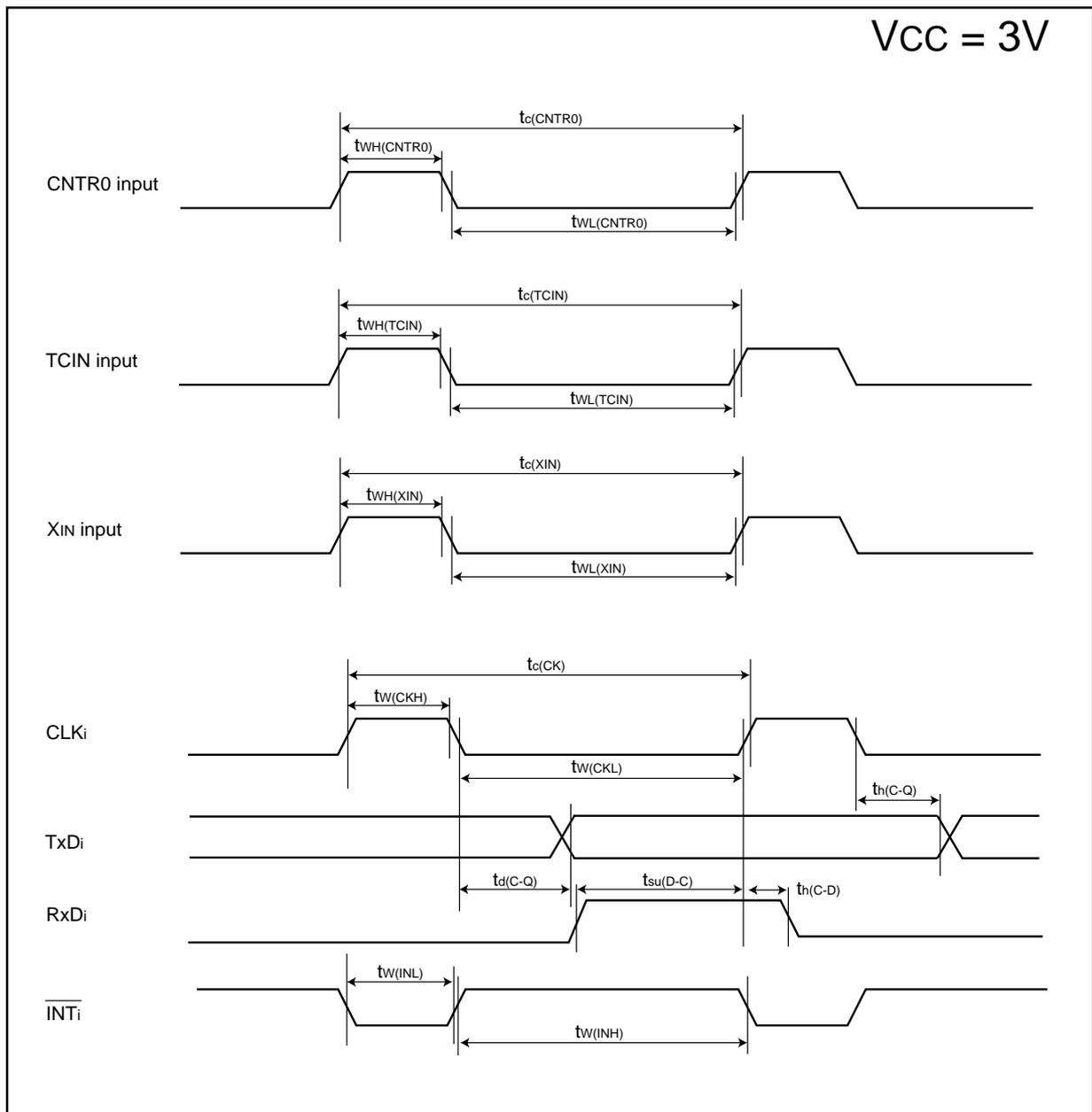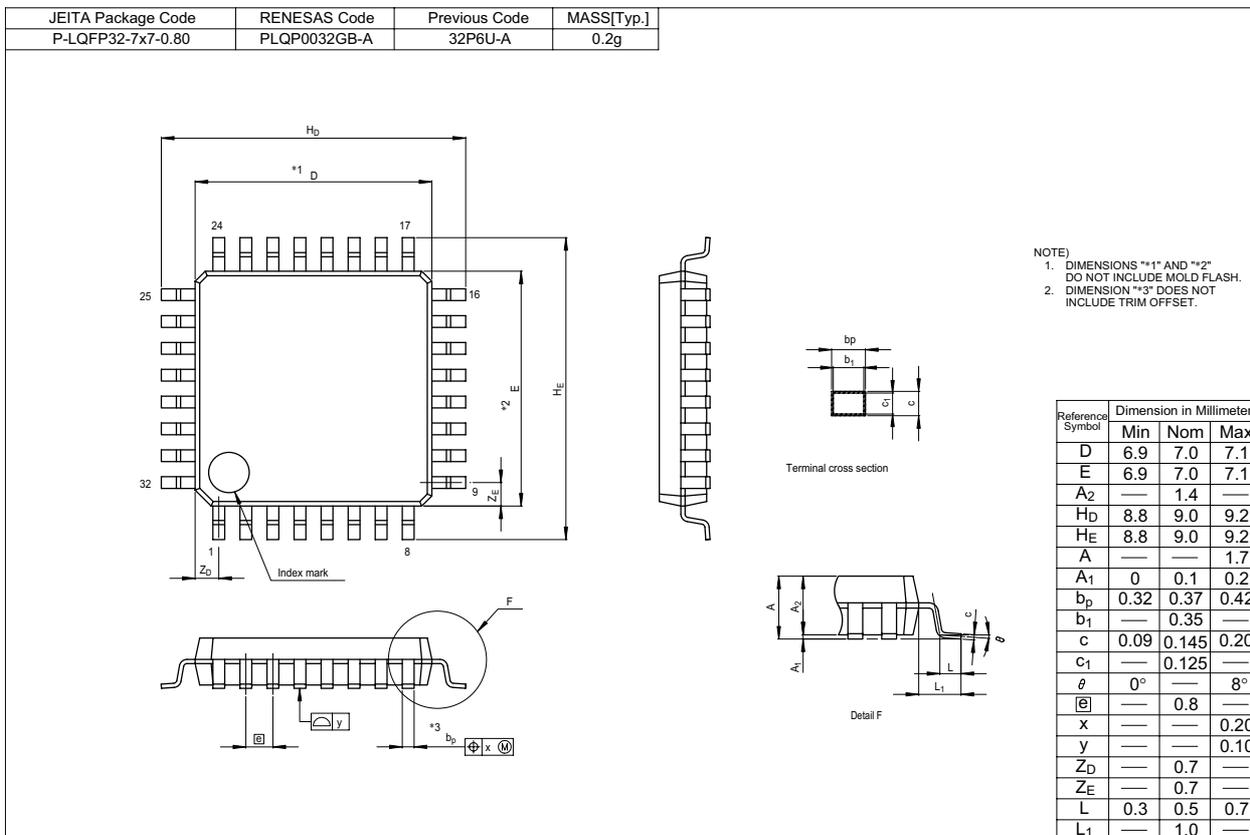2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

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Figure 5.4 Vcc=3V timing diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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REVISION HISTORY		R8C/10 Group Datasheet	

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 12 14	Table 1.1: Shortest instruction execution time and f(X_{IN}) changed Figure 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR0}$ Table 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR0}$ The value of Time C register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 14 15 16 18 19 20 21 22 23 24	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Table 5.2: Note 3 and Note 4 deleted t_{samp} in Table 5.3 deleted Figure 5.1 added Table 5.7: Vcc changed from "4.2 to 5.5V" to "3.3V to 5.5V", on-chip oscillator changed from "on 100kHz" to "125kHz", X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.8 to Table 5.12 added Figure 5.2 added Table 5.13: Note 1, f($BCLK$)=5 MHz changed to 10 MHz Table 5.14: on-chip oscillator changed from "on 100kHz" to "125kHz", X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.15 to Table 5.19 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.40	Sep 30, 2004	All pages 2 5 6 10-13 12 14 15 17 18 19 21 22 23	Words standardized (on-chip oscillator, serial interface, A/D) Table 1.1 revised Figure 1.3, NOTES 3 added Table 1.3 revised One body sentence in chapter 4 added ; Titles 4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised Table 5.2 revised Table 5.3 revised ; Table 5.4 revised Table 5.6 revised Table 5.7 revised Table 5.8 revised ; Table 5.12 revised Table 5.13 revised Table 5.14 revised Table 5.15 revised ; Table 5.17 revised ; Table 5.19 revised
1.50	Apr.27.2005	4 5 10	Table 1.2, Figure 1.2 package name revised Figure 1.3 package name revised Table 4.1 revised

REVISION HISTORY			R8C/10 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.50	Apr.27.2005	12	Table 4.3 revised
		15	Table 5.3 partly revised
			Table 5.4 partly added
			Table 5.5 partly revised
		17	Table 5.6 partly revised
		21	Table 5.13 partly revised
		25	Package Dimensions revised
1.60	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2
			"Product List" → "Product Informaton" revised
			Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised
			Figure 2.1 CPU register revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised
		11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3);
			0081_{16}: "Prescaler Y" → "Prescaler Y Register"
			0082_{16}: "Timer Y Secondary" → "Timer Y Secondary Register"
			0083_{16}: "Timer Y Primary" → "Timer Y Primary Register"
			0085_{16}: "Prescaler Z" → "Prescaler Z Register"
			0086_{16}: "Timer Z Secondary" → "Timer Z Secondary Register"
			0087_{16}: "Timer Z Primary" → "Timer Z Primary Register"
			$008C_{16}$: "Prescaler X" → "Prescaler X Register" revised
			NOTES:1 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		14	Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		15	Table 5.3 A/D Conversion Characteristics;
			"A/D operation clock frequency" → "A/D operating clock frequency" revised
			NOTES: 1, 2, 3, 4 revised
			Table 5.4 Flash Memory (Program ROM) Electrical Characteristics;
			"Data retention duration" → "Data hold time" revised
			"Topr" → "Ambient temperature" revised
			NOTES: 2 added
			Measuring condition of byte program time and block erase time deleted
		17	Table 5.6 Electrical Characteristics (1) [Vcc=5V];
			"P1$_0$ to P1$_7$ Except X$_{OUT}$" → "Except P1$_0$ to P1$_7$, X$_{OUT}$" revised
		18	Table 5.7 Electrical Characteristics (2) [Vcc=5V]
			NOTES: 1, 2 revised
			Measuring condition: Stop mode "Topr = 25 °C"
		21	Table 5.13 Electrical Characteristics (3) [Vcc=3V]
			"P1$_0$ to P1$_7$ Except X$_{OUT}$" → "Except P1$_0$ to P1$_7$, X$_{OUT}$" revised
		22	Table 5.14 Electrical Characteristics (4) [Vcc=3V]
			NOTES: 1, 2 revised
			Measuring condition: Stop mode "Topr = 25 °C"

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