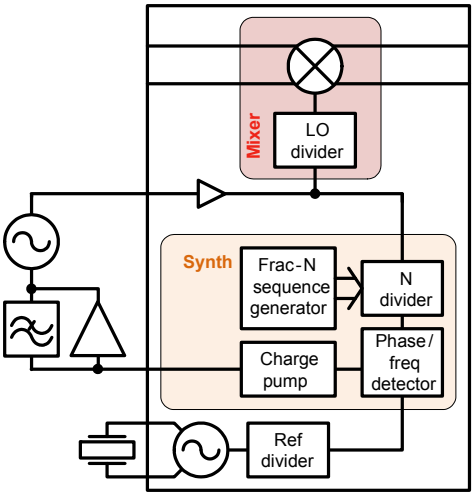
RF2053

HIGH PERFORMANCE FRACTIONAL-N SYNTHESIZER WITH INTEGRATED RF MIXER

Package: QFN, 32-Pin, 5mmx5mm



Functional Block Diagram

Features

- Fractional-N Synthesizer
- Very Fine Frequency Resolution 1.5Hz for 26MHz Reference
- 300MHz to 2400MHz External VCO Frequency Range
- On-Chip Crystal-Sustaining Circuit With Programmable Loading Capacitors
- Integrated LO Buffer and LO Divider
- High-Linearity RF Mixer
- Mixer Input IP3 +23dBm Typ.
- Mixer Bias Adjustable for Low Power Operation
- Mixer Frequency Range 30MHz to 2500MHz
- 2.7V to 3.6V Power Supply
- Low Current Consumption 50mA to 70mA at 3V
- 3-Wire Serial Interface

Applications

- CATV Head-Ends
- Digital TV Up/Down Converters
- Digital TV Repeaters
- Multi-Dwelling Units
- Frequency Band Shifters
- UHF/VHF Radios
- Software Defined Radios
- Satellite Communications
- Super-Heterodyne Radios

Product Description

The RF2053 is a low power, high performance, wideband RF frequency conversion chip with integrated local oscillator (LO) generation and RF mixer. The RF synthesizer includes an integrated fractional-N phase locked loop that can control an external VCO to produce a low-phase noise LO signal with a very fine frequency resolution. The VCO output frequency can be divided by 1, 2, or 4 in the LO divider, whose output is buffered and drives the built-in RF mixer which converts the signal into the required frequency band. The mixer bias current can be programmed dependent on the required performance and available supply current. The LO generation blocks have been designed to operate with external VCOs covering the frequency range from 300MHz to 2400MHz. The RF mixer is very broad band and operates from 30MHz to 2500MHz at the input and output, enabling both up and down conversion. An external crystal of between 10MHz and 52MHz or an external reference source of between 10MHz and 104MHz can be used with the RF2053 to accommodate a variety of reference frequency options.

All on-chip registers are controlled through a simple three-wire serial interface. The RF2053 is designed for 2.7V to 3.6V operation for compatibility with portable, battery powered devices. It is available in a plastic 32-pin, 5mmx5mm QFN package.

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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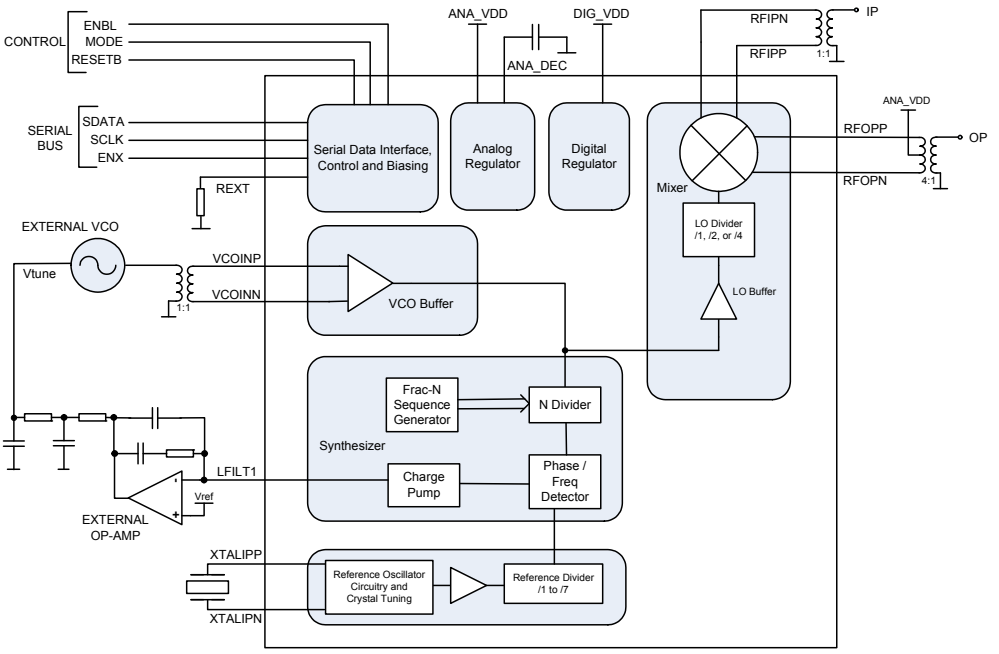
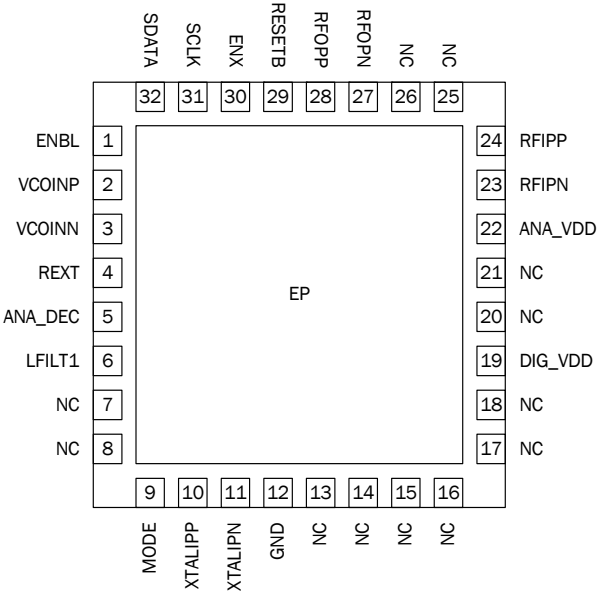
Detailed Functional Block Diagram



Pin Out



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Pin	Function	Description
1	ENBL	Ensure that the ENBL high voltage level is not greater than V_{DD}. An RC low-pass filter could be used to reduce digital noise.
2	VCOINP	External VCO differential input. See note 1.
3	VCOINN	External VCO differential input. See note 1.
4	REXT	External bandgap bias resistor. Connect a 51kΩ resistor from this pin to ground to set the bandgap reference bias current. This could be a sensitive low frequency noise injection point.
5	ANA_DEC	Analog supply decoupling capacitor. Connect to analog supply and apply RF decoupling to a good quality ground as close to the pin as possible.
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node.
7	NC	
8	NC	
9	MODE	Mode select pin. Connect to DIG_VDD if mode switching is not required.
10	XTALIPP	Reference crystal / reference oscillator input. Should be AC-coupled if an external reference is used. See note 3.
11	XTALIPN	Reference crystal / reference oscillator input. Should be AC-coupled to ground if an external reference is used. See note 3.
12	GND	Connect to ground.
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible.
20	NC	
21	NC	
22	ANA_VDD	Analog supply. Should be decoupled as close to the pin as possible.
23	RFIPN	Differential input. See note 1.
24	RFIPP	Differential input. See note 1.
25	NC	
26	NC	
27	RFOPN	Differential output. See note 2.
28	RFOPP	Differential output. See note 2.
29	RESETB	Chip reset (active low). Connect to DIG_VDD if external reset is not required.
30	ENX	Serial interface select (active low). An RC low-pass filter could be used to reduce digital noise.
31	SCLK	Serial interface clock. An RC low-pass filter could be used to reduce digital noise.
32	SDATA	Serial interface data. An RC low-pass filter could be used to reduce digital noise.
EP	Exposed pad	Connect to ground. This is the ground reference for the circuit. All decoupling should be connected here through low impedance paths.

Note 1: The signal should be connected to this pin such that DC current cannot flow into or out of the chip, either by using AC coupling capacitors or by use of a transformer (see evaluation board schematic).

Note 2: DC current needs to flow from ANA_VDD into this pin, either through an RF inductor, or transformer (see evaluation board schematic).

Note 3: Alternatively an external reference can be AC-coupled to pin 11 XTALIPN, and pin 10 XTALIPP decoupled to ground. This may make PCB routing simpler.

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +3.6	V
Input Voltage (V_{IN}), any Pin	-0.3 to V_{DD}+0.3	V
RF/IF Mixer Input Power	+15	dBm
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2011/65/EU (at time of this document revision).

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RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD Requirements					
Human Body Model					
General	2000			V	
RF Pins	1000			V	
Machine Model					
General	200			V	
RF Pins	100			V	
Operating Conditions					
Supply Voltage (V_{DD})	2.7	3.0	3.6	V	
Temperature (T_{OP})	-40		+85	°C	
Logic Inputs/Outputs					V_{DD}=Supply to DIG_VDD pin
Input Low Voltage	-0.3		+0.5	V	
Input High Voltage	V_{DD} / 1.5		V_{DD}	V	
Input Low Current	-10		+10	uA	Input=0V
Input High Current	-10		+10	uA	Input=V_{DD}
Output Low Voltage	0		0.2*V_{DD}	V	
Output High Voltage	0.8*V_{DD}		V_{DD}	V	
Load Resistance	10			kΩ	
Load Capacitance			20	pF	
Static					
Programmable Supply Current (I_{DD})					
Low Current Setting		50		mA	
High Linearity Setting		70		mA	
Standby		3		mA	Reference oscillator and bandgap only.
Power Down Current		140		µA	ENBL=0 and REF_STBY=0
Mixer					Mixer output driving 4:1 balun.
Gain		-2		dB	Not including balun losses.
Noise Figure					
Low Current Setting		9.5		dB	
High Linearity Setting		12		dB	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Mixer, cont.					
IIP3					
Low Current Setting		+12		dBm	
High Linearity Setting		+23		dBm	
Pin1dB					
Low Current Setting		+2		dBm	
High Linearity Setting		+12		dBm	
RF and IF Port Frequency Range	30		2500	MHz	
Mixer Input Return Loss		10		dB	100Ω differential
Voltage Controlled Oscillator Differential Input					
External VCO Input Frequency	300		2400	MHz	
External VCO Input Level	-6	-3	0	dBm	
Reference Oscillator					
Xtal Frequency	10		52	MHz	
External Reference Frequency	10		104	MHz	
Reference Divider Ratio	1		7		
External Reference Input Level	500	800	1500	mV_{P-P}	AC-coupled
Local Oscillator					
Synthesizer Output Frequency	75		2400	MHz	At LO divider output
Phase Detector Frequency			52	MHz	
Closed Loop Phase-Noise at 1kHz Offset					26MHz phase detector frequency
2GHz LO Frequency		-85		dBc/Hz	
1GHz LO Frequency		-91		dBc/Hz	
500MHz LO Frequency		-97		dBc/Hz	
Closed Loop Phase-Noise at 10kHz Offset					26MHz phase detector frequency
2GHz LO Frequency		-90		dBc/Hz	
1GHz LO Frequency		-95		dBc/Hz	
500MHz LO Frequency		-102		dBc/Hz	
Charge Pump					
Charge Pump Current		120	240	μA	
Charge Pump Output Voltage	+0.7	+1.1	+1.5	V	

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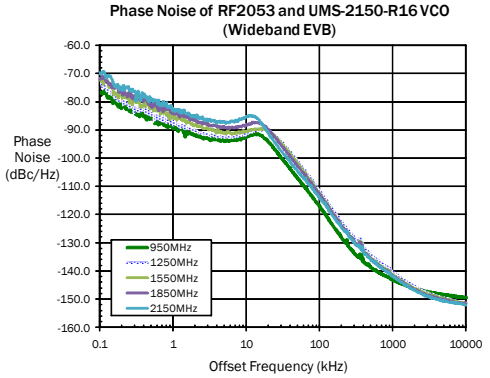
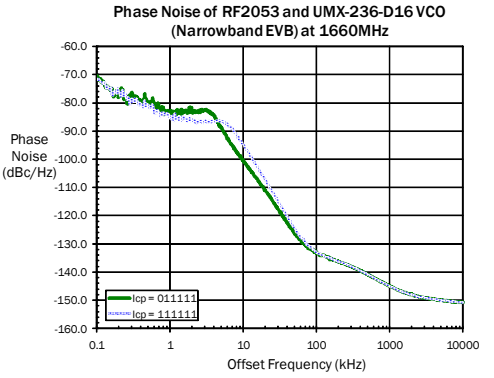
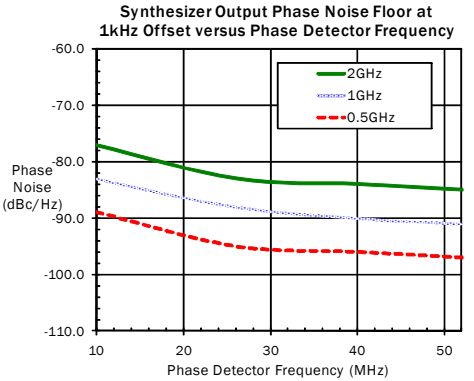
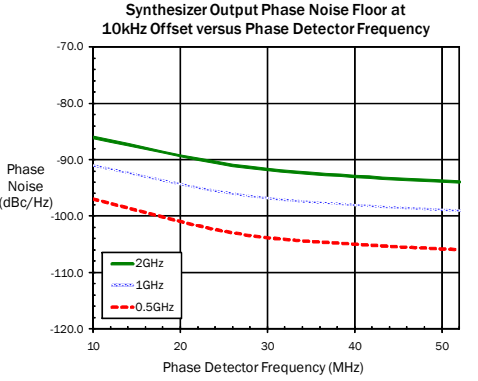
Typical Performance Characteristics for the RF2053 synthesizer

V_{DD}=3V, T_A=25°C, as measured on RF2053 evaluation board, Phase Detector Frequency=26MHz.

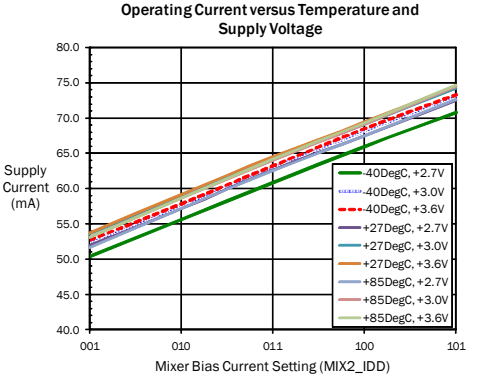








Typical Performance Characteristics for the RF2053



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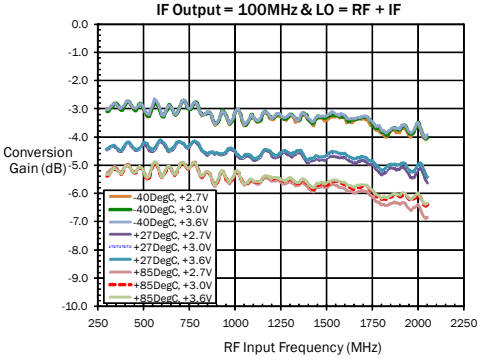
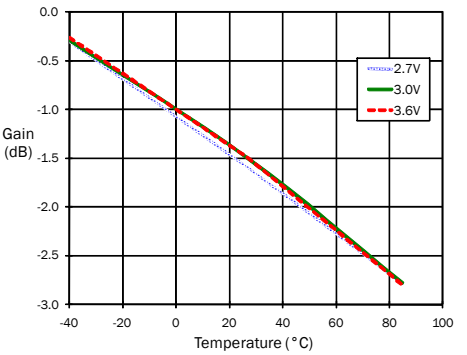
Typical Performance Characteristics for the RF2053 mixer

V_{DD}=3V, T_A=25°C, unless stated, as measured on RF2053 wideband evaluation board, Phase Detector Frequency=26MHz.

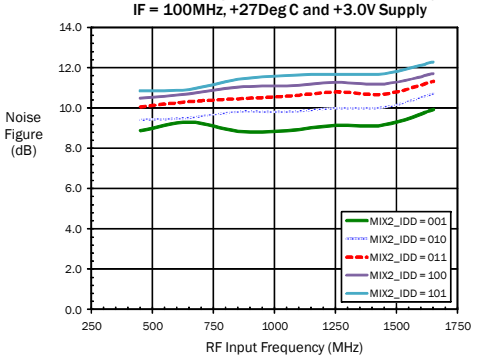
RF2053 Mixer Conversion Gain
IF Output = 100MHz & LO = RF + IF



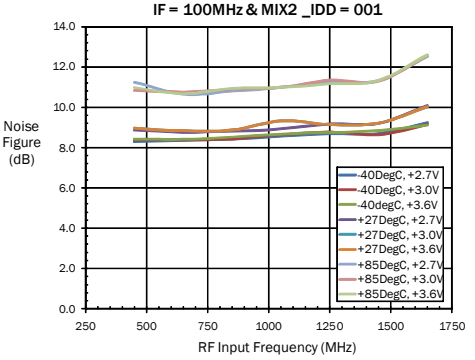
Gain versus Temperature and Supply Voltage
(Excluding losses in PCB and Baluns)



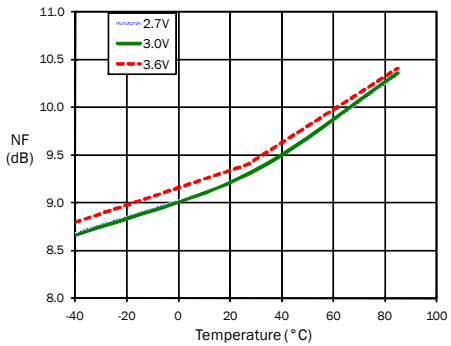
Mixer Noise Figure versus RF Input Frequency
IF = 100MHz, +27Deg C and +3.0V Supply



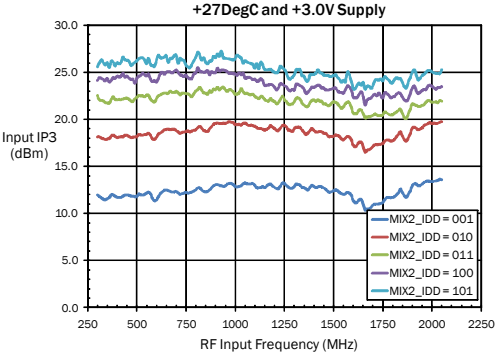
Mixer Noise Figure versus Temperature & Voltage
IF = 100MHz & MIX2 _IDD = 001



NF versus Temperature and Supply Voltage
(Low Noise Mode MIX2_IDD=001)



Mixer Input IP3 versus RF Input Frequency
IF = 100MHz & LO = RF - IF
+27DegC and +3.0V Supply



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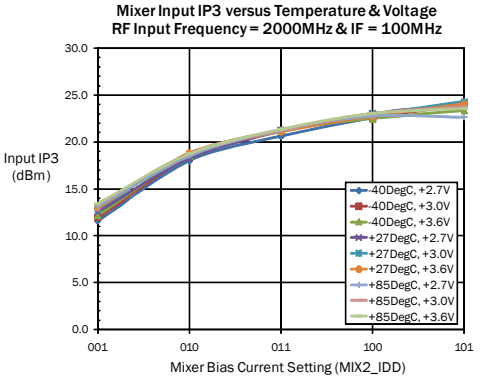
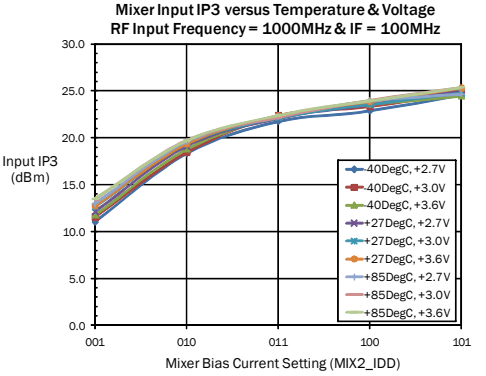
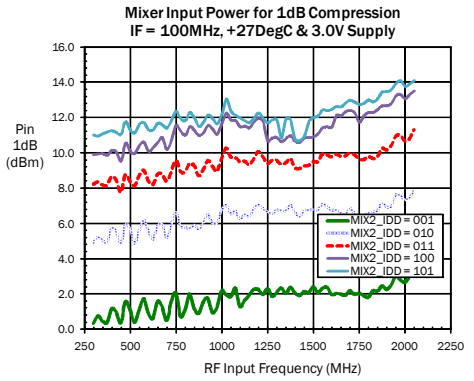
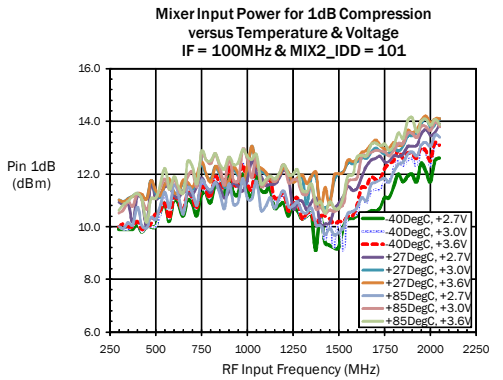
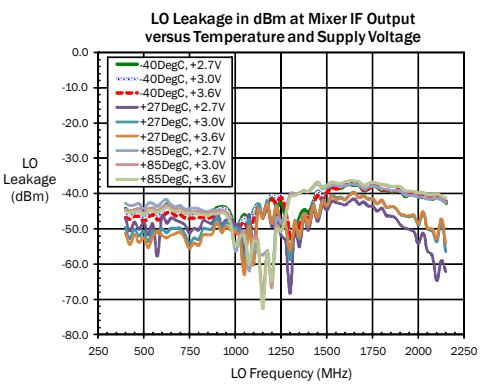
Typical Performance Characteristics for the RF2053 mixer
V_{DD}=3V, T_A=25°C, unless stated, as measured on RF2053 wideband evaluation board, Phase Detector Frequency=26MHz

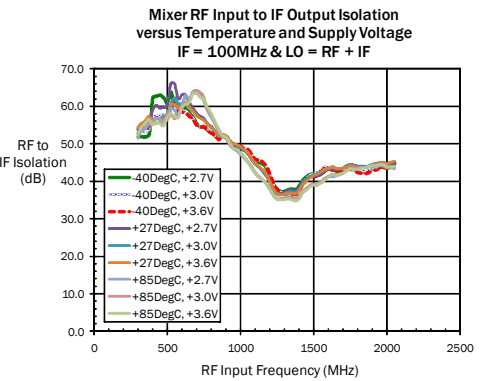












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Detailed Description

The RF2053 is a wideband RF frequency converter chip which includes a fractional-N phase-locked loop, a crystal oscillator circuit, an LO buffer, and an RF mixer. The PLL operates with an external VCO. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. All on-chip registers are programmed through a simple three-wire serial interface.

VCO

The RF2053 has been designed for use with an external VCO. The VCO inputs on pins 2 and 3 are differential.

In order to route the VCO input through buffers to the PLL divide circuits then CFG1:EXT_VCO must be set high and the VCO control word must be set to VCO3, PLL2x0:P2_VCOSEL=10.

The course tuning calibration (CT_CAL) which is not used by the RF2053 should be disabled in order to minimize the PLL lock time. The VCO signal can be divided by 1, 2, or 4 in the LO divider circuit. The LO divide ratio is set by the PLL2x0:P2_LODIV control words.

For applications where the required LO frequency is above 2GHz it is recommended that the LO buffer current be increased by setting CFG5:LO2_I to 1100 (hex value C).

Fractional-N PLL

The IC contains a charge-pump based fractional-N phase locked loop (PLL) for controlling the external VCO. The PLL is intended to use a reference frequency signal of 10MHz to 104MHz. A reference divider (divide by 1 to divide by 7) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz. The reference divider bypass is controlled by bit CLK_DIV_BYP, set low to enable the reference divider and set high for divider bypass (divide by 1). The remaining three bits CLK_DIV<15:13> set the reference divider value, divide by 2 (010) to 7 (111) when the reference divider is enabled.

Two PLL programming banks are provided, the first bank is preceded by the label PLL1 and the second bank is preceded by the label PLL2. For the RF2053 the default programming bank is PLL2, selected by setting the MODE pin high.

The PLL will lock the VCO to the frequency F_{VCO} according to:

$$F_{VCO} = N_{EFF} * F_{OSC} / R$$

where N_{EFF} is the programmed fractional N divider value, F_{OSC} is the reference input frequency, and R is the programmed R divider value (1 to 7).

The N divider is a fractional divider, containing a dual-modulus prescaler and a digitally spur-compensated fractional sequence generator to allow fine frequency steps. The N divider is programmed using the N and NUM bits as follows:

First determine the desired, effective N divider value, N_{EFF}:

$$N_{EFF} = F_{VCO} * R / F_{OSC}$$

N(9:0) should be set to the integer part of N_{EFF}. NUM should be set to the fractional part of N_{EFF} multiplied by $2^{24}=16777216$.

Example: VCO operating at 2220MHz, 23.92MHz reference frequency, the desired effective divider value is:

$$N_{EFF} = F_{VCO} * R / F_{OSC} = 2220 * 1 / 23.92 = 92.80936454895.$$

The N value is set to 92, equal to the integer part of N_{EFF}, and the NUM value is set to the fractional portion of N_{EFF} multiplied by 2^{24}:

$$NUM = 0.80936454895 * 2^{24} = 13{,}578{,}884.$$

Converting N and NUM into binary results in the following:

N=0 0101 1100
NUM=1100 1111 0011 0010 1000 0100

So the registers would be programmed:

P2_N=0 0101 1100
P2_NUM_MSB=1100 1111 0011 0010
P2_NUM_LSB=1000 0100

The maximum N_{EFF} is 511, and the minimum N_{EFF} is 15, when in fractional mode. The minimum step size is $F_{OSC}/R*2^{24}$. Thus for a 23.92MHz reference, the frequency step size would be 1.4Hz. The minimum reference frequency that can be used is simply the maximum VCO frequency required divided by 511. For example for a VCO frequency of 2400MHz, the minimum reference frequency, is 2400/511, 4.697MHz (approx).

Phase Detector and Charge Pump

The chip provides a current output to drive an external loop filter. An external low noise operational amplifier can be used to design an active loop filter or a passive design can be implemented. This depends on the tuning range of the external VCO. The maximum charge pump output current is set by the value contained in the P2_CP_DEF field and CP_LO_I.

In the default state (P2_CP_DEF=31 and CP_LO_I=0) the charge pump current (ICPset) is 120uA. If CP_LO_I is set to 1 this current is reduced to 30uA. Note that lowest phase noise within the loop bandwidth is achieved with the maximum charge pump current.

The charge pump current can be altered by changing the value of P2_CP_DEF. The charge pump current is defined as:

ICP= ICPset*CP_DEF / 31

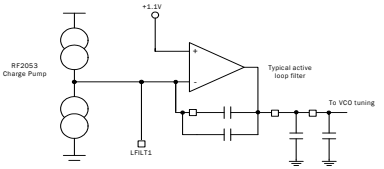
Changing the charge pump current will vary the loop filter response, higher current corresponding to a wider loop bandwidth.

The phase detector will operate with a maximum input frequency of 52MHz.

The loop filter calibration (KV_CAL) is not used by the RF2053 and is disabled by default.

Loop Filter

The PLL may be designed to use an active or a passive loop filter as required. The active loop filter uses an external low noise op-amp. The CFG1:LF_ACT bit is set low in both cases so that the internal op-amp is disabled and a high impedance is presented to the LFILT1 pin. The RF205x Programming Tool software can assist with loop filter designs. Because the op-amp is used in an inverting configuration in active mode, when the passive loop filter mode is selected the phase-detector polarity should be inverted. For active mode, CFG1:PDP=1, for passive mode, CFG1:PDP=0.



The charge pump output voltage compliance range is typically +0.7V to +1.5V. For applications using a passive loop filter the required VCO tuning voltage must fall within this voltage range under all conditions. When using an external op-amp as an integrator for the loop filter, as shown above, the non-inverting terminal should be referenced to +1.1V. This holds the charge pump output at this voltage in the center of its compliance range. The op-amp power supplies must be adequate to provide the necessary VCO tuning voltage.

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Crystal Oscillator

The PLL may be used with an external reference source, or its own crystal oscillator. If an external source (such as a TCXO) is being used it should be AC-coupled into one of the XO inputs, and the other input should be AC-coupled to ground.

A crystal oscillator typically takes many milliseconds to settle, and so for applications requiring rapid pulsed operation of the PLL (such as a TDMA system, or Rx/Tx half-duplex system) it is necessary to keep the XO running between bursts. However, when the PLL is used less frequently, it is desirable to turn off the XO to minimize current draw. The REFSTBY register is provided to allow for either mode of operation. If REFSTBY is programmed high, the XO will continue to run even when ENBL is asserted low. Thus the XO will be stable and a clock is immediately available when ENBL is asserted high, allowing the chip to assume normal operation. On cold start, or if REFSTBY is programmed low, the XO will need a warm-up period before it can provide a stable clock. The length of this warm-up period will be dependant on the crystal characteristics.

The crystal oscillator circuit contains internal loading capacitors. No external loading capacitors are required, dependant on the crystal loading specification. The internal loading capacitors are a combination of fixed capacitance, and an array of switched capacitors. The switched capacitors can be used to tune the crystal oscillator onto the required center frequency and minimize frequency error. The PCB stray capacitance and oscillator input and output capacitance will also contribute to the crystal's total load capacitance. The register settings in the CFG4 register for the switched capacitors are as follows:

- Coarse Tune XO_CT (4 bits) 15 * 0.55pF, default 0100
- Fine Step XO_CR_S (1 bit) 1 * 0.25pF, default 0

The on chip fixed capacitance is approximately 4.2pF.

Wideband Mixer

The RF2053 includes a wideband, double-balanced Gilbert cell mixer. It supports RF/IF frequencies of 30MHz to 2500MHz. The mixer has an input port and an output port that can be used for either IF or RF, i.e. for up conversion or down conversion. The mixer current can be programmed to between 15mA and 35mA depending on linearity requirements, using the MIX-2_IDD<3:0> word in the CFG2 register. The majority of the mixer current is sourced through the output pins via either a centre-tapped balun or an RF choke in the external matching circuitry to the supply.

The RF mixer input and output ports are differential and require simple matching circuits optimized to the specific application frequencies. A conversion gain of approximately -3dB to 0dB is achieved with 100Ω differential input impedance, and the outputs driving 200Ω differential load impedance. Increasing the mixer output load increases the conversion gain.

The mixer has a broadband common gate input. The input impedance is dominated by the resistance set by the mixer 1/gm term, which is inversely proportional to the mixer current setting. The resistance will be approximately 85Ω at the default mixer current setting (100). There is also some shunt capacitance at the mixer input, and the inductance of the bond wires to consider at higher frequencies.

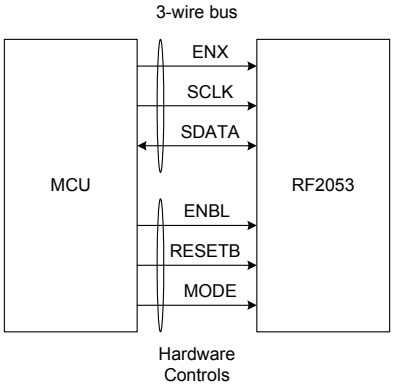
The mixer output is high impedance, consisting of a resistance of approximately 2kΩ in parallel with some capacitance. The mixer output does not need to be matched as such, just to see a resistive load. A higher resistance load will give higher output voltage and gain. A shunt inductor can be used to resonate with the mixer output capacitance at the frequency of interest. This inductor may not be required at lower frequencies where the impedance of the output capacitance is less significant. At higher output frequencies the inductance of the bond wires becomes more significant.

For more information about the mixer port impedances and matching, please refer to the RF205x Family Application Note on Matching Circuits and Baluns.

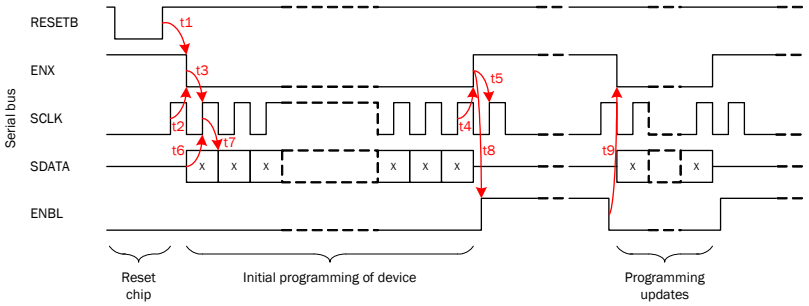
General Programming Information

Serial Interface

All on-chip registers in the RF2053 are programmed using a 3-wire serial bus which supports both write and read operations. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. Certain functions and operations require the use of hardware controls via the ENBL, MODE, and RESETB pins in addition to programming via the serial bus. For most applications the MODE pin can be held high.



Serial Data Timing Characteristics



Parameter	Description	Time
t1	Reset delay	>5ns
t2	Programming setup time	>5ns
t3	Programming hold time	>5ns
t4	ENX setup time	>5ns
t5	ENX hold time	>5ns
t6	Data setup time	>5ns
t7	Data hold time	>5ns
t8	ENBL setup time	>0ns
t9	ENBL hold time	>0ns

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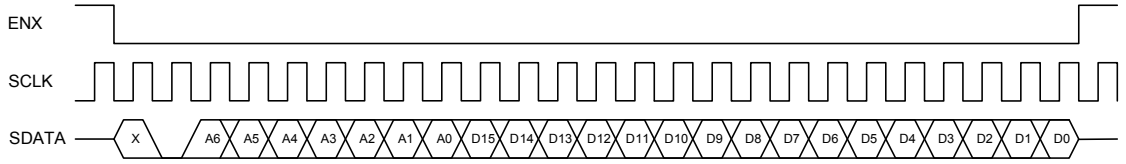
Write



Initially ENX is high and SDATA is high impedance. The write operation begins with the controller starting SCLK. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In write mode the baseband will drive SDATA for the entire telegram. RF2053 will read the data bit on the rising edge of SCLK.

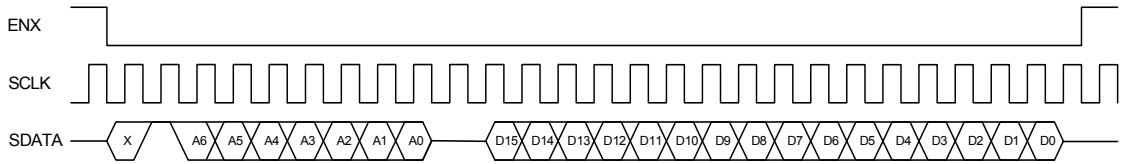
The next 7 data bits are the register address, MSB first. This is followed by the payload of 16 data bits for a total write mode transfer of 24 bits. Data is latched into RF2053 on the last rising edge of SCLK (after ENX is asserted high).

For more information, please refer to the timing diagram on page 12.

The maximum clock speed for a register write is 19.2MHz. A register write therefore takes approximately 1.3us. The data is latched on the rising edge of the clock. The datagram consists of a single start bit followed by a '0' (to indicate a write operation). This is then followed by a seven bit address and a sixteen bit data word.

Note that since the serial bus does not require the presence of the crystal clock, it is necessary to insert an additional rising clock edge before the ENX line is set low to ensure the address/data are read correctly.

Read



Initially ENX is high and SDATA is high impedance. The read operation begins with the controller starting SCLK. The controller is in control of the SDATA line during the address write operation. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In read mode the baseband will drive SDATA for the address portion of the telegram, and then control will be handed over to RF2053 for the data portion. RF2053 will read the data bits of the address on the rising edge of SCLK. After the address has been written, control of the SDATA line is handed over to RF2053. One and a half clocks are reserved for turn-around, and then the data bits are presented by RF2053. The data is set up on the rising edge of SCLK, and the controller latches the data on the falling edge of SCLK. At the end of the data transmission, RF2053 will release control of the SDATA line, and the controller asserts ENX high. The SDATA port on RF2053 transitions from high impedance to low impedance on the first rising edge of the data portion of the transaction (for example, 3 rising edges after the last address bit has been read), so the controller chip should be presenting a high impedance by that time.

For more information, please refer to the timing diagram on page 12.

The maximum clock speed for a register read is 19.2MHz. A register read therefore takes approximately 1.4us. The address is latched on the rising edge of the clock and the data output on the falling edge. The datagram consists of a single start bit fol-

lowed by a '1' (to indicate a read operation), followed by a seven bit address. A 1.5 bit delay is introduced before the sixteen bit data word representing the register content is presented to the receiver.

Note that since the serial bus does not require the presence of the crystal clock, it is necessary to insert an additional rising clock edge before the ENX line is set low to ensure the address is read correctly.

Hardware Control

Three hardware control pins are provided: ENBL, MODE, and RESETB.

ENBL Pin

The ENBL pin has two functions: to enable the analog circuits in the chip and to trigger the PLL to lock.

ENBL Pin	REFSTBY Bit	XO and Bias Block	Analogue Block	Digital Block
Low	0	Off	Off	On
Low	1	On	Off	On
High	0	On	On	On
High	1	On	On	On

Every time the frequency of the synthesizer is re-programmed, ENBL has to be taken high to initiate PLL locking.

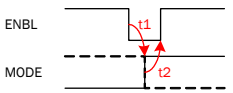
RESETB Pin

The RESETB pin is a hardware reset control that will reset all digital circuits to their start-up state when asserted low. The device includes a power-on-reset function, so this pin should not normally be required, in which case it should be connected to the positive supply.

MODE Pin

The MODE pin controls which PLL programming register bank is active.

For normal operation of the RF2053 the MODE pin should be set high to select the default PLL2 programming registers. It is possible to set the FULLD bit in the CFG1 register high. This allows the MODE pin to select either PLL1 register bank (MODE=low) or PLL2 register bank (MODE=high). This may be useful for some applications where two LO frequencies can be programmed into the registers then the MODE pin used to toggle between them. The ENBL pin will also need to be cycled to re-lock the synthesizer for each frequency.



Parameter	Description	Time
t1	MODE setup time	>5ns
t2	MODE hold time	>5ns

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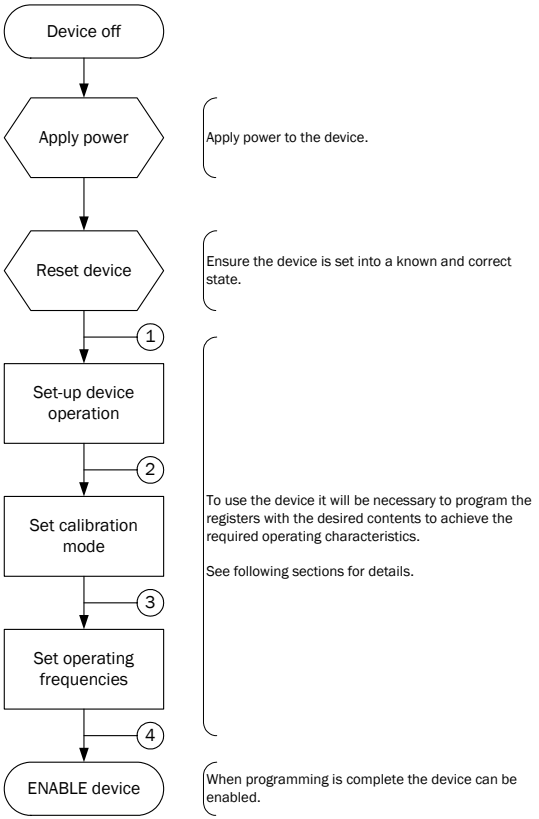
Programming the RF2053

The figure below shows an overview of the device programming.



Note: The set-up processes 1 to 2, 2 to 3, and 3 to 4 are explained further below.

Additional information on device use and programming can be found on the RF205x family page of the RFMD web site (http://www.rfmd.com/rf205x). The following documents may be particularly helpful:

- RF205x Frequency Synthesizer User Guide
- RF205x Calibration User Guide

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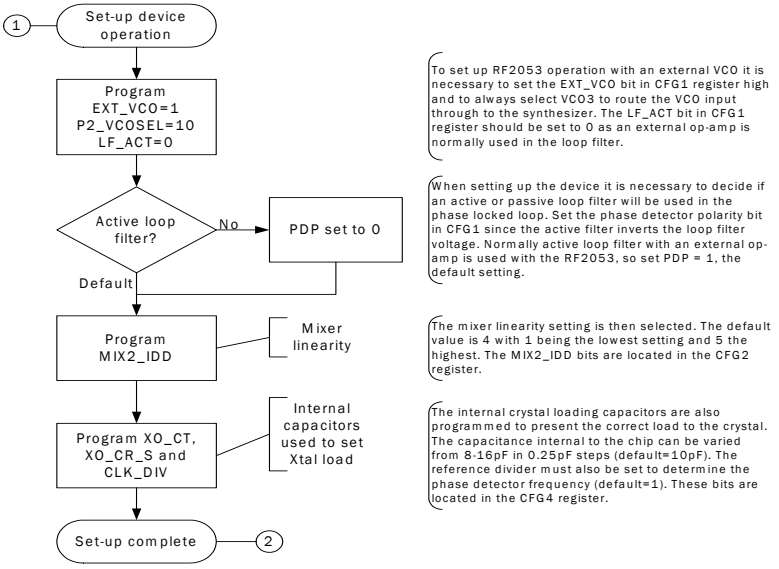
Start-up

When starting up and following device reset then REFSTBY=0, REFSTBY should be asserted high approximately 500ecs. before ENBL is taken high. This is to allow the XO to settle and will depend on XO characteristics. After taking ENBL high there is typically 20usecs for the PLL state machine and charge pump to initialize, the VCO warm-up state, before PLL locking starts. The time spent in the VCO warm-up state is set by CFG1:TVCO, which should be set to 00111 when using a 26MHz clock. Following the warm-up period there will be the additional time taken for the PLL to settle to the required frequency. All of these timings will be dependent upon application specific factors such as loop filter bandwidth, reference clock frequency, and XO characteristics. The fastest turn-on and lock time will be obtained by leaving REFSTBY asserted high, disabling all calibration routines (always the case for the RF2053), minimizing the VCO warm-up time, and setting the PLL loop bandwidth as wide as possible.

The device can be reset into its initial state (default settings) at any time by performing a hard reset. This is achieved by setting the RESETB pin low for at least 100ns.

Setting Up Device Operation

The device offers a number of operating modes which need to be set up in the device before it will work as intended. This is achieved as follows.



Three registers need to be written, taking 3.9us at the maximum clock speed.

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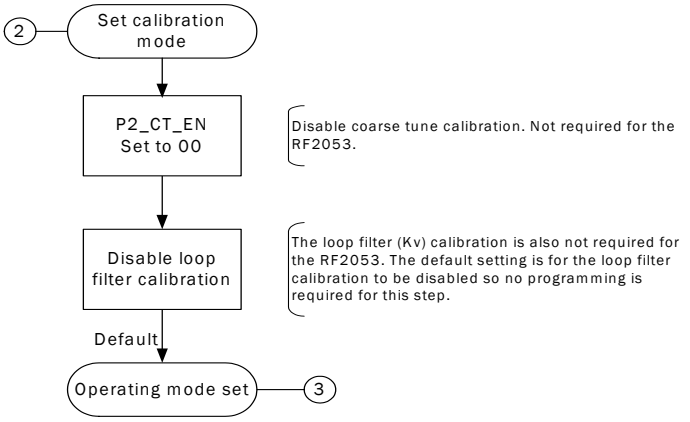
Disabling Calibration

The VCO coarse tune calibration should be disabled as it is not used on the RF5203. The loop filter calibration, also unused, is disabled by default.



One register needs to be written taking 1.3us at maximum clock speed. Since it is necessary to program this register when setting the operating frequency (see next section) this operation usually carries no overhead.

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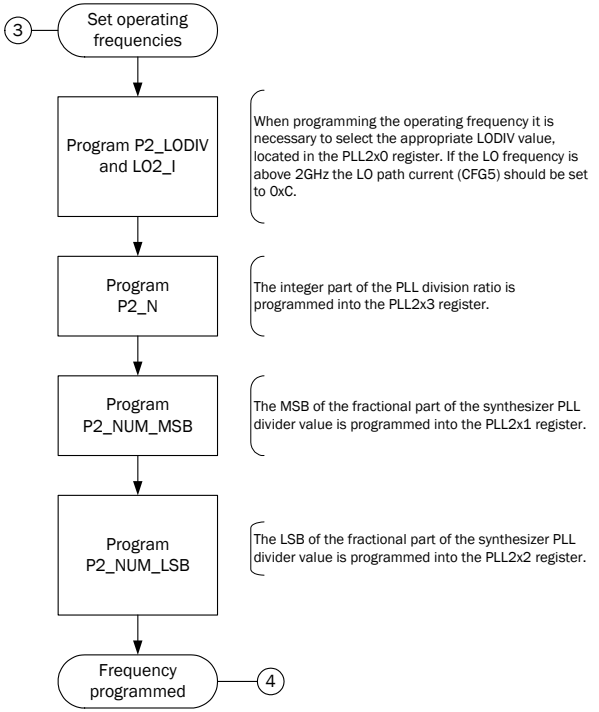
Setting The Operating Frequency

Setting the operating frequency of the device requires a number of registers to be programmed.



A total of four registers must be programmed to set the device operating frequency. This will take 5.2us for each path at maximum clock speed.

To change the frequency of the VCO it will be necessary to repeat these operations. However, if the frequency shift is small it may not be necessary to reprogram all the bits reducing the number of register writes to three.

For an example on how to determine the integer and fractional parts of the synthesizer PLL division ratio please refer to the detailed description of the PLL on page 9.

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Programming Registers

Register Map Diagram

Reg. Name	R/W	Add	Data														
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG1	R/W	00	LD_EN	LD_LEV	TVCO					PDP	LF_ACT	CPL		CT_POL	Res	EXT_VCO	FULLD	CP_LO_I
CFG2	R/W	01	MIX1_IDD			MIX1_VB	MIX2_IDD				MIX2_VB	Res		KV_RNG	NBR_CT_AVG		NBR_KV_AVG	
CFG3	R/W	02	TKV1				TKV2				Res				FLL_FACT		CT_CPOL	REFSTBY
CFG4	R/W	03	CLK_DIV_BYPASS				XO_CT				XO_I2	XO_I1	XO_CR_S	TCT				
CFG5	R/W	04	LO1_I				LO2_I				T_PH_ALGN							
CFG6	R/W	05	SU_WAIT										Res					
PLL1x0	R/W	08	P1_VCOSEL		P1_CT_EN		P1_KV_EN		P1_LO-DIV		Res		P1_CP_DEF					
PLL1x1	R/W	09	P1_NUM_MSB															
PLL1x2	R/W	0A	P1_NUM_LSB								P1_CT_DEF							Res
PLL1x3	R/W	0B	P1_N									Res			P1_VCOI			
PLL1x4	R/W	0C	P1_DN									P1_CT_GAIN			P1_KV_GAIN			Res
PLL1x5	R/W	0D	P1_N_PHS_ADJ									Res		P1_CT_V				
PLL2x0	R/W	10	P2_VCOSEL		P2_CT_EN		P2_KV__EN		P2_LO-DIV		Res		P2_CP_DEF					
PLL2x1	R/W	11	P2_NUM_MSB															
PLL2x2	R/W	12	P2_NUM_LSB								P2_CT_DEF							Res
PLL2x3	R/W	13	P2_N									Res			P2_VCOI			
PLL2x4	R/W	14	P2_DN									P2_CT_GAIN			P2_KV_GAIN			Res
PLL2x5	R/W	15	P2_N_PHS_ADJ									Res		P2_CT_V				
GPO	R/W	18	Res	P1_G-PO1	Res	P1_GPO3	P1_GPO4	Res			P2_G-PO1	Res	P2_G-PO3	P2_GPO4	Res			
CHIPREV	R	19	PARTNO								REVNO							
RB1	R	1C	LOCK	CT_CAL							CP_CAL						Res	
RB2	R	1D	VO_CAL								V1_CAL							
RB3	R	1E	RSM_STATE						Res									
TEST	R	1F	TEN	TMUX			CPU	CPD	FNZ	LDO_BYP	TSEL	Res	DACTEST		Res			

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CFG1 (00h) - Operational Configuration Parameters

#	Bit Name	Default		Function
15	LD_EN	1	9	Enable lock detector circuitry
14	LD_LEV	0		Modify lock range for lock detector
13	TVCO(4:0)	0		VCO warm-up time=TVCO/(F_{REF}*256)
12		0		
11		0	1	
10		0		
9		0		
8	PDP	1		Phase detector polarity: 0=positive, 1=negative
7	LF_ACT	1	C	Active loop filter enable, 1=Active 0=Passive
6	CPL(1:0)	1		Charge pump leakage current: 00=no leakage, 01=low leakage, 10=mid leakage, 11=high leakage
5		0		
4	CT_POL	0		Polarity of VCO coarse-tune word: 0=positive, 1=negative
3		0	0	
2	EXT_VCO	0		Set to 1=external VCO (VCO3 disabled, KV_CAL and CT_CAL must be disabled)
1	FULLD	0		0=Half duplex, mixer is enabled according to MODE pin, 1=Full duplex, both mixers enabled. For RF2053 setting FULLD high gives access to both PLL register banks using MODE pin.
0	CP_LO_I	0		0=High charge pump current, 1=low charge pump current

CFG2 (01h) - Mixer Bias and PLL Calibration

#	Bit Name	Default		Function
15	MIX1_IDD	1	8	This register is not used for the RF2053.
14		0		
13		0		
12	MIX1_VB	0		This register is not used for the RF2053.
11		1	C	
10	MIX2_IDD	1		Mixer 2 current setting: 000=0mA to 111=35mA in 5mA steps
9		0		
8		0		
7	MIX2_VB	0	5	Mixer 2 voltage bias
6		1		
5		0		
4	KV_RNG	1		Sets accuracy of voltage measurement during KV calibration: 0=8bits, 1=9bits
3	NBR_CT_AVG	1	8	Number of averages during CT cal
2		0		
1	NBR_KV_AVG	0		Number of averages during KV cal
0		0		

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CFG3 (02h) - PLL Calibration

#	Bit Name	Default		Function
15	TKV1	0	0	Settling time for first measurement in LO KV compensation
14		0		
13		0		
12		0		
11	TKV2	0	4	Settling time for second measurement in LO KV compensation
10		1		
9		0		
8		0		
7		0	0	
6		0		
5		0		
4		0		
3	FLL_FACT	0	4	Default setting 01. Needs to be set to 00 for N<28. This case can arise when higher phase detector frequencies are used.
2		1		
1	CT_CPOL	0		
0	REFSTBY	0		Reference oscillator standby mode 0=XO is off in standby mode, 1=XO is on in standby mode

CFG4 (03h) - Crystal Oscillator and Reference Divider

#	Bit Name	Default		Function
15	CLK_DIV	0	1	Reference divider, divide by 2 (010) to 7 (111) when reference divider is enabled
14		0		
13		0		
12	CLK_DIV_BYPASS	1		Reference divider enabled=0, divider bypass (divide by 1)=1
11	XO_CT	1	8	Crystal oscillator coarse tune (approximately 0.5pF steps from 8pF to 16pF)
10		0		
9		0		
8		0		
7	XO_I2	0	0	Crystal oscillator current setting
6	XO_I1	0		
5	XO_CR_S	0		Crystal oscillator additional fixed capacitance (approximately 0.25pF)
4	TCT	0		Duration of coarse tune acquisition
3		1	F	
2		1		
1		1		
0		1		

CFG5 (04h) - LO Bias

#	Bit Name	Default		Function
15	LO1_I	0	0	Local oscillator Path1 current setting
14		0		
13		0		
12		0		
11	LO2_I	0	0	Local oscillator Path2 current setting
10		0		
9		0		
8		0		
7	T_PH_ALGN	0	0	Phase alignment timer
6		0		
5		0		
4		0		
3		0	4	
2		1		
1		0		
0		0		

CFG6 (05h) - Start-up Timer

#	Bit Name	Default		Function
15	SU_WAIT	0	0	Crystal oscillator settling timer.
14		0		
13		0		
12		0		
11		0	1	
10		0		
9		0		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	0	
2		0		
1		0		
0		0		

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PLL1x0 (08h) - VCO, LO Divider and Calibration Select

#	Bit Name	Default		Function
15	P1_VCOSEL	0	7	Path 1 VCO band select: 00=VCO1, 01=VCO2, 10=VCO3, 11=Reserved Always set to 10 for VCO3.
14		1		
13	P1_CT_EN	1		Path 1 VCO coarse tune: 00=disabled, 11=enabled Set to 00 to disable VCO coarse tune.
12		1		
11	P1_KV_EN	0	1	Path 1 VCO tuning gain calibration: 00=disabled, 11=enabled Set to 00 to disable calibration.
10		0		
9	P1_LODIV	0		Path 1 local oscillator divider: 00=divide by 1, 01=divide by 2, 10=divide by 4, 11=reserved
8		1		
7		0	1	
6		0		
5	P1_CP_DEF	0		Charge pump current setting If P1_KV_EN=11 this value sets charge pump current during KV compensation only
4		1		
3		1	F	
2		1		
1		1		
0		1		

PLL1x1 (09h) - MSB of Fractional Divider Ratio

#	Bit Name	Default		Function
15	P1_NUM_MSB	0	6	Path 1 VCO divider numerator value, most significant 16 bits
14		1		
13		1		
12		0		
11		0	2	
10		0		
9		1		
8		0		
7		0	7	
6		1		
5		1		
4		1		
3		0	6	
2		1		
1		1		
0		0		

PLL1x2 (0Ah) - LSB of Fractional Divider Ratio and CT Default

#	Bit Name	Default		Function
15	P1_NUM_LSB	0	2	Path 1 VCO divider numerator value, least significant 8 bits
14		0		
13		1		
12		0		
11		0	7	
10		1		
9		1		
8		1		
7	P1_CT_DEF	0	7	Path 1 VCO coarse tuning value, not required for RF2053.
6		1		
5		1		
4		1		
3		1	E	
2		1		
1		1		
0		0		

PLL1x3 (0Bh) - Integer Divider Ratio and VCO Current

#	Bit Name	Default		Function
15	P1_N	0	2	Path 1 VCO divider integer value
14		0		
13		1		
12		0		
11		0	3	
10		0		
9		1		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	2	
2	P1_VCOI	0		Path 1 VCO bias setting: 000=minimum value, 111=maximum value
1		1		
0		0		

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PLL1x4 (0Ch) - Calibration Settings

#	Bit Name	Default		Function
15	P1_DN	0	1	Path 1 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		1		
11		0	7	
10		1		
9		1		
8		1		
7		1	E	
6	P1_CT_GAIN	1		Path 1 coarse tuning calibration gain
5		1		
4		0		
3	P1_KV_GAIN	0	4	Path 1 VCO tuning gain calibration gain
2		1		
1		0		
0		0		

PLL1x5 (0Dh) - More Calibration Settings

#	Bit Name	Default		Function
15	P1_N_PHS_ADJ	0	0	Path 1 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7		0	1	
6		0		
5		0		
4	P1_CT_V	1		Path 1 course tuning voltage setting when performing course tuning calibration. Not used by RF2053.
3		0	0	
2		0		
1		0		
0		0		

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PLL2x0 (10h) - VCO, LO Divider and Calibration Select

#	Bit Name	Default		Function
15	P2_VCOSEL	0	7	Path 2 VCO band select: 00=VCO1, 01=VCO2, 10=VCO3, 11=Reserved. Always set to 10 for VCO3.
14		1		
13	P2_CT_EN	1		Path 2 VCO coarse tune: 00=disabled, 11=enabled. Set to 00 to disable VCO coarse tune.
12		1		
11	P2_KV_EN	0	1	Path 2 VCO tuning gain calibration: 00=disabled, 11=enabled. Set to 00 to disable calibration.
10		0		
9	P2_LODIV	0		Path 2 local oscillator divider: 00=divide by 1, 01=divide by 2, 10=divide by 4, 11=reserved
8		1		
7			1	
6				
5	P2_CP_DEF	0		Charge pump current setting. If P2_KV_EN=11 this value sets charge pump current during KV compensation only
4		1		
3		1	F	
2		1		
1		1		
0		1		

PLL2x1 (11h) - MSB of Fractional Divider Ratio

#	Bit Name	Default		Function
15	P2_NUM_MSB	0	6	Path 2 VCO divider numerator value, most significant 16 bits
14		1		
13		1		
12		0		
11		0	2	
10		0		
9		1		
8		0		
7		0	7	
6		1		
5		1		
4		1		
3		0	6	
2		1		
1		1		
0		0		

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PLL2x2 (12h) - LSB of Fractional Divider Ratio and CT Default

#	Bit Name	Default		Function
15	P2_NUM_LSB	0	2	Path 2 VCO divider numerator value, least significant 8 bits.
14		0		
13		1		
12		0		
11		0	7	
10		1		
9		1		
8		1		
7	P2_CT_DEF	0	7	Path 2 VCO coarse tuning value. Not required for RF2053.
6		1		
5		1		
4		1		
3		1	E	
2		1		
1		1		
0		0		

PLL2x3 (13h) - Integer Divider Ratio and VCO Current

#	Bit Name	Default		Function
15	P2_N	0	2	Path 2 VCO divider integer value
14		0		
13		1		
12		0		
11		0	3	
10		0		
9		1		
8		1		
7		0	0	
6		0		
5		0		
4		0		
3		0	2	
2	P2_VCOI	0		Path 1 VCO bias setting: 000=minimum value, 111=maximum value
1		1		
0		0		

PLL2x4 (14h) - Calibration Settings

#	Bit Name	Default		Function
15	P2_DN	0	1	Path 2 frequency step size used in VCO tuning gain calibration
14		0		
13		0		
12		1		
11		0	7	
10		1		
9		1		
8		1		
7		1	E	
6	P2_CT_GAIN	1		Path 2 coarse tuning calibration gain
5		1		
4		0		
3	P2_KV_GAIN	0	4	Path 2 VCO tuning gain calibration gain
2		1		
1		0		
0		0		

PLL2x5 (15h) - More Calibration Settings

#	Bit Name	Default		Function
15	P2_N_PHS_ADJ	0	0	Path 2 synthesizer phase adjustment
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7		0	1	
6		0		
5		0		
4	P2_CT_V	1		Path 2 course tuning voltage setting when performing course tuning calibration. Not used by RF2053.
3		0	0	
2		0		
1		0		
0		0		

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GPO (18h) - Internal Control Output Settings

#	Bit Name	Default		Function
15		0	0	
14	P1_GPO1	0		Setting of GPO1 when path 1 is active, used internally only
13		0		
12	P1_GPO3	0		Setting of GPO3 when path 1 is active, used internally only
11	P1_GPO4	0	0	Setting of GPO4 when path 1 is active, used internally only
10		0		
9		0		
8		0		
7		0	0	
6	P2_GPO1	0		Setting of GPO1 when path 2 is active, used internally only
5		0		
4	P2_GPO3	0		Setting of GPO3 when path 2 is active, used internally only
3	P2_GPO4	0	0	Setting of GPO4 when path 2 is active, used internally only
2		0		
1		0		
0		0		

CHIPREV (19h) - Chip Revision Information

#	Bit Name	Default		Function
15	PARTNO	0	0	RFMD Part number for device
14		0		
13		0		
12		0		
11		0	0	
10		0		
9		0		
8		0		
7	REVNO	X	X	Part revision number
6		X		
5		X		
4		X		
3		X	X	
2		X		
1		X		
0		X		

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RB1 (1Ch) - PLL Lock and Calibration Results Read-back

#	Bit Name	Default		Function
15	LOCK	X	X	PLL lock detector, not used by RF2053.
14	CT_CAL	X		CT setting, not used by RF2053.
12		X		
11		X	X	
10		X		
9		X		
8		X		
7	CP_CAL	X	X	CP setting, not used by RF2053.
5		X		
4		X		
3		X	X	
2		X		
1		0		
0		0		

RB2 (1Dh) - Calibration Results Read-Back

#	Bit Name	Default		Function
15	VO_CAL	X	X	The VCO voltage measured at the start of a VCO gain calibration. Not used by RF2053.
14		X		
13		X		
12		X		
11		X	X	
10		X		
9		X		
8		X		
7	V1_CAL	X	X	The VCO voltage measured at the end of a VCO gain calibration. Not used by RF2053.
6		X		
5		X		
4		X		
3		X	X	
2		X		
1		X		
0		X		

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RB3 (1Eh) - PLL state Read-Back

#	Bit Name	Default		Function
15	RSM_STATE	X	X	State of the radio state machine
14		X		
13		X		
12		X		
11		X	X	
10		X		
9		0		
8		0		
7		0	0	
6		0		
5		0		
4		0		
3		0	0	
2		0		
1		0		
0		0		

TEST (1Fh) - Test Modes

#	Bit Name	Default		Function
15	TEN	0	0	Enables test mode
14	TMUX	0		Sets test multiplexer state
13		0		
12		0		
11	CPU	0	0	Set charge pump to pump up, 0=normal operation 1=pump down
10	CPD	0		Set charge pump to pump down, 0=normal operation 1=pump down
9	FNZ	0		0=normal operation, 1=fractional divider modulator disabled
8	LDO_BYP	0		On chip low drop out regulator bypassed
7	TSEL	0	0	
6		0		
5		0		
4	DACTEST	0		DAC test
3		0	0	
2		0		
1		0		
0		0		

Evaluation Board

The following diagrams show the schematic and PCB layout of the RF2053 evaluation boards.The standard evaluation board, DK2053, has been configured with a narrowband VCO covering 1646MHz to 1670MHz. The wideband evaluation board, DK2053-WB, has a VCO covering over an octave, 950MHz to 2150MHz. The mixer input and output on both boards have been configured for broadband oeration. Application notes have been produced showing how the device is matched and on balun implementations for narrowband applications. The evaluation boards are provided as part of a design kit (DK2053 and DK2053-WB), along with the necessary cables and programming software tool to enable full evaluation of the RF2053.

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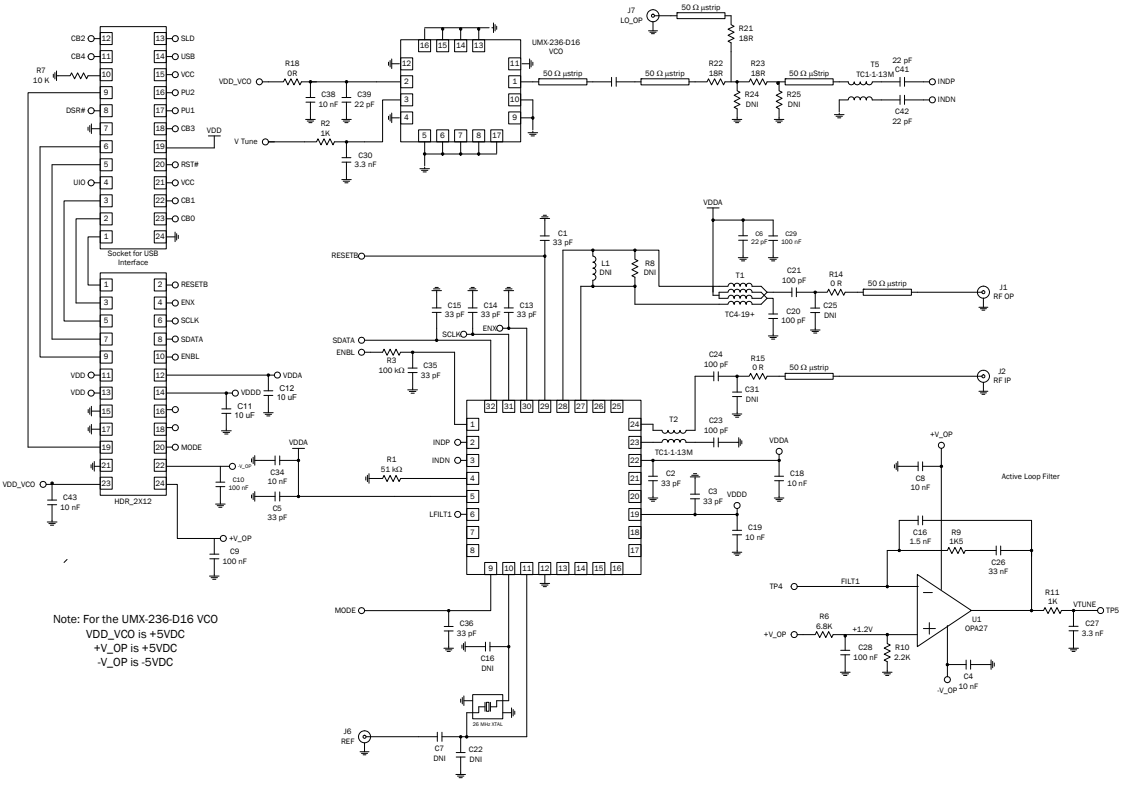
Evaluation Board Schematic
Narrowband with UMX-236-D16 VCO



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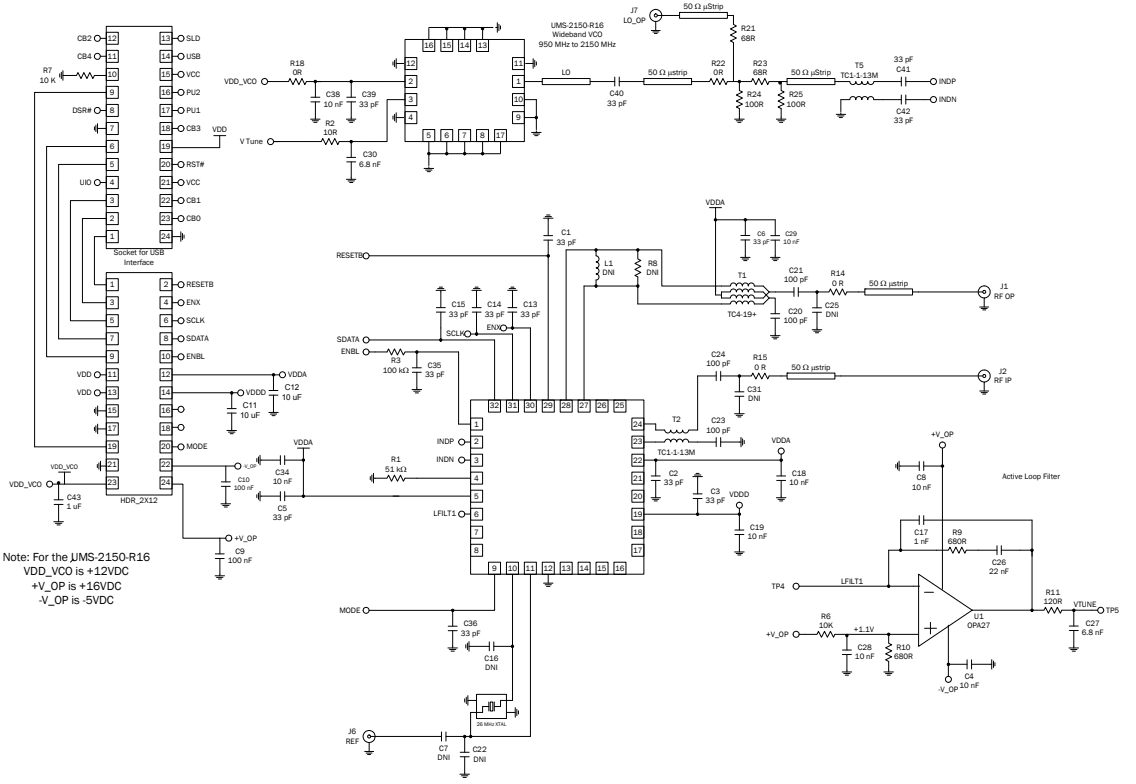
Wideband with UMS-2150-R16 VCO



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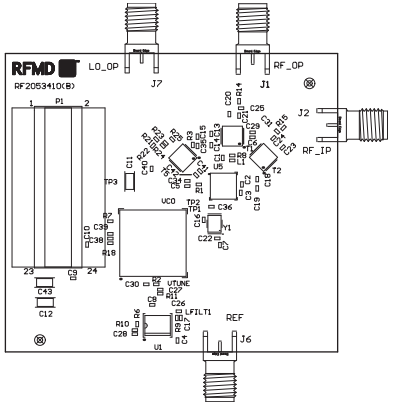
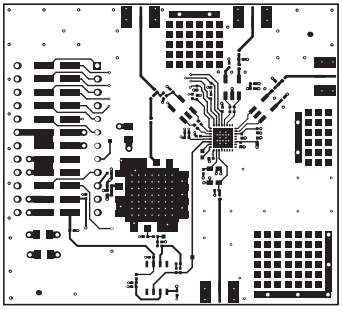
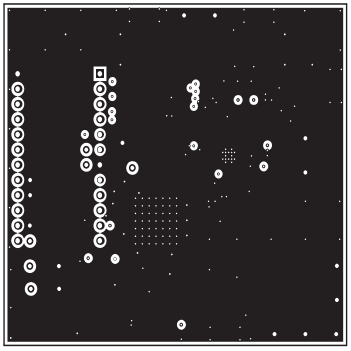
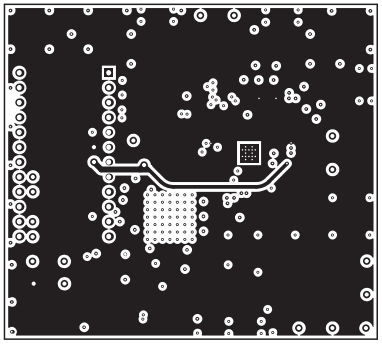
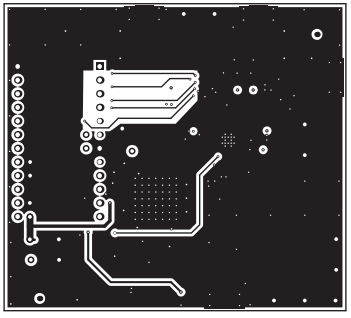
Evaluation Board Layout
Board Size 2.5”x2.5”
Board Thickness 0.040”, Board Material FR-4











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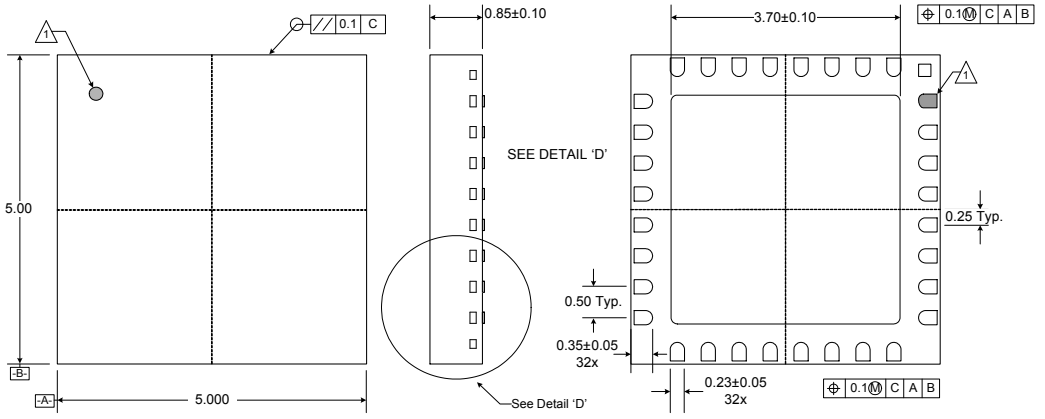
Package Drawing
QFN, 32-Pin, 5mmx5mm



Support and Applications Information

Application notes and support material can be downloaded from the product web page: www.rfmd.com/rf205x.

Ordering Information

Part Number	Package	Quantity
RF2053	32-Pin QFN	25pcs sample bag
RF2053SB	32-Pin QFN	5pcs sample bag
RF2053SR	32-Pin QFN	100pcs reel
RF2053TR7	32-Pin QFN	750pcs reel
RF2053TR13	32-Pin QFN	2500pcs reel
DK2053	Complete Design Kit Narrowband VCO Evaluation Board	1 box
DK2053WB	Complete Design Kit Wideband VCO Evaluation Board	1 box

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