MIC261203-ZA

28V, 12A, Hyper Speed Control™ Synchronous DC-to-DC Buck Regulator

SuperSwitcher™ II

General Description

The Micrel MIC261203-ZA is a constant-frequency, synchronous buck regulator featuring a unique adaptive on-time control architecture. The MIC261203-ZA operates over an input supply range of 4.5V to 28V and provides a regulated output of up to 12A of output current. The output voltage is adjustable down to 0.6V with a guaranteed accuracy of ±1%, and the device operates at a switching frequency of 600kHz.

Micrel's Hyper Speed Control™ architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High V_{IN})/(Low V_{OUT}) operation possible. This adaptive t_{ON} ripple control architecture combines the advantages of fixed-frequency operation and fast transient response in a single device.

The MIC261203-ZA offers a full suite of features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, foldback current limit, "hiccup mode" short-circuit protection, and thermal shutdown. An open-drain Power Good (PG) pin is provided.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

SuperSwitcher™ II

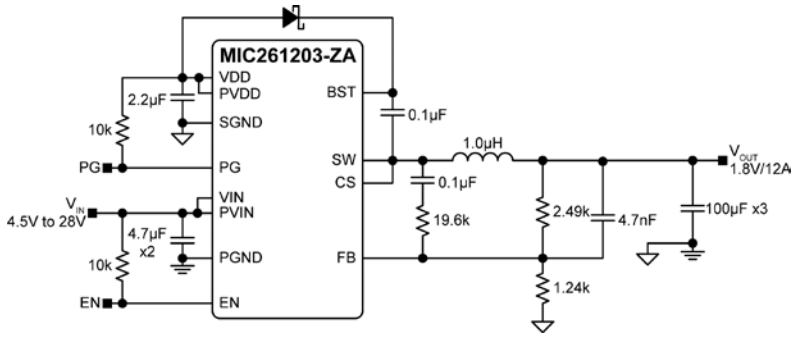
Features

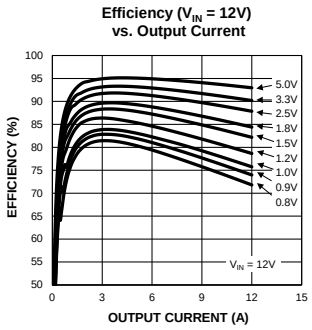
- Hyper Speed Control architecture enables
  - High Delta V operation (V_{IN} = 28V and V_{OUT} = 0.6V)
  - Small output capacitance
- 4.5V to 28V voltage input
- 12A output current capability and 95% peak efficiency
- Adjustable output from 0.6V to 5.5V
- ±1% feedback accuracy
- Any Capacitor™ stable - zero-to-high ESR
- 600kHz switching frequency
- No external compensation
- Power Good (PG) output
- Foldback I-limit and "hiccup" short-circuit protection
- Supports safe startup into a pre-biased load
- –40°C to +125°C junction temperature range
- 28-pin 5mm × 6mm QFN package

Applications

- Distributed POL and telecom/networking infrastructure
- Printers, scanners, graphic and video cards
- Set-top boxes, gateways and routers

Typical Application

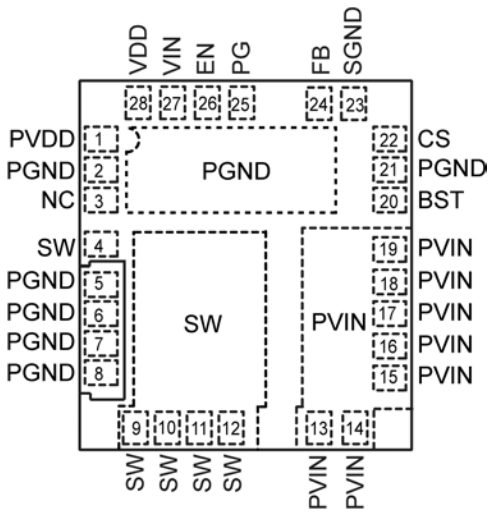




Ordering Information

Part Number	Voltage	Switching Frequency	Package	Junction Temperature Range	Lead Finish
MIC261203-ZAYJL	Adjustable	600kHz	28-Pin 5mm × 6mm QFN	–40°C to +125°C	Pb-Free

Pin Configuration



28-Pin 5mm × 6mm QFN (JL)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PVDD	5V Internal Linear Regulator output: PVDD supply is the power MOSFET gate drive supply voltage created by internal LDO from V_{IN}. When V_{IN} < +5.5V, PVDD should be tied to the PVIN pins. A 2.2µF ceramic capacitor from the PVDD pin to PGND (pin 2) must be placed next to the IC.
2, 5, 6, 7, 8, 21	PGND	Power Ground: PGND is the ground path for the MIC261203-ZA buck converter power stage. The PGND pins connect to the low-side N-Channel internal MOSFET gate drive supply ground, the sources of the MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the signal ground (SGND) loop.
3	NC	No Connect.
4, 9, 10, 11, 12	SW	Switch Node output: Internal connection for the high-side MOSFET source and low-side MOSFET drain. Because of the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes.
13,14,15,16, 17,18,19	PVIN	High-Side N-Internal MOSFET Drain Connection input: The PVIN operating voltage range is from 4.5V to 28V. Input capacitors between the PVIN pins and the power ground (PGND) are required and keep the connection short.
20	BST	Boost output: Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. Adding a small resistor at the BST pin can reduce the turn-on time of high-side N-Channel MOSFETs.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
22	CS	Current Sense input: The CS pin senses current by monitoring the voltage across the low-side MOSFET during the OFF-time. The current sensing is necessary for short circuit protection. To sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection. The CS pin is also the high-side MOSFET's output driver return.
23	SGND	Signal Ground: SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer (see "PCB Layout Guidelines" for details).
24	FB	Feedback input: Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.6V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
25	PG	Power Good output: Open drain output. The PG pin is externally tied with a resistor to VDD. A high output is asserted when V_{OUT} > 92% of nominal.
26	EN	Enable input: A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, the supply current of the device is greatly reduced (typically 5µA). Do not leave the EN pin open.
27	VIN	Power Supply Voltage input: Requires a bypass capacitor to SGND.
28	VDD	5V Internal Linear Regulator output: VDD supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. VDD is created by internal LDO from V_{IN}. When V_{IN} < +5.5V, VDD should be tied to PVIN pins. A 1µF ceramic capacitor from the VDD pin to SGND pins must be placed next to the IC.

Absolute Maximum Ratings[1]

PVIN to PGND ..... –0.3V to +29V
VIN to PGND ..... –0.3V to PVIN
PVDD, VDD to PGND ..... –0.3V to +6V
V_{SW}, V_{CS} to PGND ..... –0.3V to (PVIN +0.3V)
V_{BST} to V_{SW} ..... –0.3V to 6V
V_{BST} to PGND ..... –0.3V to 35V
V_{FB}, V_{PG} to PGND ..... –0.3V to (VDD + 0.3V)
V_{EN} to PGND ..... –0.3V to (VIN +0.3V)
PGND to SGND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C
ESD Rating[4] ..... ESD Sensitive

Operating Ratings[2]

Supply Voltage (PVIN, VIN) ..... 4.5V to 28V
PVDD, VDD Supply Voltage ..... 4.5V to 5.5V
Enable Input (V_{EN}) ..... 0V to VIN
Junction Temperature (T_J) ..... –40°C to +125°C
Maximum Power Dissipation ..... Note 3
Package Thermal Resistance[3]
5mm x 6mm QFN (θ_{JA}) ..... 28°C/W

Electrical Characteristics[5]

PVIN = VIN = V_{EN} = 12V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (VIN, PVIN)		**4.5**		**28**	V
Quiescent Supply Current	V_{FB} = 1.5V (non-switching)		730	**1500**	µA
Shutdown Supply Current	V_{EN} = 0V		5	**10**	µA
VDD Supply Voltage					
VDD Output Voltage	VIN = 7V to 28V, I_{DD} = 40mA	**4.8**	5	**5.4**	V
VDD UVLO Threshold	VDD Rising	**3.7**	4.2	**4.5**	V
VDD UVLO Hysteresis			400		mV
Dropout Voltage (VIN – VDD)	I_{DD} = 25mA		380	**600**	mV
DC/DC Controller					
Output Voltage Adjust Range (V_{OUT})	–40°C ≤ T_J ≤ 85°C	0.6		**5.5**	V
Reference					
Feedback Voltage	0°C ≤ T_J ≤ 85°C, ±1.0%	**0.594**	0.6	**0.606**	V
	–40°C ≤ T_J ≤ 125°C, ±1.5%	**0.591**	0.6	**0.609**	
Load Regulation	I_{OUT} = 0A to 12A		0.25		%
Line Regulation	VIN = 4.5V to 28V		0.25		%
FB Bias Current	V_{FB} = 0.6V		50		nA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. $PD_{(MAX)} = (T_{J(MAX)} – T_A)/ \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. A 5-in^2 4 layer, 0.62”, FR-4 PCB with 2oz finish copper weight per layer is used for the θ_{JA}.
4. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.

Electrical Characteristics[5] (Continued)

PVIN = VIN = V_{EN} = 12V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate −40°C ≤ T_J ≤ +125°C.

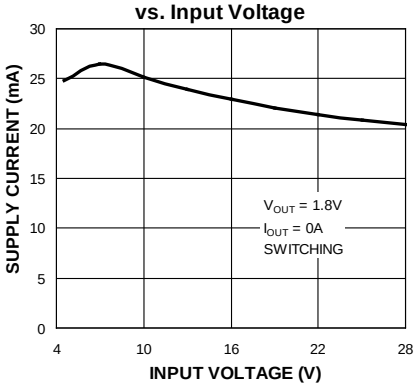
Parameter	Condition	Min.	Typ.	Max.	Units
Enable Control					
EN Logic Level High		**1.8**			V
EN Logic Level Low				**0.6**	V
EN Bias Current	V_{EN} = 12V		6	**30**	µA
Oscillator					
Switching Frequency[6]		**450**	600	**750**	kHz
Maximum Duty Cycle[7]	V_{FB} = 0V		82		%
Minimum Duty Cycle	V_{FB} = 1.0V		0		%
Minimum OFF-Time			300		ns
Soft-Start					
Soft-Start Time			5		ms
Short-Circuit Protection					
Current-Limit Threshold	V_{FB} = 0.6V, T_J = 25°C	18.75	26	33	A
Current-Limit Threshold	V_{FB} = 0.6V, T_J = 125°C	17.36	26	33	A
Short-Circuit Current	V_{FB} = 0V		6		A
Internal FETs					
Top-MOSFET $R_{DS\ (ON)}$	I_{SW} = 3A		13		mΩ
Bottom-MOSFET $R_{DS\ (ON)}$	I_{SW} = 3A		5.3		mΩ
SW Leakage Current	V_{EN} = 0V			**60**	µA
V_{IN} Leakage Current	V_{EN} = 0V			**25**	µA
Power Good (PG)					
PG Threshold Voltage	Sweep V_{FB} from Low-to-High	**85**	92	**95**	$\%V_{OUT}$
PG Hysteresis	Sweep V_{FB} from High-to-Low		5.5		$\%V_{OUT}$
PG Delay Time	Sweep V_{FB} from Low-to-High		100		µs
PG Low Voltage	Sweep V_{FB} < 0.9 × V_{NOM}, I_{PG} = 1mA		70	**200**	mV
Thermal Protection					
Overtemperature Shutdown	T_J Rising		160		°C
Overtemperature Shutdown Hysteresis			15		°C

Notes:

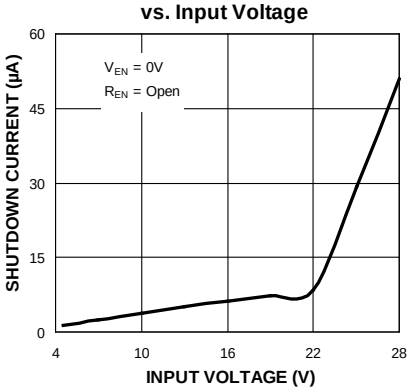
6. Measured in test mode.
7. The maximum duty-cycle is limited by the fixed mandatory OFF-time t_{OFF}, typically 300ns.

Typical Characteristics

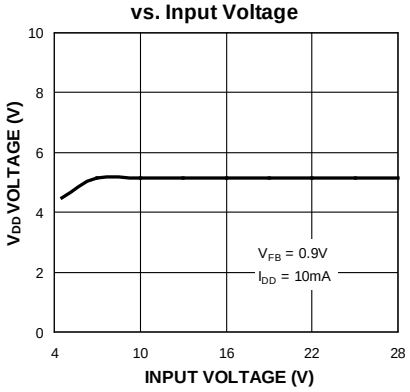
V_{IN} Operating Supply Current vs. Input Voltage



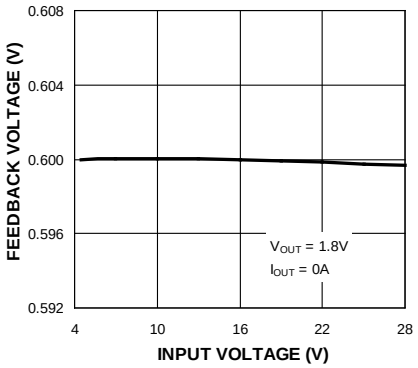
V_{IN} Shutdown Current vs. Input Voltage



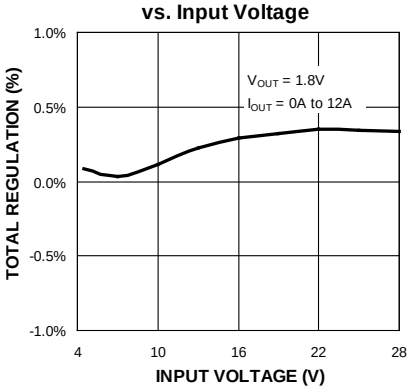
V_{DD} Output Voltage vs. Input Voltage



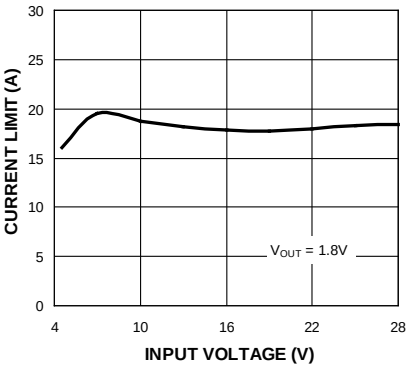
Feedback Voltage vs. Input Voltage



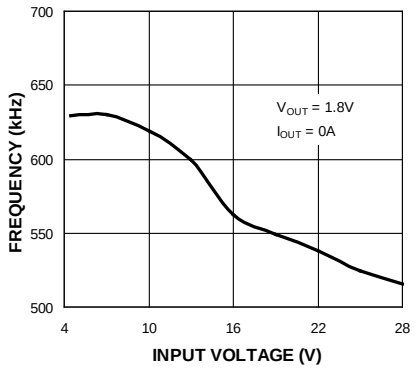
Total Regulation vs. Input Voltage



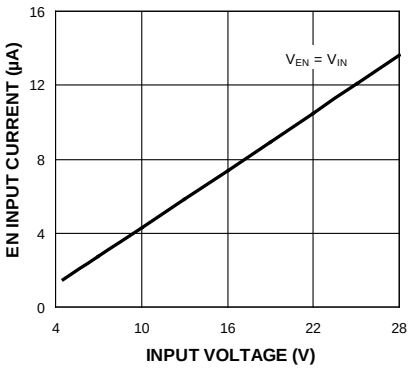
Current Limit vs. Input Voltage



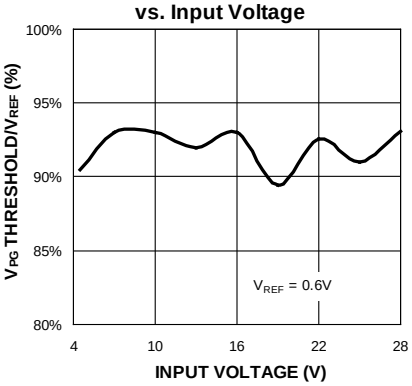
Switching Frequency vs. Input Voltage



Enable Input Current vs. Input Voltage

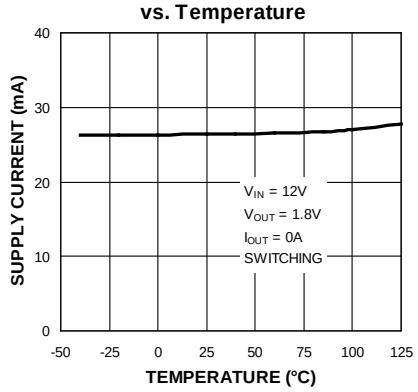


PG Threshold/V_{REF} Ratio vs. Input Voltage

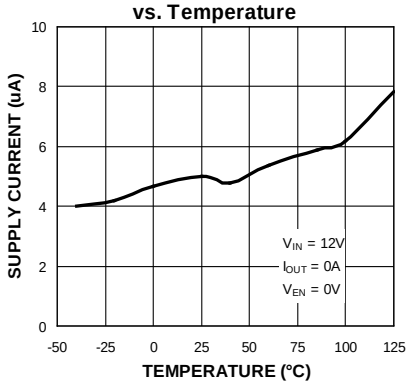


Typical Characteristics (Continued)

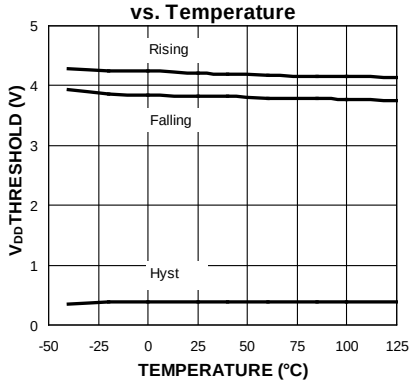
V_{IN} Operating Supply Current vs. Temperature



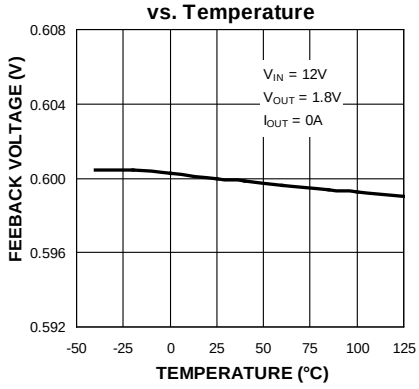
V_{IN} Shutdown Current vs. Temperature



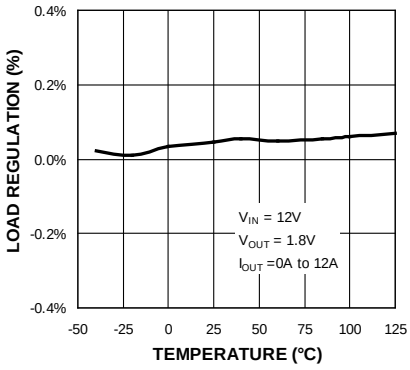
V_{DD} UVLO Threshold vs. Temperature



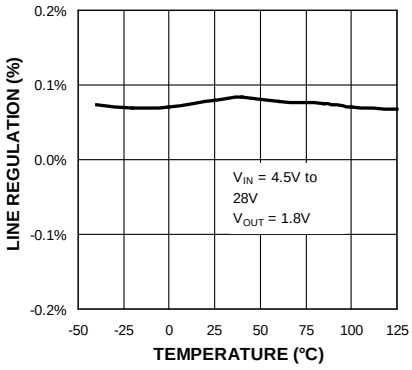
Feedback Voltage vs. Temperature



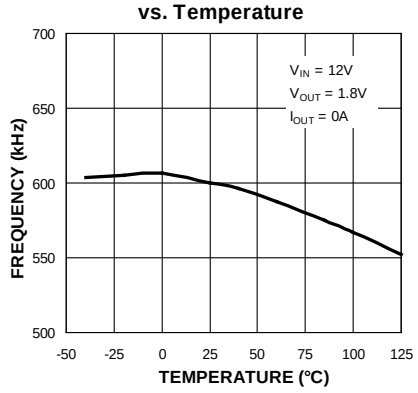
Load Regulation vs. Temperature



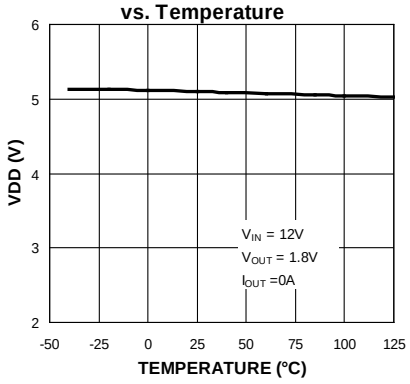
Line Regulation vs. Temperature



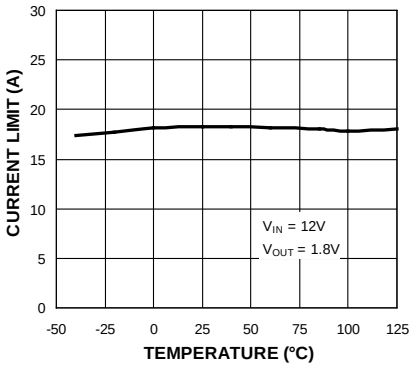
Switching Frequency vs. Temperature



V_{DD} vs. Temperature

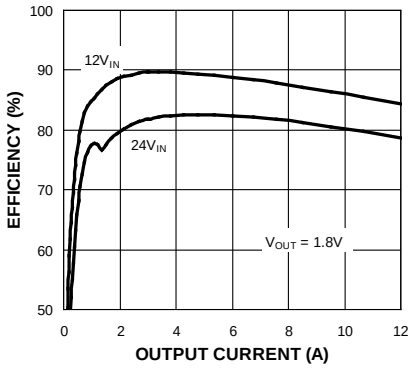


Current Limit vs. Temperature

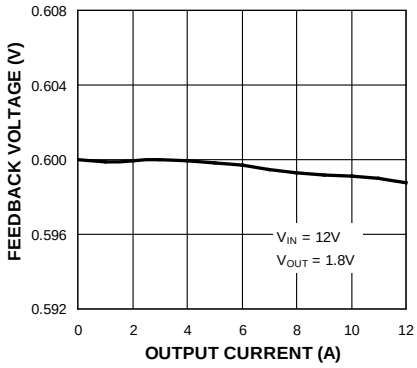


Typical Characteristics (Continued)

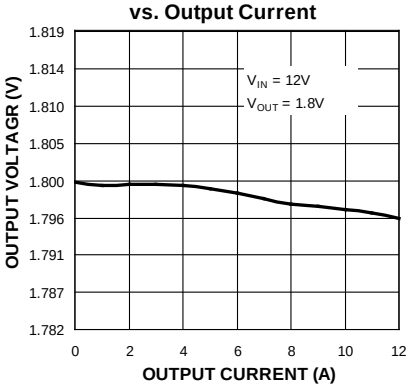
Efficiency vs. Output Current



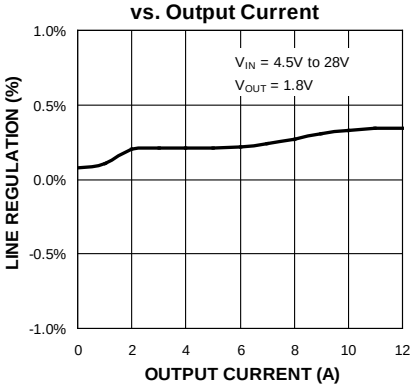
Feedback Voltage vs. Output Current



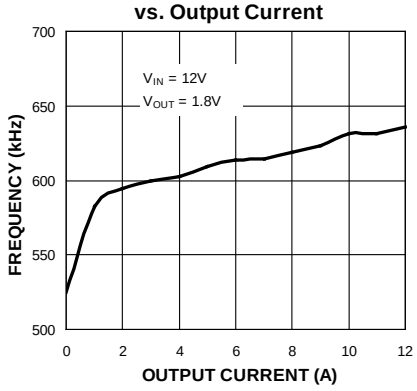
Output Voltage vs. Output Current



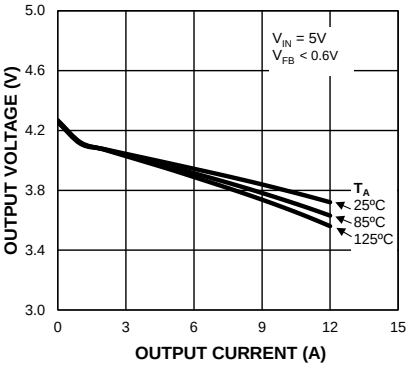
Line Regulation vs. Output Current



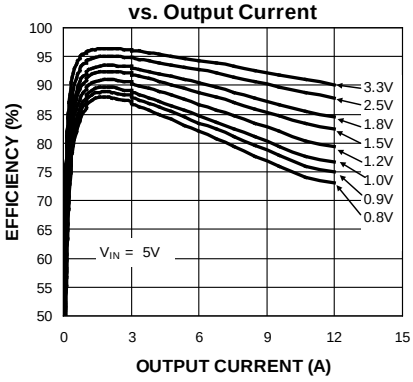
Switching Frequency vs. Output Current



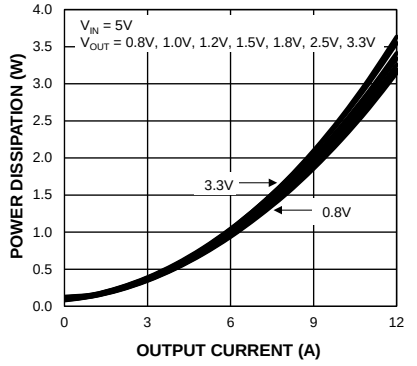
Output Voltage (V_{IN} = 5V) vs. Output Current



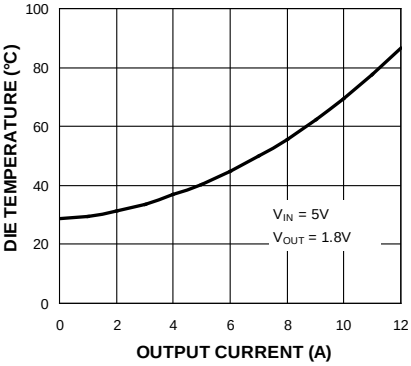
Efficiency (V_{IN} = 5V) vs. Output Current



IC Power Dissipation (V_{IN} = 5V) vs. Output Current

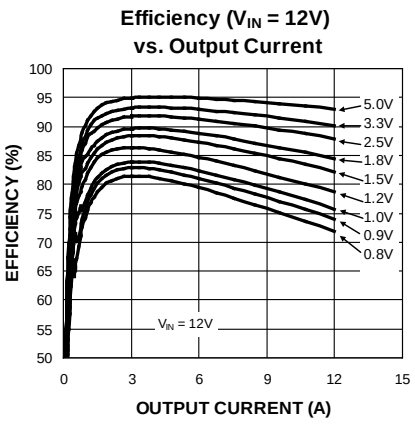


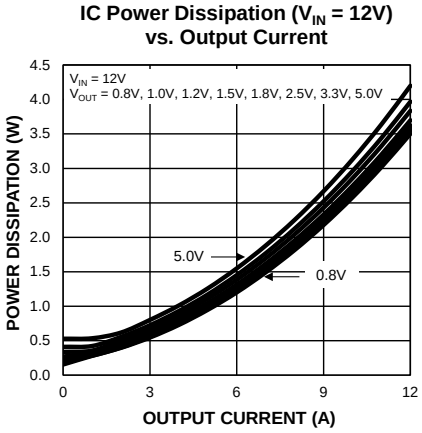
Die Temperature* (V_{IN} = 5V) vs. Output Current

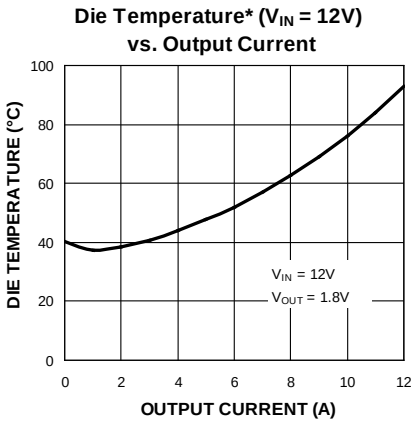


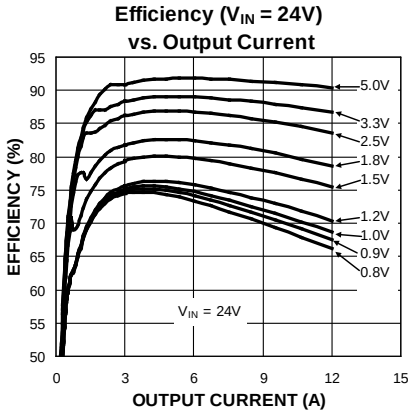
Die Temperature* : The temperature measurement was taken at the hottest point on the MIC261203-ZA while it was case mounted on a $5in^2$ 4-layer, 0.62", FR-4 PCB, with 2oz finish copper weight per layer. See the "Thermal Measurements" section for more details. Actual results will depend on the size of the PCB, ambient temperature, and proximity to other heat emitting components.

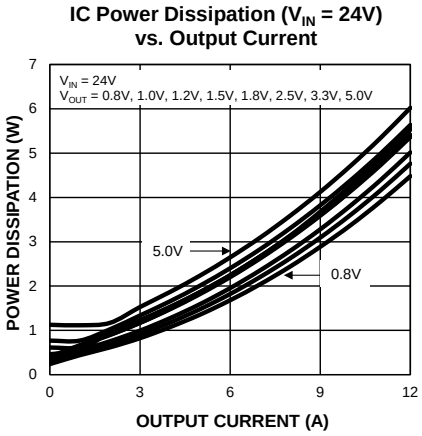
Typical Characteristics (Continued)

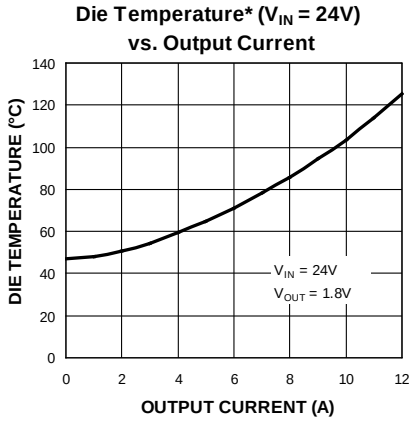


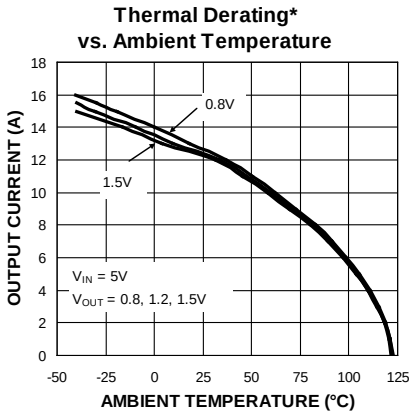


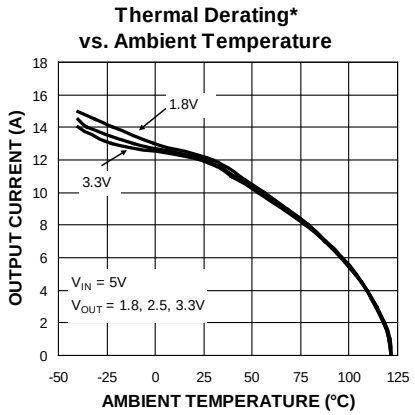


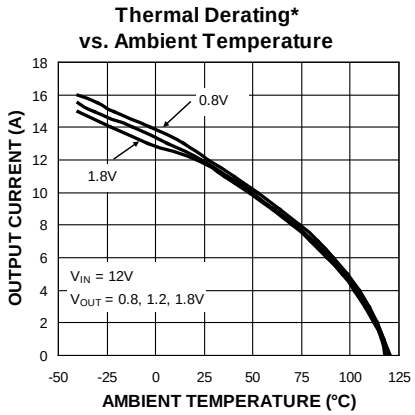






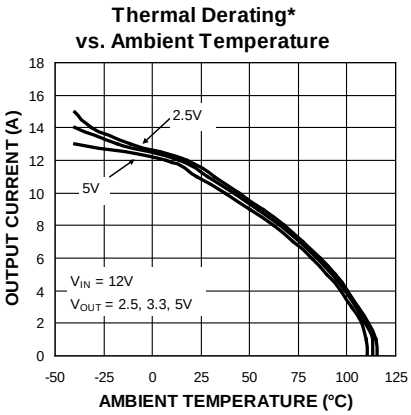


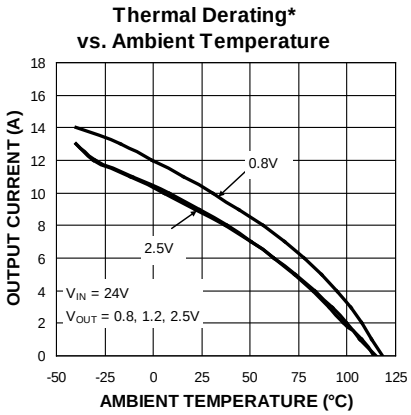




Die Temperature* : The temperature measurement was taken at the hottest point on the MIC261203-ZA while it was case mounted on a $5in^2$ 4-layer, 0.62", FR-4 PCB, with 2oz finish copper weight per layer. See the "Thermal Measurements" section for more details. Actual results will depend on the size of the PCB, ambient temperature, and proximity to other heat emitting components.

Typical Characteristics (Continued)





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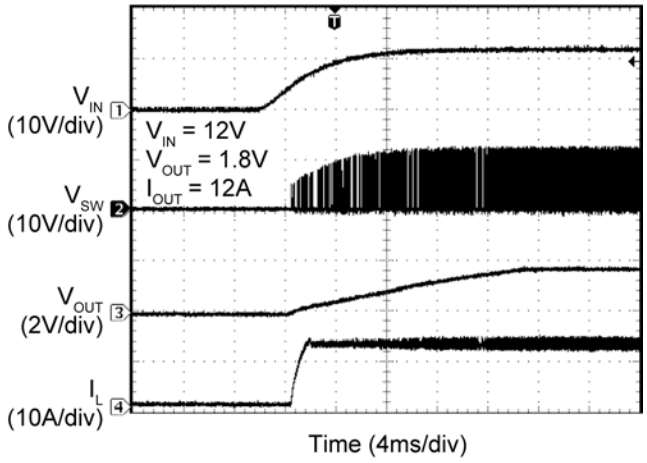
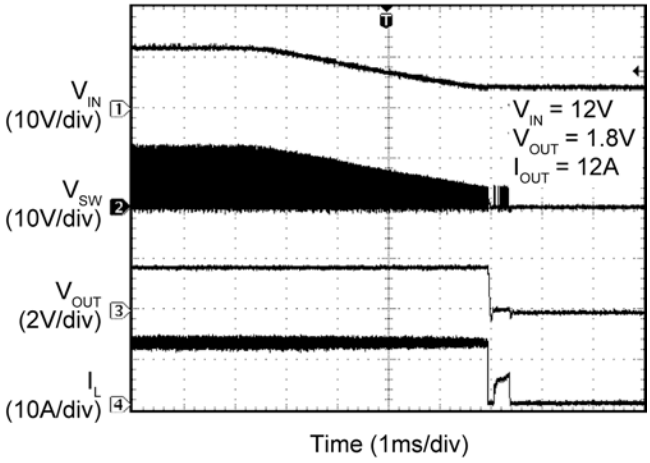
Functional Characteristics

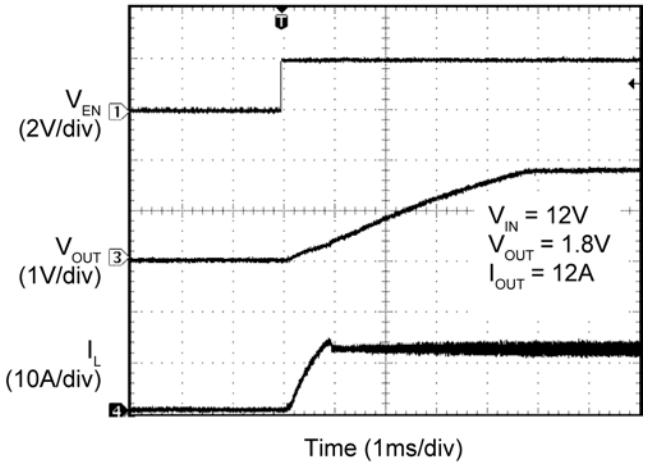
V_{IN} Soft Turn-On



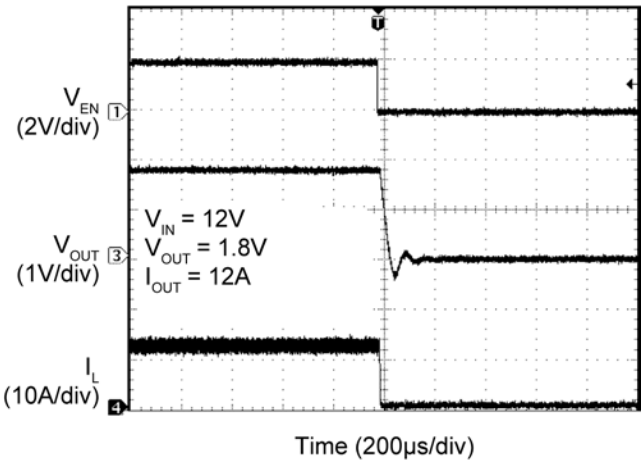
V_{IN} Soft Turn-Off



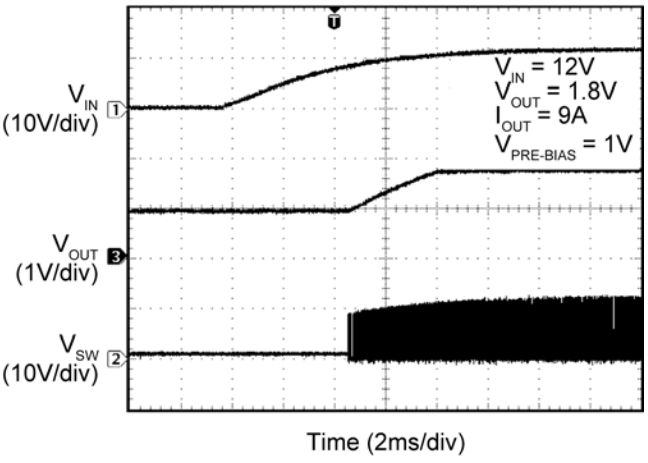
Enable Turn-On Delay and Rise Time



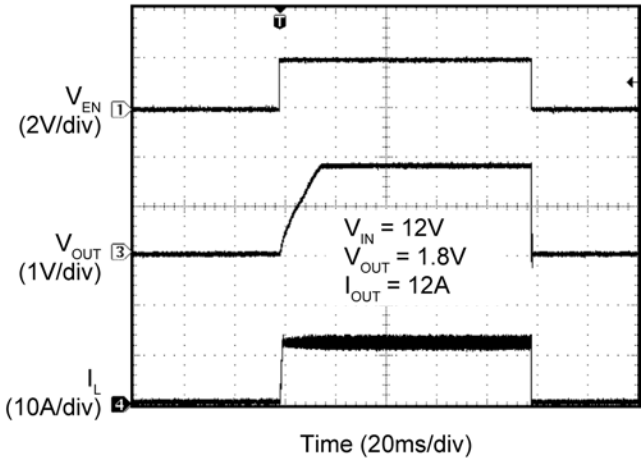
Enable Turn-Off Delay and Fall Time



V_{IN} Start-Up with Pre-Biased Output

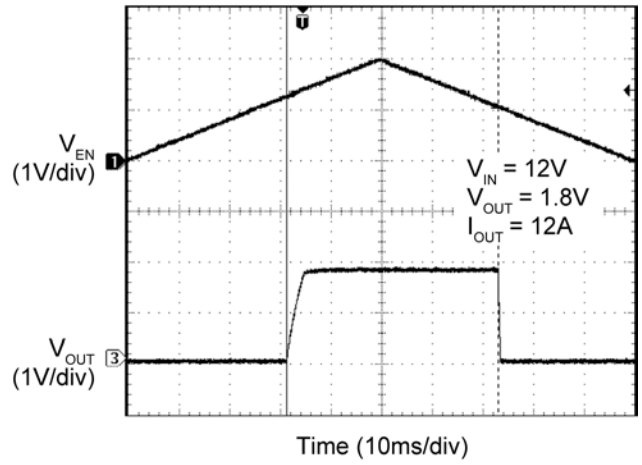


Enable Turn-On/Turn-Off

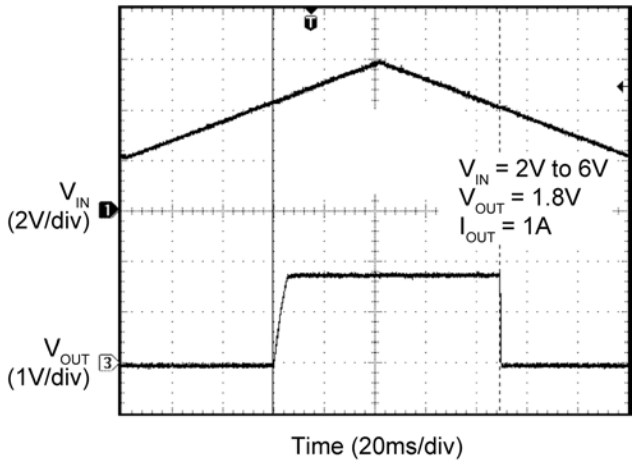


Functional Characteristics (Continued)

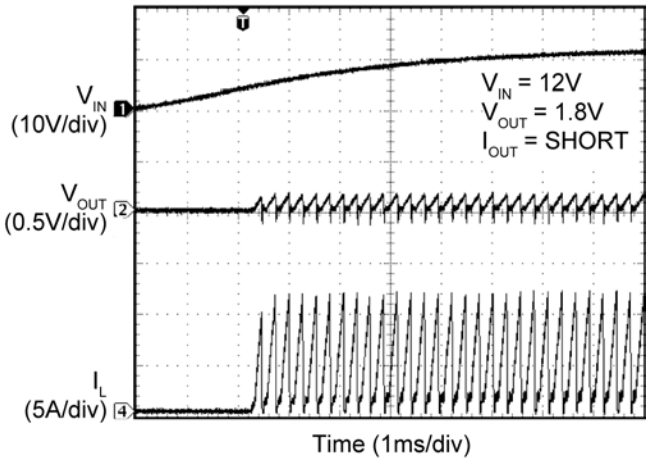
Enable Thresholds



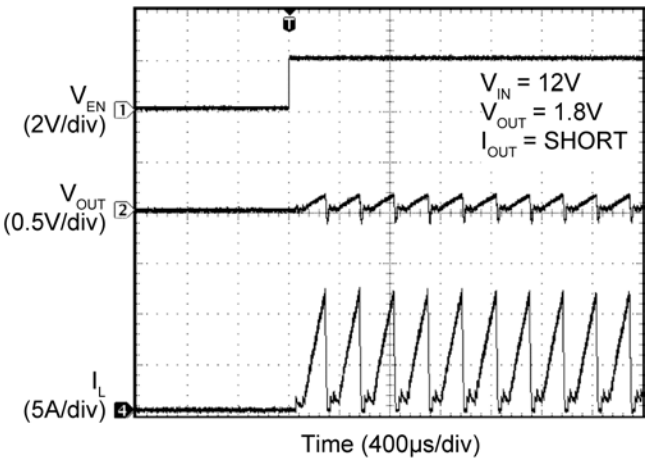
V_{IN} UVLO Thresholds



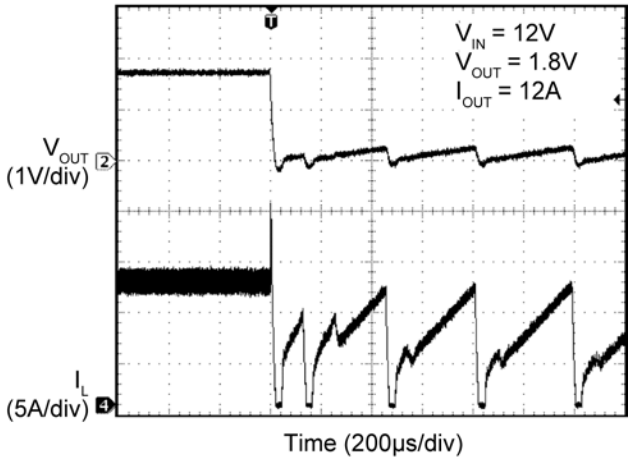
Power Up into Short Circuit



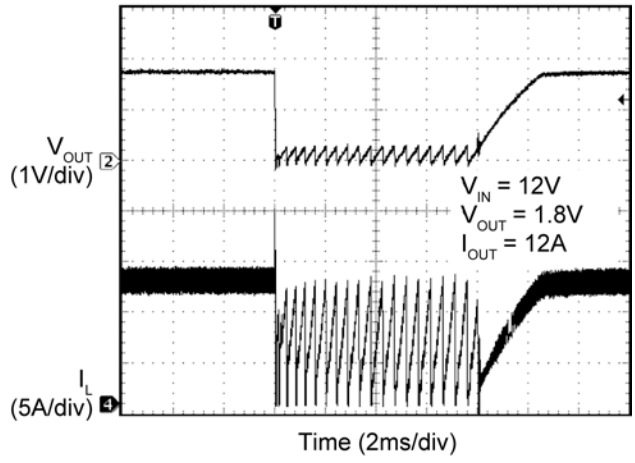
Enabled into Short



Short Circuit

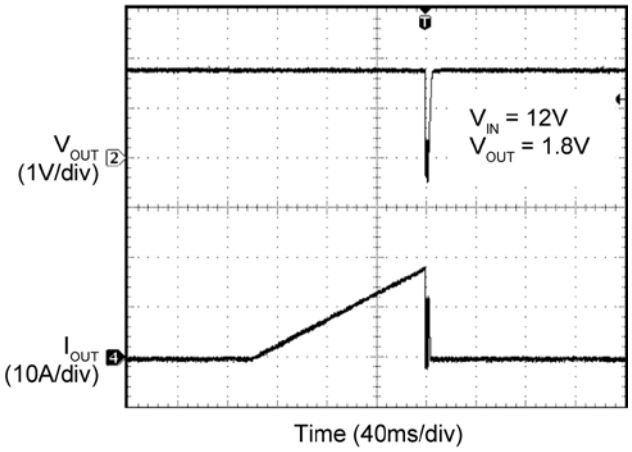


Output Recovery from Short Circuit

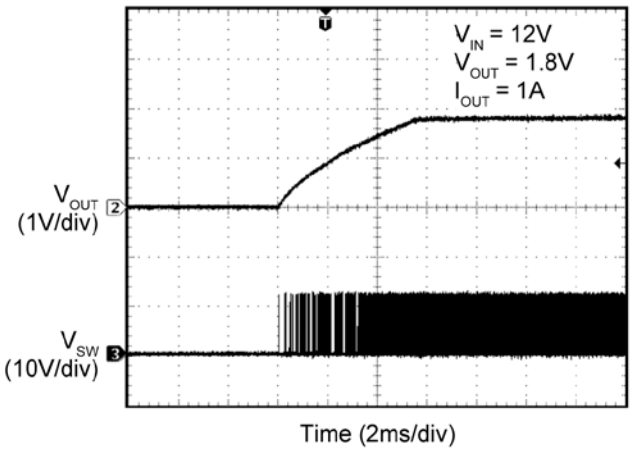


Functional Characteristics (Continued)

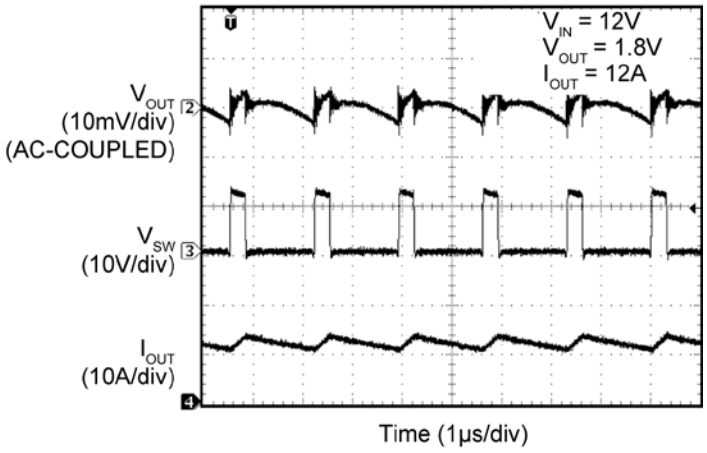
Peak Current Limit Threshold



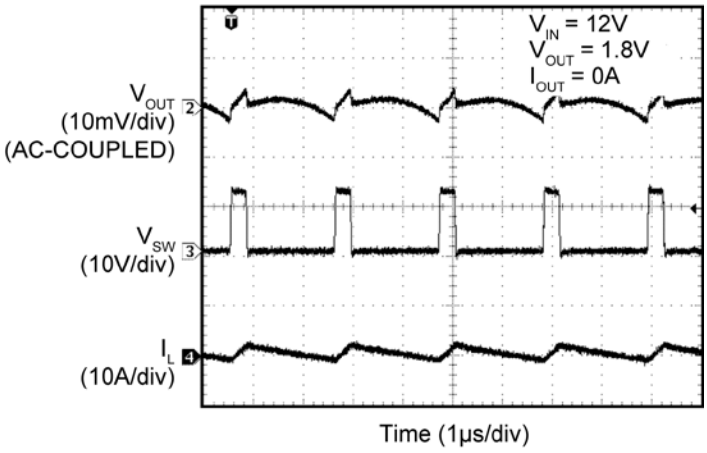
Output Recovery from Thermal Shutdown



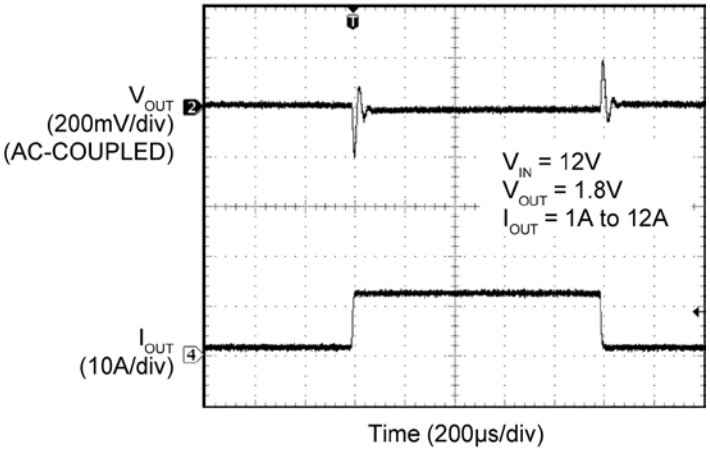
Switching Waveforms



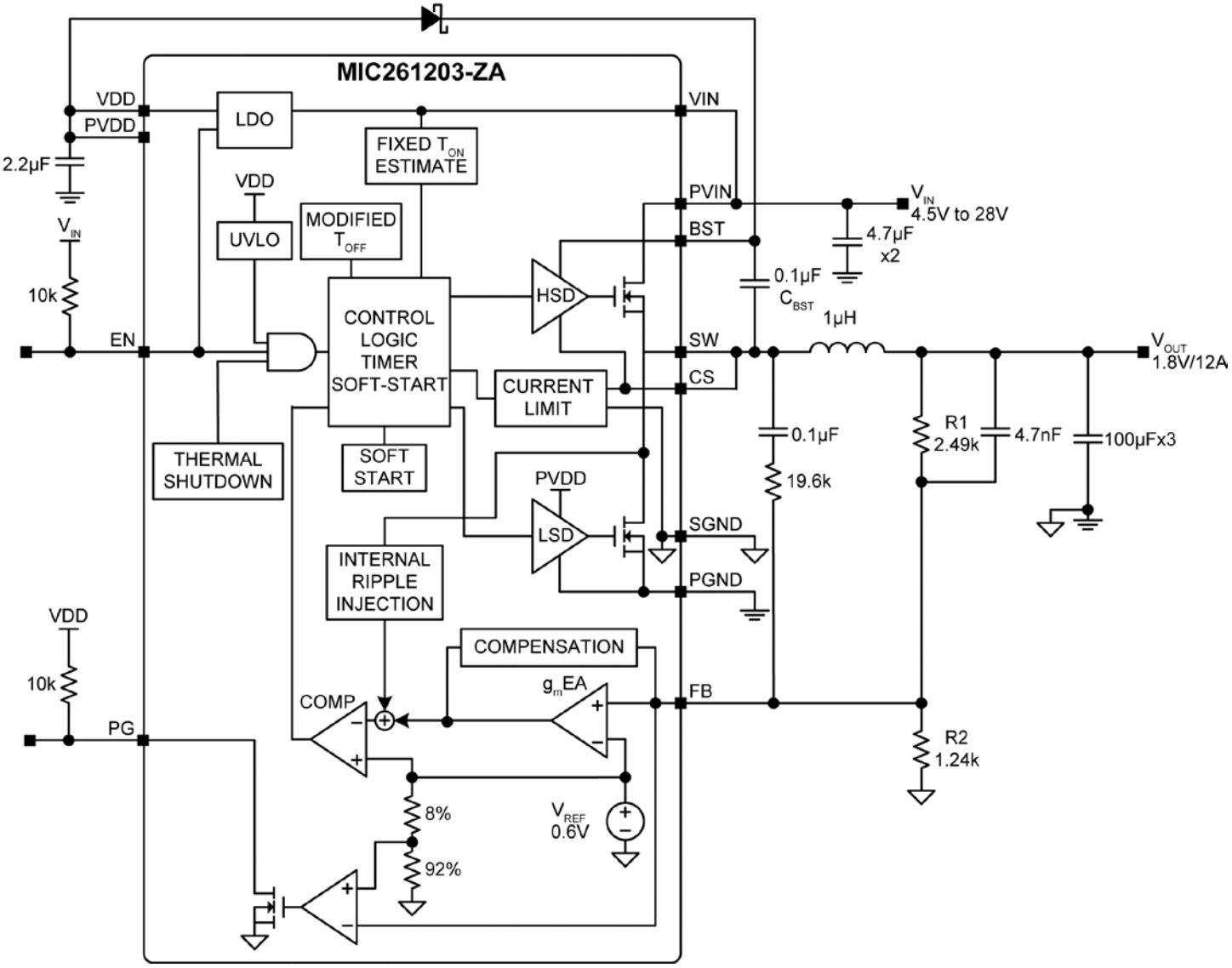
Switching Waveforms, I_{OUT} = 0A



Transient Response



Functional Diagram



Functional Description

The MIC261203-ZA is an adaptive ON-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a Power Good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 28V and provides a regulated output voltage at up to 7A of output current. An adaptive ON-time control scheme is used to get a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented without using an external sense resistor. The device includes an internal soft-start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

The MIC261203-ZA operates in a continuous mode, as shown in the *Functional Diagram*.

Continuous Mode

In continuous mode, the output voltage is sensed by the MIC261203-ZA feedback pin FB through the voltage divider R1 and R2. It is then compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "FIXED t_{ON} ESTIMATION" circuitry.

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times 600kHz} \quad \text{Eq. 1}$$

where V_{OUT} is the output voltage and V_{IN} is the power stage input voltage.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 300ns, the MIC261203-ZA control logic will apply the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300ns $t_{OFF(min)}$.

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{300ns}{t_S} \quad \text{Eq. 2}$$

where t_S = 1/600kHz = 1.66µs.

Using the MIC261203-ZA with an OFF-time close to $t_{OFF(min)}$ during steady-state operation is not recommended. Also, as V_{OUT} increases, the internal ripple injection increases and reduces the line regulation performance. Therefore, the maximum output voltage of the MIC261203-ZA should be limited to 5.5V and the maximum external ripple injection should be limited to 200mV. Please refer to the "Setting Output Voltage" subsection in Application Information for more details.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the VDD voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 24V to 1.0V. The minimum t_{ON} measured on the MIC261203-ZA evaluation board is about 100ns. During load transients, the switching frequency is changed because of the varying OFF-time.

To illustrate the control loop operation, the datasheet will discuss both the steady-state and load transient scenarios. Figure 1 shows the MIC261203-ZA control loop timing during steady-state operation. During steady-state operation, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF-time period ends and the next ON-time period is triggered through the control logic circuitry.

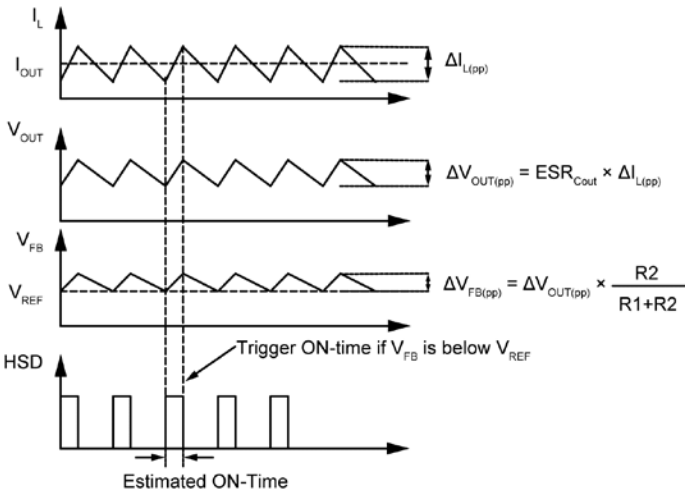


Figure 1. MIC261203-ZA Control Loop Timing

Figure 2 shows the operation of the MIC261203-ZA during a load transient. The output voltage drops because of the sudden load increase, which makes the V_{FB} less than V_{REF}. This causes the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} because the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered by the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency after the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC261203-ZA converter.

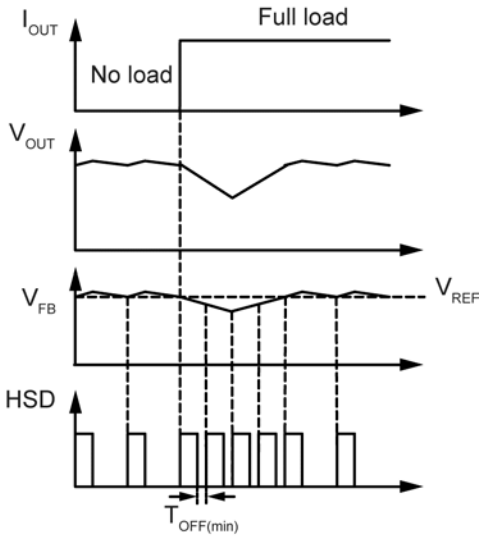


Figure 2. MIC261203-ZA Load Transient Response

Unlike true current-mode control, the MIC261203-ZA uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC261203-ZA control loop has the advantage of eliminating the need for slope compensation.

To meet the stability requirements, the MIC261203-ZA feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the "Ripple Injection" subsection in *Application Information* for more details about the ripple injection technique.

VDD Regulator

The MIC261203-ZA provides a 5V regulated output for input voltage VIN ranging from 5.5V to 28V. When VIN < 5.5V, VDD should be tied to PVIN pins to bypass the internal linear regulator

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC261203-ZA implements an internal digital soft-start by making the 0.6V reference voltage V_{REF} ramp from 0 to 100% in about 5ms in 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. After the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. VDD must be powered up at the same time or after VIN to make the soft-start function correctly.

Current Limit

The MIC261203-ZA uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense overcurrent conditions. This method avoids adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC261203-ZA converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF-time period. If the peak inductor current is greater than 26A, then the MIC261203-ZA turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The load current-limit threshold has a foldback characteristic related to the feedback voltage, as shown in Figure 3.

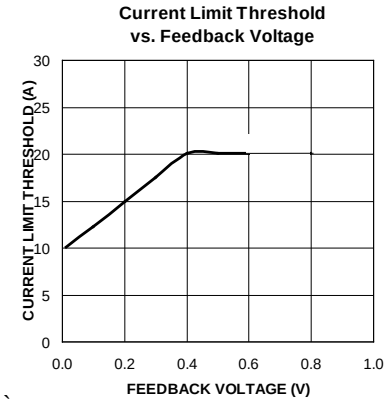


Figure 3. MIC261203-ZA Current-Limit Foldback Characteristic

Power Good (PG)

The Power Good (PG) pin is an open-drain output that indicates logic high when the output is nominally 92% of its steady state voltage. A pull-up resistor of more than 10kΩ should be connected from PG to VDD.

MOSFET Gate Drive

The *Functional Diagram* shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF capacitor is enough to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, that is, ΔBST = 10mA × 1.67µs/0.1µF = 167mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the VDD supply voltage. The nominal low-side gate drive voltage is VDD and the nominal high-side gate drive voltage is approximately VDD – V_{DIODE}, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current equal to 20% of the maximum output current. The inductance value is calculated in Equation 3.

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \quad \text{Eq. 3}$$

where:

f_{SW} = switching frequency, 600kHz

20% = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \quad \text{Eq. 4}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad \text{Eq. 5}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad \text{Eq.6}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC261203-ZA requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 7.

$$P_{INDUCTOR(CU)} = I_{L(RMS)}^2 \times R_{WINDING} \quad \text{Eq. 7}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad \text{Eq. 8}$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the stability of the control loop.

The maximum value of ESR is calculated using Equation 9.

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad \text{Eq. 9}$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 10:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad \text{Eq. 10}$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_{SW} = switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, the MIC261203-ZA requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 11.

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad \text{Eq. 11}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \quad \text{Eq. 12}$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents which are caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple primarily depends on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{C_{IN}} \quad \text{Eq. 13}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \quad \text{Eq. 14}$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN} \quad \text{Eq. 15}$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC261203-ZA g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator can't sense it, then the MIC261203-ZA will lose control and the output voltage is not regulated.

In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage caused by the large ESR of the output capacitors.

   As shown in Figure 4, the converter is stable without any ripple injection. The feedback voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \quad \text{Eq. 16}$$

   where $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the feedback voltage caused by the small ESR of the output capacitors.

   The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 5. The typical C_{ff} value is between 1nF and 100nF. With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad \text{Eq. 17}$$

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors.

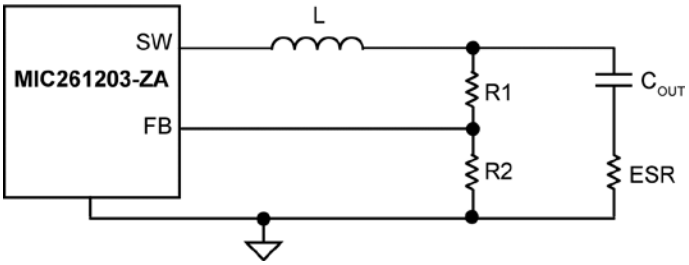


Figure 4. Enough Ripple at FB

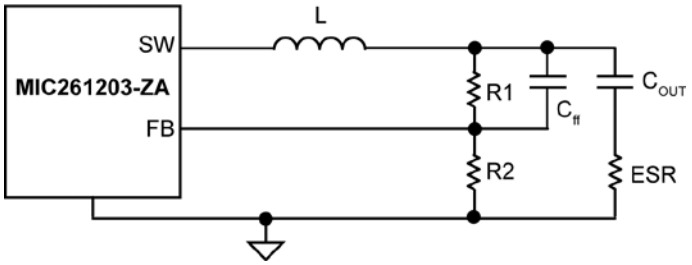


Figure 5. Inadequate Ripple at FB

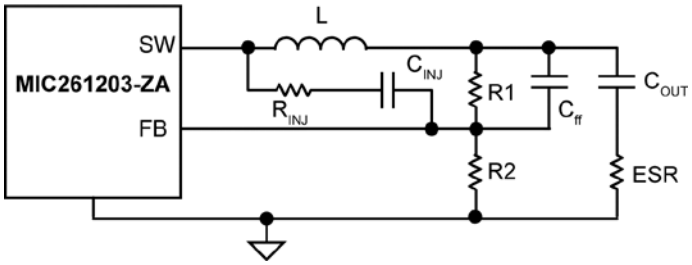


Figure 6. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ}, as shown in Figure 6. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad \text{Eq. 18}$$

$$K_{div} = \frac{R1//R2}{R_{INJ} + R1//R2} \quad \text{Eq. 19}$$

where:

V_{IN} = Power stage input voltage

D = duty cycle

f_{SW} = switching frequency

$\tau = (R1//R2//R_{INJ}) \times C_{ff}$

In Equations 18 and 19, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \quad \text{Eq. 20}$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{ff} of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{INJ} is used, which could be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select R_{INJ} according to the expected feedback voltage ripple using Equation 19:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)} \quad \text{Eq. 21}$$

Then the value of R_{INJ} is obtained as:

$$R_{INJ} = (R1//R2) \times (\frac{1}{K_{div}} - 1) \quad \text{Eq. 22}$$

Step 3. Select C_{INJ} as 100nF, which could be considered as short for a wide range of the frequencies.

Setting Output Voltage

The MIC261203-ZA requires two resistors to set the output voltage, as shown in Figure 7.

The output voltage is determined by Equation 23:

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \quad \text{Eq. 23}$$

where V_{FB} = 0.6V.

A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 24.

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \quad \text{Eq. 24}$$

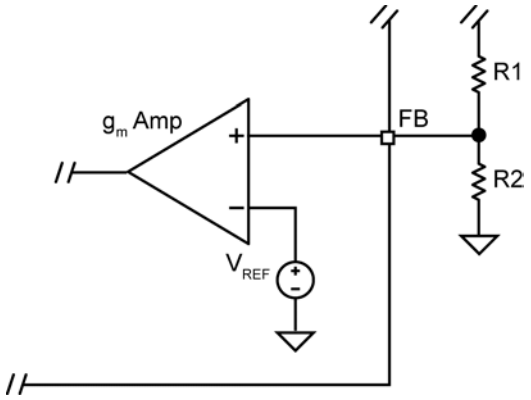


Figure 7. Voltage-Divider Configuration

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC261203-ZA, as shown in Figure 8. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} increases, the swing of V_{INJ} is clamped. The clamped V_{INJ} reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC261203-ZA should be limited to 5.5V to avoid this problem.

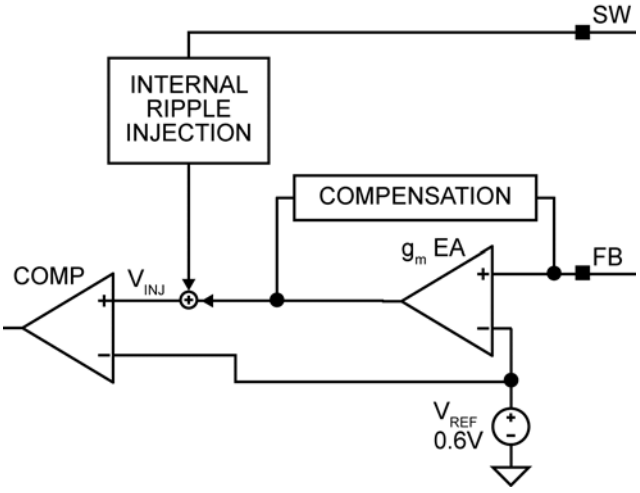


Figure 8. Internal Ripple Injection

Thermal Measurements

Measuring the IC's case temperature is recommended to ensure that it is within its operating limits. Although this might seem like an elementary task, it is easy to get false results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

PCB Layout Guidelines

Note: To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal, and return paths.

Follow these guidelines to ensure proper MIC261203-ZA regulator operation:

IC

- A 2.2µF ceramic capacitor, which is connected to the PVDD pin, must be located right at the IC. The PVDD pin is very noise sensitive, so placement of the capacitor is critical. Use wide traces to connect to the PVDD and PGND pins.
- A 1µF ceramic capacitor must be placed right between VDD and the signal ground (SGND). SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Keep signal and power grounds separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitor on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply when power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- Connect the CS pin directly to the SW pin to accurately sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

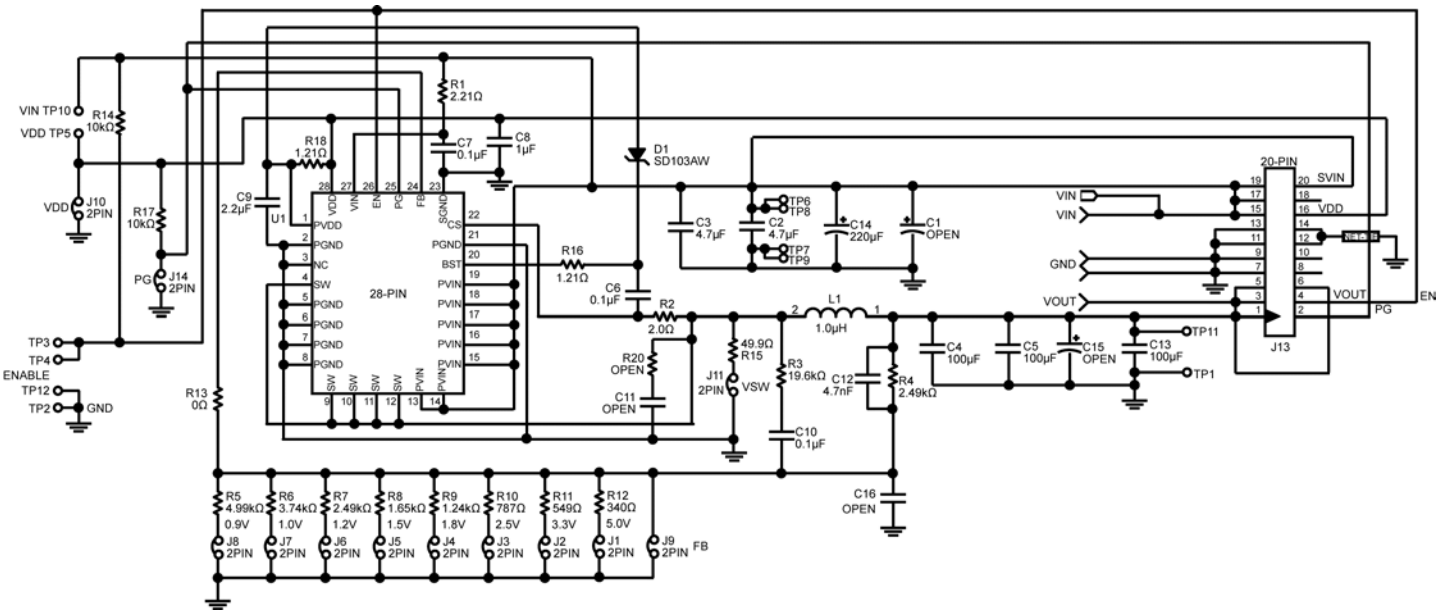
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin changes as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as near as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Optional RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

Evaluation Board Schematic



Schematic of MIC261203-ZA Evaluation Board
(J11, R13, R15 are for testing purposes)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	Open			
C2, C3	12105C475KAZ2A	AVX[8]	4.7µF Ceramic Capacitor, X7R, Size 1210, 50V	2
	GRM32ER71H475KA88L	Murata[9]		
	C3225X7R1H475K	TDK[10]		
C15	Open			
C4, C5, C13	12106D107MAT2A	AVX	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	3
	GRM32ER60J107ME20L	Murata		
	C3225X5R0J107M	TDK		
C6, C7, C10	06035C104KAT2A	AVX	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	3
	GRM188R71H104KA93D	Murata		
	C1608X7R1H104K	TDK		

Notes:

8. AVX: www.avx.com.
9. Murata: www.murata.com.
10. TDK: www.tdk.com.

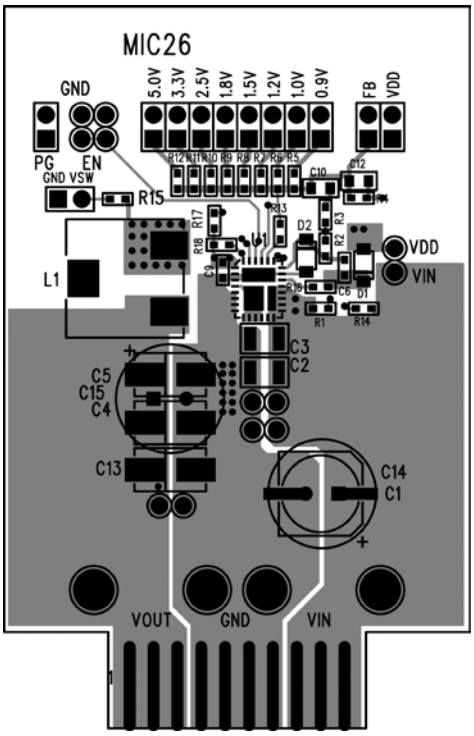
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
C8	0603ZC105KAT2A	AVX	1.0µF Ceramic Capacitor, X7R, Size 0603, 10V	1
	GRM188R71A105KA61D	Murata		
	C1608X7R1A105K	TDK		
C9	0603ZD225KAT2A	AVX	2.2µF Ceramic Capacitor, X7R, Size 0603, 10V	1
	GRM188R61A225KE34D	Murata		
	C1608X5R1A225K	TDK		
C12	06035C472KAZ2A	AVX	4.7nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H472K	Murata		
	C1608X7R1H472K	TDK		
C14	B41851F7227M	EPCOS[11]	220µF Aluminum Capacitor, 35V	1
C11, C16	Open			
D1	SD103AWS	MCC[12]	40V, 350mA, Schottky Diode, SOD323	1
	SD103AWS-7	Diodes Inc.[13]		
	SD103AWS	Vishay[14]		
L1	HCF1305-1R0-R	Cooper Bussmann[15]	1.0µH Inductor, 21A Saturation Current	1
R1	CRCW06032R21FKEA	Vishay Dale	2.21Ω Resistor, Size 0603, 1%	1
R2	CRCW06032R00FKEA	Vishay Dale	2.00Ω Resistor, Size 0603, 1%	1
R3	CRCW060319K6FKEA	Vishay Dale	19.6kΩ Resistor, Size 0603, 1%	1
R4	CRCW06032K49FKEA	Vishay Dale	2.49kΩ Resistor, Size 0603, 1%	1
R5	CRCW06034K99FKEA	Vishay Dale	4.99kΩ Resistor, Size 0603, 1%	1
R6	CRCW06033K74FKEA	Vishay Dale	3.74kΩ Resistor, Size 0603, 1%	1
R7	CRCW06032K49FKEA	Vishay Dale	2.49kΩ Resistor, Size 0603, 1%	1
R8	CRCW06031K65FKEA	Vishay Dale	1.65kΩ Resistor, Size 0603, 1%	1
R9	CRCW06031K24FKEA	Vishay Dale	1.24kΩ Resistor, Size 0603, 1%	1
R10	CRCW0603787RFKEA	Vishay Dale	787Ω Resistor, Size 0603, 1%	1
R11	CRCW0603549RFKEA	Vishay Dale	549Ω Resistor, Size 0603, 1%	1
R12	CRCW0603340RFKEA	Vishay Dale	340Ω Resistor, Size 0603, 1%	1
R13	CRCW06030000FKEA	Vishay Dale	0Ω Resistor, Size 0603, 5%	1
R14, R17	CRCW060310K0FKEA	Vishay Dale	10.0kΩ Resistor, Size 0603, 1%	2
R15	CRCW060349R9FKEA	Vishay Dale	49.9Ω Resistor, Size 0603, 1%	1
R16, R18	CRCW06031R21FKEA	Vishay Dale	1.21Ω Resistor, Size 0603, 1%	2
R20	Open			
U1	**MIC261203-ZAYJL**	**Micrel. Inc.[16]**	**28V, 12A, Hyper Speed Control Synchronous DC-to-DC Buck Regulator – SuperSwitcher II**	**1**

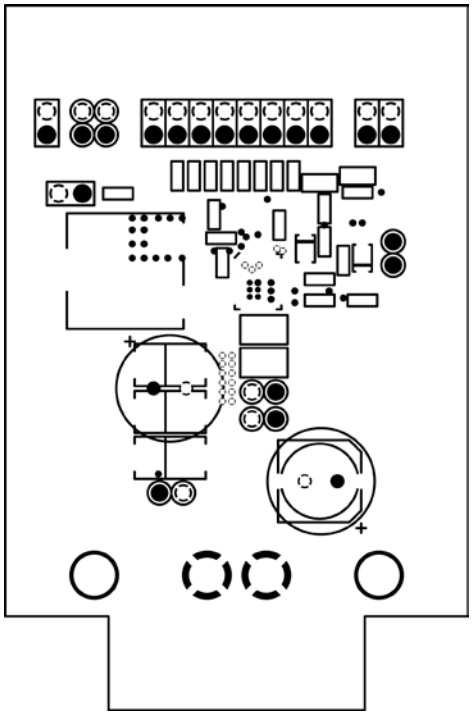
Notes:

11. EPCOS: www.epcos.com.
12. MCC: www.mccsemi.com.
13. Diodes Inc.: www.diodes.com.
14. Vishay: www.vishay.com.
15. Cooper Bussmann: www.cooperbussmann.com.
16. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

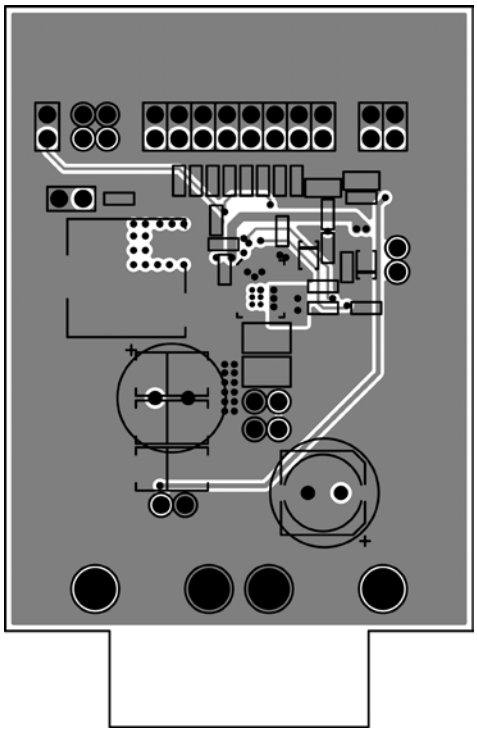


MIC261203-ZA Evaluation Board Top Layer

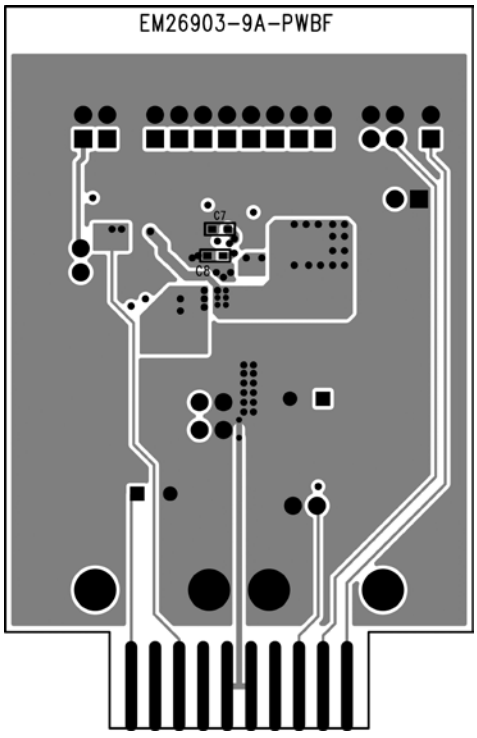


MIC261203-ZA Evaluation Board Mid-Layer 1 (Ground Plane)

PCB Layout Recommendations (Continued)

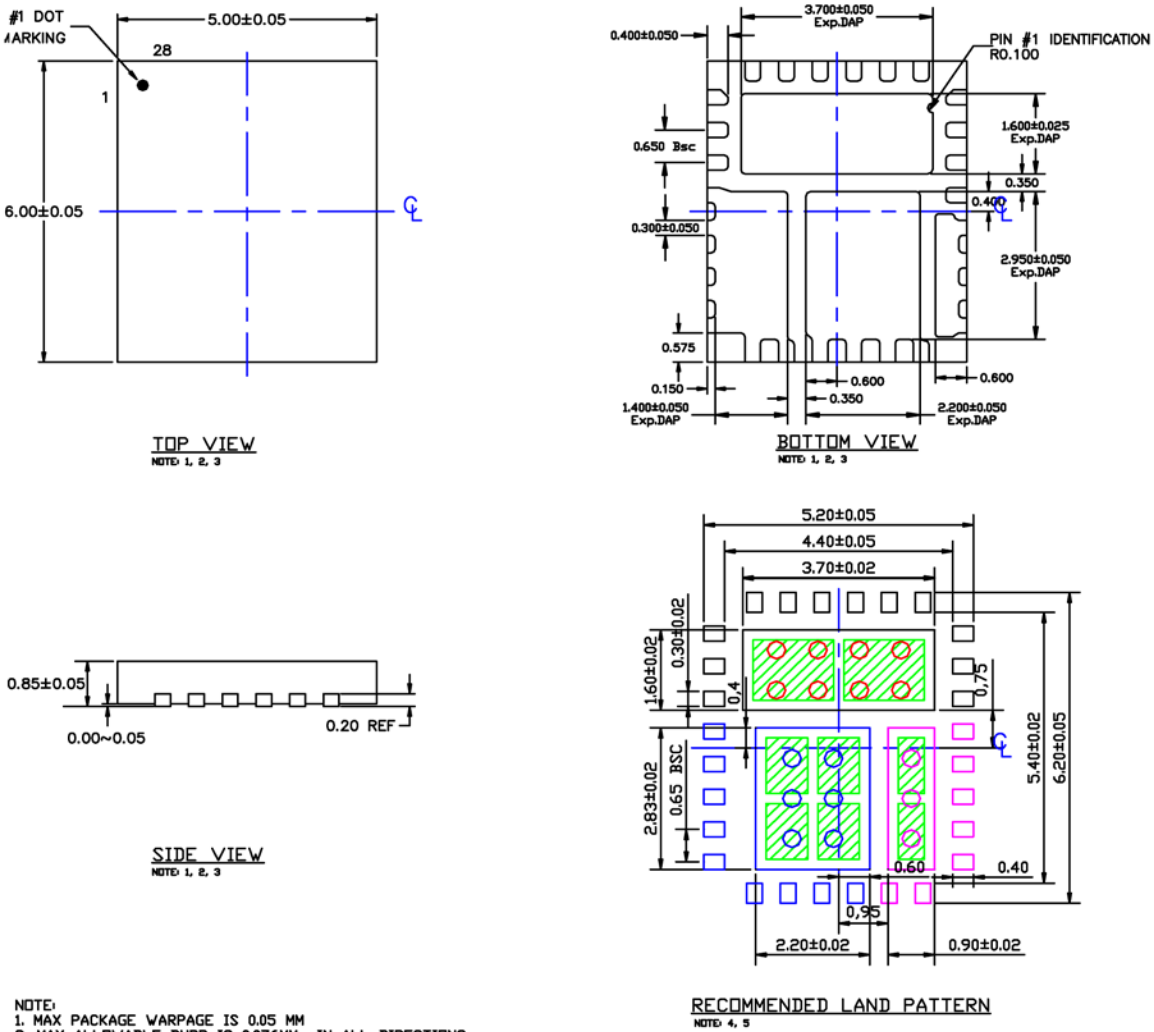


MIC261203-ZA Evaluation Board Mid-Layer 2



MIC261203-ZA Evaluation Board Bottom Layer

Package Information and Recommended Land Pattern[17]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. BLUE COLORED PADS & PURPLE COLORED PADS REPRESENT DIFFERENTPOTENTIALS. DO NOT CONNECT TO GND.
7. RECOMMENDED SOLDER STENCIL OPENING AND VIA SIZES.

28-Pin 5mm x 6mm QFN (JL)

Note:

17. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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