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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

MB9B120TA Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The MB9B120TA Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the Arm® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I^2C, LIN).

The products which are described in this data sheet are placed into TYPE12 product categories in "FM3 Family PERIPHERAL MANUAL".

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p1
- Up to 60 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Dual operation Flash memory
  - Main area:
    - Up to 1.5 Mbytes (1008 Kbytes(ROM0) + 512 Kbytes (ROM1) of Upper bank and 16 Kbytes (ROM0) of Lower bank.)
  - Work area
    - 64 Kbytes(ROM1) of Lower bank
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 96 Kbytes
- SRAM1: Up to 96 Kbytes

External Bus Interface

- Supports SRAM, NOR NAND Flash memory device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY function

Multi-function Serial Interface (Max 16channels)

- 16 channels with 16 steps×9-bit FIFO
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission/reception by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed to 13 to 16-bit length)
- LIN break delimiter generation (can be changed to 1 to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[I²C]

Standard - mode (Max 100 kbps) / Fast - mode (Max 400 kbps) supported

DMA Controller (8channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 24channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 2units
- Conversion time: 1.0µs @ 2.7V to 5.5V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

D/A Converter (Max 2 channels)

- R-2R type
- 10-bit resolution

Base Timer (Max 16channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 154 high-speed general-purpose I/O Ports@176 pin Package
- Some ports are 5V tolerant.
  See "List of Pin Functions" and "I/O Circuit Type" to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Quadrature Position/Revolution Counter (QPRC) (Max 2channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

HDMI-CEC/Remote Control Reception (Up to 2channels)

- HDMI-CEC transmission
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC reception
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control reception
  - 4 bytes reception buffer
  - Repeat code detection function available

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activation compare × 2 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter

The Watch counter is used for wake up from sleep and timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- Up to 32 external interrupt input pins @ 176 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (2channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except RTC, STOP, Deep standby RTC, Deep standby STOP modes.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)
Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)
This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode
Six low-power consumption modes supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable between keeping the value of RAM and not)
- Deep standby STOP (selectable between keeping the value of RAM and not)

Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocell (ETM)

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Wide range voltage: VCC = 2.7 V to 5.5 V

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1. Product Lineup

Memory size

Product name		MB9BF128SA/TA	MB9BF129SA/TA
On-chip Flash memory	Main area	1 Mbytes	1.5 Mbytes
	Work area	64 Kbytes	64 Kbytes
On-chip SRAM	SRAM0	80 Kbytes	96 Kbytes
	SRAM1	80 Kbytes	96 Kbytes
	Total	160 Kbytes	192 Kbytes

Function

Product name			MB9BF128SA MB9BF129SA	MB9BF128TA MB9BF129TA
Pin count			144	176/192
CPU			Cortex-M3	
	Freq.		60 MHz	
Power supply voltage range			2.7 V to 5.5 V	
DMAC			8 ch.	
External Bus Interface			Addr: 25-bit (Max) R/Wdata : 8-/16-bit (Max) CS: 8 (Max) SRAM , NOR Flash memory , NAND Flash memory	
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			16 ch. (Max) with 16steps × 9-bit FIFO	
Base Timer (PWC/Reload timer/PWM/PPG)			16 ch. (Max)	
MF-Timer	A/D activation compare	2 ch.	1 unit	
	Input capture	4 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG	3 ch.		
QPRC			1 ch.(Max)	2 ch. (Max)
Dual Timer			1 unit	
HDMI-CEC/ Remote Control Reception			2 ch. (Max)	
Real-Time Clock			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1 ch. (SW) + 1 ch. (HW)	
External Interrupts			32 pins (Max) + NMI × 1	
I/O ports			122 pins (Max)	154 pins (Max)
12-bit A/D converter			24 ch. (2 units)	
10-bit D/A converter			2 ch. (Max)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2 ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP / ETM	
Unique ID			Yes	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See "Electrical Characteristics 12.4 AC Characteristics (12.4.3) Built-in CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

Package / Product name	MB9BF128SA MB9BF129SA	MB9BF128TA MB9BF129TA
LQFP: LQS144 (0.5 mm pitch)	❍	-
LQFP: LQP176 (0.5 mm pitch)	-	❍
BGA: LBE192 (0.8 mm pitch)	-	❍

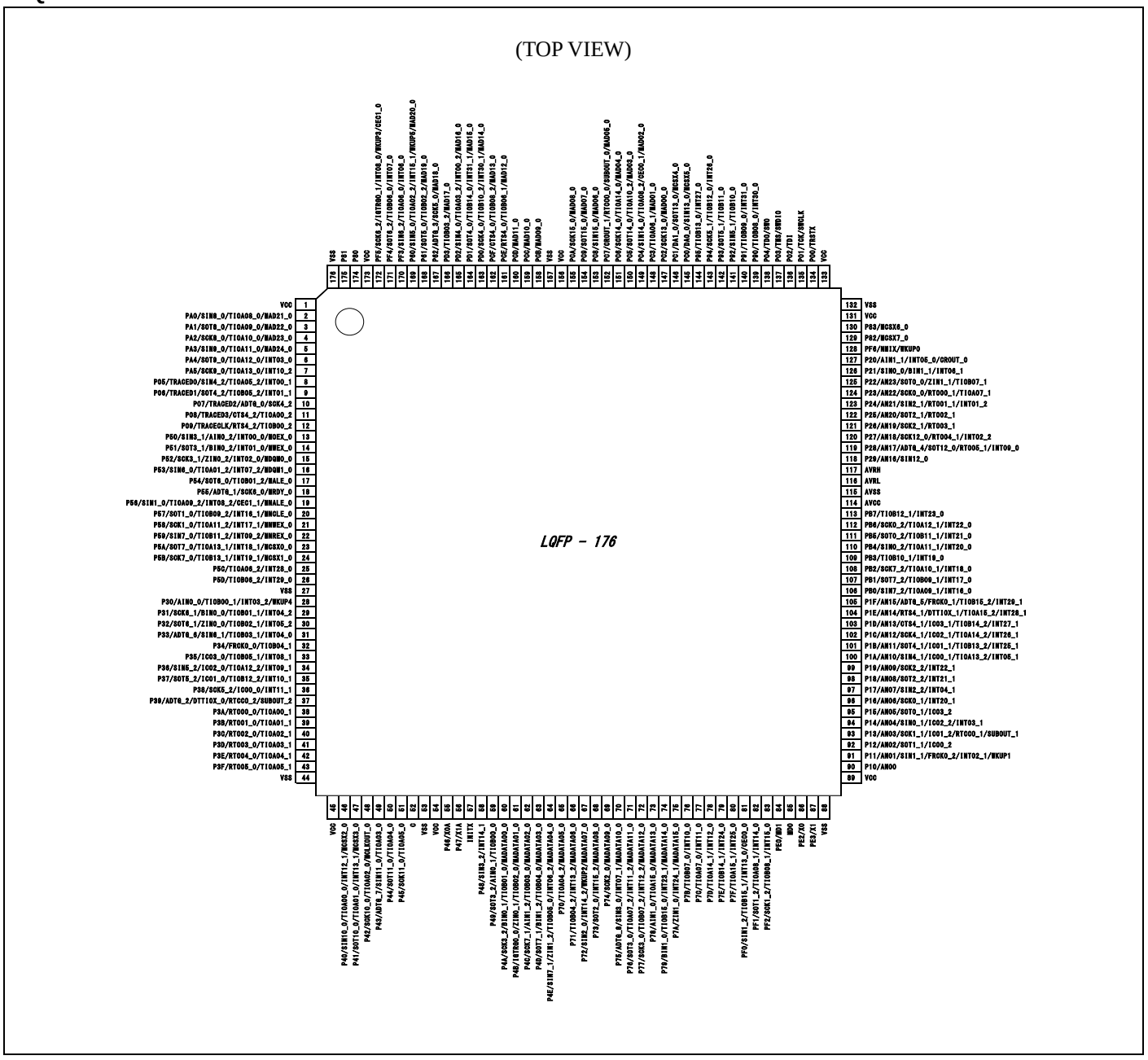
❍: Supported

Note:

- *See "Package Dimensions" for detailed information on each package.*

3. Pin Assignment

LQP176

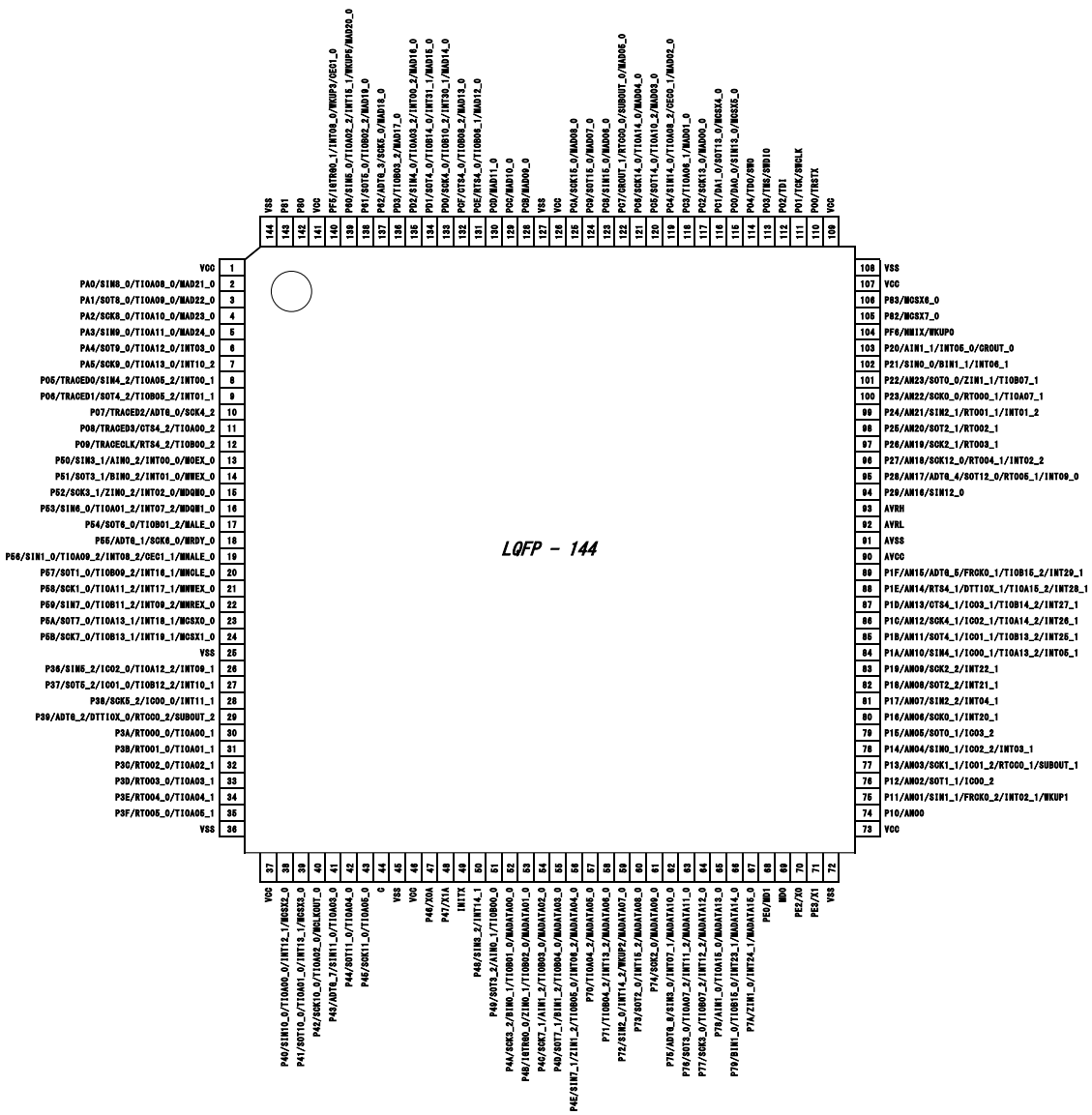


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LQS144

(TOP VIEW)

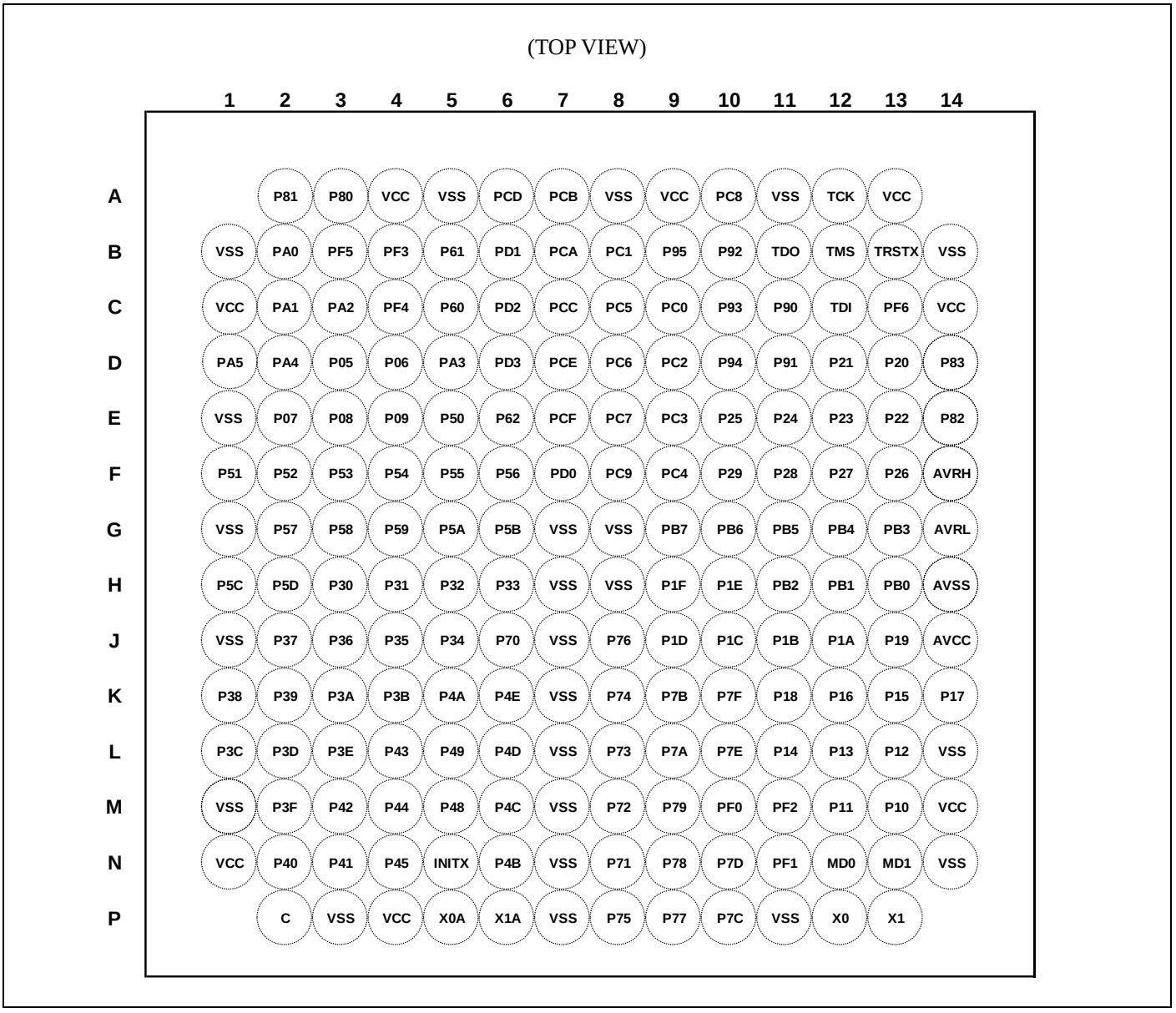


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LBE192

(TOP VIEW)



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
1	1	C1	VCC	-	
2	2	B2	PA0 SIN8_0 TIOA08_0 MAD21_0	I*	J
3	3	C2	PA1 SOT8_0 TIOA09_0 MAD22_0	I*	J
4	4	C3	PA2 SCK8_0 TIOA10_0 MAD23_0	I*	J
5	5	D5	PA3 SIN9_0 TIOA11_0 MAD24_0	I*	J
6	6	D2	PA4 SOT9_0 TIOA12_0 INT03_0	I*	K
7	7	D1	PA5 SCK9_0 TIOA13_0 INT10_2	I*	K
8	8	D3	P05 TRACED0 SIN4_2 TIOA05_2 INT00_1	E	Q
9	9	D4	P06 TRACED1 SOT4_2 TIOB05_2 INT01_1	E	Q

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
10	10	E2	P07	E	P
			TRACED2		
			ADTG_0		
			SCK4_2		
11	11	E3	P08	E	P
			TRACED3		
			CTS4_2		
			TIOA00_2		
12	12	E4	P09	E	P
			TRACECLK		
			RTS4_2		
			TIOB00_2		
13	13	E5	P50	E	K
			SIN3_1		
			AIN0_2		
			INT00_0		
			MOEX_0		
14	14	F1	P51	E	K
			SOT3_1		
			BIN0_2		
			INT01_0		
			MWEX_0		
15	15	F2	P52	E	K
			SCK3_1		
			ZIN0_2		
			INT02_0		
			MDQM0_0		

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
16	16	F3	P53	E	K
			SIN6_0		
			TIOA01_2		
			INT07_2		
			MDQM1_0		
17	17	F4	P54	E	J
			SOT6_0		
			TIOB01_2		
			MALE_0		
18	18	F5	P55	E	J
			ADTG_1		
			SCK6_0		
			MRDY_0		
19	19	F6	P56	I*	S
			SIN1_0		
			TIOA09_2		
			INT08_2		
			CEC1_1		
			MNALE_0		
20	20	G2	P57	I*	K
			SOT1_0		
			TIOB09_2		
			INT16_1		
			MNCLE_0		
21	21	G3	P58	I*	K
			SCK1_0		
			TIOA11_2		
			INT17_1		
			MNWEX_0		
22	22	G4	P59	E	K
			SIN7_0		
			TIOB11_2		
			INT09_2		
			MNREX_0		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
23	23	G5	P5A SOT7_0 TIOA13_1 INT18_1 MCSX0_0	E	K
24	24	G6	P5B SCK7_0 TIOB13_1 INT19_1 MCSX1_0	E	K
25	-	H1	P5C TIOA06_2 INT28_0	E	K
26	-	H2	P5D TIOB06_2 INT29_0	E	K
27	25	A5	VSS	-	
28	-	H3	P30 AIN0_0 TIOB00_1 INT03_2 WKUP4	E	U
29	-	H4	P31 SCK6_1 BIN0_0 TIOB01_1 INT04_2	E	K
30	-	H5	P32 SOT6_1 ZIN0_0 TIOB02_1 INT05_2	E	K
31	-	H6	P33 ADTG_6 SIN6_1 TIOB03_1 INT04_0	E	K

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
32	-	J5	P34 FRCK0_0 TIOB04_1	E	J
33	-	J4	P35 IC03_0 TIOB05_1 INT08_1	E	K
34	26	J3	P36 SIN5_2 IC02_0 TIOA12_2 INT09_1	E	K
35	27	J2	P37 SOT5_2 IC01_0 TIOB12_2 INT10_1	E	K
36	28	K1	P38 SCK5_2 IC00_0 INT11_1	E	K
37	29	K2	P39 ADTG_2 DTTI0X_0 RTCCO_2 SUBOUT_2	E	J
38	30	K3	P3A RTO00_0 TIOA00_1	F	J
39	31	K4	P3B RTO01_0 TIOA01_1	F	J
40	32	L1	P3C RTO02_0 TIOA02_1	F	J
41	33	L2	P3D RTO03_0 TIOA03_1	F	J
42	34	L3	P3E RTO04_0 TIOA04_1	F	J

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
43	35	M2	P3F RTO05_0 TIOA05_1	F	J
44	36	A8	VSS	-	
45	37	N1	VCC	-	
46	38	N2	P40 SIN10_0 TIOA00_0 INT12_1 MCSX2_0	E	K
47	39	N3	P41 SOT10_0 TIOA01_0 INT13_1 MCSX3_0	E	K
48	40	M3	P42 SCK10_0 TIOA02_0 MCLKOUT_0	E	J
49	41	L4	P43 ADTG_7 SIN11_0 TIOA03_0	I*	J
50	42	M4	P44 SOT11_0 TIOA04_0	I*	J
51	43	N4	P45 SCK11_0 TIOA05_0	I*	J
52	44	P2	C	-	
53	45	A11	VSS	-	
54	46	P4	VCC	-	
55	47	P5	P46 X0A	D	F
56	48	P6	P47 X1A	D	G
57	49	N5	INITX	B	C
58	50	M5	P48 SIN3_2 INT14_1	E	K

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
59	51	L5	P49 SOT3_2 AIN0_1 TIOB00_0	E	J
60	52	K5	P4A SCK3_2 BIN0_1 TIOB01_0 MADATA00_0	E	J
61	53	N6	P4B IGTRG0_0 ZIN0_1 TIOB02_0 MADATA01_0	E	J
62	54	M6	P4C SCK7_1 AIN1_2 TIOB03_0 MADATA02_0	E	J
63	55	L6	P4D SOT7_1 BIN1_2 TIOB04_0 MADATA03_0	E	J
64	56	K6	P4E SIN7_1 ZIN1_2 TIOB05_0 INT06_2 MADATA04_0	E	K
65	57	J6	P70 TIOA04_2 MADATA05_0	E	J
66	58	N8	P71 TIOB04_2 INT13_2 MADATA06_0	E	K

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
67	59	M8	P72 SIN2_0 INT14_2 WKUP2 MADATA07_0	E	U
68	60	L8	P73 SOT2_0 INT15_2 MADATA08_0	E	K
69	61	K8	P74 SCK2_0 MADATA09_0	E	J
70	62	P8	P75 ADTG_8 SIN3_0 INT07_1 MADATA10_0	E	K
71	63	J8	P76 SOT3_0 TIOA07_2 INT11_2 MADATA11_0	E	K
72	64	P9	P77 SCK3_0 TIOB07_2 INT12_2 MADATA12_0	E	K
73	65	N9	P78 AIN1_0 TIOA15_0 MADATA13_0	E	J
74	66	M9	P79 BIN1_0 TIOB15_0 INT23_1 MADATA14_0	E	K
-	-	M1	VSS	-	
-	-	P3	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
75	67	L9	P7A	E	K
			ZIN1_0		
			INT24_1		
			MADATA15_0		
76	-	K9	P7B	E	K
			TIOB07_0		
			INT10_0		
77	-	P10	P7C	E	K
			TIOA07_0		
			INT11_0		
78	-	N10	P7D	E	K
			TIOA14_1		
			INT12_0		
79	-	L10	P7E	E	K
			TIOB14_1		
			INT24_0		
80	-	K10	P7F	E	K
			TIOA15_1		
			INT25_0		
81	-	M10	PF0	I*	S
			SIN1_2		
			TIOB15_1		
			INT13_0		
			CEC0_0		
82	-	N11	PF1	I*	K
			SOT1_2		
			TIOA08_1		
			INT14_0		
83	-	M11	PF2	I*	K
			SCK1_2		
			TIOB08_1		
			INT15_0		
84	68	N13	PE0	C	E
			MD1		
85	69	N12	MD0	J	D
86	70	P12	PE2	A	A
			X0		
87	71	P13	PE3	A	B
			X1		
88	72	E1	VSS	-	
89	73	M14	VCC	-	
-	-	P7	VSS	-	
-	-	N7	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
90	74	M13	P10	G	L
			AN00		
91	75	M12	P11	G	N
			AN01		
			SIN1_1		
			FRCK0_2		
			INT02_1		
			WKUP1		
92	76	L13	P12	G	L
			AN02		
			SOT1_1		
			IC00_2		
93	77	L12	P13	G	L
			AN03		
			SCK1_1		
			IC01_2		
			RTCCO_1		
			SUBOUT_1		
94	78	L11	P14	G	M
			AN04		
			SIN0_1		
			IC02_2		
			INT03_1		
95	79	K13	P15	G	L
			AN05		
			SOT0_1		
			IC03_2		
96	80	K12	P16	G	M
			AN06		
			SCK0_1		
			INT20_1		
97	81	K14	P17	G	M
			AN07		
			SIN2_2		
			INT04_1		
-	-	M7	VSS	-	
-	-	L7	VSS	-	
-	-	K7	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
98	82	K11	P18	G	M
			AN08		
			SOT2_2		
			INT21_1		
99	83	J13	P19	G	M
			AN09		
			SCK2_2		
			INT22_1		
100	84	J12	P1A	G	M
			AN10		
			SIN4_1		
			IC00_1		
			TIOA13_2		
			INT05_1		
101	85	J11	P1B	G	M
			AN11		
			SOT4_1		
			IC01_1		
			TIOB13_2		
			INT25_1		
102	86	J10	P1C	G	M
			AN12		
			SCK4_1		
			IC02_1		
			TIOA14_2		
			INT26_1		
103	87	J9	P1D	G	M
			AN13		
			CTS4_1		
			IC03_1		
			TIOB14_2		
			INT27_1		
104	88	H10	P1E	G	M
			AN14		
			RTS4_1		
			DTTI0X_1		
			TIOA15_2		
			INT28_1		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
105	89	H9	P1F AN15 ADTG_5 FRCK0_1 TIOB15_2 INT29_1	G	M
106	-	H13	PB0 SIN7_2 TIOA09_1 INT16_0	E	K
107	-	H12	PB1 SOT7_2 TIOB09_1 INT17_0	E	K
108	-	H11	PB2 SCK7_2 TIOA10_1 INT18_0	E	K
109	-	G13	PB3 TIOB10_1 INT19_0	E	K
110	-	G12	PB4 SIN0_2 TIOA11_1 INT20_0	E	K
111	-	G11	PB5 SOT0_2 TIOB11_1 INT21_0	E	K
112	-	G10	PB6 SCK0_2 TIOA12_1 INT22_0	E	K
113	-	G9	PB7 TIOB12_1 INT23_0	E	K
114	90	J14	AVCC	-	
115	91	H14	AVSS	-	
-	-	J7	VSS	-	
-	-	P11	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
116	92	G14	AVRL	-	
117	93	F14	AVRH	-	
118	94	F10	P29	G	L
			AN16		
			SIN12_0		
119	95	F11	P28	G	M
			AN17		
			ADTG_4		
			SOT12_0		
			RTO05_1		
			INT09_0		
120	96	F12	P27	G	M
			AN18		
			SCK12_0		
			RTO04_1		
			INT02_2		
121	97	F13	P26	G	L
			AN19		
			SCK2_1		
			RTO03_1		
122	98	E10	P25	G	L
			AN20		
			SOT2_1		
			RTO02_1		
123	99	E11	P24	G	M
			AN21		
			SIN2_1		
			RTO01_1		
			INT01_2		

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
124	100	E12	P23	G	L
			AN22		
			SCK0_0		
			RTO00_1		
			TIOA07_1		
125	101	E13	P22	G	L
			AN23		
			SOT0_0		
			ZIN1_1		
			TIOB07_1		
126	102	D12	P21	E	K
			SIN0_0		
			BIN1_1		
			INT06_1		
127	103	D13	P20	E	K
			AIN1_1		
			INT05_0		
			CROUT_0		
128	104	C13	PF6	I*	H
			NMIX		
			WKUP0		
129	105	E14	P82	E	J
			MCSX7_0		
130	106	D14	P83	E	J
			MCSX6_0		
131	107	C14	VCC	-	
132	108	G7	VSS	-	
133	109	A13	VCC	-	
134	110	B13	P00	E	I
			TRSTX		
135	111	A12	P01	E	I
			TCK		
			SWCLK		
136	112	C12	P02	E	I
			TDI		
137	113	B12	P03	E	I
			TMS		
			SWDIO		
138	114	B11	P04	E	I
			TDO		
			SWO		
139	-	C11	P90	E	K
			TIOB08_0		
			INT30_0		
-	-	N14	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
140	-	D11	P91 TIOB09_0 INT31_0	E	K
141	-	B10	P92 SIN5_1 TIOB10_0	E	J
142	-	C10	P93 SOT5_1 TIOB11_0	E	J
143	-	D10	P94 SCK5_1 TIOB12_0 INT26_0	E	K
144	-	B9	P95 TIOB13_0 INT27_0	E	K
145	115	C9	PC0 DA0_0 SIN13_0 MCSX5_0	H	O
146	116	B8	PC1 DA1_0 SOT13_0 MCSX4_0	H	O
147	117	D9	PC2 SCK13_0 MAD00_0	E	J
148	118	E9	PC3 TIOA06_1 MAD01_0	E	J
149	119	F9	PC4 SIN14_0 TIOA08_2 CEC0_1 MAD02_0	I*	R
150	120	C8	PC5 SOT14_0 TIOA10_2 MAD03_0	I*	J
-	-	L14	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
151	121	D8	PC6	I*	J
			SCK14_0		
			TIOA14_0		
			MAD04_0		
152	122	E8	PC7	E	J
			CROUT_1		
			RTCCO_0		
			SUBOUT_0		
			MAD05_0		
153	123	A10	PC8	E	J
			SIN15_0		
			MAD06_0		
154	124	F8	PC9	E	J
			SOT15_0		
			MAD07_0		
155	125	B7	PCA	E	J
			SCK15_0		
			MAD08_0		
156	126	A9	VCC	-	
157	127	G8	VSS	-	
158	128	A7	PCB	E	J
			MAD09_0		
159	129	C7	PCC	E	J
			MAD10_0		
160	130	A6	PCD	E	J
			MAD11_0		
161	131	D7	PCE	E	J
			RTS4_0		
			TIOB06_1		
			MAD12_0		
162	132	E7	PCF	E	J
			CTS4_0		
			TIOB08_2		
			MAD13_0		
163	133	F7	PD0	E	K
			SCK4_0		
			TIOB10_2		
			INT30_1		
			MAD14_0		
164	134	B6	PD1	E	K
			SOT4_0		
			TIOB14_0		
			INT31_1		
			MAD15_0		
-	-	B14	VSS	-	
-	-	H7	VSS	-	
-	-	B1	VSS	-	
-	-	G1	VSS	-	

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
165	135	C6	PD2 SIN4_0 TIOA03_2 INT00_2 MAD16_0	E	K
166	136	D6	PD3 TIOB03_2 MAD17_0	E	J
167	137	E6	P62 ADTG_3 SCK5_0 MAD18_0	E	J
168	138	B5	P61 SOT5_0 TIOB02_2 MAD19_0	E	J
169	139	C5	P60 SIN5_0 TIOA02_2 INT15_1 WKUP5 MAD20_0	E	U
170	-	B4	PF3 SIN6_2 TIOA06_0 INT06_0	I*	K
171	-	C4	PF4 SOT6_2 TIOB06_0 INT07_0	I*	K
172	140 -	B3	PF5 IGTRG0_1 INT08_0 WKUP3 CEC1_0 SCK6_2	I*	T
173	141	A4	VCC	-	
174	142	A3	P80	K	V
175	143	A2	P81	K	V
176	144	H8	VSS	-	
-	-	J1	VSS	-	

*: 5V tolerant I/O

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
ADC	ADTG_0	A/D converter external trigger input pin	10	10	E2
	ADTG_1		18	18	F5
	ADTG_2		37	29	K2
	ADTG_3		167	137	E6
	ADTG_4		119	95	F11
	ADTG_5		105	89	H9
	ADTG_6		31	-	H6
	ADTG_7		49	41	L4
	ADTG_8		70	62	P8
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	90	74	M13
	AN01		91	75	M12
	AN02		92	76	L13
	AN03		93	77	L12
	AN04		94	78	L11
	AN05		95	79	K13
	AN06		96	80	K12
	AN07		97	81	K14
	AN08		98	82	K11
	AN09		99	83	J13
	AN10		100	84	J12
	AN11		101	85	J11
	AN12		102	86	J10
	AN13		103	87	J9
	AN14		104	88	H10
	AN15		105	89	H9
	AN16		118	94	F10
	AN17		119	95	F11
	AN18		120	96	F12
	AN19		121	97	F13
	AN20		122	98	E10
	AN21		123	99	E11
	AN22		124	100	E12
	AN23		125	101	E13

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 0	TIOA00_0	Base timer ch.0 TIOA pin	46	38	N2
	TIOA00_1		38	30	K3
	TIOA00_2		11	11	E3
	TIOB00_0	Base timer ch.0 TIOB pin	59	51	L5
	TIOB00_1		28	-	H3
	TIOB00_2		12	12	E4
Base Timer 1	TIOA01_0	Base timer ch.1 TIOA pin	47	39	N3
	TIOA01_1		39	31	K4
	TIOA01_2		16	16	F3
	TIOB01_0	Base timer ch.1 TIOB pin	60	52	K5
	TIOB01_1		29	-	H4
	TIOB01_2		17	17	F4
Base Timer 2	TIOA02_0	Base timer ch.2 TIOA pin	48	40	M3
	TIOA02_1		40	32	L1
	TIOA02_2		169	139	C5
	TIOB02_0	Base timer ch.2 TIOB pin	61	53	N6
	TIOB02_1		30	-	H5
	TIOB02_2		168	138	B5
Base Timer 3	TIOA03_0	Base timer ch.3 TIOA pin	49	41	L4
	TIOA03_1		41	33	L2
	TIOA03_2		165	135	C6
	TIOB03_0	Base timer ch.3 TIOB pin	62	54	M6
	TIOB03_1		31	-	H6
	TIOB03_2		166	136	D6
Base Timer 4	TIOA04_0	Base timer ch.4 TIOA pin	50	42	M4
	TIOA04_1		42	34	L3
	TIOA04_2		65	57	J6
	TIOB04_0	Base timer ch.4 TIOB pin	63	55	L6
	TIOB04_1		32	-	J5
	TIOB04_2		66	58	N8
Base Timer 5	TIOA05_0	Base timer ch.5 TIOA pin	51	43	N4
	TIOA05_1		43	35	M2
	TIOA05_2		8	8	D3
	TIOB05_0	Base timer ch.5 TIOB pin	64	56	K6
	TIOB05_1		33	-	J4
	TIOB05_2		9	9	D4
Base Timer 6	TIOA06_0	Base timer ch.6 TIOA pin	170	-	B4
	TIOA06_1		148	118	E9
	TIOA06_2		25	-	H1
	TIOB06_0	Base timer ch.6 TIOB pin	171	-	C4
	TIOB06_1		161	131	D7
	TIOB06_2		26	-	H2

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 7	TIOA07_0	Base timer ch.7 TIOA pin	77	-	P10
	TIOA07_1		124	100	E12
	TIOA07_2		71	63	J8
	TIOB07_0	Base timer ch.7 TIOB pin	76	-	K9
	TIOB07_1		125	101	E13
	TIOB07_2		72	64	P9
Base Timer 8	TIOA08_0	Base timer ch.8 TIOA pin	2	2	B2
	TIOA08_1		82	-	N11
	TIOA08_2		149	119	F9
	TIOB08_0	Base timer ch.8 TIOB pin	139	-	C11
	TIOB08_1		83	-	M11
	TIOB08_2		162	132	E7
Base Timer 9	TIOA09_0	Base timer ch.9 TIOA pin	3	3	C2
	TIOA09_1		106	-	H13
	TIOA09_2		19	19	F6
	TIOB09_0	Base timer ch.9 TIOB pin	140	-	D11
	TIOB09_1		107	-	H12
	TIOB09_2		20	20	G2
Base Timer 10	TIOA10_0	Base timer ch.10 TIOA pin	4	4	C3
	TIOA10_1		108	-	H11
	TIOA10_2		150	120	C8
	TIOB10_0	Base timer ch.10 TIOB pin	141	-	B10
	TIOB10_1		109	-	G13
	TIOB10_2		163	133	F7
Base Timer 11	TIOA11_0	Base timer ch.11 TIOA pin	5	5	D5
	TIOA11_1		110	-	G12
	TIOA11_2		21	21	G3
	TIOB11_0	Base timer ch.11 TIOB pin	142	-	C10
	TIOB11_1		111	-	G11
	TIOB11_2		22	22	G4
Base Timer 12	TIOA12_0	Base timer ch.12 TIOA pin	6	6	D2
	TIOA12_1		112	-	G10
	TIOA12_2		34	26	J3
	TIOB12_0	Base timer ch.12 TIOB pin	143	-	D10
	TIOB12_1		113	-	G9
	TIOB12_2		35	27	J2
Base Timer 13	TIOA13_0	Base timer ch.13 TIOA pin	7	7	D1
	TIOA13_1		23	23	G5
	TIOA13_2		100	84	J12
	TIOB13_0	Base timer ch.13 TIOB pin	144	-	B9
	TIOB13_1		24	24	G6
	TIOB13_2		101	85	J11

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 14	TIOA14_0	Base timer ch.14 TIOA pin	151	121	D8
	TIOA14_1		78	-	N10
	TIOA14_2		102	86	J10
	TIOB14_0	Base timer ch.14 TIOB pin	164	134	B6
	TIOB14_1		79	-	L10
	TIOB14_2		103	87	J9
Base Timer 15	TIOA15_0	Base timer ch.15 TIOA pin	73	65	N9
	TIOA15_1		80	-	K10
	TIOA15_2		104	88	H10
	TIOB15_0	Base timer ch.15 TIOB pin	74	66	M9
	TIOB15_1		81	-	M10
	TIOB15_2		105	89	H9
Debugger	SWCLK	Serial wire debug interface clock input	135	111	A12
	SWDIO	Serial wire debug interface data input / output	137	113	B12
	SWO	Serial wire viewer output	138	114	B11
	TCK	JTAG test clock input	135	111	A12
	TDI	JTAG test data input	136	112	C12
	TDO	JTAG debug data output	138	114	B11
	TMS	JTAG test mode state input/output	137	113	B12
	TRACECLK	Trace CLK output of ETM	12	12	E4
	TRACED0	Trace data output of ETM	8	8	D3
	TRACED1		9	9	D4
	TRACED2		10	10	E2
	TRACED3		11	11	E3
	TRSTX	JTAG test reset Input	134	110	B13

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Bus	MAD00_0	External bus interface address bus	147	117	D9
	MAD01_0		148	118	E9
	MAD02_0		149	119	F9
	MAD03_0		150	120	C8
	MAD04_0		151	121	D8
	MAD05_0		152	122	E8
	MAD06_0		153	123	A10
	MAD07_0		154	124	F8
	MAD08_0		155	125	B7
	MAD09_0		158	128	A7
	MAD10_0		159	129	C7
	MAD11_0		160	130	A6
	MAD12_0		161	131	D7
	MAD13_0		162	132	E7
	MAD14_0		163	133	F7
	MAD15_0		164	134	B6
	MAD16_0		165	135	C6
	MAD17_0		166	136	D6
	MAD18_0		167	137	E6
	MAD19_0		168	138	B5
	MAD20_0		169	139	C5
	MAD21_0		2	2	B2
	MAD22_0		3	3	C2
	MAD23_0		4	4	C3
	MAD24_0		5	5	D5
	MCSX0_0	External bus interface chip select output pin	23	23	G5
	MCSX1_0		24	24	G6
	MCSX2_0		46	38	N2
	MCSX3_0		47	39	N3
	MCSX4_0		146	116	B8
	MCSX5_0		145	115	C9
	MCSX6_0		130	106	D14
	MCSX7_0		129	105	E14
	MDQM0_0	External bus interface byte mask signal output	15	15	F2
	MDQM1_0		16	16	F3
	MOEX_0	External bus interface read enable signal for SRAM	13	13	E5
	MWEX_0	External bus interface write enable signal for SRAM	14	14	F1

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Bus	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	19	19	F6
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	20	20	G2
	MNREX_0	External bus interface read enable signal to control NAND Flash	22	22	G4
	MNWEX_0	External bus interface write enable signal to control NAND Flash	21	21	G3
	MADATA00_0	External bus interface data bus (Address / data multiplex bus)	60	52	K5
	MADATA01_0		61	53	N6
	MADATA02_0		62	54	M6
	MADATA03_0		63	55	L6
	MADATA04_0		64	56	K6
	MADATA05_0		65	57	J6
	MADATA06_0		66	58	N8
	MADATA07_0		67	59	M8
	MADATA08_0		68	60	L8
	MADATA09_0		69	61	K8
	MADATA10_0		70	62	P8
	MADATA11_0		71	63	J8
	MADATA12_0		72	64	P9
	MADATA13_0		73	65	N9
	MADATA14_0		74	66	M9
	MADATA15_0		75	67	L9
	MALE_0	External bus interface Address Latch enable output signal for multiplex	17	17	F4
	MRDY_0	External bus interface external RDY input signal	18	18	F5
	MCLKOUT_0	External bus interface external clock output	48	40	M3

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT00_0	External interrupt request 00 input pin	13	13	E5
	INT00_1		8	8	D3
	INT00_2		165	135	C6
	INT01_0	External interrupt request 01 input pin	14	14	F1
	INT01_1		9	9	D4
	INT01_2		123	99	E11
	INT02_0	External interrupt request 02 input pin	15	15	F2
	INT02_1		91	75	M12
	INT02_2		120	96	F12
	INT03_0	External interrupt request 03 input pin	6	6	D2
	INT03_1		94	78	L11
	INT03_2		28	-	H3
	INT04_0	External interrupt request 04 input pin	31	-	H6
	INT04_1		97	81	K14
	INT04_2		29	-	H4
	INT05_0	External interrupt request 05 input pin	127	103	D13
	INT05_1		100	84	J12
	INT05_2		30	-	H5
	INT06_0	External interrupt request 06 input pin	170	-	B4
	INT06_1		126	102	D12
	INT06_2		64	56	K6
	INT07_0	External interrupt request 07 input pin	171	-	C4
	INT07_1		70	62	P8
	INT07_2		16	16	F3
	INT08_0	External interrupt request 08 input pin	172	140	B3
	INT08_1		33	-	J4
	INT08_2		19	19	F6
	INT09_0	External interrupt request 09 input pin	119	95	F11
	INT09_1		34	26	J3
	INT09_2		22	22	G4
	INT10_0	External interrupt request 10 input pin	76	-	K9
	INT10_1		35	27	J2
	INT10_2		7	7	D1
	INT11_0	External interrupt request 11 input pin	77	-	P10
	INT11_1		36	28	K1
	INT11_2		71	63	J8
	INT12_0	External interrupt request 12 input pin	78	-	N10
	INT12_1		46	38	N2
	INT12_2		72	64	P9
	INT13_0	External interrupt request 13 input pin	81	-	M10
	INT13_1		47	39	N3
	INT13_2		66	58	N8
	INT14_0	External interrupt request 14 input pin	82	-	N11
	INT14_1		58	50	M5
	INT14_2		67	59	M8

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT15_0	External interrupt request 15 input pin	83	-	M11
	INT15_1		169	139	C5
	INT15_2		68	60	L8
	INT16_0	External interrupt request 16 input pin	106	-	H13
	INT16_1		20	20	G2
	INT17_0	External interrupt request 17 input pin	107	-	H12
	INT17_1		21	21	G3
	INT18_0	External interrupt request 18 input pin	108	-	H11
	INT18_1		23	23	G5
	INT19_0	External interrupt request 19 input pin	109	-	G13
	INT19_1		24	24	G6
	INT20_0	External interrupt request 20 input pin	110	-	G12
	INT20_1		96	80	K12
	INT21_0	External interrupt request 21 input pin	111	-	G11
	INT21_1		98	82	K11
	INT22_0	External interrupt request 22 input pin	112	-	G10
	INT22_1		99	83	J13
	INT23_0	External interrupt request 23 input pin	113	-	G9
	INT23_1		74	66	M9
	INT24_0	External interrupt request 24 input pin	79	-	L10
	INT24_1		75	67	L9
	INT25_0	External interrupt request 25 input pin	80	-	K10
	INT25_1		101	85	J11
	INT26_0	External interrupt request 26 input pin	143	-	D10
	INT26_1		102	86	J10
	INT27_0	External interrupt request 27 input pin	144	-	B9
	INT27_1		103	87	J9
	INT28_0	External interrupt request 28 input pin	25	-	H1
	INT28_1		104	88	H10
	INT29_0	External interrupt request 29 input pin	26	-	H2
	INT29_1		105	89	H9
	INT30_0	External interrupt request 30 input pin	139	-	C11
	INT30_1		163	133	F7
	INT31_0	External interrupt request 31 input pin	140	-	D11
	INT31_1		164	134	B6
	NMIX	Non-Maskable Interrupt input	128	104	C13

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P00	General-purpose I/O port 0	134	110	B13
	P01		135	111	A12
	P02		136	112	C12
	P03		137	113	B12
	P04		138	114	B11
	P05		8	8	D3
	P06		9	9	D4
	P07		10	10	E2
	P08		11	11	E3
	P09		12	12	E4
	P10	General-purpose I/O port 1	90	74	M13
	P11		91	75	M12
	P12		92	76	L13
	P13		93	77	L12
	P14		94	78	L11
	P15		95	79	K13
	P16		96	80	K12
	P17		97	81	K14
	P18		98	82	K11
	P19		99	83	J13
	P1A		100	84	J12
	P1B		101	85	J11
	P1C		102	86	J10
	P1D		103	87	J9
	P1E		104	88	H10
	P1F		105	89	H9
	P20	General-purpose I/O port 2	127	103	D13
	P21		126	102	D12
	P22		125	101	E13
	P23		124	100	E12
	P24		123	99	E11
	P25		122	98	E10
	P26		121	97	F13
	P27		120	96	F12
	P28		119	95	F11
	P29		118	94	F10

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P30	General-purpose I/O port 3	28	-	H3
	P31		29	-	H4
	P32		30	-	H5
	P33		31	-	H6
	P34		32	-	J5
	P35		33	-	J4
	P36		34	26	J3
	P37		35	27	J2
	P38		36	28	K1
	P39		37	29	K2
	P3A		38	30	K3
	P3B		39	31	K4
	P3C		40	32	L1
	P3D		41	33	L2
	P3E		42	34	L3
	P3F		43	35	M2
	P40	General-purpose I/O port 4	46	38	N2
	P41		47	39	N3
	P42		48	40	M3
	P43		49	41	L4
	P44		50	42	M4
	P45		51	43	N4
	P46		55	47	P5
	P47		56	48	P6
	P48		58	50	M5
	P49		59	51	L5
	P4A		60	52	K5
	P4B		61	53	N6
	P4C		62	54	M6
	P4D		63	55	L6
	P4E		64	56	K6
	P50	General-purpose I/O port 5	13	13	E5
	P51		14	14	F1
	P52		15	15	F2
	P53		16	16	F3
	P54		17	17	F4
	P55		18	18	F5
	P56		19	19	F6
	P57		20	20	G2
	P58		21	21	G3
	P59		22	22	G4
	P5A		23	23	G5
	P5B		24	24	G6
	P5C		25	-	H1
	P5D		26	-	H2

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P60	General-purpose I/O port 6	169	139	C5
	P61		168	138	B5
	P62		167	137	E6
	P70	General-purpose I/O port 7	65	57	J6
	P71		66	58	N8
	P72		67	59	M8
	P73		68	60	L8
	P74		69	61	K8
	P75		70	62	P8
	P76		71	63	J8
	P77		72	64	P9
	P78		73	65	N9
	P79		74	66	M9
	P7A		75	67	L9
	P7B		76	-	K9
	P7C		77	-	P10
	P7D		78	-	N10
	P7E		79	-	L10
	P7F		80	-	K10
	P80	General-purpose I/O port 8	174	142	A3
	P81		175	143	A2
	P82		129	105	E14
	P83		130	106	D14
	P90	General-purpose I/O port 9	139	-	C11
	P91		140	-	D11
	P92		141	-	B10
	P93		142	-	C10
	P94		143	-	D10
	P95		144	-	B9
	PA0	General-purpose I/O port A	2	2	B2
	PA1		3	3	C2
	PA2		4	4	C3
	PA3		5	5	D5
	PA4		6	6	D2
	PA5		7	7	D1
	PB0	General-purpose I/O port B	106	-	H13
	PB1		107	-	H12
	PB2		108	-	H11
	PB3		109	-	G13
	PB4		110	-	G12
	PB5		111	-	G11
	PB6		112	-	G10
	PB7		113	-	G9

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	PC0	General-purpose I/O port C	145	115	C9
	PC1		146	116	B8
	PC2		147	117	D9
	PC3		148	118	E9
	PC4		149	119	F9
	PC5		150	120	C8
	PC6		151	121	D8
	PC7		152	122	E8
	PC8		153	123	A10
	PC9		154	124	F8
	PCA		155	125	B7
	PCB		158	128	A7
	PCC		159	129	C7
	PCD		160	130	A6
	PCE		161	131	D7
	PCF		162	132	E7
	PD0	General-purpose I/O port D	163	133	F7
	PD1		164	134	B6
	PD2		165	135	C6
	PD3		166	136	D6
	PE0	General-purpose I/O port E	84	68	N13
	PE2		86	70	P12
	PE3		87	71	P13
	PF0	General-purpose I/O port F*	81	-	M10
	PF1		82	-	N11
	PF2		83	-	M11
	PF3		170	-	B4
	PF4		171	-	C4
	PF5		172	140	B3
	PF6		128	104	C13

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin	126	102	D12
	SIN0_1		94	78	L11
	SIN0_2		110	-	G12
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	125	101	E13
	SOT0_1 (SDA0_1)		95	79	K13
	SOT0_2 (SDA0_2)		111	-	G11
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	124	100	E12
	SCK0_1 (SCL0_1)		96	80	K12
	SCK0_2 (SCL0_2)		112	-	G10
Multi Function Serial 1	SIN1_0	Multifunction serial interface ch.1 input pin	19	19	F6
	SIN1_1		91	75	M12
	SIN1_2		81	-	M10
	SOT1_0 (SDA1_0)	Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	20	20	G2
	SOT1_1 (SDA1_1)		92	76	L13
	SOT1_2 (SDA1_2)		82	-	N11
	SCK1_0 (SCL1_0)	Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	21	21	G3
	SCK1_1 (SCL1_1)		93	77	L12
	SCK1_2 (SCL1_2)		83	-	M11

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 2	SIN2_0	Multifunction serial interface ch.2 input pin	67	59	M8
	SIN2_1		123	99	E11
	SIN2_2		97	81	K14
	SOT2_0 (SDA2_0)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	68	60	L8
	SOT2_1 (SDA2_1)		122	98	E10
	SOT2_2 (SDA2_2)		98	82	K11
	SCK2_0 (SCL2_0)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	69	61	K8
	SCK2_1 (SCL2_1)		121	97	F13
	SCK2_2 (SCL2_2)		99	83	J13
Multi Function Serial 3	SIN3_0	Multifunction serial interface ch.3 input pin	70	62	P8
	SIN3_1		13	13	E5
	SIN3_2		58	50	M5
	SOT3_0 (SDA3_0)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	71	63	J8
	SOT3_1 (SDA3_1)		14	14	F1
	SOT3_2 (SDA3_2)		59	51	L5
	SCK3_0 (SCL3_0)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	72	64	P9
	SCK3_1 (SCL3_1)		15	15	F2
	SCK3_2 (SCL3_2)		60	52	K5

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin	165	135	C6
	SIN4_1		100	84	J12
	SIN4_2		8	8	D3
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	164	134	B6
	SOT4_1 (SDA4_1)		101	85	J11
	SOT4_2 (SDA4_2)		9	9	D4
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	163	133	F7
	SCK4_1 (SCL4_1)		102	86	J10
	SCK4_2 (SCL4_2)		10	10	E2
	RTS4_0	Multifunction serial interface ch.4 RTS output pin	161	131	D7
	RTS4_1		104	88	H10
	RTS4_2		12	12	E4
	CTS4_0	Multifunction serial interface ch.4 CTS input pin	162	132	E7
	CTS4_1		103	87	J9
	CTS4_2		11	11	E3
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin	169	139	C5
	SIN5_1		141	-	B10
	SIN5_2		34	26	J3
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	168	138	B5
	SOT5_1 (SDA5_1)		142	-	C10
	SOT5_2 (SDA5_2)		35	27	J2
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	167	137	E6
	SCK5_1 (SCL5_1)		143	-	D10
	SCK5_2 (SCL5_2)		36	28	K1

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin	16	16	F3
	SIN6_1		31	-	H6
	SIN6_2		170	-	B4
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	17	17	F4
	SOT6_1 (SDA6_1)		30	-	H5
	SOT6_2 (SDA6_2)		171	-	C4
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	18	18	F5
	SCK6_1 (SCL6_1)		29	-	H4
	SCK6_2 (SCL6_2)		172	-	B3
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin	22	22	G4
	SIN7_1		64	56	K6
	SIN7_2		106	-	H13
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	23	23	G5
	SOT7_1 (SDA7_1)		63	55	L6
	SOT7_2 (SDA7_2)		107	-	H12
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	24	24	G6
	SCK7_1 (SCL7_1)		62	54	M6
	SCK7_2 (SCL7_2)		108	-	H11

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 8	SIN8_0	Multifunction serial interface ch.8 input pin	2	2	B2
	SOT8_0 (SDA8_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I^2C (operation mode 4).	3	3	C2
	SCK8_0 (SCL8_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8 when it is used in an I^2C (operation mode 4).	4	4	C3
Multi Function Serial 9	SIN9_0	Multifunction serial interface ch.9 input pin	5	5	D5
	SOT9_0 (SDA9_0)	Multifunction serial interface ch.9 output pin. This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I^2C (operation mode 4).	6	6	D2
	SCK9_0 (SCL9_0)	Multifunction serial interface ch.9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9 when it is used in an I^2C (operation mode 4).	7	7	D1

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 10	SIN10_0	Multifunction serial interface ch.10 input pin	46	38	N2
	SOT10_0 (SDA10_0)	Multifunction serial interface ch.10 output pin. This pin operates as SOT10 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA10 when it is used in an I^2C (operation mode 4).	47	39	N3
	SCK10_0 (SCL10_0)	Multifunction serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I^2C (operation mode 4).	48	40	M3
Multi Function Serial 11	SIN11_0	Multifunction serial interface ch.11 input pin	49	41	L4
	SOT11_0 (SDA11_0)	Multifunction serial interface ch.11 output pin. This pin operates as SOT11 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA11 when it is used in an I^2C (operation mode 4).	50	42	M4
	SCK11_0 (SCL11_0)	Multifunction serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I^2C (operation mode 4).	51	43	N4

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 12	SIN12_0	Multifunction serial interface ch.12 input pin	118	94	F10
	SOT12_0 (SDA12_0)	Multifunction serial interface ch.12 output pin. This pin operates as SOT12 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA12 when it is used in an I^2C (operation mode 4).	119	95	F11
	SCK12_0 (SCL12_0)	Multifunction serial interface ch.12 clock I/O pin. This pin operates as SCK12 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL12 when it is used in an I^2C (operation mode 4).	120	96	F12
Multi Function Serial 13	SIN13_0	Multifunction serial interface ch.13 input pin	145	115	C9
	SOT13_0 (SDA13_0)	Multifunction serial interface ch.13 output pin. This pin operates as SOT13 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA13 when it is used in an I^2C (operation mode 4).	146	116	B8
	SCK13_0 (SCL13_0)	Multifunction serial interface ch.13 clock I/O pin. This pin operates as SCK13 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL13 when it is used in an I^2C (operation mode 4).	147	117	D9

Pin function	Pin name	Function description	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 14	SIN14_0	Multifunction serial interface ch.14 input pin	149	119	F9
	SOT14_0 (SDA14_0)	Multifunction serial interface ch.14 output pin. This pin operates as SOT14 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA14 when it is used in an I^2C (operation mode 4).	150	120	C8
	SCK14_0 (SCL14_0)	Multifunction serial interface ch.14 clock I/O pin. This pin operates as SCK14 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL14 when it is used in an I^2C (operation mode 4).	151	121	D8
Multi Function Serial 15	SIN15_0	Multifunction serial interface ch.15 input pin	153	123	A10
	SOT15_0 (SDA15_0)	Multifunction serial interface ch.15 output pin. This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I^2C (operation mode 4).	154	124	F8
	SCK15_0 (SCL15_0)	Multifunction serial interface ch.15 clock I/O pin. This pin operates as SCK15 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL15 when it is used in an I^2C (operation mode 4).	155	125	B7

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	37	29	K2
	DTTI0X_1		104	88	H10
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	32	-	J5
	FRCK0_1		105	89	H9
	FRCK0_2		91	75	M12
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. ICxx describes channel number.	36	28	K1
	IC00_1		100	84	J12
	IC00_2		92	76	L13
	IC01_0		35	27	J2
	IC01_1		101	85	J11
	IC01_2		93	77	L12
	IC02_0		34	26	J3
	IC02_1		102	86	J10
	IC02_2		94	78	L11
	IC03_0		33	-	J4
	IC03_1		103	87	J9
	IC03_2		95	79	K13
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	38	30	K3
	RTO00_1 (PPG00_1)		124	100	E12
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	39	31	K4
	RTO01_1 (PPG00_1)		123	99	E11
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	40	32	L1
	RTO02_1 (PPG02_1)		122	98	E10
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	41	33	L2
	RTO03_1 (PPG02_1)		121	97	F13
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	42	34	L3
	RTO04_1 (PPG04_1)		120	96	F12
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	43	35	M2
	RTO05_1 (PPG04_1)		119	95	F11
	IGTRG0_0	PPG IGBT mode external trigger input pin	61	53	N6
	IGTRG0_1		172	140	B3

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	28	-	H3
	AIN0_1		59	51	L5
	AIN0_2		13	13	E5
	BIN0_0	QPRC ch.0 BIN input pin	29	-	H4
	BIN0_1		60	52	K5
	BIN0_2		14	14	F1
	ZIN0_0	QPRC ch.0 ZIN input pin	30	-	H5
	ZIN0_1		61	53	N6
	ZIN0_2		15	15	F2
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	73	65	N9
	AIN1_1		127	103	D13
	AIN1_2		62	54	M6
	BIN1_0	QPRC ch.1 BIN input pin	74	66	M9
	BIN1_1		126	102	D12
	BIN1_2		63	55	L6
	ZIN1_0	QPRC ch.1 ZIN input pin	75	67	L9
	ZIN1_1		125	101	E13
	ZIN1_2		64	56	K6
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	152	122	E8
	RTCCO_1		93	77	L12
	RTCCO_2		37	29	K2
	SUBOUT_0	Sub clock output pin	152	122	E8
	SUBOUT_1		93	77	L12
	SUBOUT_2		37	29	K2

Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
Reset	INITX	External Reset Input. A reset is valid when INITX="L".	57	49	N5
Mode	MD0	Mode 0 Pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	85	69	N12
	MD1	Mode 1 Pin. During serial programming to Flash memory, MD1="L" must be input.	84	68	N13
Power	VCC	Power supply Pin	1	1	C1
			45	37	N1
			54	46	P4
			89	73	M14
			131	107	C14
			133	109	A13
			156	126	A9
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	128	104	C13
	WKUP1	Deep standby mode return signal input pin 1	91	75	M12
	WKUP2	Deep standby mode return signal input pin 2	67	59	M8
	WKUP3	Deep standby mode return signal input pin 3	172	140	B3
	WKUP4	Deep standby mode return signal input pin 4	28	-	H3
	WKUP5	Deep standby mode return signal input pin 5	169	139	C5
HDMI-CEC/ Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	81	-	M10
	CEC0_1		149	119	F9
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	172	140	B3
	CEC1_1		19	19	F6
DAC	DA0_0	D/A converter ch.0 analog output pin	145	115	C9
	DA1_0	D/A converter ch.1 analog output pin	146	116	B8

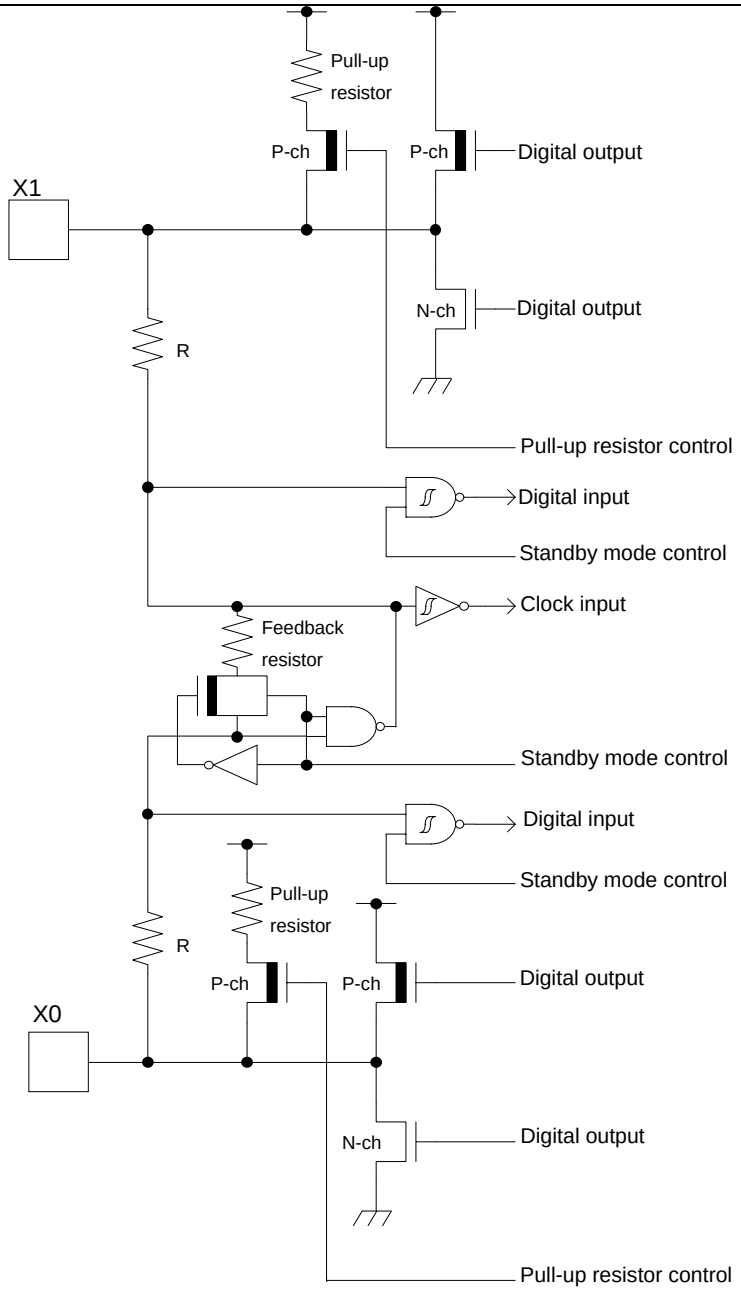
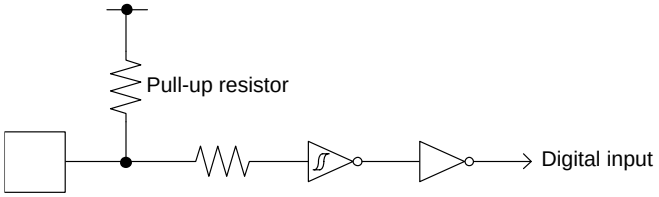
Pin function	Pin name	Function description	Pin No		
			LQFP-176	LQFP-144	BGA-192
GND	VSS	GND Pin	27	25	A5
			44	36	A8
			53	45	A11
			88	72	E1
			132	108	G7
			157	127	G8
			176	144	H8
			-	-	M1
			-	-	P3
			-	-	P7
			-	-	N7
			-	-	M7
			-	-	L7
			-	-	K7
			-	-	J7
			-	-	P11
			-	-	N14
			-	-	L14
			-	-	B14
			-	-	H7
			-	-	B1
			-	-	G1
			-	-	J1
Clock	X0	Main clock (oscillation) input pin	86	70	P12
	X0A	Sub clock (oscillation) input pin	55	47	P5
	X1	Main clock (oscillation) I/O pin	87	71	P13
	X1A	Sub clock (oscillation) I/O pin	56	48	P6
	CROUT_0	Built-in high-speed CR-osc clock output port	127	103	D13
	CROUT_1		152	122	E8
Analog Power	AVCC	A/D converter, D/A converter analog power pin	114	90	J14
	AVRH	A/D converter analog reference voltage input pin	117	93	F14
Analog GND	AVSS	A/D converter, D/A converter GND pin	115	91	H14
	AVRL	A/D converter analog reference voltage input pin	116	92	G14
C pin	C	Power supply stabilization capacity pin	52	44	P2

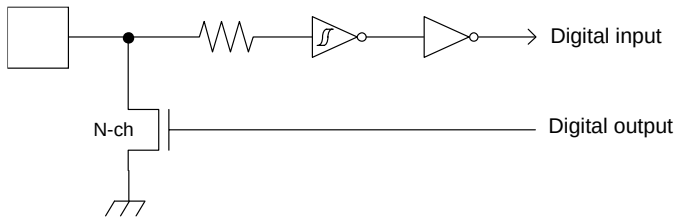
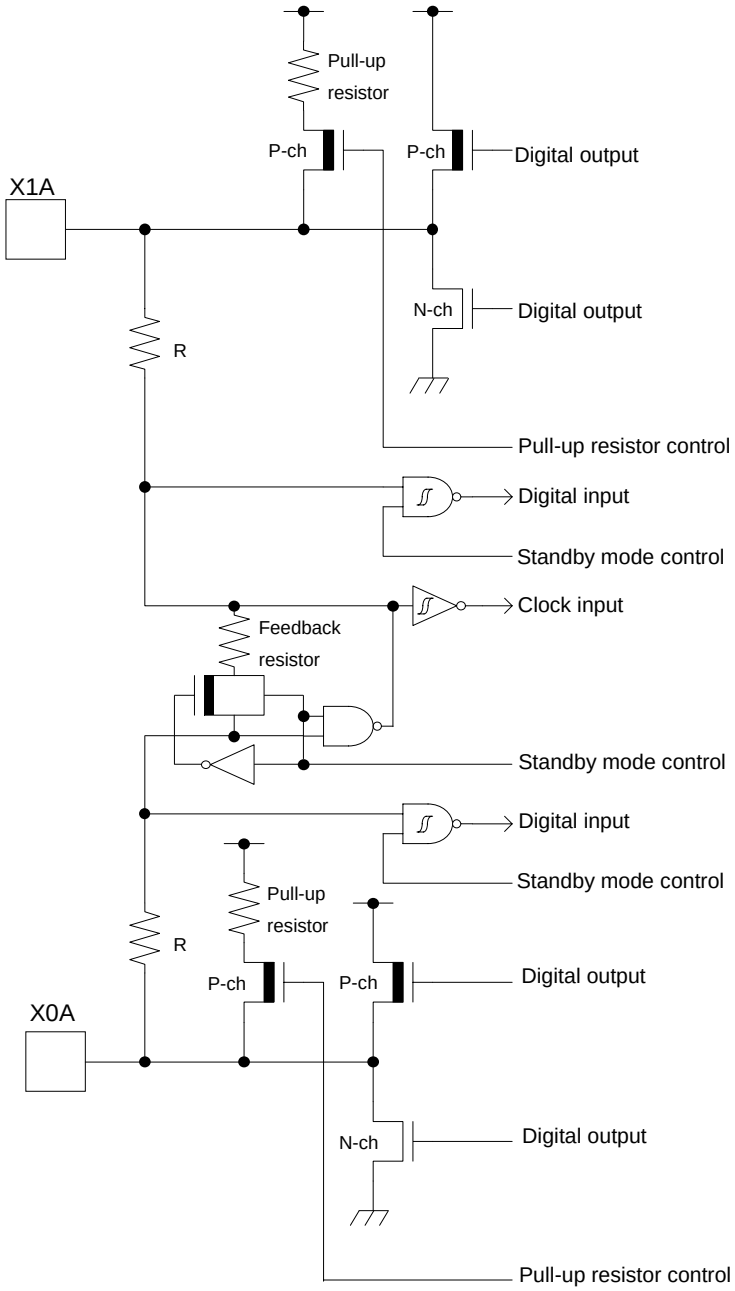
*: 5V tolerant I/O

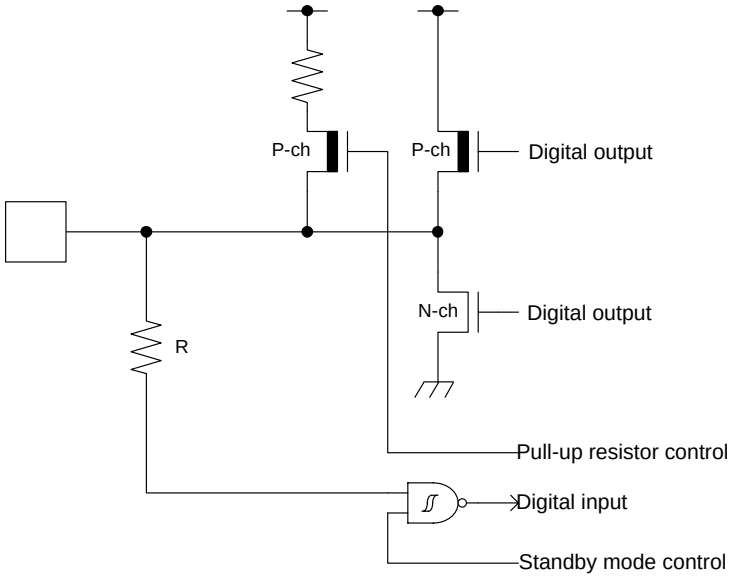
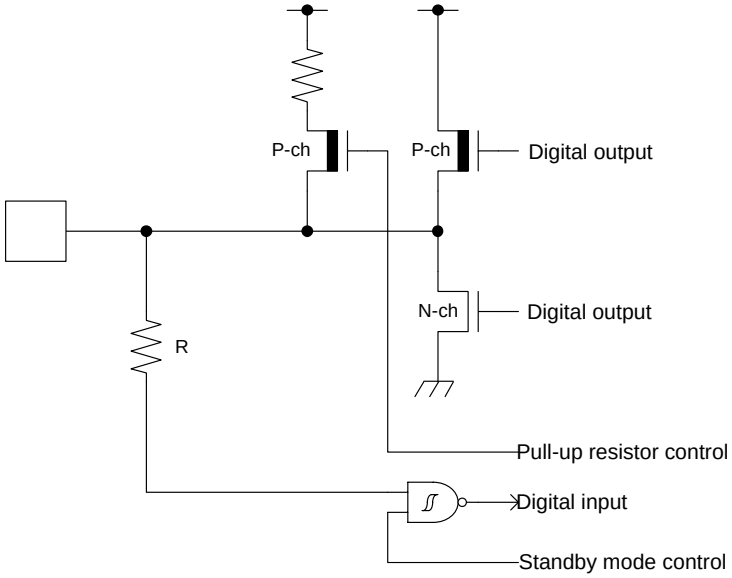
Note:

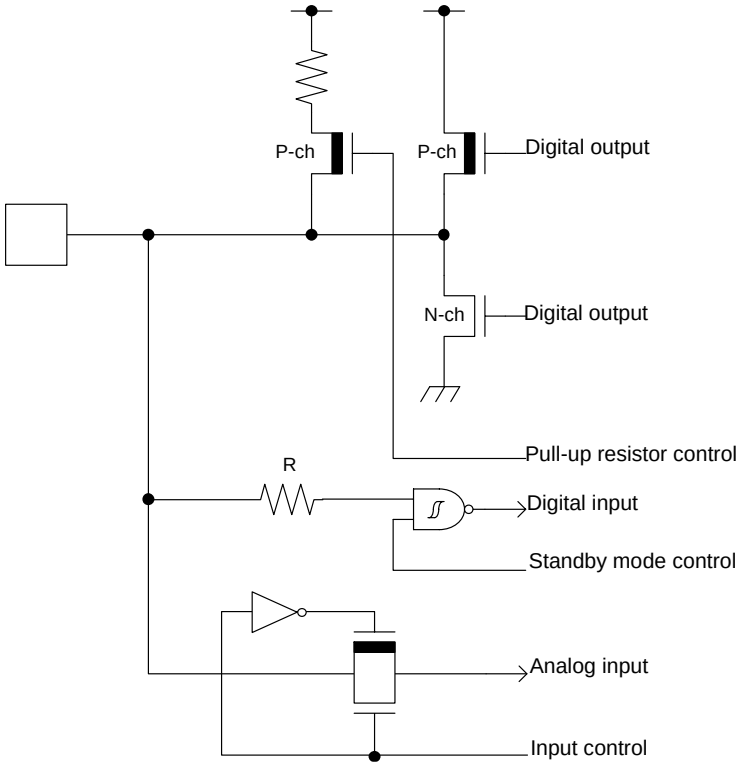
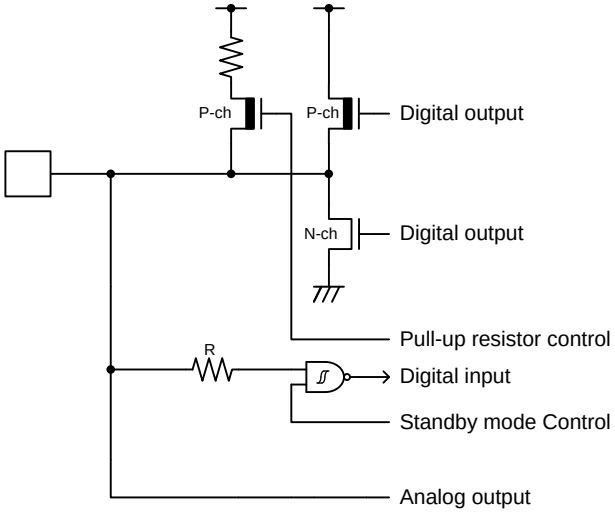
- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

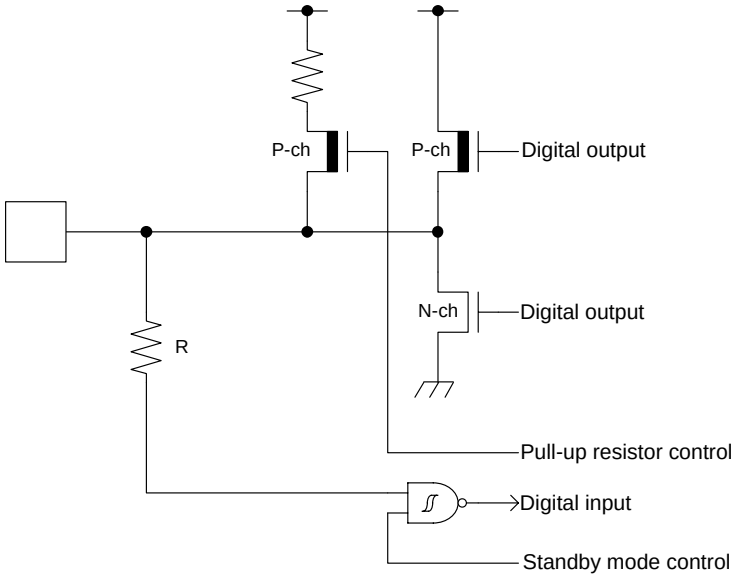
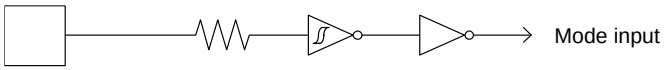
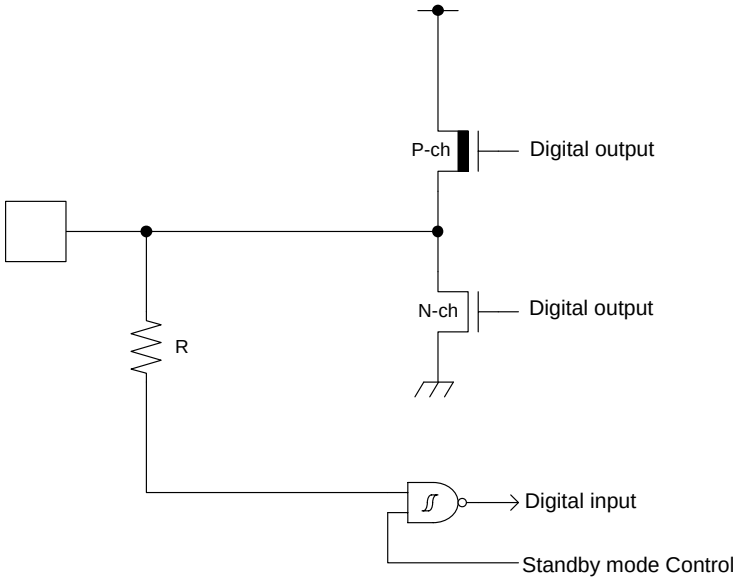
5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input available
F		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -12 mA, I_{OL}= 12 mA • +B input available

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input available
H		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}= -18.0 mA, I_{OL}= 16.5 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

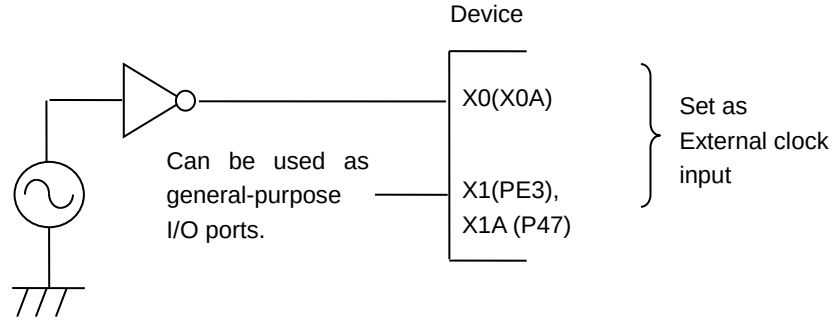
This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm × 1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

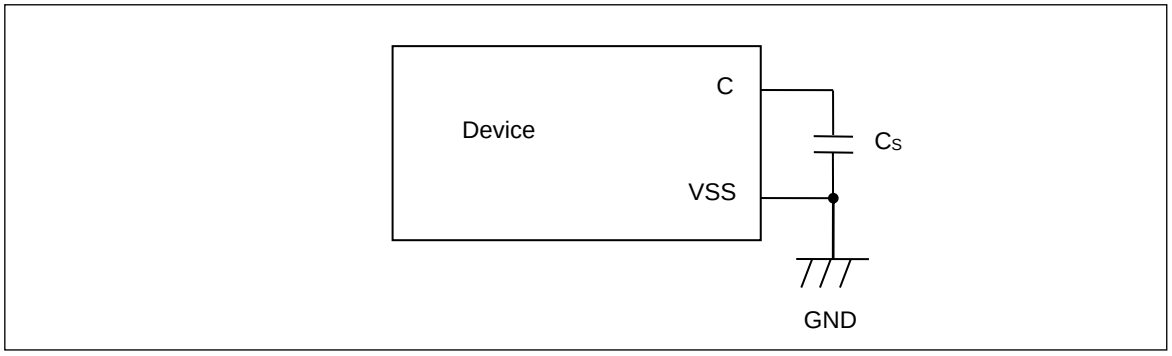


Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

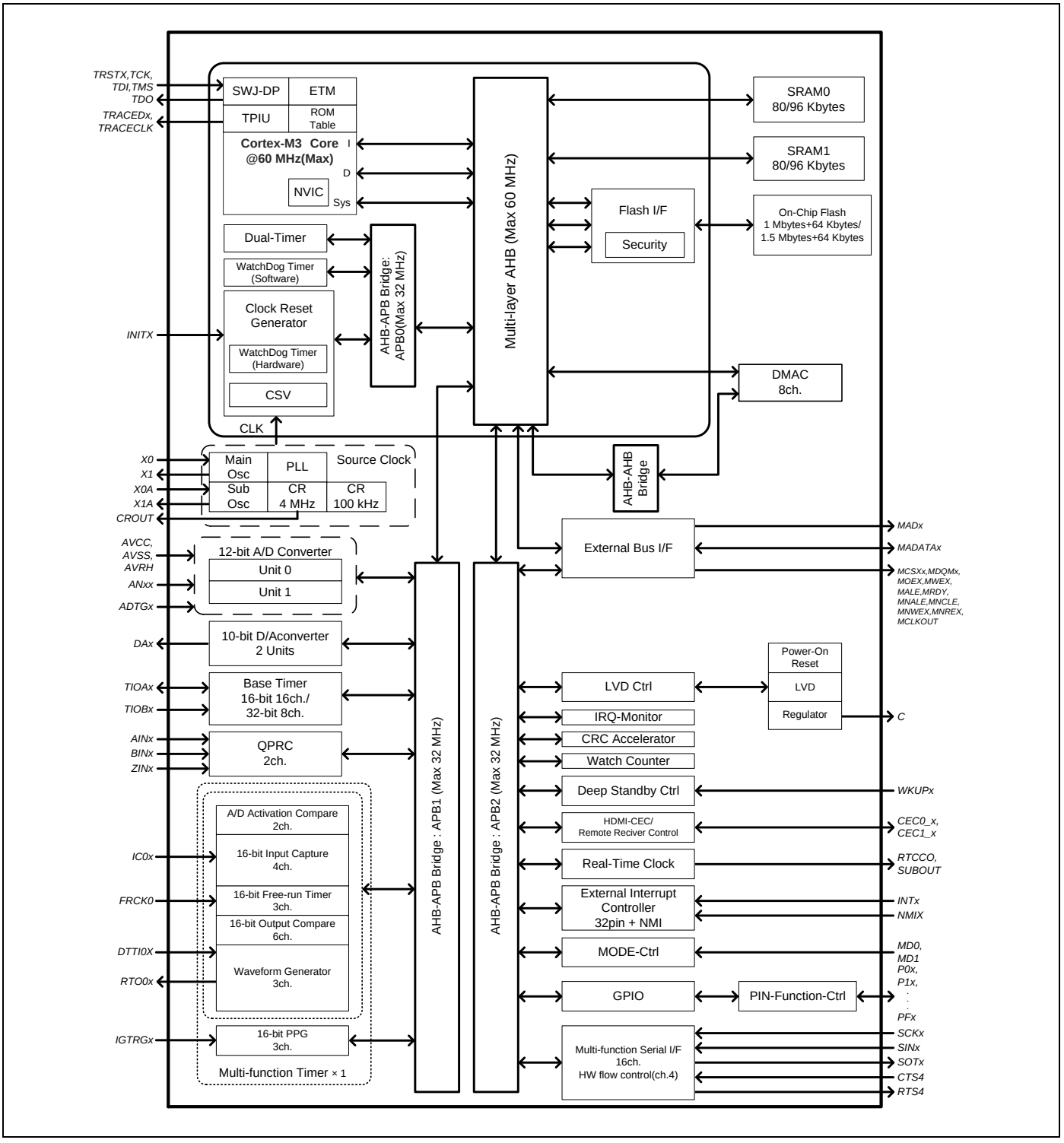
Pull-Up function of 5V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

Adjoining wiring on circuit board

If wiring of the crystal oscillation circuit (X0/X1 and X0A/X1A) adjoins and also runs in parallel with the wiring of GPIO, there is a possibility that the oscillation erroneously counts because oscillation wave has noise with the change of GPIO. Keep as much distance as possible between both wirings and insert the ground pattern between them in order to avoid this possibility.

8. Block Diagram

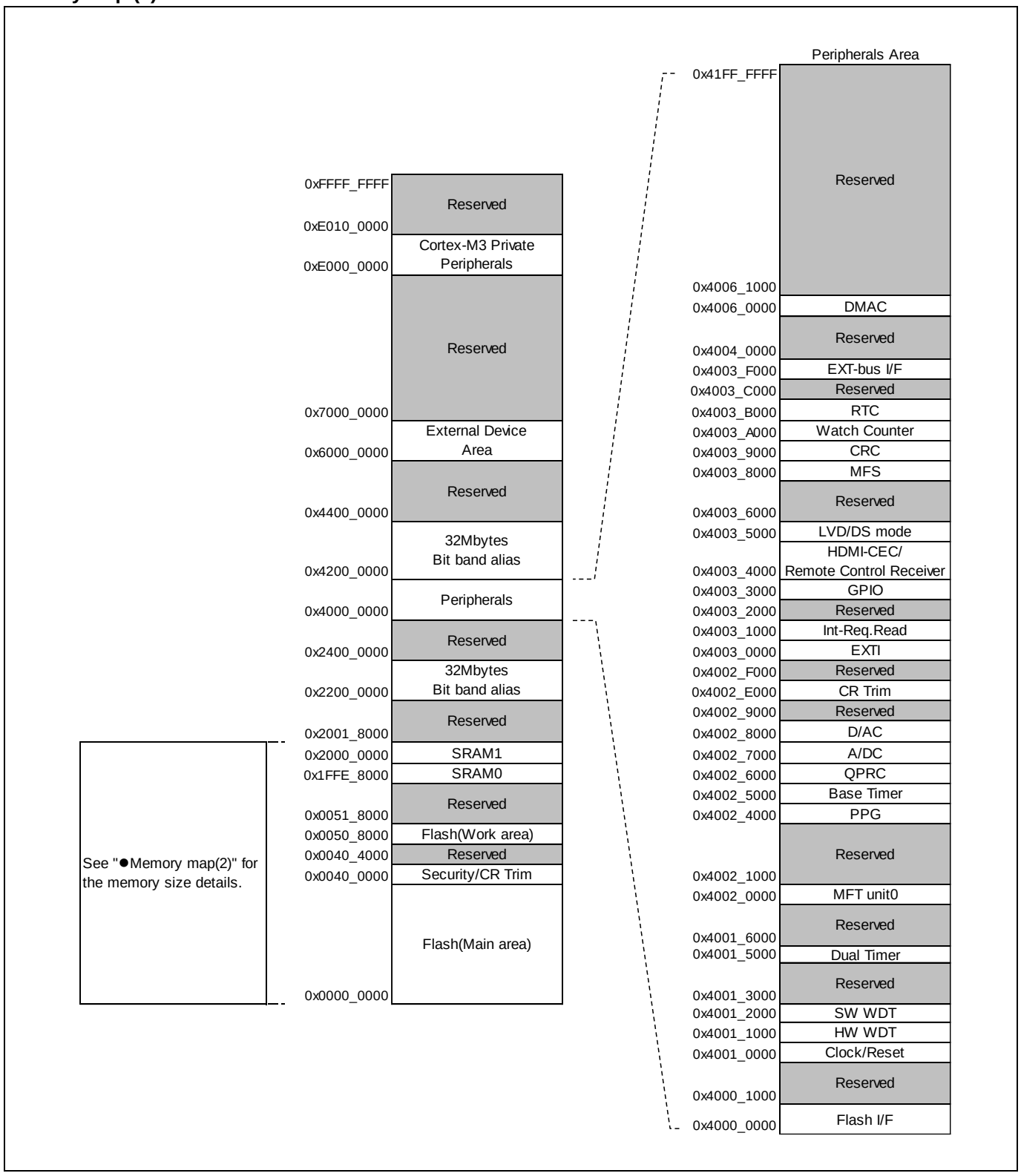


9. Memory Size

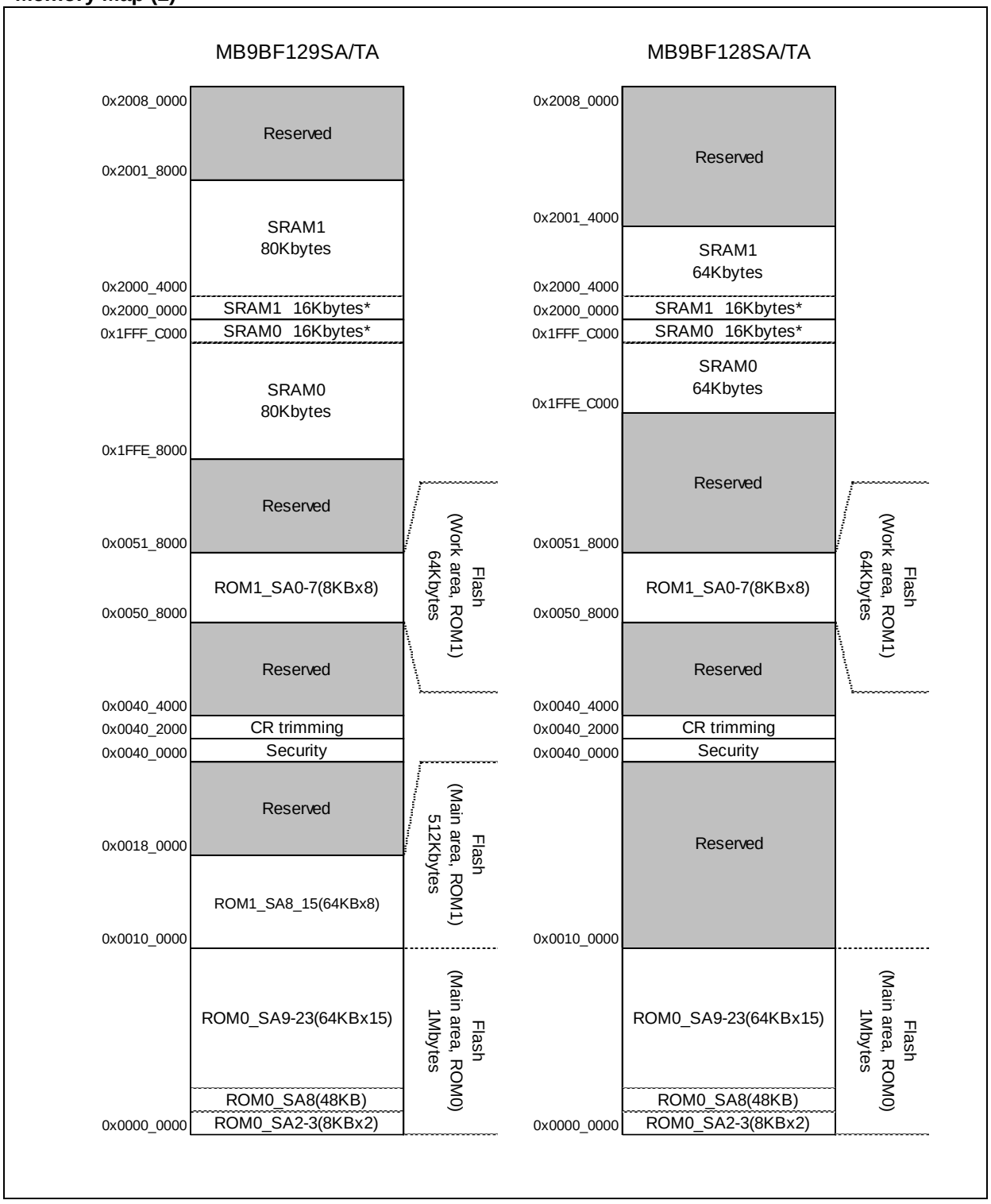
See “Memory size" in "Product Lineup" to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



The content of SRAM can be retained at the deep standby modes by the setting of Deep Standby RAM Retention Register (DSRAMR).
See "MB9B520T/420T/320T/120T Series Flash Programming Manual" for sector structure of Flash.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter (QPRC)
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Resister
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote control Reception
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External bus interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the "L" level.

- INITX=1

  This is the period when the INITX pin is the "H" level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z/ Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
H	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
I	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
J	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
O	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at "0"			
	GPIO selected									
P	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
Q	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
S	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
T	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled							WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
U	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
V	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected

*1: Oscillation is stopped at Sub timer mode, Low-speed CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2: Oscillation is stopped at STOP mode and Deep standby STOP mode.

*3: Maintain previous state at timer mode. GPIO selected Internal input fixed at "0" at RTC mode, STOP mode.

*4: Maintain previous state at timer mode. Hi-Z/Internal input fixed at "0" at RTC mode, STOP mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
		V_{SS} - 0.5	V_{SS} + 3.63	V	5V tolerant*8
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
"L" level maximum output current*4	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80/P81
"L" level average output current*5	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			16.5	mA	P80/P81
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80/P81
"H" level average output current*5	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 18	mA	P80/P81
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	390	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

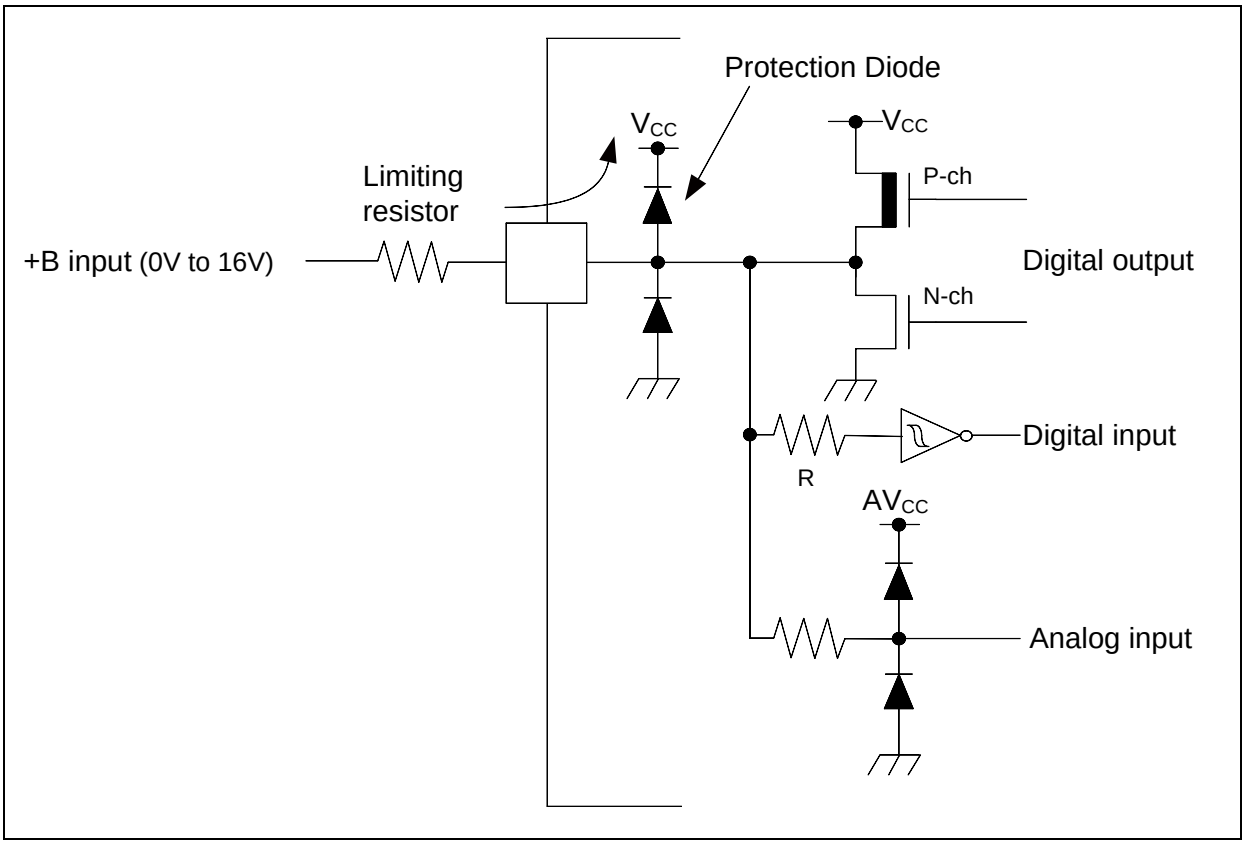
*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

*7: $V_{CC} = AV_{CC} = AVRH = V_{SS} = AV_{SS} = AVRL = 0.0$ V

*8:

- See "List of Pin Functions" and "I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

– *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
Do not exceed any of these ratings.

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For built-in Regulator*1
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: See "C Pin" in "Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition.
  Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
  No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

12.3 DC Characteristics

12.3.1 Current Rating

Parameter	Symbol (Pin name)	Conditions		Value		Unit	Remarks
				Typ*1	Max*2		
Power supply current	I_{CC}	PLL RUN mode	CPU: 60 MHz, Peripheral: 30 MHz *3,*5	29	37	mA	
			CPU: 60 MHz, Peripheral clock stops *3,*5	19	26	mA	
		High-speed CR RUN mode	CPU/ Peripheral: 4 MHz *4,*3	3.1	6.4	mA	
		Sub RUN mode	CPU/ Peripheral: 32 kHz *3,*6	170	2300	µA	
		Low-speed CR RUN mode	CPU/ Peripheral: 100 kHz *3	210	2300	µA	
	I_{CCS}	PLL SLEEP mode	Peripheral: 30 MHz *3,*5	19	26	mA	
		High-speed CR SLEEP mode	Peripheral: 4 MHz*4 *3	2.1	5.1	mA	
		Sub SLEEP mode	Peripheral: 32 kHz *3,*6	160	2200	µA	
		Low-speed CR SLEEP mode	Peripheral: 100 kHz *3	190	2200	µA	
	I_{CCH}	STOP mode	T_A = + 25°C *3	20	75	µA	
			T_A = + 105°C *3	-	1.3	mA	
	I_{CCT}	Main TIMER mode	T_A = + 25°C *3,*6	2.8	5.5	mA	
			T_A = + 105°C *3,*6	-	6.5	mA	
		Sub TIMER mode	T_A = + 25°C *3,*6	24	95	µA	
			T_A = + 105°C *3,*6	-	1.7	mA	
	I_{CCR}	RTC mode	T_A = + 25°C *3,*6	21	89	µA	
			T_A = + 105°C *3,*6	-	1.7	mA	

*1: T_A=+25°C,V_{CC}= 3.3 V

*2: T_A=+105°C,V_{CC}=5.5 V

*3: When all ports are fixed.

*4: When setting it to 4 MHz by trimming.

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Parameter	Symbol (Pin name)	Conditions		Value		Unit	Remarks
				Typ*1	Max*2		
Power supply current	I_{CCHD}	Deep Standby STOP mode	T_A = + 25°C, When RAM is off *3	1.9	13	µA	
			T_A = + 25°C, When RAM is on(16 KB) *4, *3	4.8	17	µA	
			T_A = + 25°C, When RAM is on(32 KB) *4, *3	5.5	20	µA	
			T_A = + 105°C, When RAM is off *3	-	300	µA	
			T_A = + 105°C, When RAM is on(16 KB) *4, *3		320	µA	
			T_A = + 105°C, When RAM is on(32 KB) *4, *3		330	µA	
	I_{CCRD}	Deep Standby RTC mode	T_A = + 25°C, When RAM is off *3, *5	2.5	14	µA	
			T_A = + 25°C, When RAM is on(16 KB) *4, *3, *5	5.4	18	µA	
			T_A = + 25°C, When RAM is on(32 KB) *4, *3, *5	6.1	21	µA	
			T_A = + 105°C, When RAM is off *3, *5	-	305	µA	
			T_A = + 105°C, When RAM is on(16 KB) *4, *3, *5		325	µA	
			T_A = + 105°C, When RAM is on(32 KB) *4, *3, *5		335	µA	

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are fixed and LVD off.

*4: For more information about RAM retention area, see "Memory Map (2)" in "Memory Map".

*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol (Pin name)	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD} (VCC)	At operation	-	0.13	0.3	µA	For occurrence of reset
			-	0.13	0.3	µA	For occurrence of interrupt

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$ (VCC)	VCC	At ROM0 Write/Erase	-	9.9	11.8	mA	*1
			At ROM1 Write/Erase	-	9.5	11.2	mA	*1

*1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

In addition, When programming or erase in flash memory ROM0 and ROM1 at the same time, Flash Memory Write/Erase current ($I_{CCFLASH}$) of both ROM0 and ROM1 are added to the Power supply current (I_{CC}).

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCAD} (VCC)	AVCC	At 1unit operation	-	0.69	0.9	mA	
			At stop	-	0.6	35	µA	
Reference power supply current (AVRH)	I_{CCAVRH} (VCC)	AVRH	At 1unit operation AVRH=5.5 V	-	1.1	1.97	mA	
			At stop	-	0.2	3.4	µA	

D/A Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*1	I_{DDA}*2 (VCC)	AVCC	At 1unit operation AV_{CC}=3.3 V	250	315	380	µA	
			At 1unit operation AV_{CC}=5.0 V	380	475	580	µA	
	I_{DSA} (VCC)		At stop	-	-	30	µA	

*1: No-load

*2: Generates the max current by the CODE about 0x200

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
"H" level output voltage	V_{OH}	4mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		12mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		P80/P81	V_{CC} ≥ 4.5 V, I_{OH} = - 18.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 12.0 mA					
"L" level output voltage	V_{OL}	4mA type	V_{CC} ≥ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2 mA					
		12mA type	V_{CC} ≥ 4.5 V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 8 mA					
		P80/P81	V_{CC} ≥ 4.5 V, I_{OL} = 16.5 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
		CEC0_0, CEC0_1, CEC1_0, CEC1_1	V_{CC} = AV_{CC} = AVRH = V_{SS} = AV_{SS} = AVRL = 0.0 V	-	-	+1.8	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	33	50	90	kΩ	
			V_{CC} < 4.5 V	-	-	180		

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH, AVRL	-	-	5	15	pF	

12.4 AC Characteristics

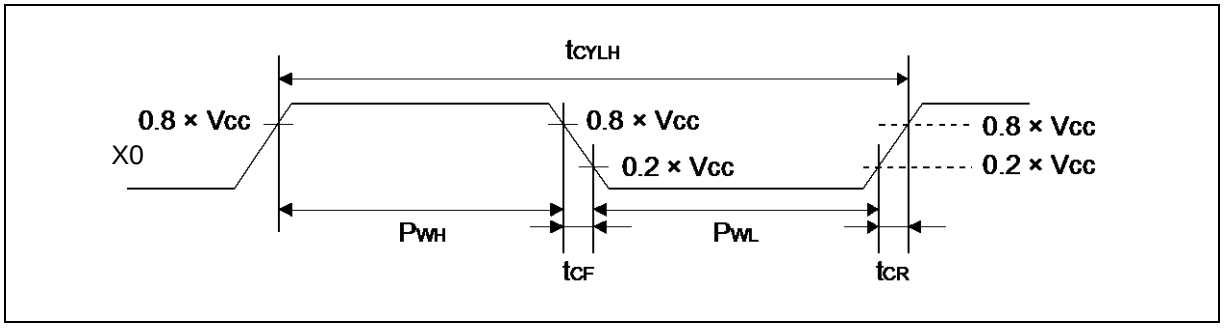
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			-	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	60	MHz	Master clock
	F_{CC}	-	-	-	60	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	32	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	32	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	32	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	16.7	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	31.25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	31.25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	31.25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

*2: For about each APB bus which each peripheral is connected to, see "Block Diagram" in this data sheet.

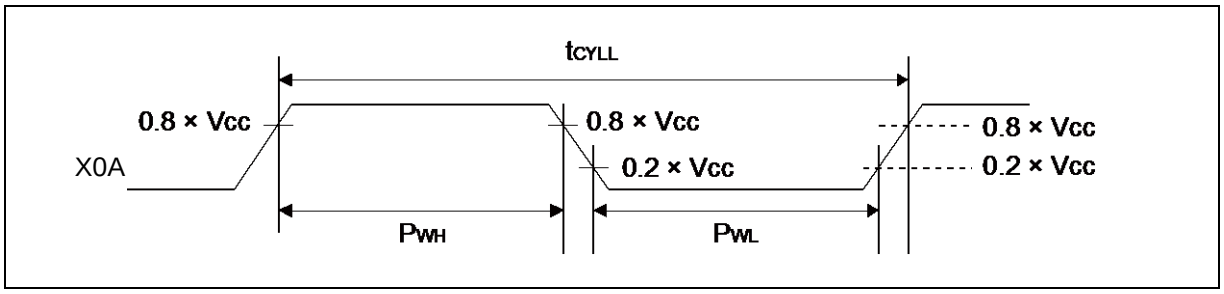


12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected*
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see "Sub crystal oscillator" in "Handling Devices".



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	T_A = + 25°C, 3.6 V < V_{CC} ≤ 5.5 V	3.92	4	4.08	MHz	When trimming*1
		T_A = 0°C to + 85°C, 3.6 V < V_{CC} ≤ 5.5 V	3.9	4	4.1		
		T_A = -40°C to + 105°C, 3.6 V < V_{CC} ≤ 5.5 V	3.88	4	4.12		
		T_A = + 25°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.94	4	4.06		
		T_A = - 20°C to + 85°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.92	4	4.08		
		T_A = - 20°C to + 105°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.9	4	4.1		
		T_A = -40°C to + 105°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.88	4	4.12		
		T_A = - 40°C to + 105°C	2.8	4	5.2		When not trimming
Frequency stability time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: Frequency stable time is time to stable of the frequency of the High-speed CR clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	60	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	60	MHz	

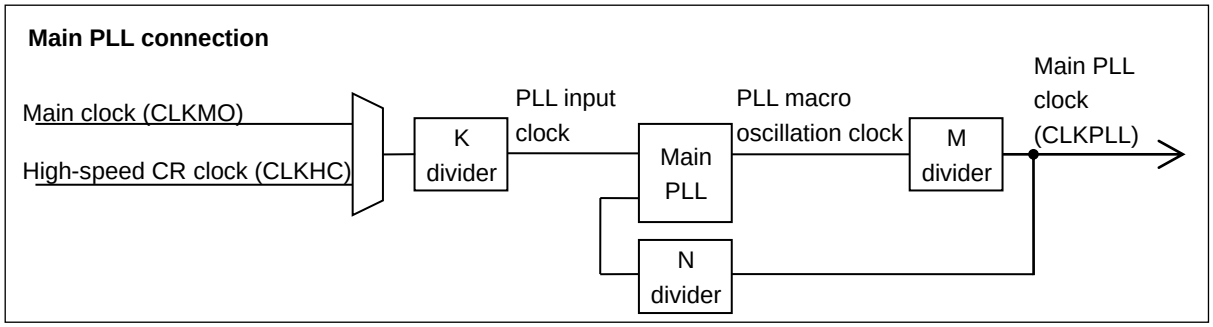
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "CHAPTER 2-1: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note:

- *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.*

Main PLL connection



12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 105°C)

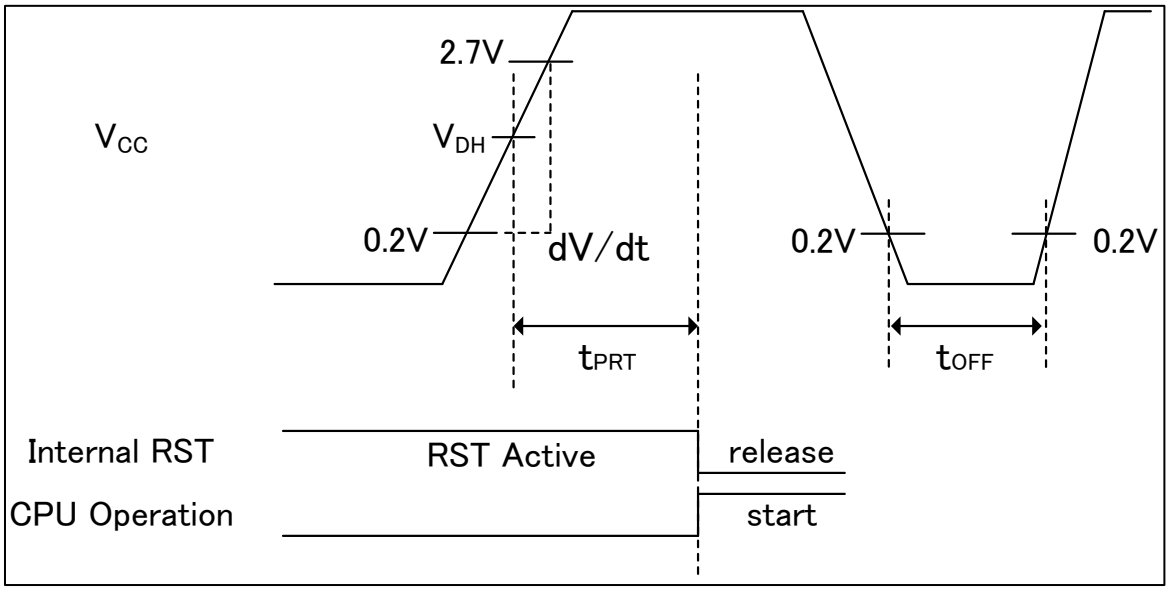
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1		-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2 V to 2.70 V	0.9		1000	mV/ /µs	*2
Time until releasing power-on reset	t_{PRT}		-	0.46		0.76	ms	

*1: Vcc must be held below 0.2 V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF} > 1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset (INTX) at power-up and at any brownout event per 12.4.6.*



Glossary

VDH : detection voltage of Low Voltage detection reset. See “12.7. Low-Voltage Detection Characteristics”

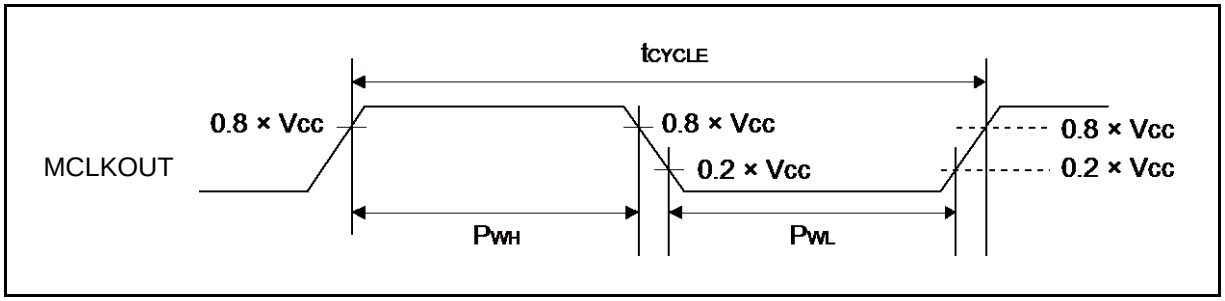
12.4.8 External Bus Timing

External bus clock output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

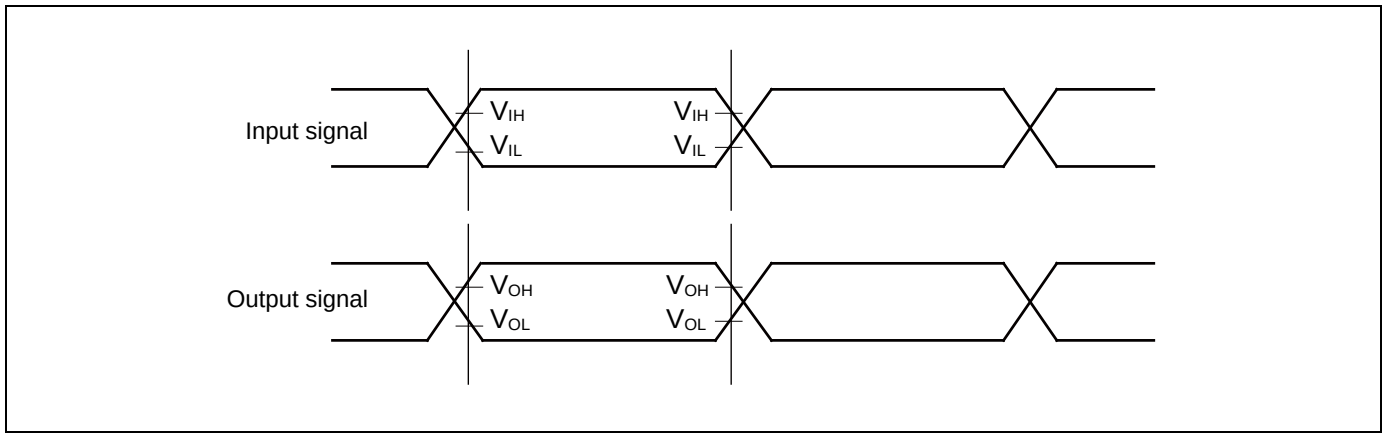
*: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see "CHAPTER 12: External Bus Interface" in "FM3 Family PERIPHERAL MANUAL".
When external bus clock is not output, this characteristics does not give any effect on external bus operation.



External bus signal input/output characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



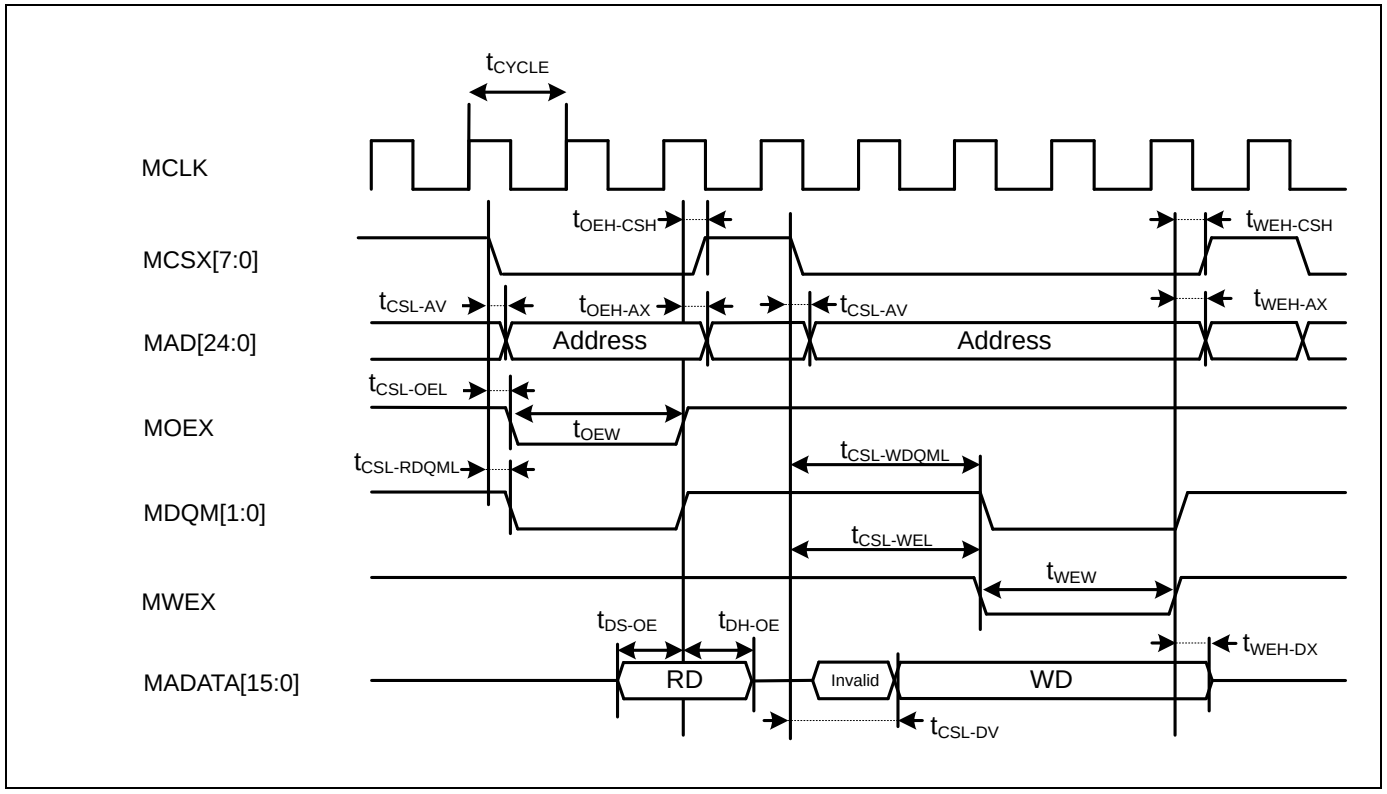
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MCSX ↓ → Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 4.5$ V	-9	+9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MOEX ↑ → Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX Min pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MWEX ↑ → Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX ↓→ MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MCSX ↓→ Data output time	t_{CSL-DV}	MCSX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5$ V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+12	ns
			$V_{CC} < 4.5$ V			

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

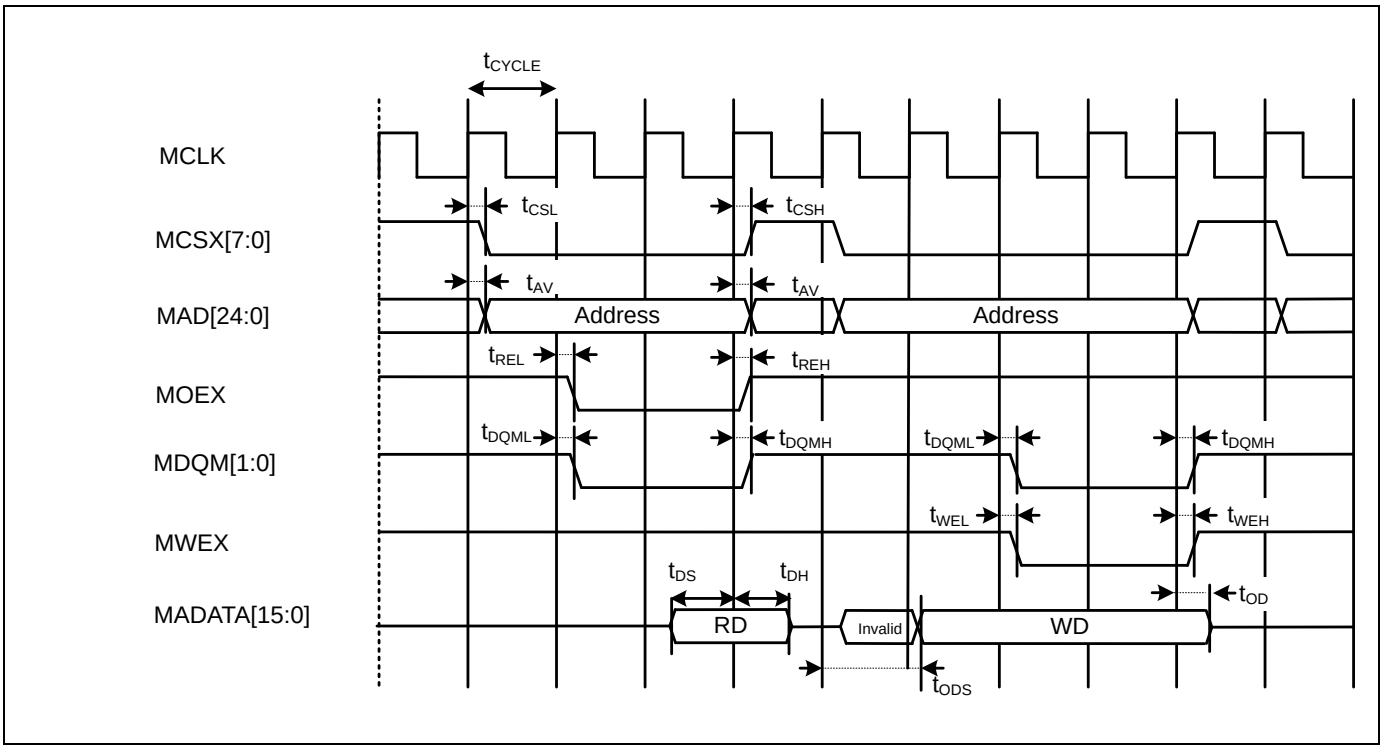
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 4.5$ V	1	12	ns
			$V_{CC} < 4.5$ V			
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{CSH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{REH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	19	-	ns
			$V_{CC} < 4.5$ V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{WEH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{DQMH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 4.5$ V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	18	ns
			$V_{CC} < 4.5$ V		24	

Note:

- *When the external load capacitance C_L = 30 pF.*


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tCSL
tCSH
tAV
tAV
Address
Address
tREL
tREH
tDQML
tDQMH
tDQML
tDQMH
tWEL
tWEH
tDS
tDH
tOD
RD
Invalid
WD
tODS

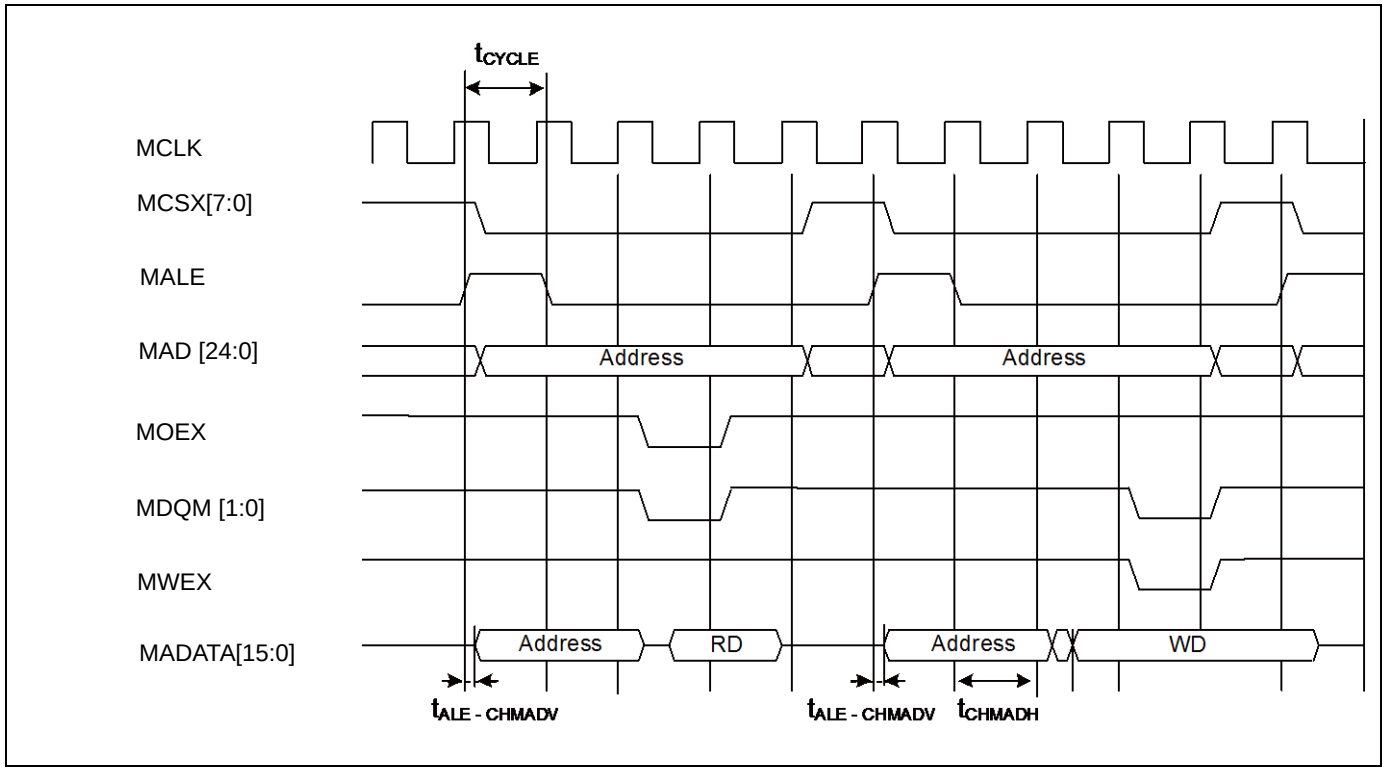
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	+10	ns
			$V_{CC} < 4.5$ V		+20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+12	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*



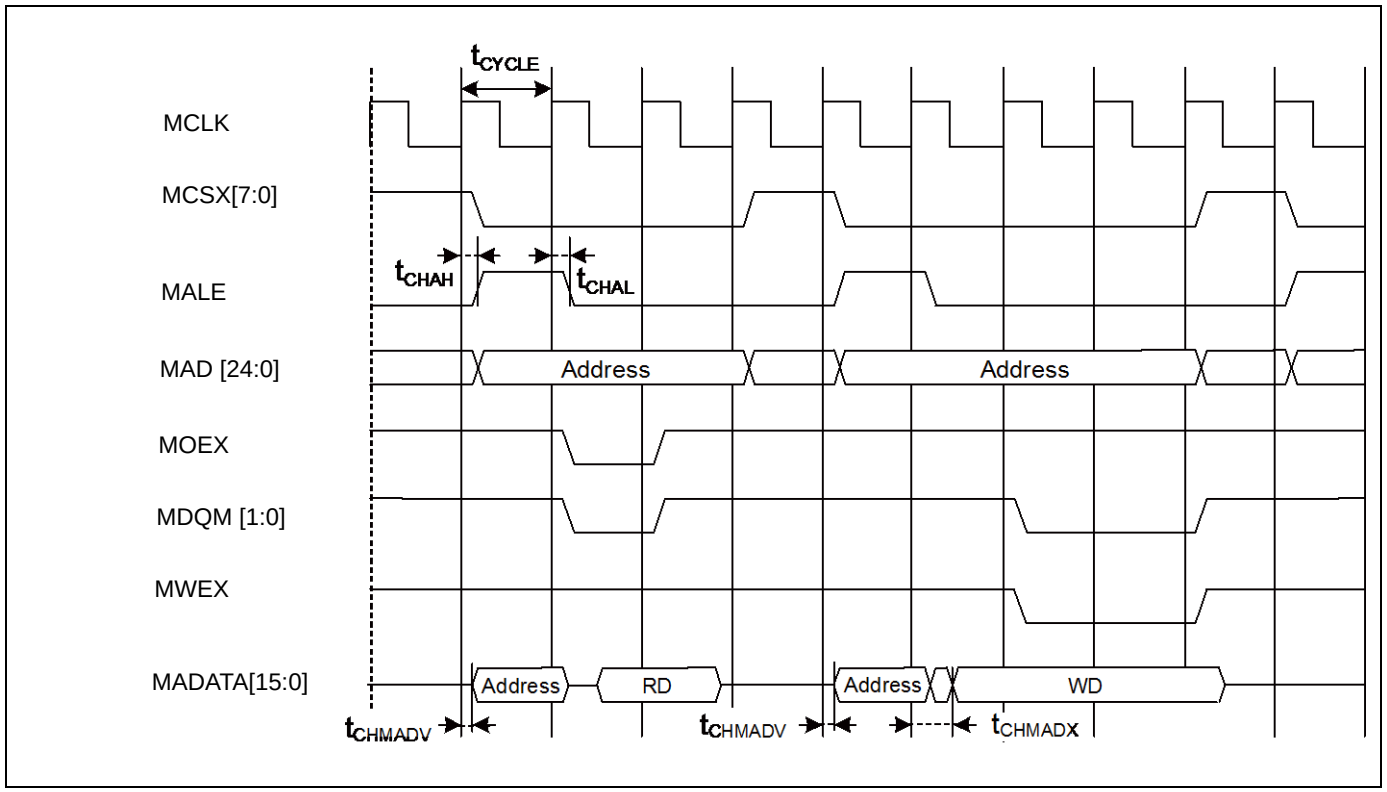
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
	t_{CHAH}		$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				

Note:

- *When the external load capacitance C_L = 30 pF.*



NAND Flash Memory Mode

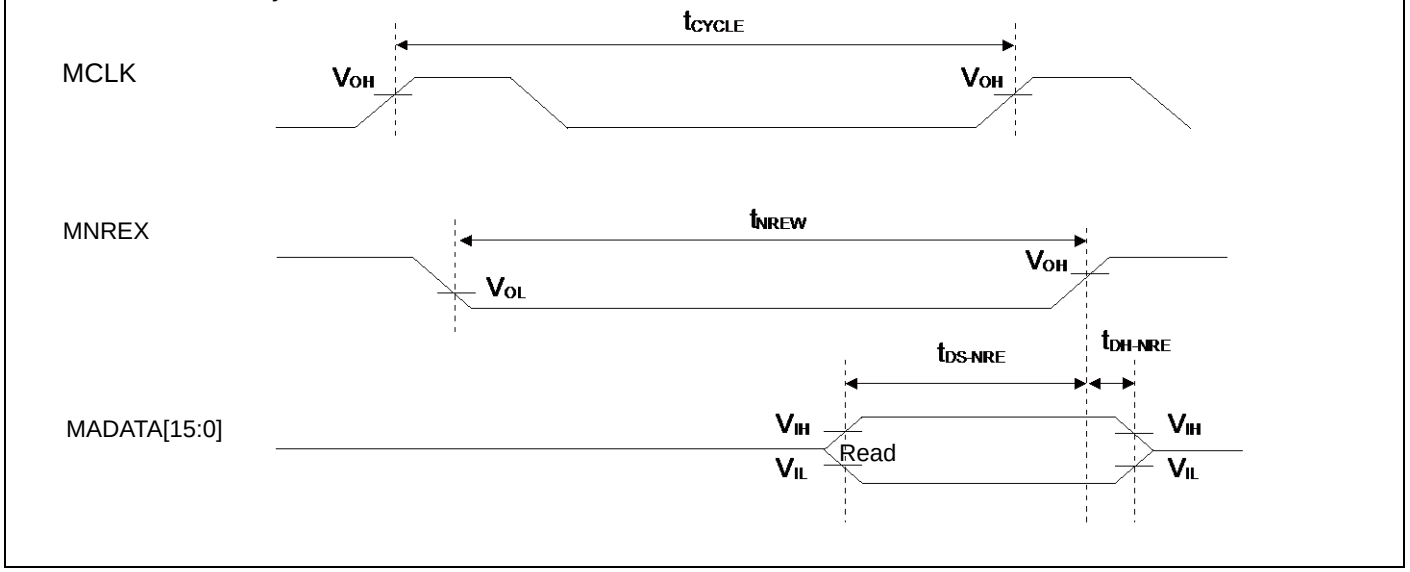
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data setup → MNREX↑time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE↑→ MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→ MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→ MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→ MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX↓→ Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX↑→ Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+11	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

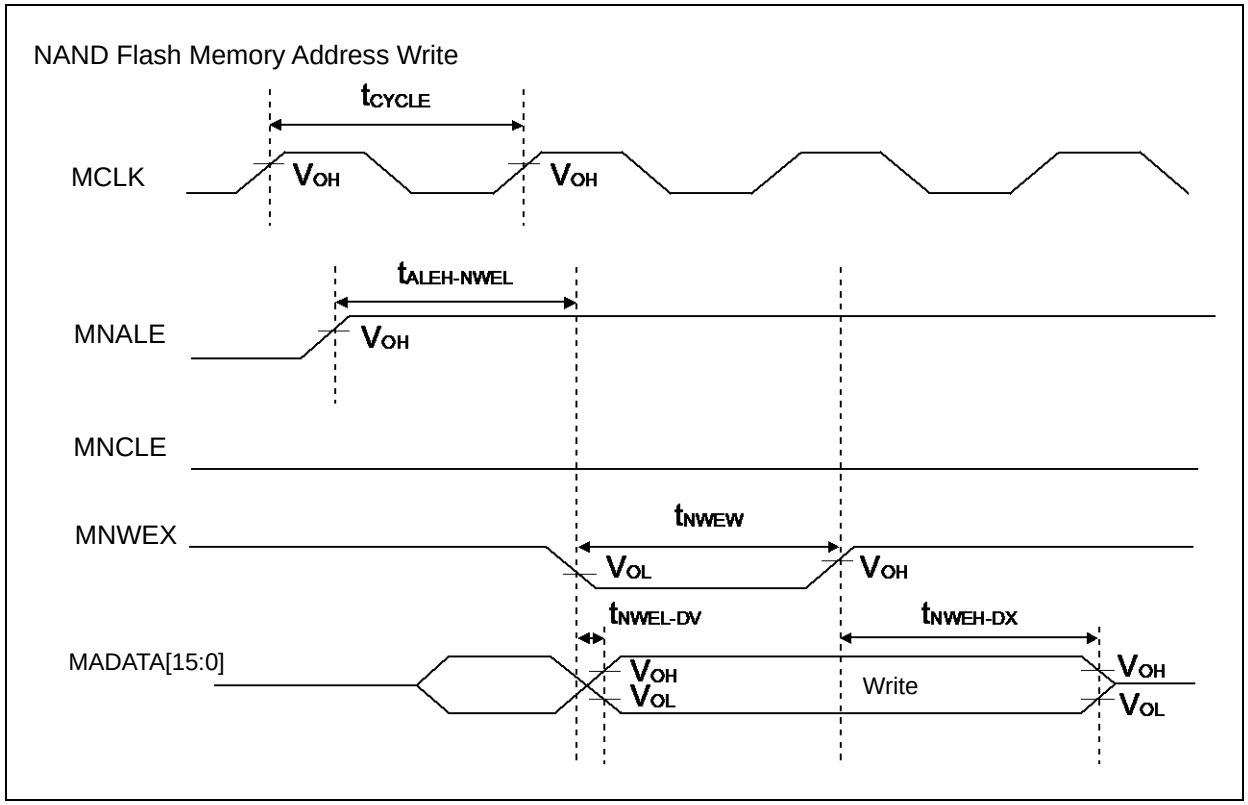
Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16).*

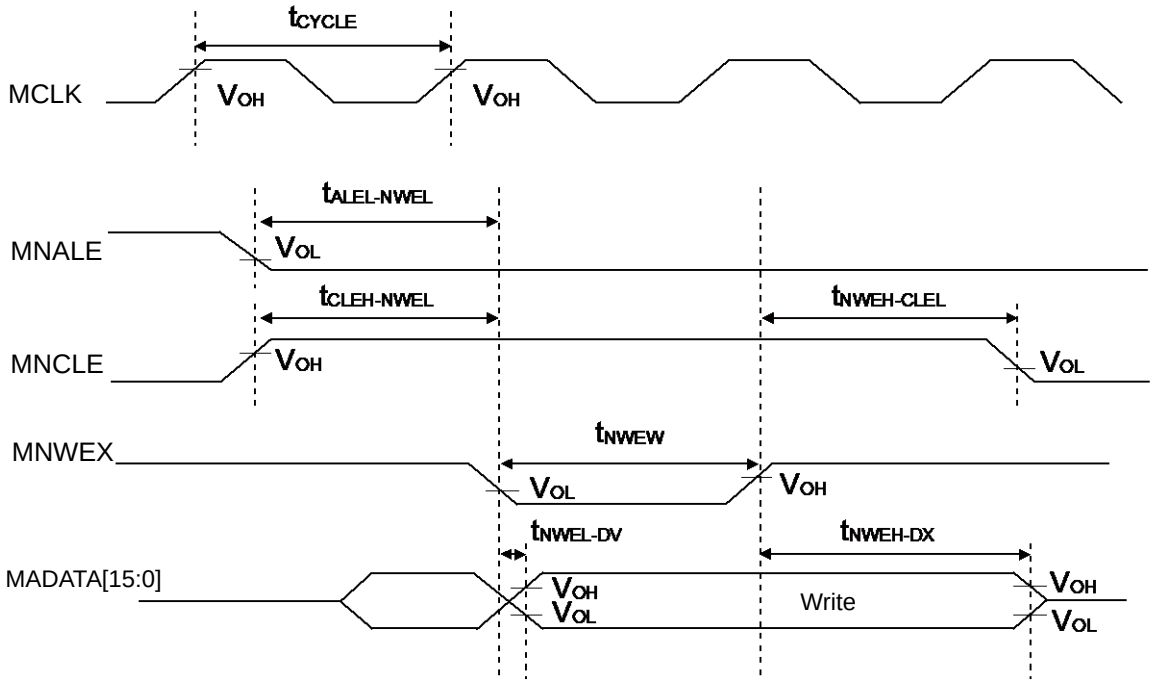
NAND Flash Memory Read



NAND Flash Memory Address Write



NAND Flash Memory Command Write

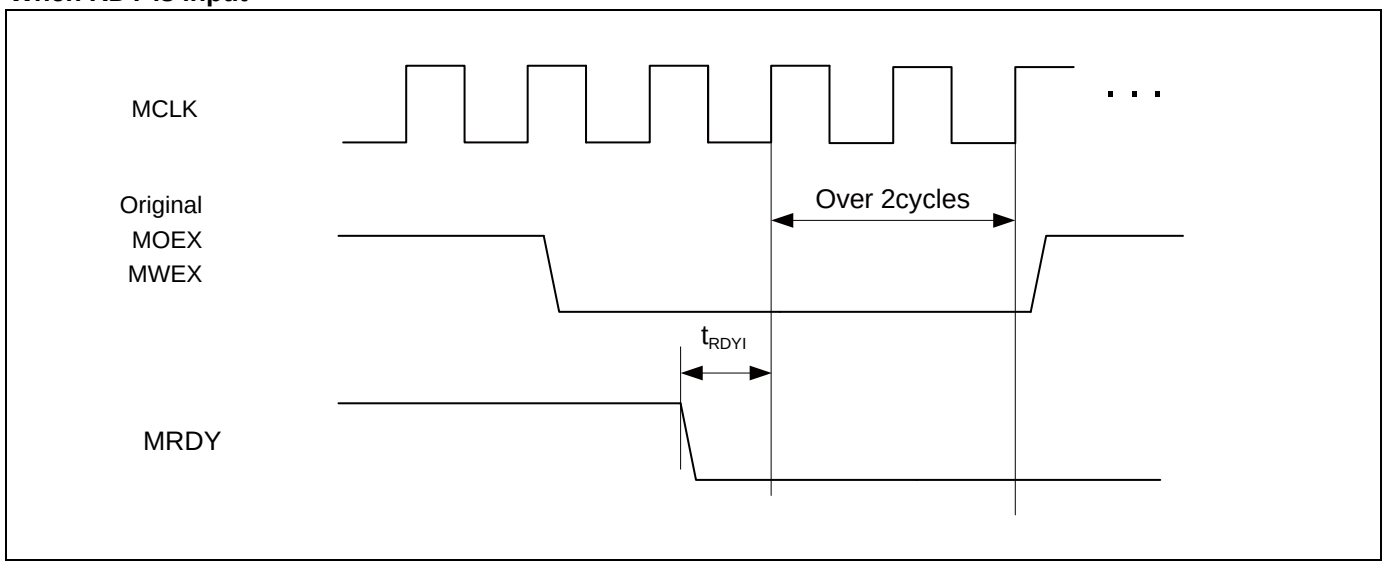


External Ready Input Timing

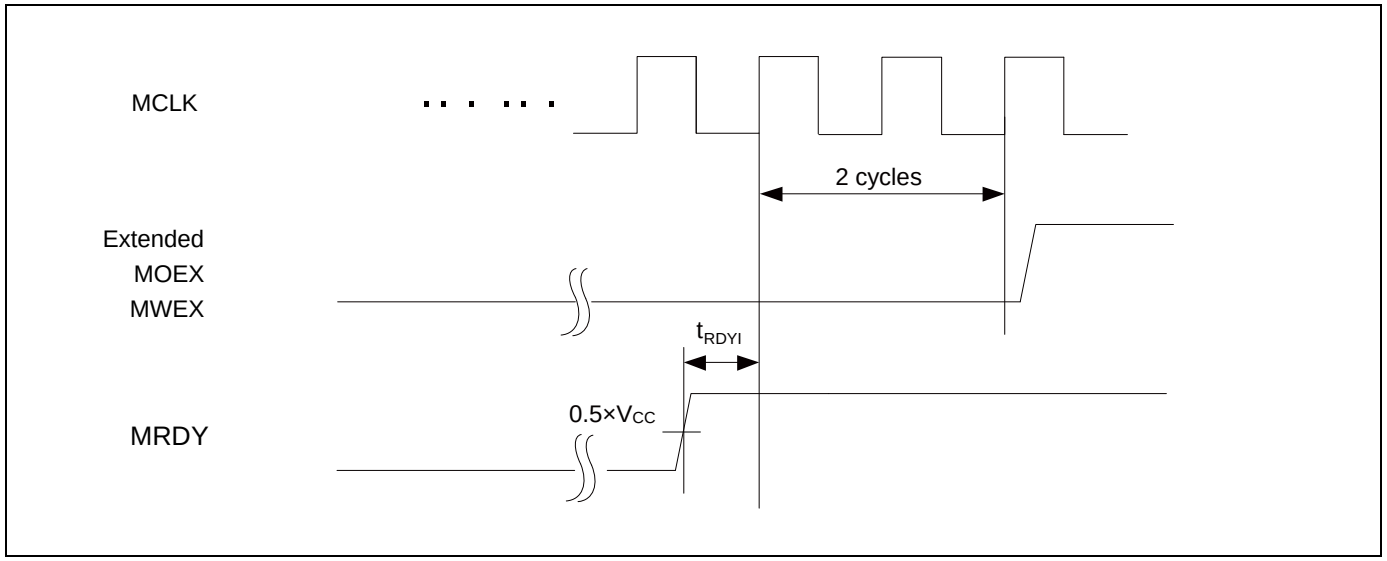
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

When RDY is input



When RDY is released

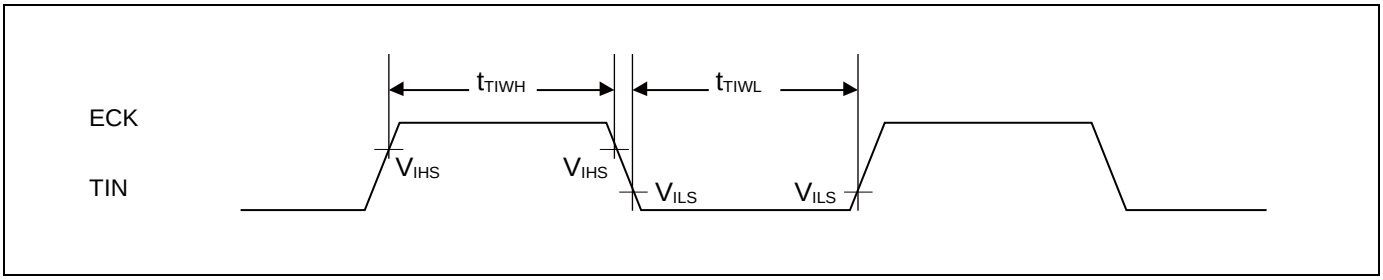


12.4.9 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

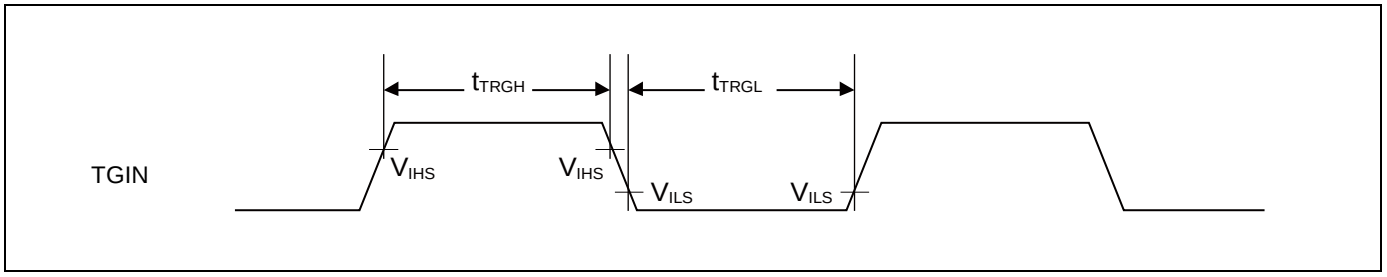
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see "Block Diagram" in this data sheet.

12.4.10 CSIO/UART Timing

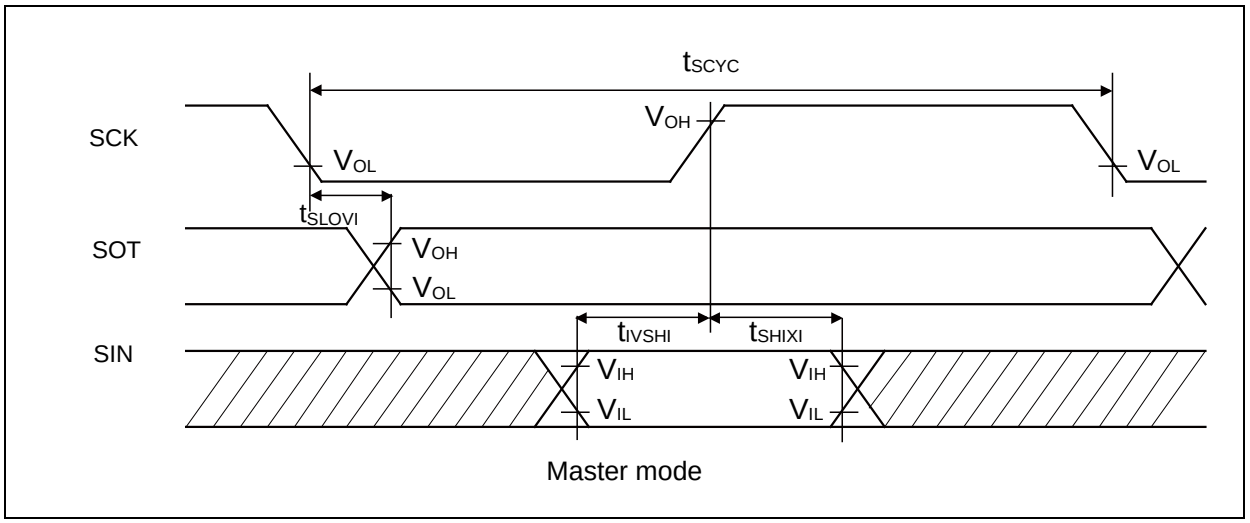
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

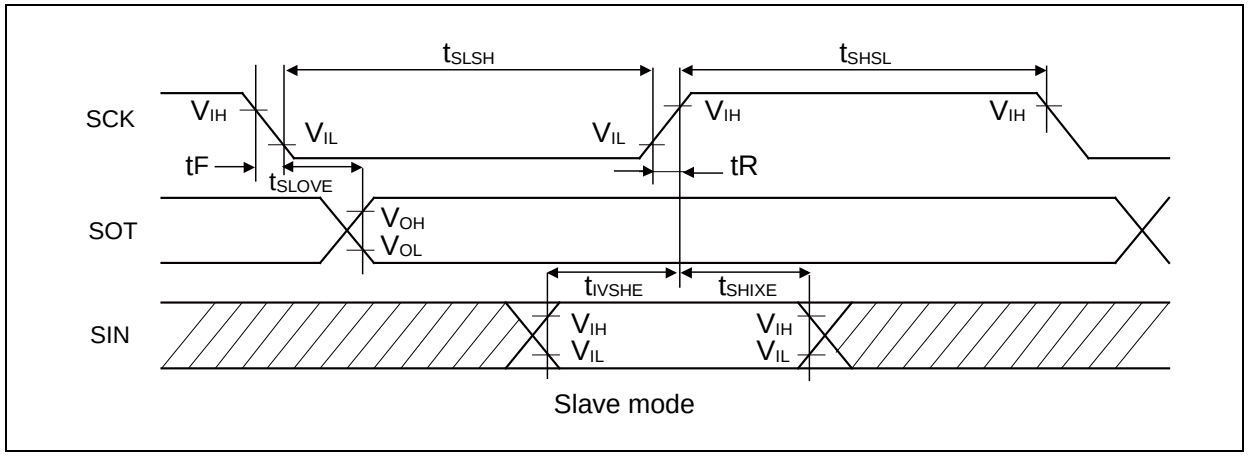
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		$V_{CC} \geq$ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number. For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

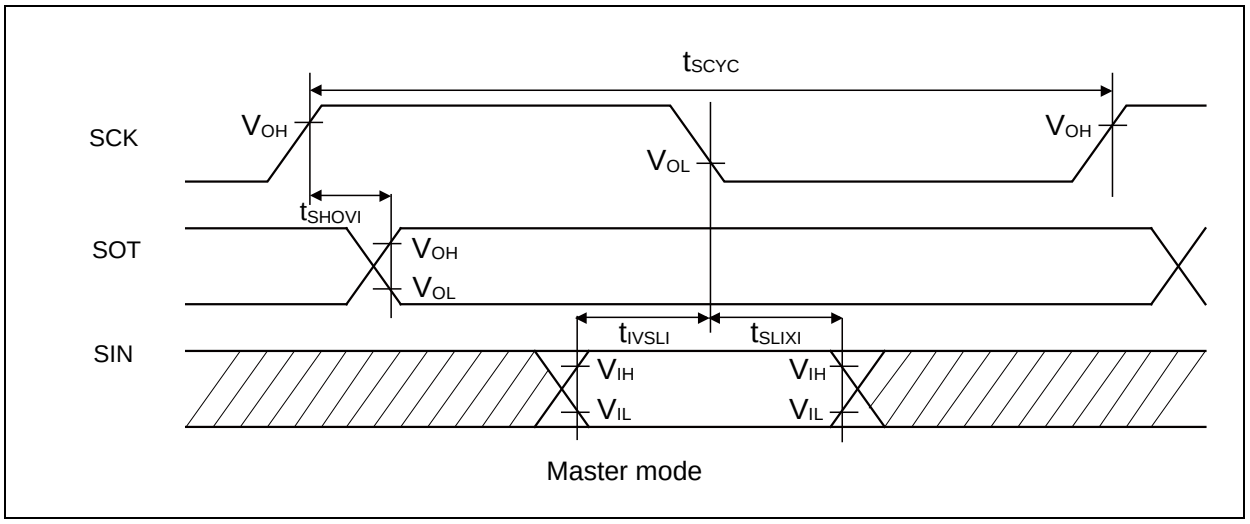
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

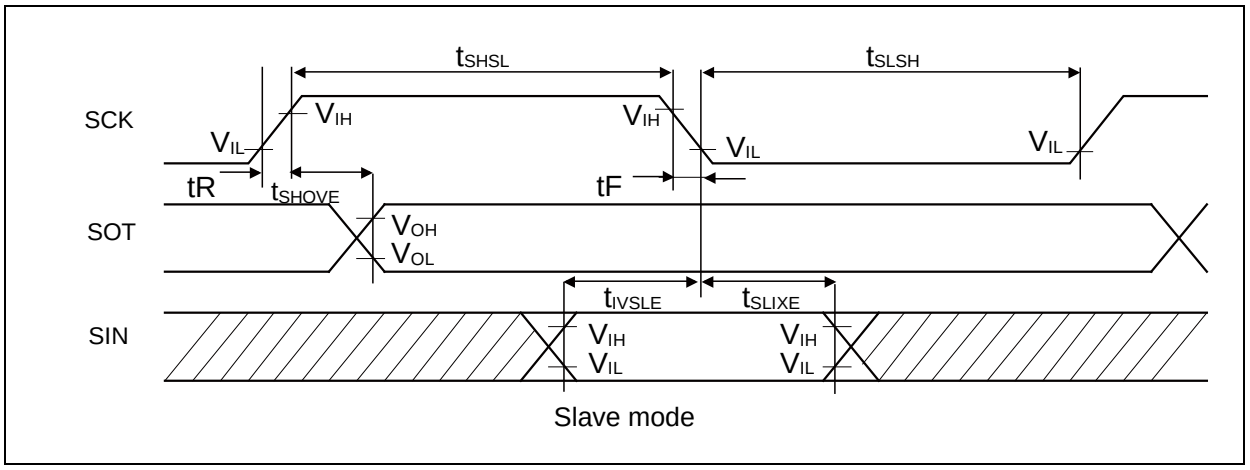
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number. For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

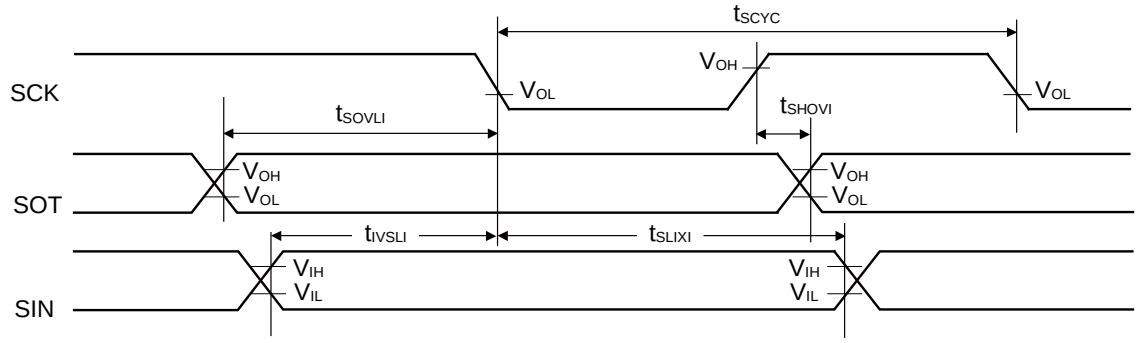
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

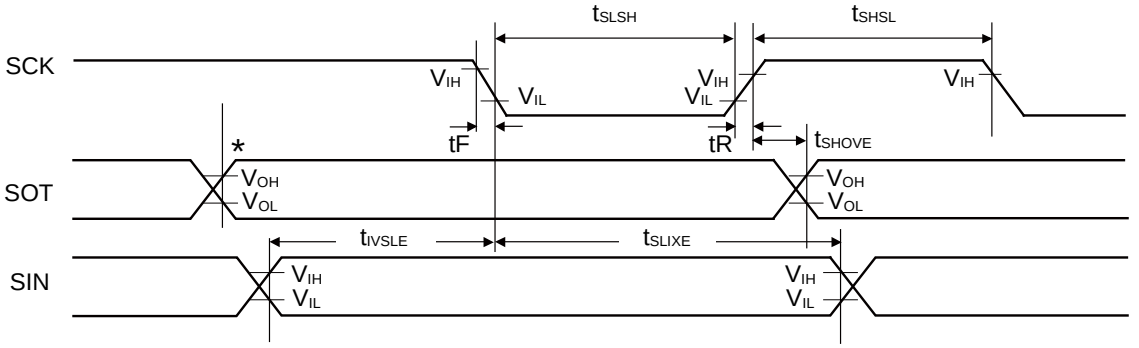
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

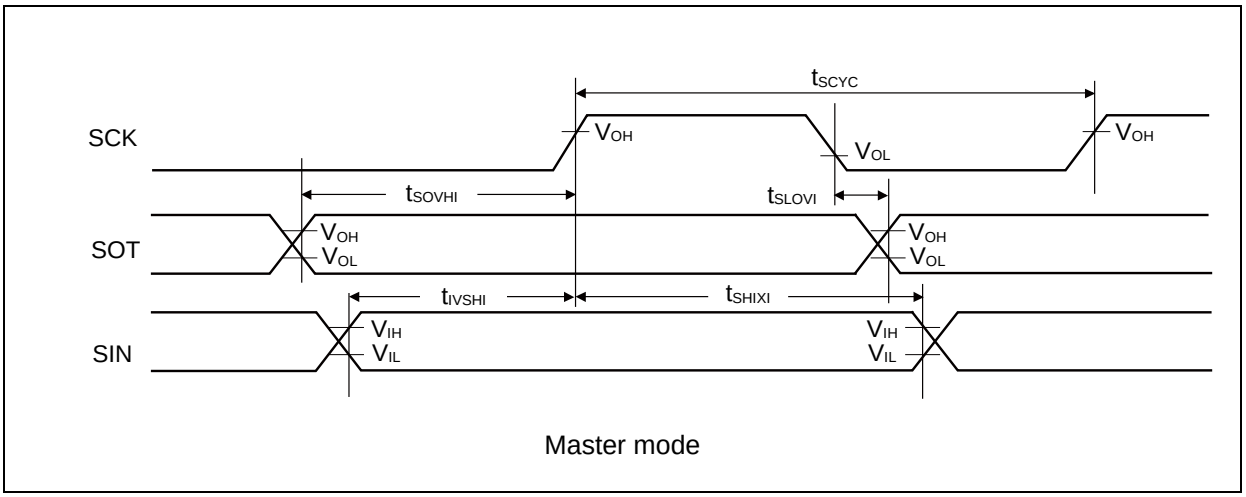
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

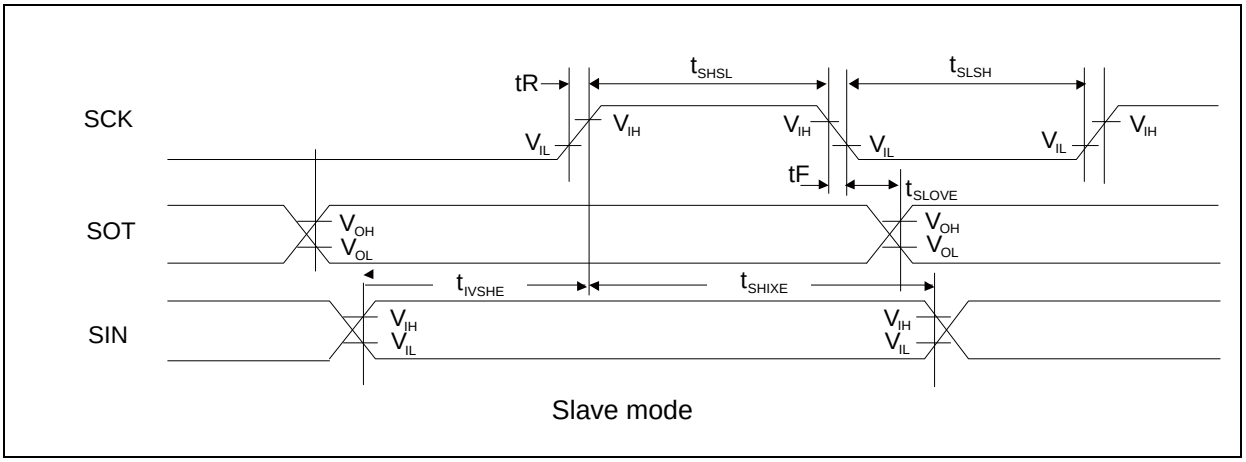
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode

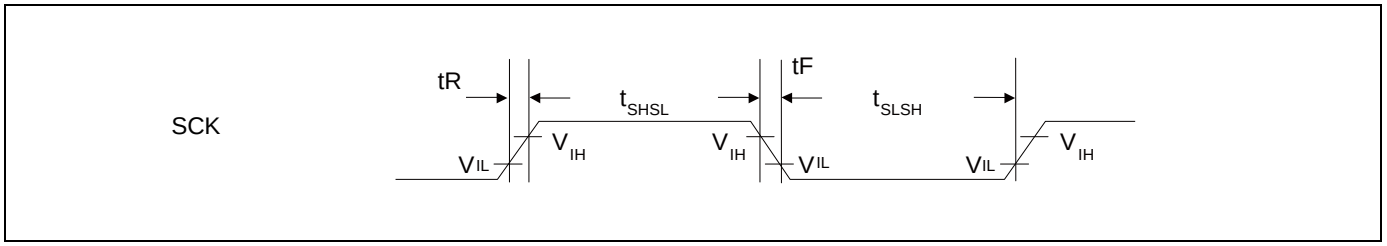


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



12.4.11 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

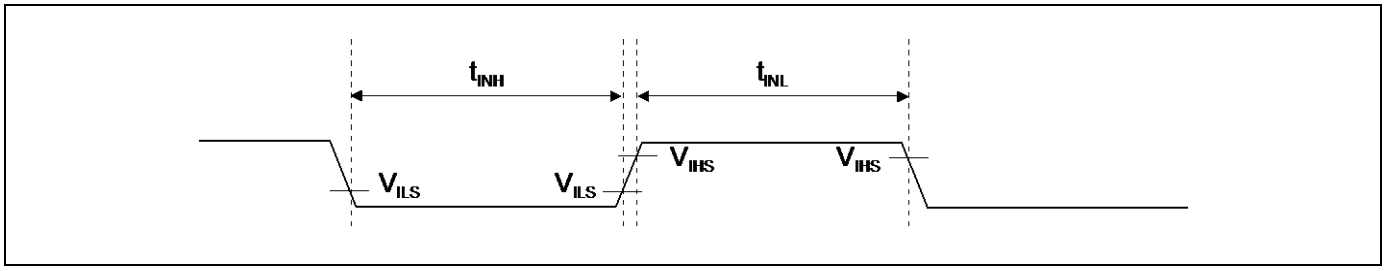
*1: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "Block Diagram" in this data sheet.

*2: When in RUN mode, in SLEEP mode.

*3: When in STOP mode, in TIMER mode.

*4: When in Deep standby RTC mode, in Deep standby STOP mode.



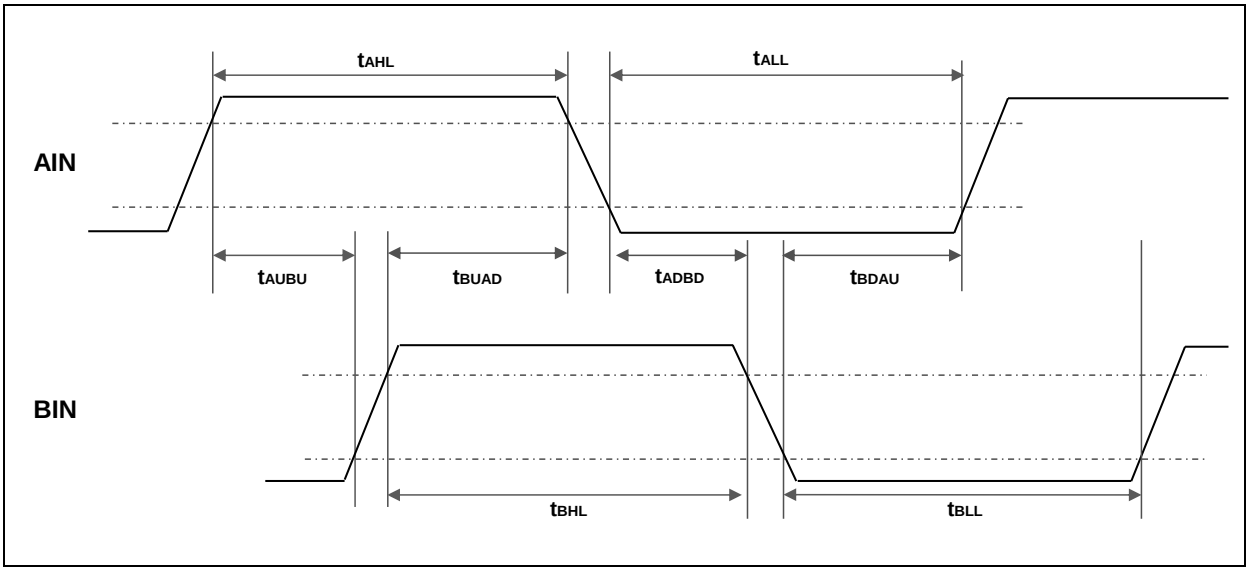
12.4.12 Quadrature Position/Revolution Counter timing

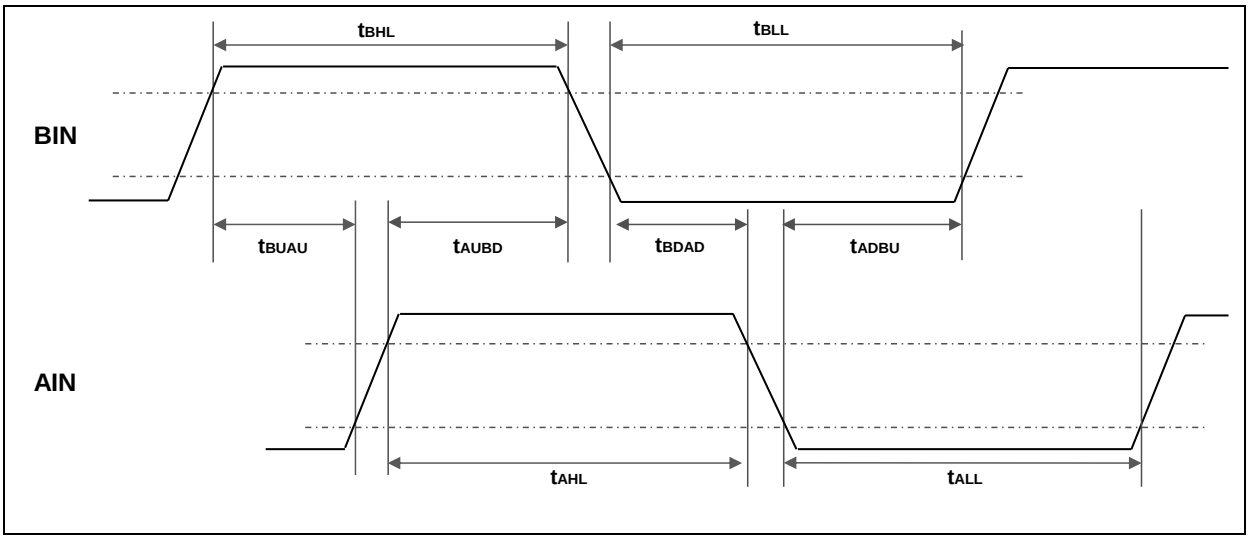
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

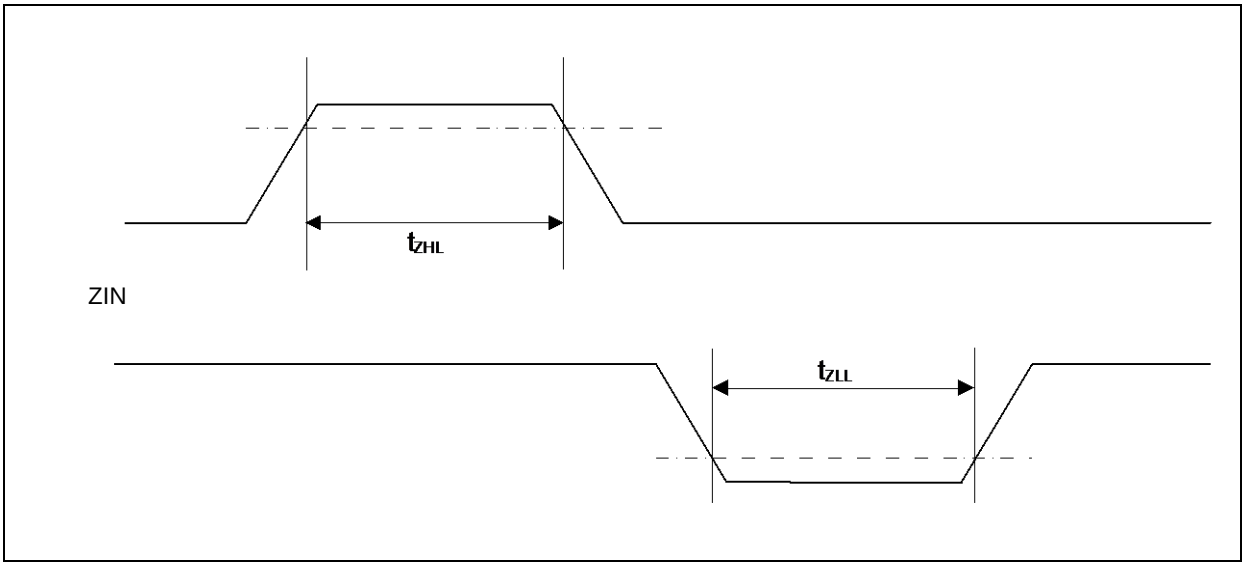
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
Time from AIN pin "H" level to BIN rise	t_{AUBU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN fall	t_{BUAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN fall	t_{ADBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN rise	t_{BDAU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN rise	t_{BUAU}	PC_Mode2 or PC_Mode3			
Time from AIN pin "H" level to BIN fall	t_{AUBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN fall	t_{BDAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN rise	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC="0"			
Time from determined ZIN level to AIN/BIN rise and fall	t_{ZABE}	QCR:CGSC="1"			
Time from AIN/BIN rise and fall time to determined ZIN level	t_{ABEZ}	QCR:CGSC="1"			

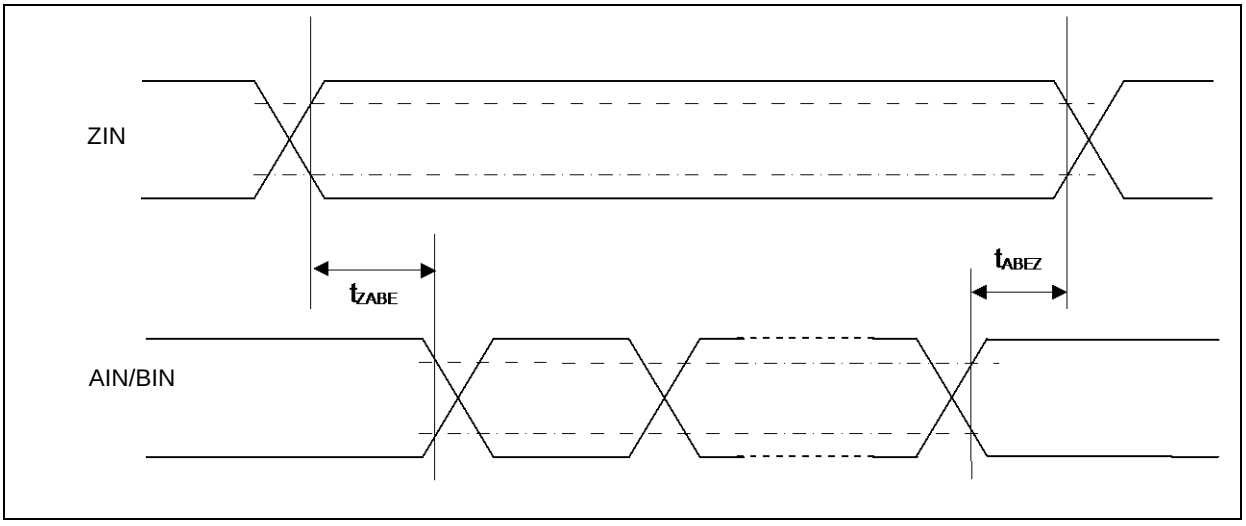
*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see "Block Diagram" in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.13 I^2C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

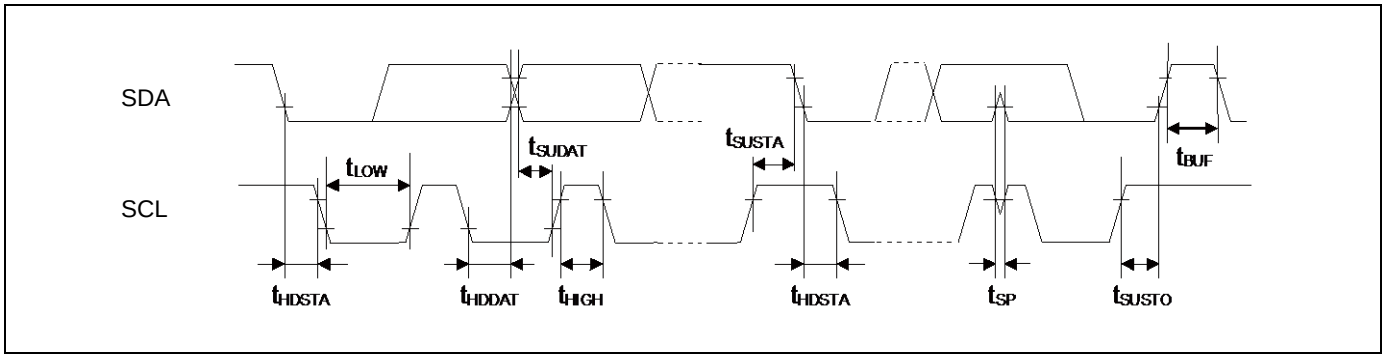
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: Fast-mode I^2C bus device can be used on Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "Block Diagram" in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



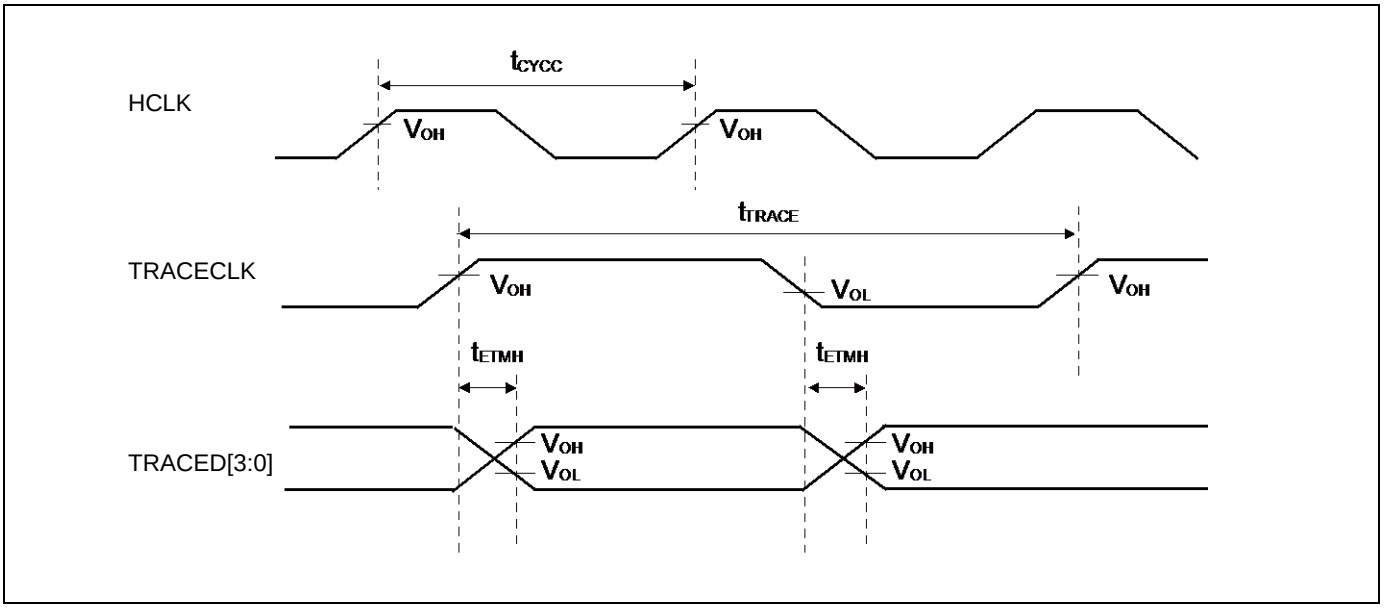
12.4.14 ETM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	$V_{CC} \geq 4.5$ V	2	10	ns	
			$V_{CC} < 4.5$ V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5$ V	-	40	MHz	
			$V_{CC} < 4.5$ V	-	20	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5$ V	25	-	ns	
			$V_{CC} < 4.5$ V	50	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



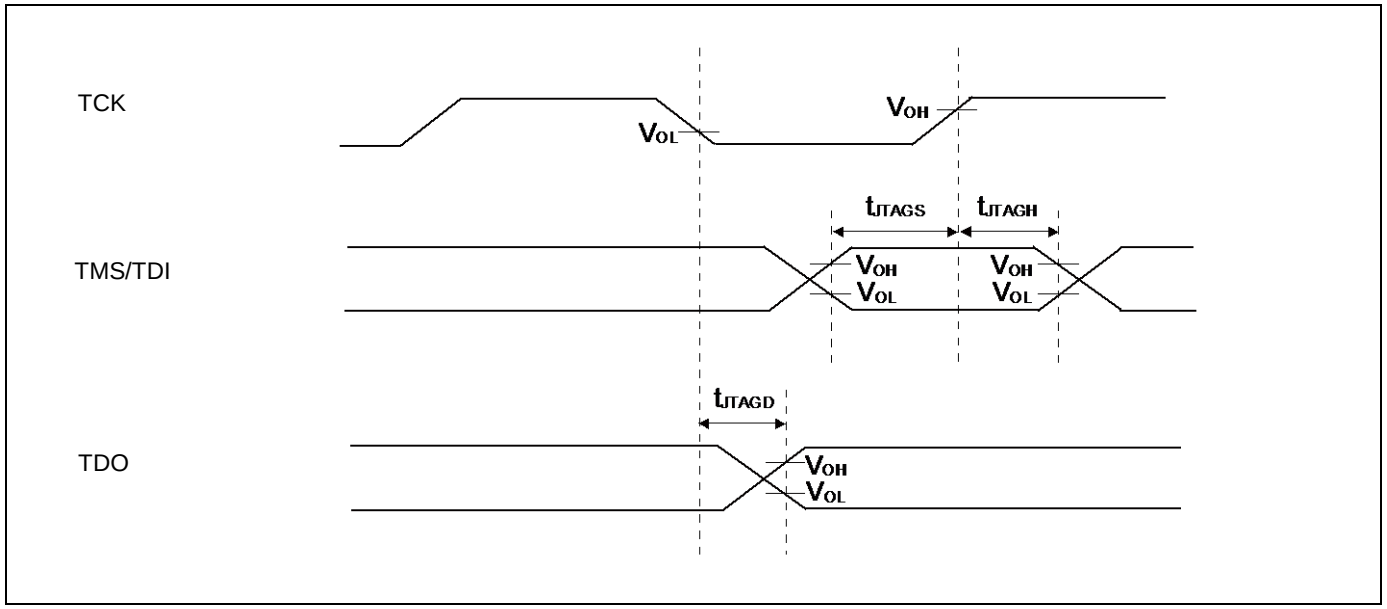
12.4.15 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.5	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 2.2	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 6	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 5	AVRH ± 15	mV	
Conversion time	-	-	1.0*1	-	-	µs	
Sampling time*2	Ts	-	0.3	-	10	µs	
Compare clock cycle*3	Tcck	-	50	-	1000	ns	
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.5	pF	
Analog input resistor	R_{AIN}	-	-	-	1.62	kΩ	AV_{CC} ≥ 4.5 V
					2.35		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is when the value of sampling time: 300 ns, the value of compare time: 700 ns (AV_{CC} ≥ 4.5 V).
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "CHAPTER 1-1: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

The register setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

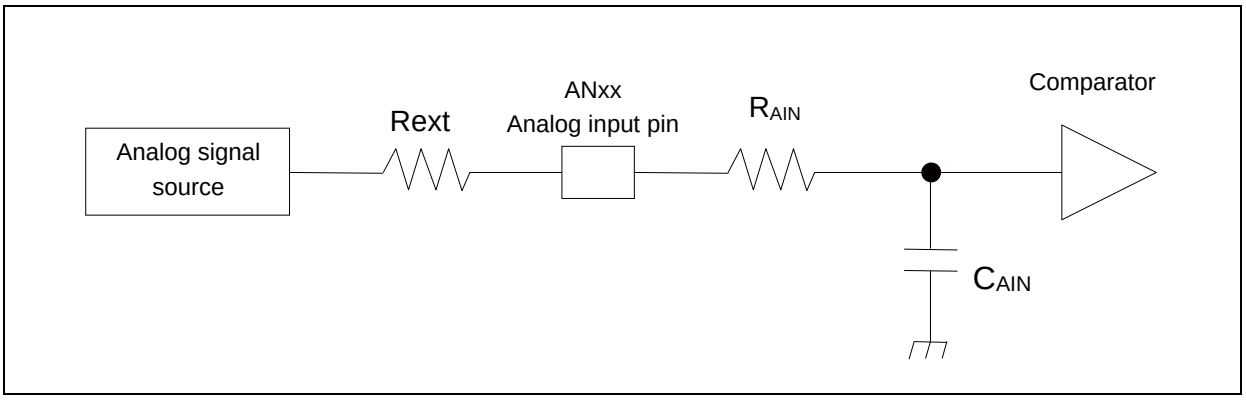
The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "Block Diagram" in this data sheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

R_{AIN}: Input resistor of A/D = 1.62 kΩ ch.0 to ch.7 at 4.5 V ≤ AV_{CC} ≤ 5.5 V
Input resistor of A/D = 1.58 kΩ ch.8 to ch.15 at 4.5 V ≤ AV_{CC} ≤ 5.5 V
Input resistor of A/D = 1.56 kΩ ch.16 to ch.23 at 4.5 V ≤ AV_{CC} ≤ 5.5 V
Input resistor of A/D = 2.35 kΩ ch.0 to ch.7 at 2.7 V ≤ AV_{CC} < 4.5 V
Input resistor of A/D = 2.3 kΩ ch.8 to ch.15 at 2.7 V ≤ AV_{CC} < 4.5 V
Input resistor of A/D = 2.25 kΩ ch.16 to ch.23 at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 9.5 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

Rext: Output impedance of external circuit

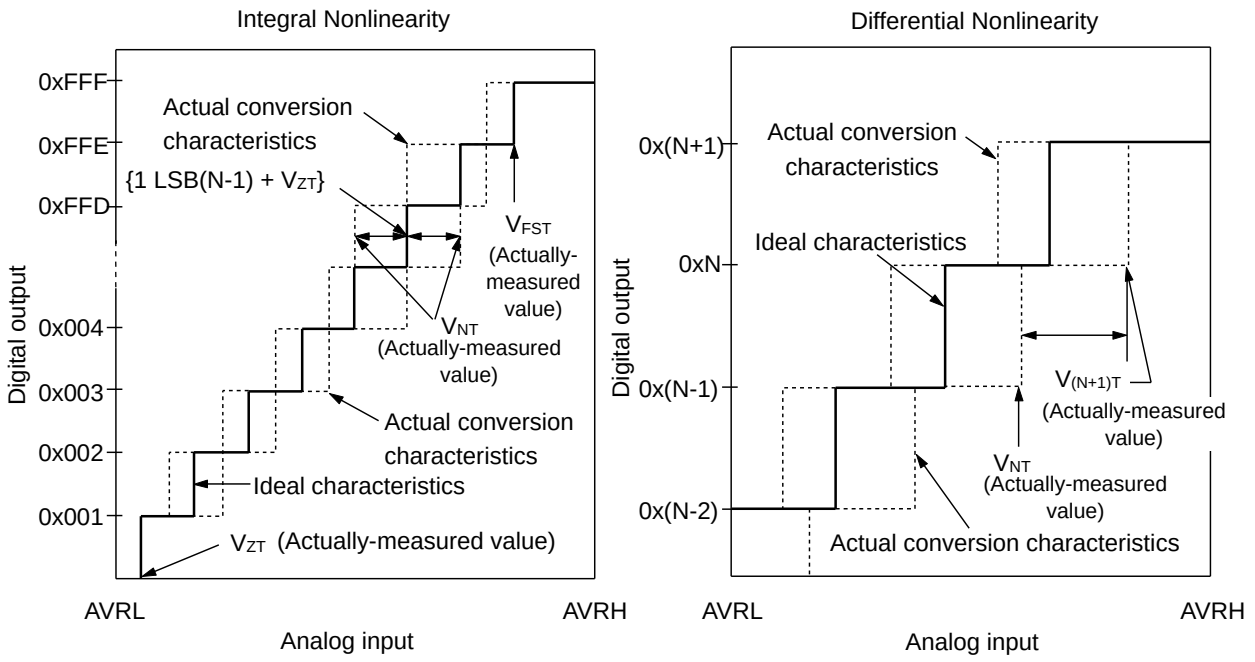
(Equation 2) Tc = Tcck × 14

Tc: Compare time

Tcck: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 10-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	tc20		0.47	0.58	0.69	µs	Load 20 pF
	tc100		2.37	2.90	3.43	µs	Load 100 pF
Integral Nonlinearity*1	INL		- 4.0	-	+ 4.0	LSB	
Differential Nonlinearity*1,*2	DNL		- 0.9	-	+ 0.9	LSB	
Output Voltage offset	V_{OFF}		-	-	10.0	mV	Code is 0x000
			- 20.0	-	+ 5.4	mV	Code is 0x3FF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	D/A stop
Output undefined period	t_R		-	-	70	ns	

*1: No-load

*2: Generates the max current by the CODE about 0x200

12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1 = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	6432 × t_{CYCP}*2	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: The SVHR bit of Low-voltage Detection Voltage Control Register (LVD_CTL) is initialized to “0000” by low-voltage detection reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

12.7.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	6432 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8 Flash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ	Max		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		20	317	µs	Not including system-level overhead time
Chip erase time		31	79	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

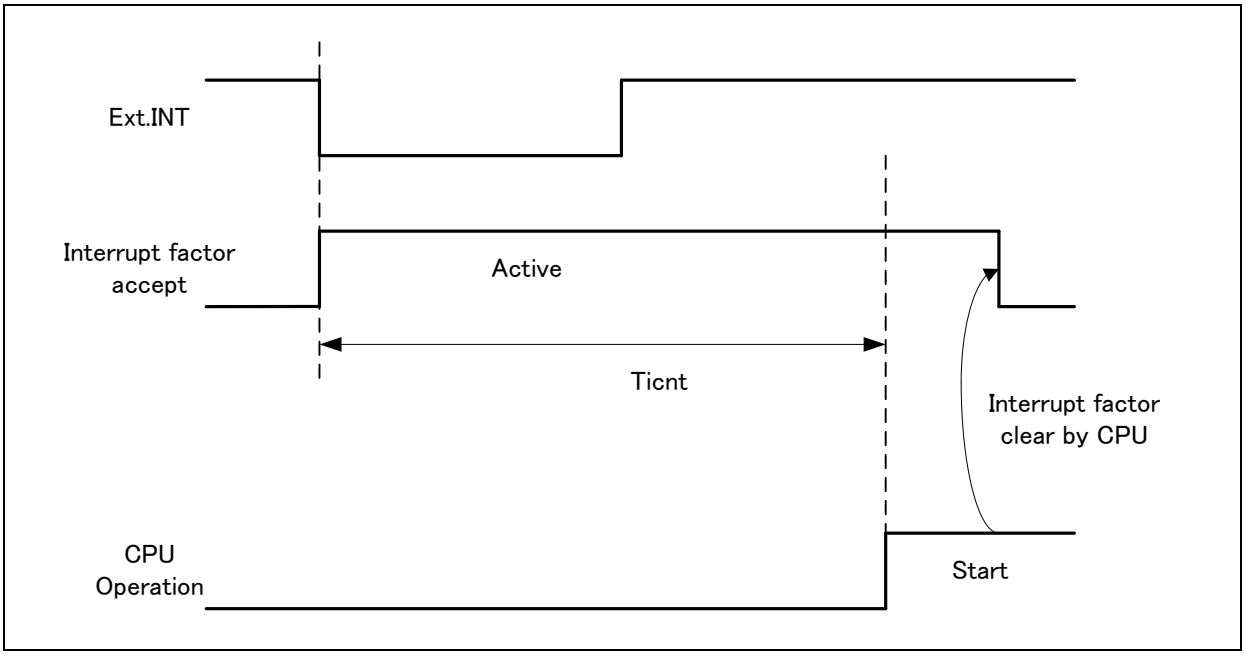
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Ticnt	t_{CYCC}		ns	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		43	83	µs	
Low-speed CR TIMER mode		310	620	µs	
Sub TIMER mode		534	724	µs	
RTC mode, STOP mode		278	479	µs	
Deep Standby RTC mode, Deep Standby STOP mode		298	543	µs	When RAM is off
		288	523	µs	When RAM is on

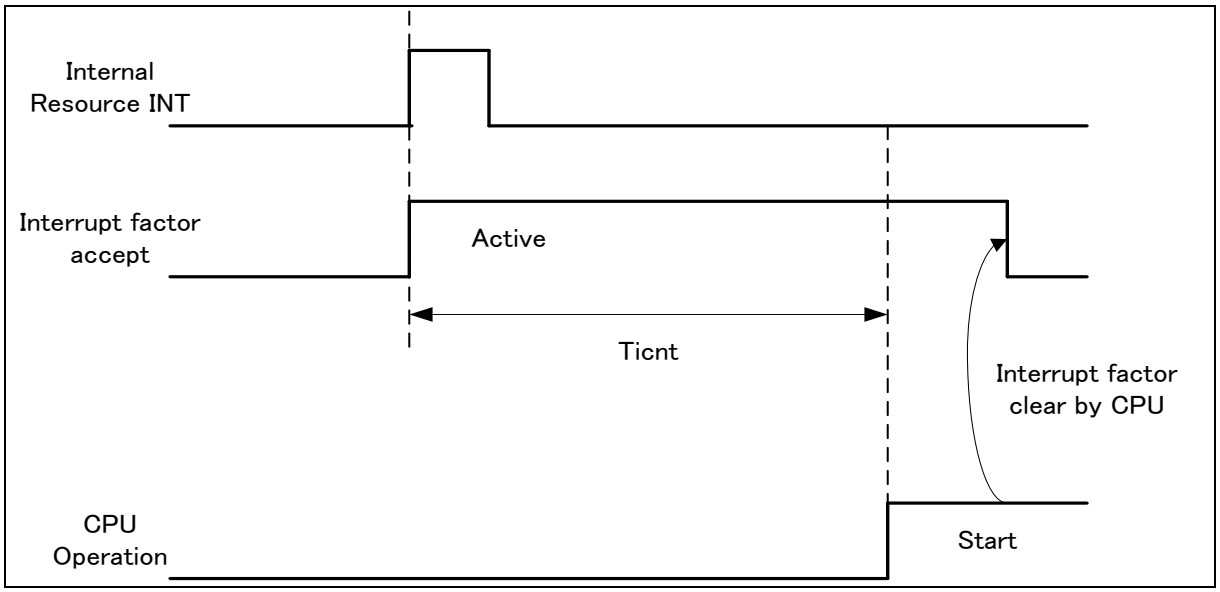
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL about the return factor from Low-Power consumption mode.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

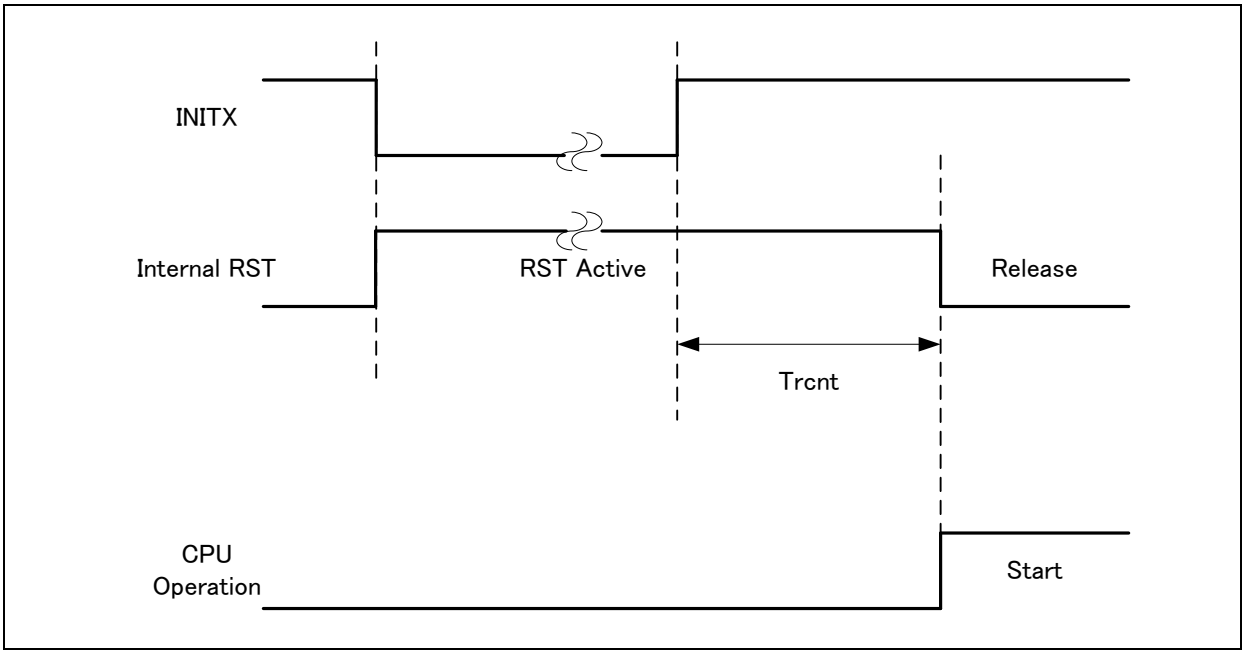
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

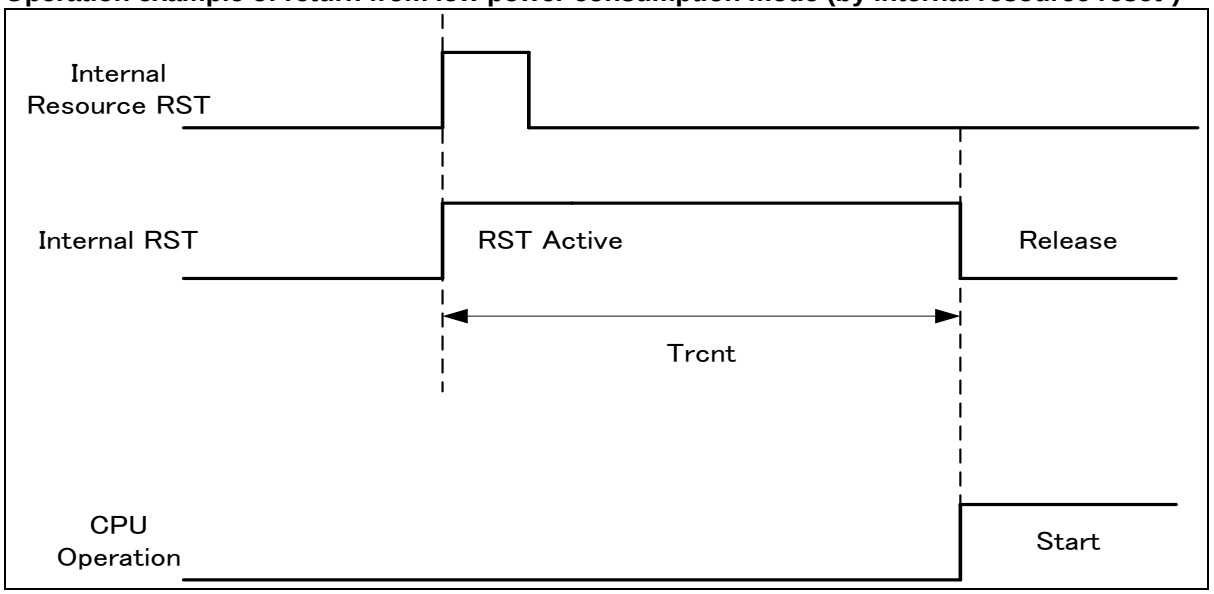
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	149	264	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		149	264	µs	
Low-speed CR TIMER mode		318	603	µs	
Sub TIMER mode		308	583	µs	
RTC/STOP mode		248	443	µs	
Deep Standby RTC mode, Deep Standby STOP mode		298	543	µs	When RAM is off
		288	523	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

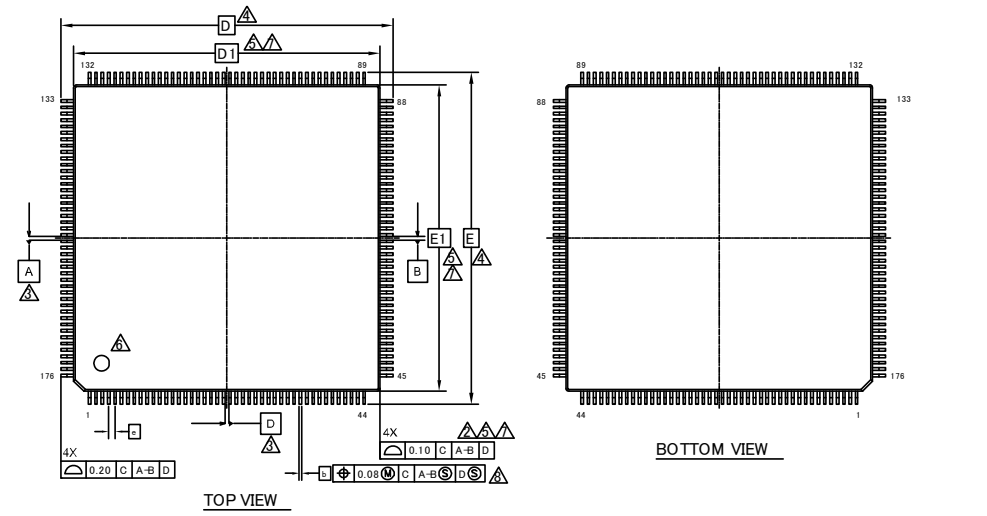
- *The return factor is different in each Low-Power consumption modes.*
  See "CHAPTER 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family PERIPHERAL MANUAL.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER 6: Low Power Consumption Mode" in "FM3 Family PERIPHERAL MANUAL".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "(6) Power-on Reset Timing in 4. AC Characteristics in Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9BF128SAPMC-GK7E2	Main: 1 Mbyte Work: 64 Kbyte	160 Kbyte	Plastic・LQFP, 144-pin (0.5 mm pitch) (LQS144)	Tray
MB9BF129SAPMC-GK7E2	Main: 1.5 Mbyte Work: 64 Kbyte	192 Kbyte		
MB9BF128TAPMC-GK7E2	Main: 1 Mbyte Work: 64 Kbyte	160 Kbyte	Plastic・LQFP, 176-pin (0.5 mm pitch) (LQP176)	
MB9BF129TAPMC-GK7E2	Main: 1.5 Mbyte Work: 64 Kbyte	192 Kbyte		

14. Package Dimensions

Package Type	Package Code
LQFP 176	LQP176



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

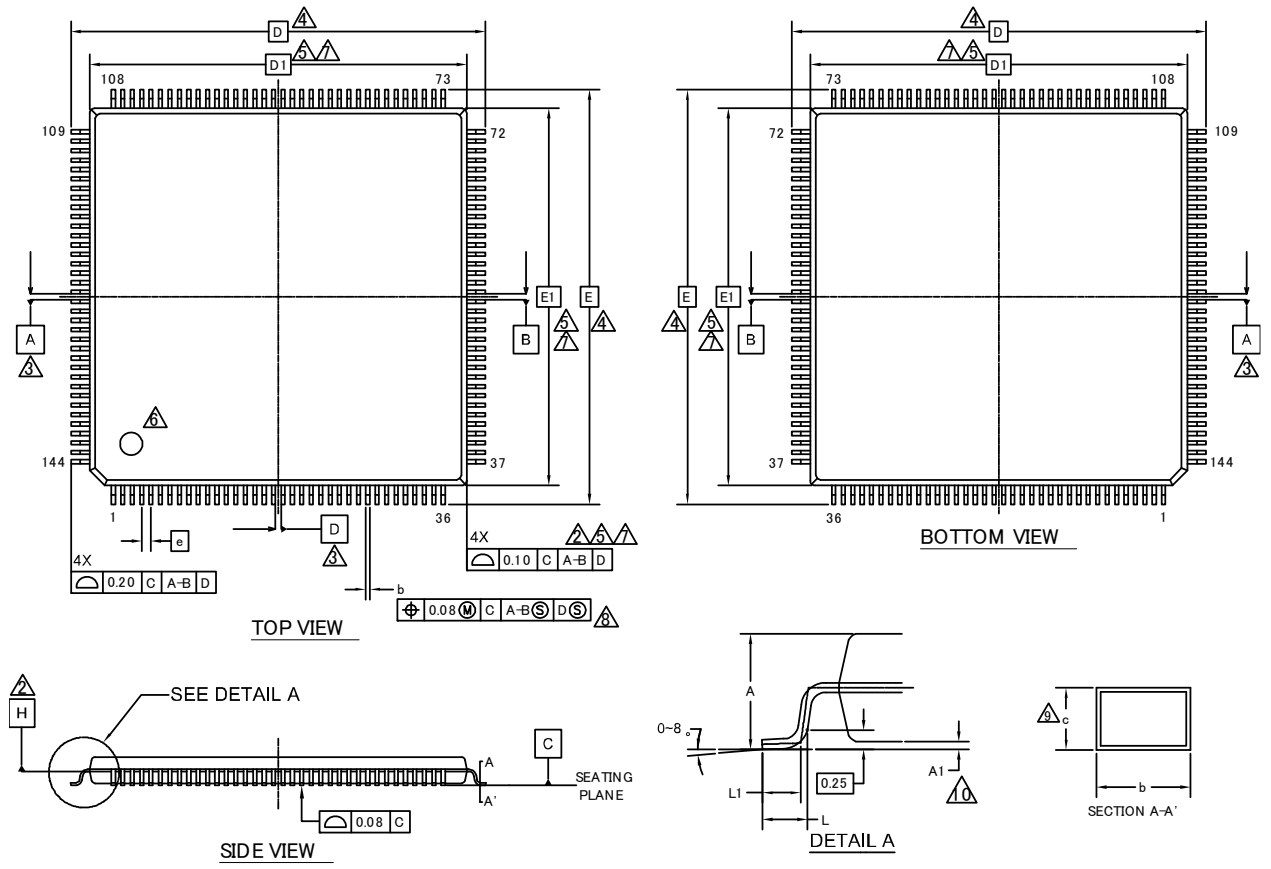
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

002-15150 **

Package Type	Package Code
LQFP 144	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

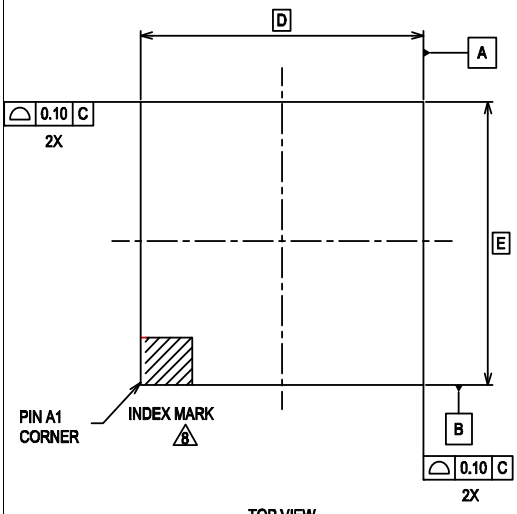
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *A

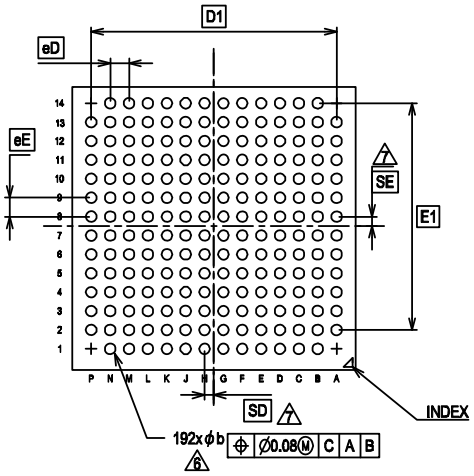
PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

Package Type	Package Code
BGA 192	LBE192

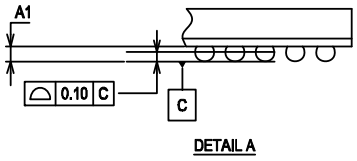
LBE192 192 BALL LOW PROFILE FINE PITCH BALL GRID ARRAY PACKAGE



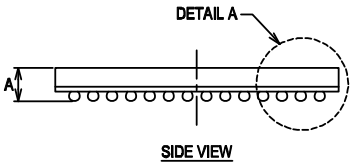
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	1.45	PROFILE
A1	0.25	0.35	0.45	TERMINAL HEIGHT
D		12.00 BSC		BODY SIZE
E		12.00 BSC		BODY SIZE
D1		10.40 BSC		MATRIX FOOTPRINT
E1		10.40 BSC		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		192		BALL COUNT
ϕb	0.35	0.45	0.55	BALL DIAMETER
eD		0.80 BSC		BALL PITCH
eE		0.80 BSC		BALL PITCH
SD / SE		0.40		SOLDER BALL PLACEMENT
		A1,A14,P1,P14		DEPOPULATED SOLDER BALL LOCATIONS

1. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE=0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE= e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0A 002-13493 *A

15. Errata

This chapter describes the errata for MB9B120T series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

15.1 Part Numbers Affected

Part Number
Initial Revision
MB9BF128TPMC-GE2, MB9BF129TPMC-GE2, MB9BF128TBGL-GE1, MB9BF129TBGL-GE1, MB9BF128SPMC-GE2, MB9BF129SPMC-GE2, MB9BF128TPMC-GK7E2, MB9BF129TPMC-GK7E2, MB9BF128TBGL-GK7E1, MB9BF129TBGL-GK7E1, MB9BF128SPMC-GK7E2, MB9BF129SPMC-GK7E2

15.2 Qualification Status

Product Status: In Production − Qual.

15.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
[1] HDMI-CEC polling message issue	Refer to 15.1	Initial rev.	Fixed in Rev. A

15.4 Errata Detail

15.4.1 HDMI-CEC polling message issue

■ PROBLEM DEFINITION
Error#1) While MCU sends a Polling Message, it always returns a NACK to a message coming to the MCU from another node.

Error#2) MCU always waits for 7-bit signal free on CEC line before it drives the line even when the last line initiator was another node.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
This error always happens.

■SCOPE OF IMPACT
MCU does not reply properly to another node.

■WORKAROUND
The software workaround is applied to Error #1.

1. Store 0x0 to SFREE register.
2. Monitor CEC line with GPIO and wait until 1 lasts for the signal free time.
3. Store frame data to TXDATA register and store 0x0F to RCADR1 or RCADR2 register.

It sends a message after 3~4 clocks of 32.768 kHz clock when TXDATA is stored 0x0F.

If the device receives a frame from another node within 2~3 clocks after storing TXDATA, the bus error occurs and if the device receives a frame from another node within 3~4 clocks after storing TXDATA, the arbitration lost occurs. In these cases:

4-A-1. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-A-2. Return back to step 2 above

If the device receives a frame from another node within 1~2 clocks after storing TXDATA, take these steps.

4-B-1. Monitor CEC line with GPIO after 50us from storing TXDATA

4-B-2. Set TXEN to 1 -> 0 -> 1 immediately when GPIO finds state low on the CEC line

4-B-3. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-B-4. Return back to step 2 above

For Error #2, there is no software workaround, but signal free time of fixed 7-bit does not violate HDMI-CEC specification. The specification says signal free time must be more than and equals to 5-bit.

■FIX STATUS
This issue was fixed in Rev. A.

16. Major Changes

Spansion Publication Number: DS706-00063

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
-	-	Company name and layout design change
Revision 1.0		
-	-	Preliminary → Full Production
2	FEATURES External Bus Interface	Added the descriptions as follows ・Maximum area size : Up to 256 Mbytes
3	FEATURES A/D Converter	Corrected conversion time
5	FEATURES Multi-function Timer	Corrected the channel count of "A/D activation compare"
7	PRODUCT LINEUP Function	Added the footnote
63	HANDLING DEVICES ・Power supply pins	Added the description
65	BLOCK DIAGRAM	Corrected the figure
66	MEMORY MAP ・Memory Map(1)	Corrected the Address of “External Device Area”
76	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Added the Item of “Input Voltage”
78	2. Recommended Operating Conditions	Added the footnote
79 - 81	3.DC Characteristics (1) Current Rating	・Corrected the Condition ・Corrected the Value ・Corrected the Remarks ・Added the footnote
83	(2) Pin Characteristics	Added the Item of “Input leak current”
88	4. AC Characteristics (6) Power-on Reset Timing	・Revised the values of “Time until releasing Power-on reset” ・Corrected the figure ・Corrected the Glossary
107	(9) CSIO Timing ・Synchronous serial (SPI=1, SCINV=1)	Corrected the figure of “MS bit=1”
	・External clock (EXT=1):asynchronous only	Corrected the figure
114	5.12-bit A/D Converter ・Electrical characteristics for the A/D converter	・Corrected the Pins name AN00 - AN23 → ANxx ・Corrected the Min Vale of “Conversion time” ・Corrected the Min Vale of “Sampling time” ・Corrected the Min Value of “Compare clock cycle” ・Corrected the “State Transition time to operation permission” ・Corrected the footnote
119	9. Electrical characteristics for the A/D converter (1) Write / Erase time	Revised the values of “TBD”

Page	Section	Change Results
120	10. Return Time from Low-Power Consumption Mode (1) Return Factor: Interrupt/WKUP • Return Count Time	Revised the values of “TBD”
122	(2) Return Factor: Reset • Return Count Time	Revised the values of “TBD”
Revision 2.0		
-	-	Changed the series name. MB9B120T Series -> MB9B120TA Series
-	-	Changed the product name as follows. MB9BF128SA, MB9BF129SA, MB9BF128TA, MB9BF129TA
41 to 48	List of Pin Functions · List of pin functions	Added LIN to the description of SOTxx
55, 56	I/O Circuit Type	Added about +B input
67	Memory Map · Memory map(2)	Added the summary of Flash memory sector
76, 77	Electrical Characteristics 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added about +B input
79, 80	Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the expression of condition · Added Main TIMER mode current
87	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added the figure of Main PLL connection
100 to 107	Electrical Characteristics 4. AC Characteristics (7) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
114	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage
125	Ordering Information	Change to full part number

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB9B120TA Series, 32-bit Arm® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05667

<table>
<tr><th>Revision</th><th>ECN</th><th>Orig. of Change</th><th>Submission Date</th><th>Description of Change</th></tr>
<tr><td>**</td><td>-</td><td>TOYO</td><td>01/30/2015</td><td>Migrated to Cypress and assigned document number 002-05667.
No change to document contents or format.</td></tr>
<tr><td>*A</td><td>5201323</td><td>TOYO</td><td>04/05/2016</td><td>Updated to Cypress template.</td></tr>
<tr><td>*B</td><td>5653479</td><td>NOSU</td><td>03/10/2017</td><td>Corrected the package codes the following chapters as the table below.
2. Packages
3. Pin Assignment
13. Ordering Information
14. Package Dimensions
<table>
<tr><th>Before</th><th>After</th></tr>
<tr><td>FPT-144P-M08</td><td>LQS144</td></tr>
<tr><td>FPT-176P-M07</td><td>LQP176</td></tr>
<tr><td>BGA-192P-M06</td><td>LBE192</td></tr>
</table>
Modified RTC description in chapter Features
Before
The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available.
After
The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute.) is available.
Corrected a word “J-TAG” to “JTAG” in 4. List of Pin Functions (Page 32)
Added a note of “TAP Controller” in 4. List of Pin Functions (Page 52)
Corrected sector size of Memory Map (2) in 10. Memory Map
ROM1_SA8_15(8KBx8) → ROM1_SA8_15(64KBx8)
Replaced a word “Ta” to “T_A” in the following chapters.
12.2. Recommended Operating Conditions
12.3. DC Characteristics
12.4. AC Characteristics
12.5. 12-bit A/D Converter
12.6. 10-bit D/A Converter
12.7. Low-Voltage Detection Characteristics
12.8. Flash Memory Write/Erase Characteristics
12.9. Return Time from Low-Power Consumption Mode
Added the Baud rate spec in 12.4.10 CSIO Timing (Page 101, 103, 105, 107)
Updated 12.4.7. Power-on Reset Timing
Corrected the following statement in chapter 12.5. 12-bit A/D Converter
Analog port input current → Analog port input leak current
Corrected the Part numbers in chapter 13. Ordering Information
MB9BF128SAPMC-GE1 → MB9BF128SAPMC-GK7E2
MB9BF129SAPMC-GE1 → MB9BF129SAPMC-GK7E2
MB9BF128TAPMC-GE1 → MB9BF128TAPMC-GK7E2
MB9BF129TAPMC-GE1 → MB9BF129TAPMC-GK7E2
MB9BF128TABGL-GE1 → MB9BF128TABGL-GK7E1
MB9BF129TABGL-GE1 → MB9BF129TABGL-GK7E1
Updated 14. Package Dimensions
Added 15. Errata
Updated to new template.</td></tr>
</table>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C	5790538	YSAT	07/04/2017	Updated Cypress Logo and Copyright.
*D	6013729	YSAT	01/12/2018	Updated 14. Package Dimensions: Updated figure of LBE192 (spec 002-13493 – Changed revision from ** to *A). Updated to new template. Completing Sunset Review.
*E	6616702	WHAO	07/08/2019	Updated Ordering Information: Updated part numbers. Updated to new template.

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