

NB7N017M

3.3V SiGe 8-Bit Dual Modulus Programmable Divider/Prescaler with CML Outputs

The NB7N017M is a high speed 8-bit dual modulus programmable divider/prescaler with 16 mA CML outputs capable of switching at input frequencies greater than 3.5 GHz. The CML output structure contains internal 50 Ω source termination resistor to V_{CC} . The device generates 400 mV output amplitude with 50 Ω receiver resistor to V_{CC} . This I/O structure enables easy implementation of the NB7N017M in 50 Ω systems.

The differential inputs contain 50 Ω termination resistors to VT pads and all differential inputs accept RSECL, ECL, LVDS, LVCMOS, LVTTTL, and CML.

Internally, the NB7N017M uses a > 3.5 GHz 8-bit programmable down counter. A select pin, SEL, is used to select between two words, Pa[0:7] and Pb[0:7], that are stored in REGa and REGb respectively. Two parallel load pins, PLa and PLb, are used to load the level triggered programming registers, REGa and REGb, respectively. A differential clock enable, CE, pin is available.

The NB7N017M offers a differential output, TC. Terminal count output, TC, goes high for one clock cycle when the counter has reached the all zeros state. To reduce output phase noise, TC is retimed with the rising edge triggered latches.

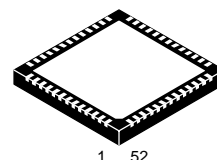
Features

- Maximum Input Clock Frequency > 3.5 GHz Typical
- Differential CLK Clock Input
- Differential CE Clock Enable Input
- Differential SEL Word Select Input
- 50 Ω Internal Input and Output Termination Resistors
- Differential TC Terminal Count Output
- All Outputs 16 mA CML with 50 Ω Internal Source Termination to V_{CC}
- All Single-Ended Control Pins CMOS and PECL/NECL Compatible
- Counter Programmed Using One of Two Single-Ended Words, Pa[0:7] and Pb[0:7], Stored in REGa and REGb
- REGa and REGb Implemented with Level Triggered Latch
- Compatible with Existing 3.3 V LVEP, EP, and SG Devices
- Ability to Program the Divider without Disturbing Current Settings
- Positive CML Output Operating Range: $V_{CC} = 3.0$ V to 3.465 V with $V_{EE} = 0$ V
- Negative CML Output Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -3.465 V
- V_{BB} Reference Voltage Output
- CML Output Level: 400 mV Peak-Peak Output with 50 Ω Receiver Resistor to V_{CC}
- Pb-Free Packages are Available*



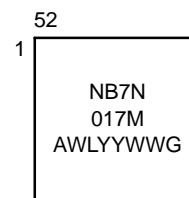
ON Semiconductor®

<http://onsemi.com>



QFN-52
MN SUFFIX
CASE 485M

MARKING DIAGRAM*



A = Assembly Site
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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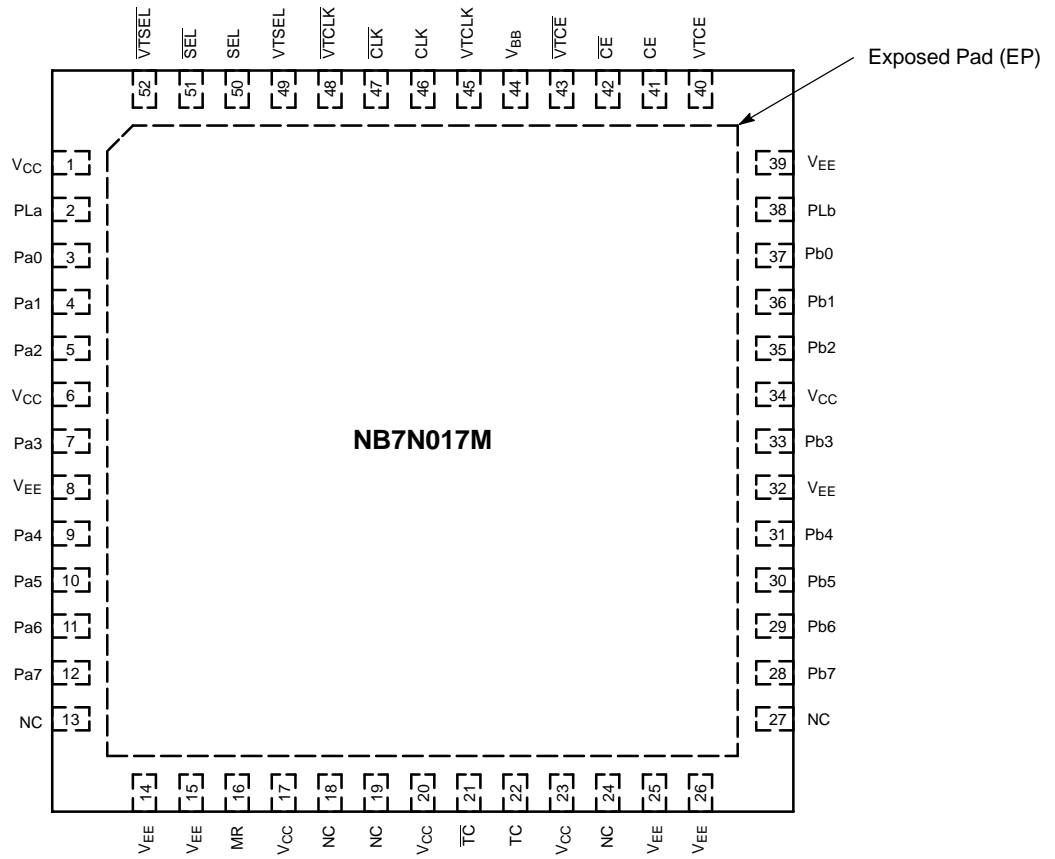


Figure 1. Pinout (Top View)

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Table 1. PIN DESCRIPTION

| Pin Name | I/O | Default State | Single/Differential (Notes 1 and 2) | Description |
|--|--------------------------------------|---------------|-------------------------------------|--|
| CLK | ECL, CML, LVCMOS, LVDS, LVTTTL Input | – | Differential | Clock |
| CE | ECL, CML, LVCMOS, LVDS, LVTTTL Input | – | Differential | Clock Enable |
| MR | CMOS, ECL Input | Low | Single | Asynchronous Master Reset: Counter set to 0000 0000 to reload at next CLK pulse, REGa and REGb = 1111 1111 and TC = 1. |
| SEL | ECL, CML, LVCMOS, LVDS, LVTTTL Input | – | Differential | Divide Select |
| PLa, PLb | CMOS, ECL Input | Low | Single | Parallel Load Counter Latch from Pa[0:7], Pb[0:7] (Level Triggered) |
| TC | CML Output | – | Differential | Terminal Count, 16 mA CML output with 50 Ω Source Termination to V _{CC} (Note 5) |
| Pa[0:7], Pb[0:7] | CMOS, ECL Input | High | Single | Counter Program Pins. CMOS and PECL/NECL compatible Pa7 = MSB, Pb7 = MSB |
| V _{CC} | Power | – | – | Positive Supply |
| V _{EE} | Power | – | – | Negative Supply |
| VTCLK, $\overline{\text{VTCLK}}$, VTSEL, $\overline{\text{VTSEL}}$, VTCE, $\overline{\text{VTCE}}$ | Termination | – | Differential | 50 Ω Internal Input Termination Resistor (Note 6) |
| V _{BB} | Output | – | – | CMOS/ECL Reference Voltage Output |
| NC | N/A | – | – | No Connect (Note 4) |
| EP | – | – | – | Exposed Pad (Note 3) |

1. All high speed inputs and outputs are differential to improve performance.
2. All single-ended inputs are CMOS and NECL/ECL compatible.
3. All V_{CC} and V_{EE} pins must be externally connected to external power supply voltage to guarantee proper device operation. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit. Exposed pad is bonded to the lowest voltage potential, V_{EE}.
4. The NC pins are electrically connected to the die and must be left open.
5. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.
6. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

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Table 2. CE Truth Table

| CE | Clock Status |
|------|----------------|
| LOW | Clock Disabled |
| HIGH | Clock Enabled |

Table 3. SEL Truth Table

| SEL | Active Register |
|------|-----------------|
| LOW | REGa |
| HIGH | REGb |

Table 4. Register Programming Values for Various Divide Ratios

| Pa7/Pb7 | Pa6/Pb6 | Pa5/Pb5 | Pa4/Pb4 | Pa3/Pb3 | Pa2/Pb2 | Pa1/Pb1 | Pa0/Pb0 | Divide By |
|---------|---------|---------|---------|---------|---------|---------|---------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | undefined |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 |
| - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 254 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |

Table 5. Function Table

| MR | Pla | PLb | SEL | CE | CLK | Function |
|----|-----|-----|-----|----|-----|---|
| H | X | X | X | X | X | Master Reset (Counter programmed to 0000 0000, REGa and REGb programmed to 1111 1111 and TC to 1) |
| L | H | L | X | X | X | REGa is transparent to Pa[0:7] |
| L | L | H | X | X | X | REGb is transparent Pb[0:7] |
| L | L | L | L | H | Z | Count; At TC pulse, load counter from REGa |
| L | L | L | H | H | Z | Count; At TC pulse, load counter from REGb |
| L | X | X | X | L | X | Hold |

X – Don't Care

H – HIGH

L – LOW

Z – Rising Edge

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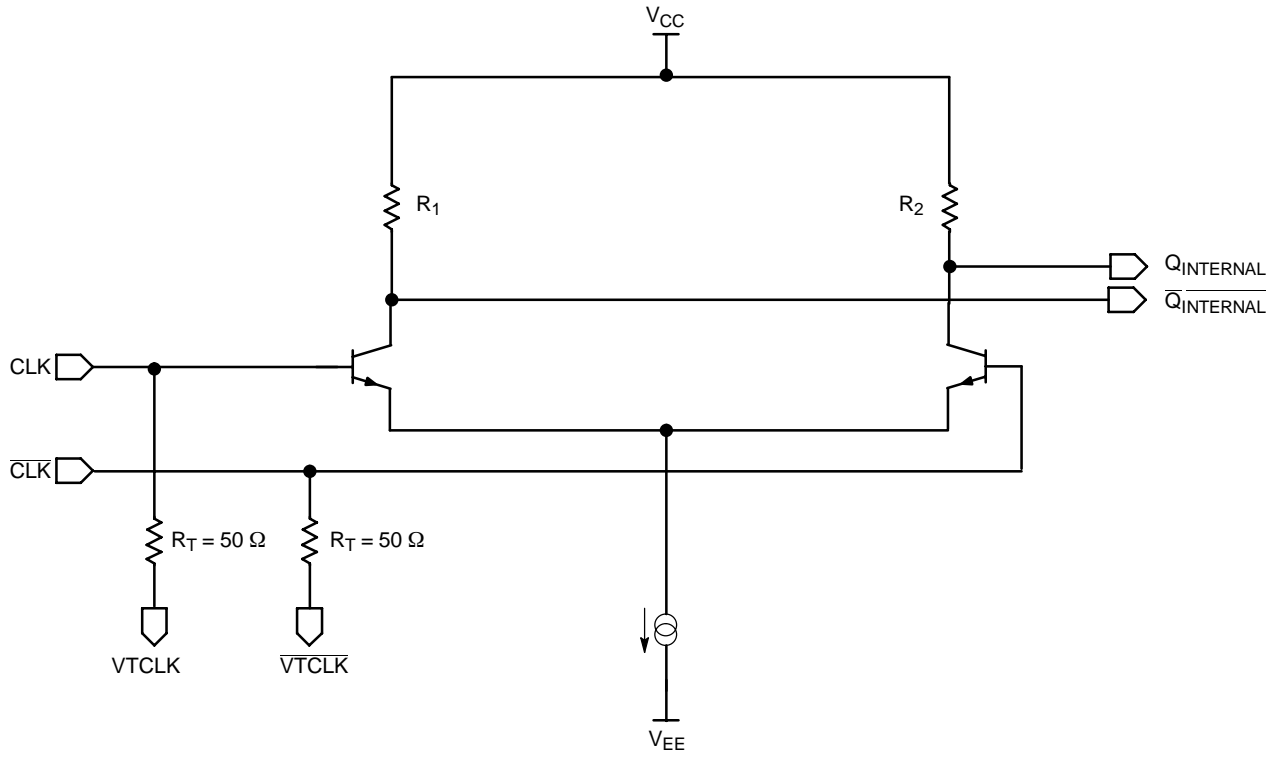


Figure 2. Input Structure

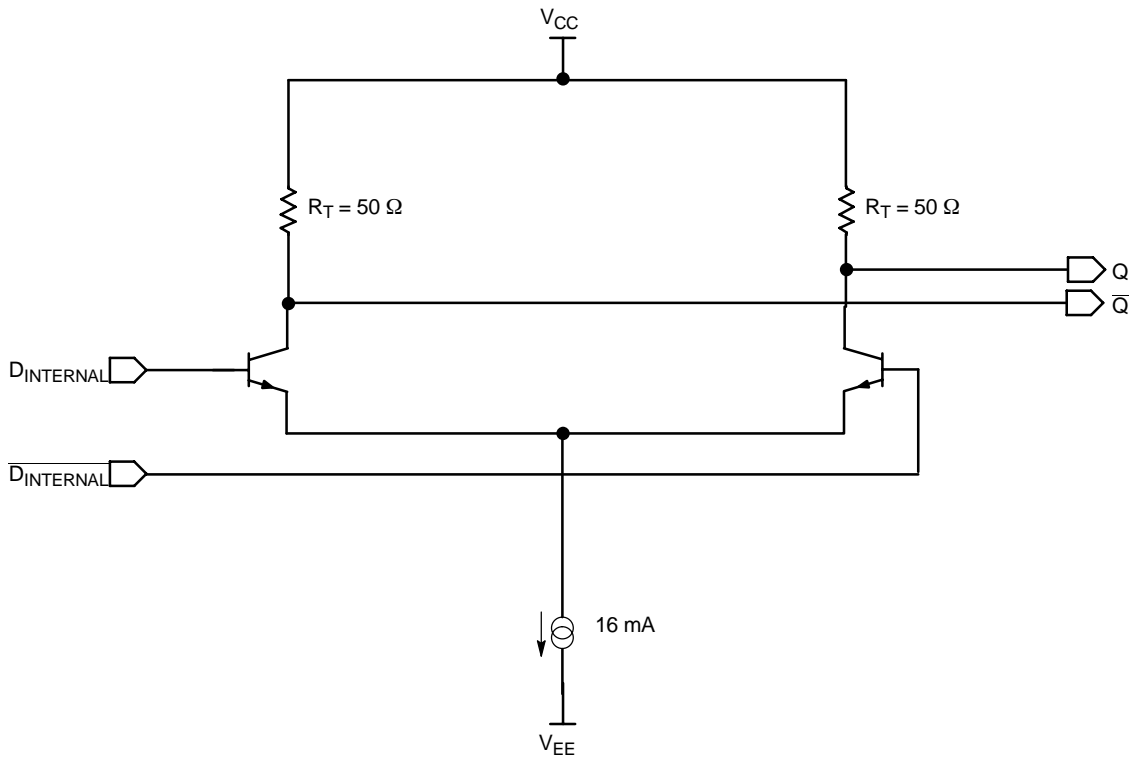


Figure 3. Output Structure

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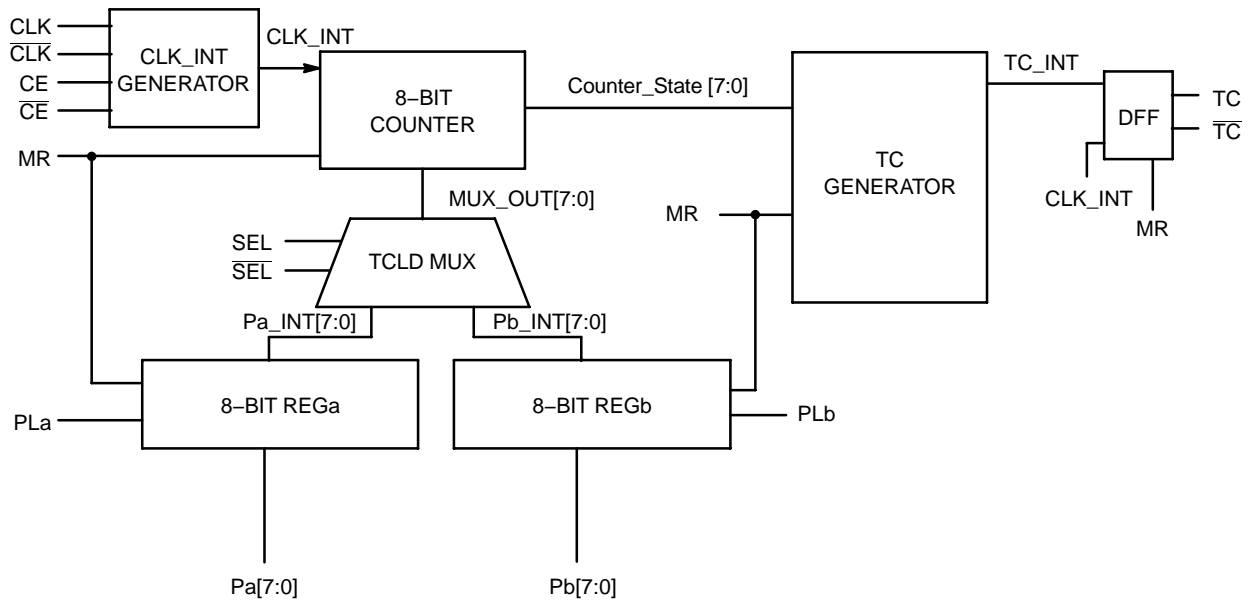


Figure 4. Block Diagram

Table 6. Interface Options

| CLK INPUT interfacing options | CLK INPUT INTERFACING OPTIONS |
|-------------------------------|---|
| CML | Connect VTCLK and \overline{VTCLK} to V_{CC} |
| LVDS | Connect VTCLK and \overline{VTCLK} together |
| AC-COUPLED | Bias VTCLK and \overline{VTCLK} Inputs within (VIHCMR) Common Mode Range |
| RSECL, PECL, NECL | Standard ECL Termination Techniques or connect VTCLK and \overline{VTCLK} to V_{TT} |
| LVTTL, LVCMOS | An Entered Voltage Should be Applied to the unused Complementary Differential Input. Nominal Voltage is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS Inputs. |

Table 7. ATTRIBUTES

| Characteristic | Value | |
|--|----------------------|-------------|
| Internal Input Pulldown Resistor (MR, PLa, PLb) | 75 k to V_{EE} | |
| Internal Input Pullup Resistor (Pa[0:7], Pb[0:7]) | 75 k to V_{CC} | |
| ESD Protection | Human Body Model | >500 V |
| | Machine Model | >10 V |
| | Charged Device Model | >2 kV |
| Moisture Sensitivity (Note 7) | Pb Pkg | Pb-Free Pkg |
| | QFN-52 | Level 2 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | 1914 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

7. For additional information, see Application Note AND8003/D.

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Table 8. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---------------|---|--|--|--------------------|--|
| V_{CC} | Positive Power Supply | $V_{EE} = 0\text{ V}$ | | 3.6 | V |
| V_{EE} | Negative Power Supply | $V_{CC} = 0\text{ V}$ | | -3.6 | V |
| V_I | Positive Input Negative Input | $V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 3.6 -3.6 | V V |
| V_{INPP} | Differential Input Voltage $ \text{CLK} - \overline{\text{CLK}} $ | $V_{CC} - V_{EE} \geq 2.8\text{ V}$ | | 2.8 V | V |
| I_{in} | Input Current through R_T (50 Ω Resistor) | Continuous Surge | | 25 50 | mA mA |
| I_{out} | Output Current | Continuous Surge | | 25 50 | mA mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (Note 8) | 0 lfpm 500 lfpm | 52 QFN 52 QFN | 25 – 32 20 – 27 | $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | 2S2P (Note 8) | 52 QFN | 4 – 15 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder Pb Pb-Free | | | 265 265 | $^{\circ}\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

8. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

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Table 9. DC CHARACTERISTICS, POSITIVE CML OUTPUT $V_{CC} = 3.0\text{ V to }3.465\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 11)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|-------------------------------|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{CC} | Positive Power Supply Current | 170 | 200 | 230 | 170 | 200 | 230 | 170 | 200 | 230 | mA |
| V_{OH} | Output HIGH Voltage (Note 12) | $V_{CC} - 40$ | $V_{CC} - 10$ | V_{CC} | $V_{CC} - 40$ | $V_{CC} - 10$ | V_{CC} | $V_{CC} - 40$ | $V_{CC} - 10$ | V_{CC} | mV |
| V_{OL} | Output LOW Voltage (Note 12) | | $V_{CC} - 400$ | $V_{CC} - 330$ | | $V_{CC} - 400$ | $V_{CC} - 330$ | | $V_{CC} - 400$ | $V_{CC} - 330$ | mV |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 19, 21)

| | | | | | | | | | | | |
|----------|--|-----------------|--|---------------|-----------------|--|---------------|-----------------|--|---------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 9) | $V_{EE} + 1125$ | | $V_{CC} - 75$ | $V_{EE} + 1125$ | | $V_{CC} - 75$ | $V_{EE} + 1125$ | | $V_{CC} - 75$ | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | $V_{th} + 75$ | | V_{CC} | $V_{th} + 75$ | | V_{CC} | $V_{th} + 75$ | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | V_{EE} | | $V_{th} - 75$ | V_{EE} | | $V_{th} - 75$ | V_{EE} | | $V_{th} - 75$ | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 20, 22)

| | | | | | | | | | | | |
|------------|--|------------------|----------------|----------------|------------------|----------------|----------------|------------------|----------------|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | $V_{EE} + 1200$ | | V_{CC} | $V_{EE} + 1200$ | | V_{CC} | $V_{EE} + 1200$ | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | V_{EE} | | $V_{CC} - 75$ | V_{EE} | | $V_{CC} - 75$ | V_{EE} | | $V_{CC} - 75$ | mV |
| V_{CMR} | Input Common Mode Range (Differential Cross-Point Voltage) (Note 10) | $V_{EE} + 1200$ | | $V_{CC} - 50$ | $V_{EE} + 1200$ | | $V_{CC} - 50$ | $V_{EE} + 1200$ | | $V_{CC} - 50$ | mV |
| V_{ID} | Differential Input Voltage | $V_{EE} + 100$ | | V_{CC} | $V_{EE} + 100$ | | V_{CC} | $V_{EE} + 100$ | | V_{CC} | mV |
| V_{BB} | Output Voltage Reference @ -100 μA | 1840 | 1970 | 2100 | 1840 | 1960 | 2100 | 1820 | 1970 | 2100 | mV |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| I_{IH} | Input HIGH Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7] | 0 0 -50 | 7 30 -10 | 15 60 0 | 0 0 -50 | 7 30 -10 | 15 60 0 | 0 0 -50 | 7 30 -10 | 15 60 0 | μA |
| I_{IL} | Input LOW Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7] | -0.5 0 -50 | 20 -20 | 0.5 60 0 | -0.5 0 -50 | 20 -20 | 0.5 60 0 | -0.5 0 -50 | 20 -20 | 0.5 60 0 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. V_{th} is applied to the complementary input when operating in single-ended mode.

10. V_{CMR} minimum varies 1:1 with V_{EE} , V_{CMR} maximum varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

11. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.165 V.

12. All loading with 50 Ω to V_{CC} .

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 10. DC CHARACTERISTICS, NEGATIVE CML OUTPUT $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V to }-3.0\text{ V}$ (Note 16)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|-------------------------------|-----------------|------------------|------------------|-----------------|------------------|------------------|-----------------|------------------|------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{CC} | Positive Power Supply Current | 170 | 200 | 230 | 170 | 200 | 230 | 170 | 200 | 230 | mA |
| V_{OH} | Output HIGH Voltage (Note 17) | V_{CC} -40 | V_{CC} -10 | V_{CC} | V_{CC} -40 | V_{CC} -10 | V_{CC} | V_{CC} -40 | V_{CC} -10 | V_{CC} | mV |
| V_{OL} | Output LOW Voltage (Note 17) | | V_{CC} -400 | V_{CC} -330 | | V_{CC} -400 | V_{CC} -330 | | V_{CC} -400 | V_{CC} -330 | mV |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 19, 21)

| | | | | | | | | | | | |
|----------|---|-------------------|--|-----------------|-------------------|--|-----------------|-------------------|--|-----------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 14) | V_{EE} +1125 | | V_{CC} -75 | V_{EE} +1125 | | V_{CC} -75 | V_{EE} +1125 | | V_{CC} -75 | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | V_{th} +75 | | V_{CC} | V_{th} +75 | | V_{CC} | V_{th} +75 | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | V_{EE} | | V_{th} -75 | V_{EE} | | V_{th} -75 | V_{EE} | | V_{th} -75 | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 20, 22)

| | | | | | | | | | | | |
|------------|--|-------------------|----------------|-----------------|-------------------|----------------|-----------------|-------------------|----------------|-----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | V_{EE} +1200 | | V_{CC} | V_{EE} +1200 | | V_{CC} | V_{EE} +1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | V_{EE} | | V_{CC} -75 | V_{EE} | | V_{CC} -75 | V_{EE} | | V_{CC} -75 | mV |
| V_{CMR} | Input Common Mode Range (Differential Cross-Point Voltage) (Note 15) | V_{EE} +1200 | | V_{CC} -50 | V_{EE} +1200 | | V_{CC} -50 | V_{EE} +1200 | | V_{CC} -50 | mV |
| V_{ID} | Differential Input Voltage | V_{EE} +100 | | V_{CC} | V_{EE} +100 | | V_{CC} | V_{EE} +100 | | V_{CC} | mV |
| V_{BB} | Output Voltage Reference @ -100 μA | -1460 | -1330 | -1200 | -1460 | -1330 | -1200 | -1460 | -1330 | -1200 | mV |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| I_{IH} | Input HIGH Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7] | 0 0 -50 | 7 30 -10 | 15 60 0 | 0 0 -50 | 7 30 -10 | 15 60 0 | 0 0 -50 | 7 30 -10 | 15 60 0 | μA |
| I_{IL} | Input LOW Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7] | -0.5 0 -50 | 0 20 -20 | 0.5 60 0 | -0.5 0 -50 | 0 20 -20 | 0.5 60 0 | -0.5 0 -50 | 0 20 -20 | 0.5 60 0 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. V_{th} is applied to the complementary input when operating in single-ended mode.

15. V_{CMR} minimum varies 1:1 with V_{EE} , V_{CMR} maximum varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

16. Input and output parameters vary 1:1 with V_{CC} .

17. All loading with 50 Ω to V_{CC} .

18. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 11. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -3.0 V or $V_{CC} = 3.0\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$ (Note 19)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|--|---|--|--|------------|--|--|--|--|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OUTPP} | Output Voltage Amplitude @ ÷ 2 Mode $f_{in} = 3.5\text{ GHz}$ (See Figure 5) | 300 | 400 | | 300 | 400 | | 300 | 400 | | mV |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential CLK to TC MR to TC | 435 100 | | 555 500 | 455 100 | | 575 500 | 475 100 | | 595 500 | ps |
| t_{JITTER} | RMS Random Clock Jitter $f_{in} = 3.5\text{ GHz}$ (See Figure 5) | | | 2.5 | | | 3.0 | | | 3.0 | ps |
| V_{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 20) | 100 | | 2500 | 100 | | 2500 | 100 | | 2500 | mV |
| t_r , t_f | Output Rise/Fall Times (20% – 80%) | 25 | 45 | 65 | 25 | 45 | 65 | 25 | 45 | 65 | ps |
| t_s | Setup Time (Figure 23) | Pa[7:0] to PLa Pb[7:0] to PLb CE to CLK SEL to CLK PLa to CLK PLb to CLK Pa[7:0] to CLK Pb[7:0] to CLK | 3750 4500 400 300 2500 3250 4750 3000 | 2500 2000 30 120 2000 2750 3500 2500 | | 3750 4500 400 300 2500 3250 4750 3000 | 2500 2000 30 120 2000 2750 3500 2500 | 3750 4500 400 300 2500 3250 4750 3000 | 2500 2000 30 120 2000 2750 3500 2500 | | ps |
| t_H | Hold Time (Figure 23) | PLa to Pa[7:0] PLb to Pb[7:0] CLK to CE CLK to SEL CLK to PLa CLK to PLb CLK to PLb[7:0] CLK to PLb[7:0] | -1500 -1250 450 0 -1750 -2250 -2250 -2000 | -2700 -1900 40 -110 -1900 -2700 -3200 -2500 | | -1500 -1250 450 0 -1750 -2250 -2250 -2000 | -2700 -1900 40 -110 -1900 -2700 -3200 -2500 | -1500 -1250 450 0 -1750 -2250 -2250 -2000 | -2700 -1900 40 -110 -1900 -2700 -3200 -2500 | | ps |
| t_{SKEW} | Device-to-Device (Note 21) | | 40 | 75 | | 40 | 75 | | 40 | 75 | ps |
| t_{PW} | Minimum Pulse Width | MR | 250 | 85 | | 250 | 85 | | 250 | 85 | ps |
| t_{RR} | Reset Recovery | MR to CLK/ $\overline{\text{CLK}}$ | 3000 | 2500 | | 3000 | 2500 | | 3000 | 2500 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

19. Measured using a 400 mV source, 50% duty cycle clock source at $f_{in} = 1\text{ GHz}$ unless stated otherwise. All loading with $50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).

20. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$.

21. Device-to-Device skew for identical transitions at identical V_{CC} levels.

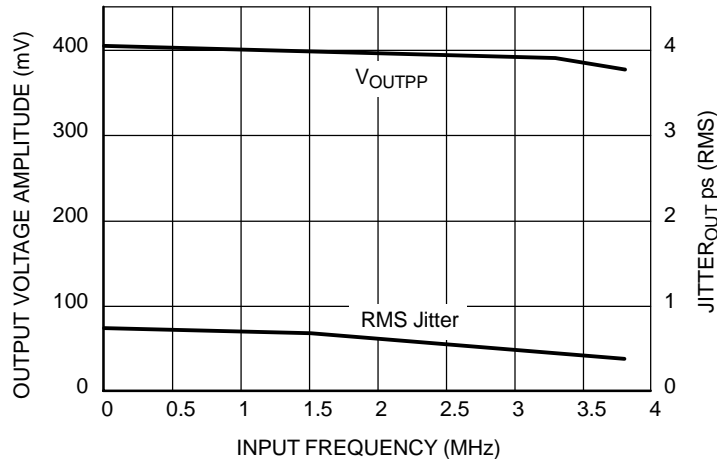


Figure 5. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) @ Ambient Temperature (Typical)

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Application Information

All NB7N017M inputs can accept PECL, CML, LVTTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are

minimum input swing of 100 mV and the maximum input swing of 450 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment ($Z = 50 \Omega$).

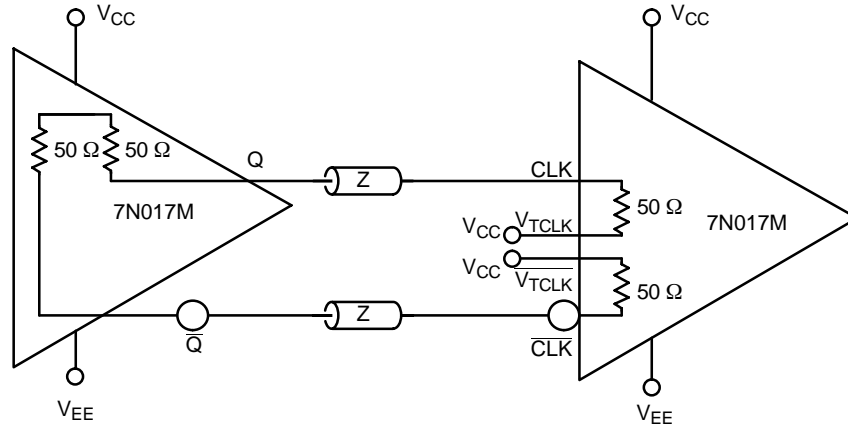


Figure 6. CML to CML Interface

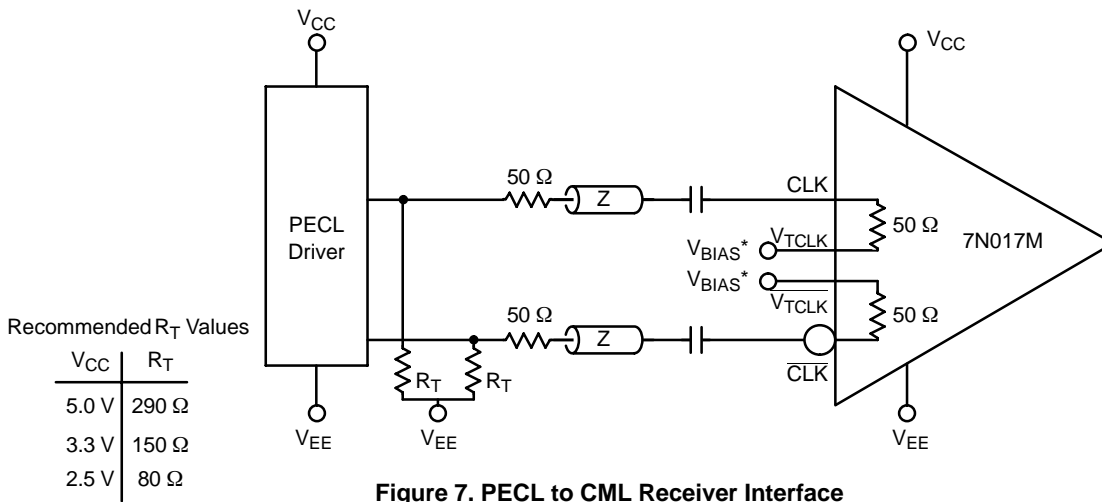


Figure 7. PECL to CML Receiver Interface

* V_{BIAS} is within V_{CMR} Range.

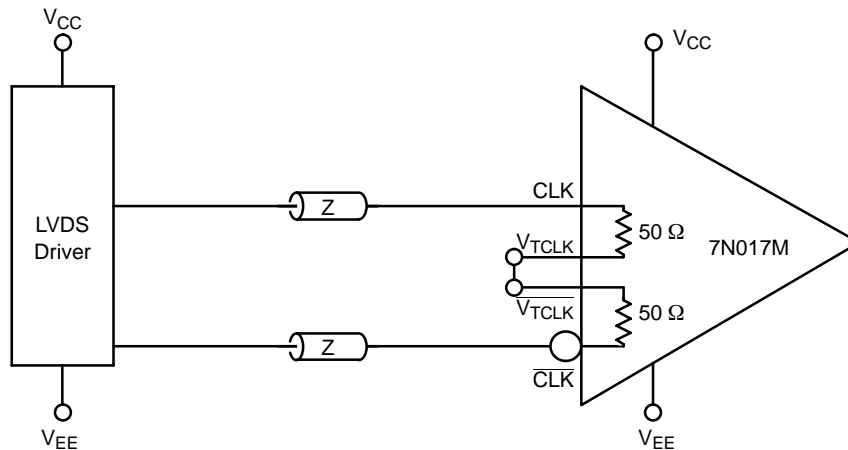


Figure 8. LVDS to CML Receiver Interface

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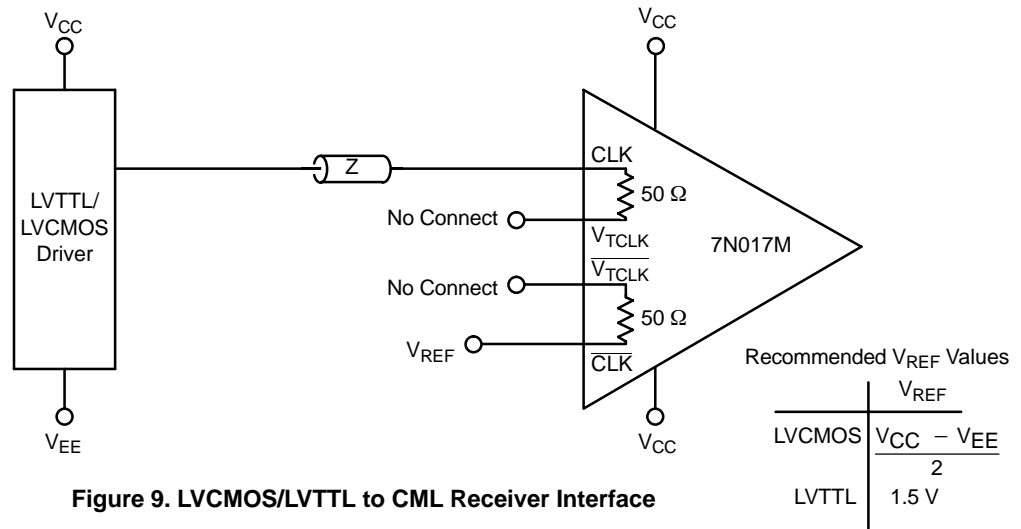


Table 12. OPERATION TABLE

| MR | Pa | PLa | Pb | PLb | SEL | CE | CLK | CLK_INT | TC_INT | TC |
|----|----------|-----|----------|-----|-----|----|-----|---------|--------|----|
| 1 | XXXXXXXX | x | XXXXXXXX | X | X | X | X | X | X | X |
| 0 | 00000101 | H | 00000100 | H | X | H | L | H | H | H |
| 0 | 00000101 | H | 00000100 | H | X | H | L | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |

X - Don't Care
H - HIGH
L - LOW

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Table 12. OPERATION TABLE

| MR | Pa | PLa | Pb | PLb | SEL | CE | CLK | CLK_INT | TC_INT | TC |
|----|----------|-----|----------|-----|-----|----|-----|---------|--------|----|
| 0 | XXXXXXXX | L | XXXXXXXX | L | H | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | L | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | L | L | L | X | X |
| 0 | 0000010 | H | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | 00000001 | H | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | H | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | L | H | H | H | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | L | L | X | X |
| 0 | XXXXXXXX | L | XXXXXXXX | L | X | H | H | H | X | X |

X – Don't Care
H – HIGH
L – LOW

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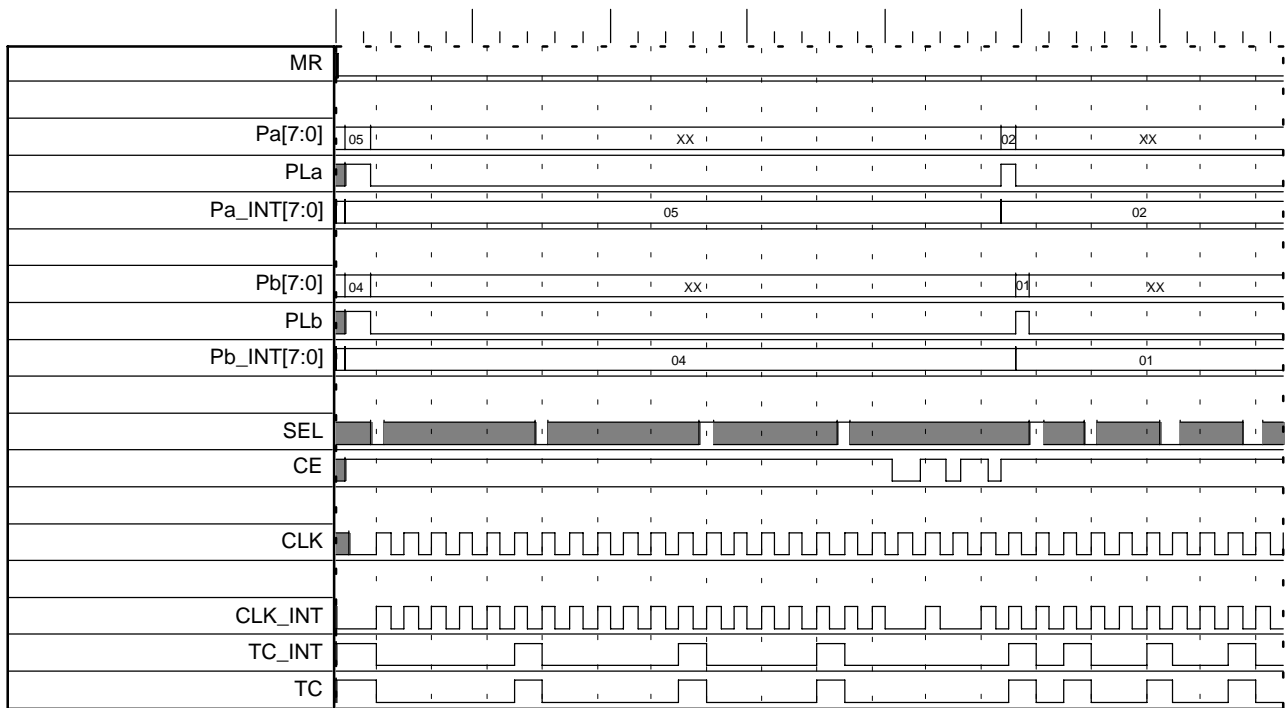


Figure 10. Device Timing Diagram for Table 12

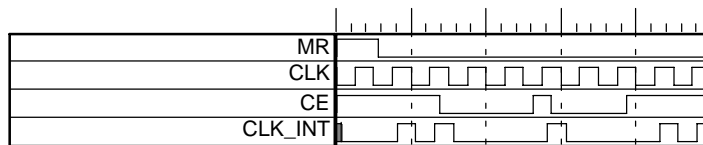
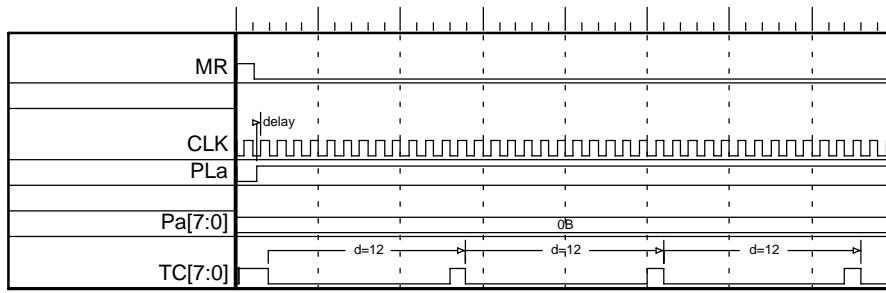
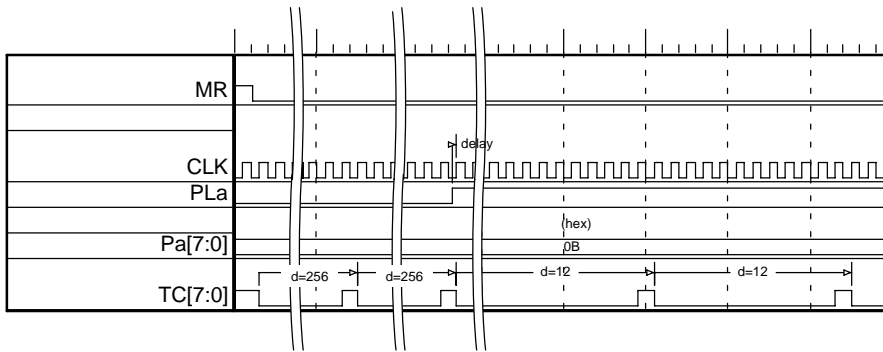


Figure 11. Timing Diagram for CE Input

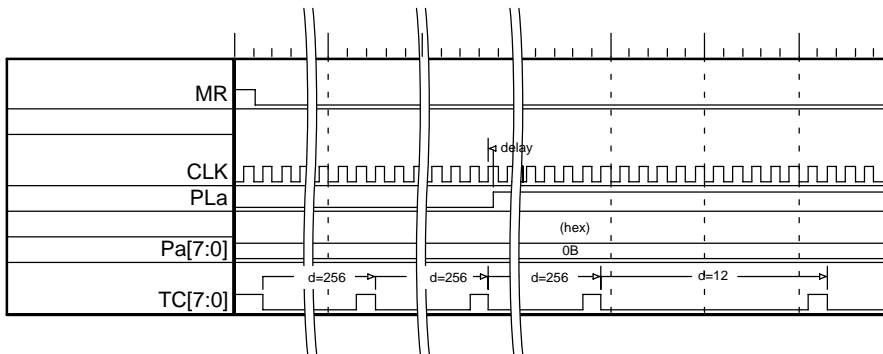
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**Figure 12. Timing Diagram for PLa / PLb Inputs
(SEL is Low)**

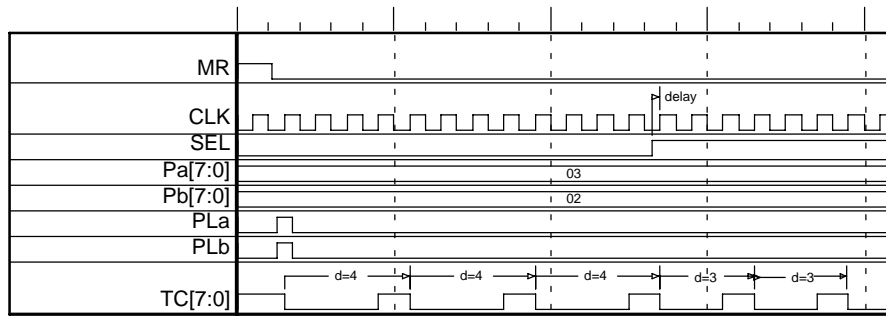


**Figure 13. Timing Diagram for PLa / PLb Inputs
(Before Critical Rising Edge of CLK)
(SEL is Low)**

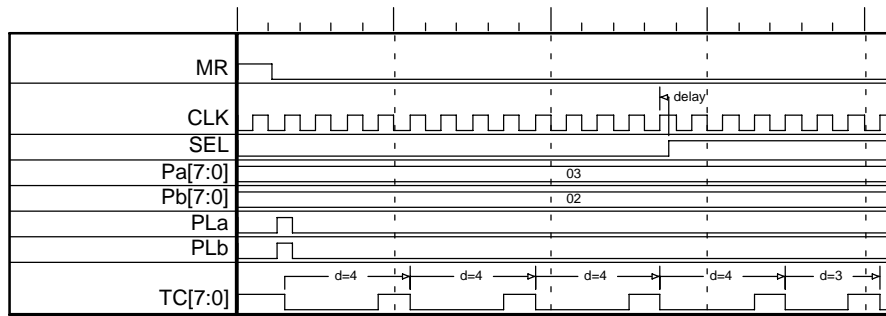


**Figure 14. Timing Diagram for PLa / PLb Inputs
(After Critical Rising Edge of CLK)
(SEL is Low)**

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**Figure 15. Timing Diagram for SEL Input
(Before Critical Rising Edge of CLK)**



**Figure 16. Timing Diagram for SEL Input
(After Critical Rising Edge of CLK)**

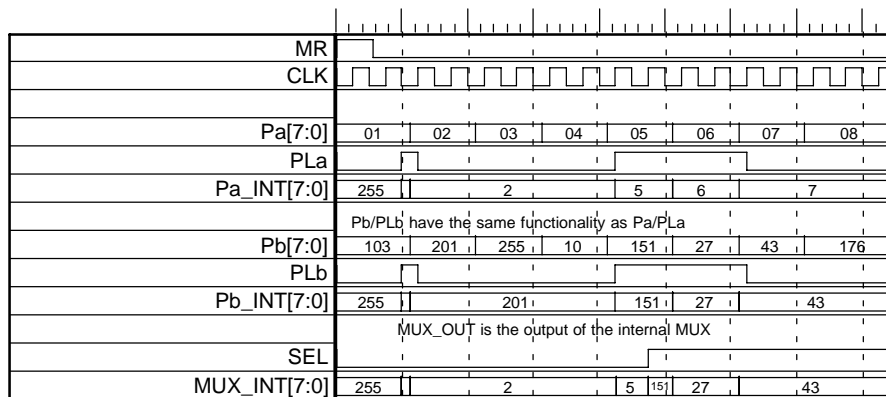


Figure 17. Timing Diagram Relating PLa, PLb, Pa(0:7), Pb(0:7)

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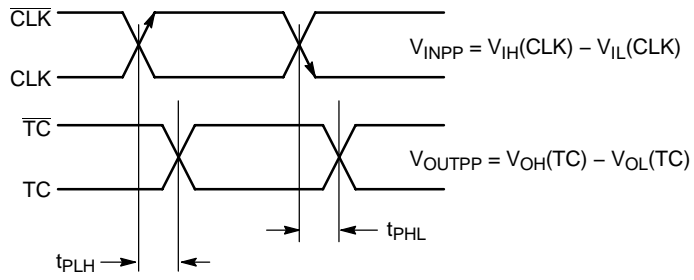


Figure 18. AC Reference Measurement

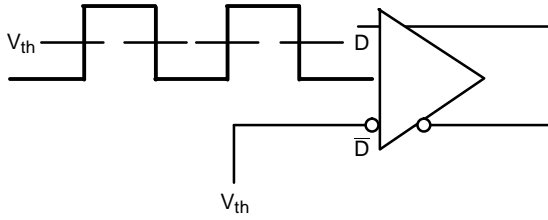


Figure 19. Differential Input Driven Single-Ended

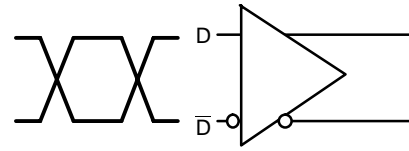


Figure 20. Differential Inputs Driven Differentially

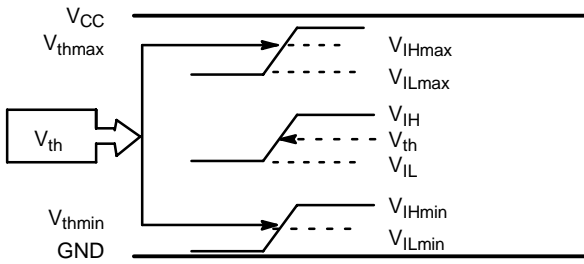


Figure 21. V_{th} Diagram

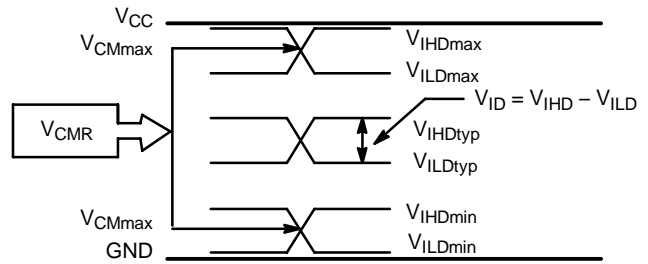


Figure 22. V_{CMR} Diagram

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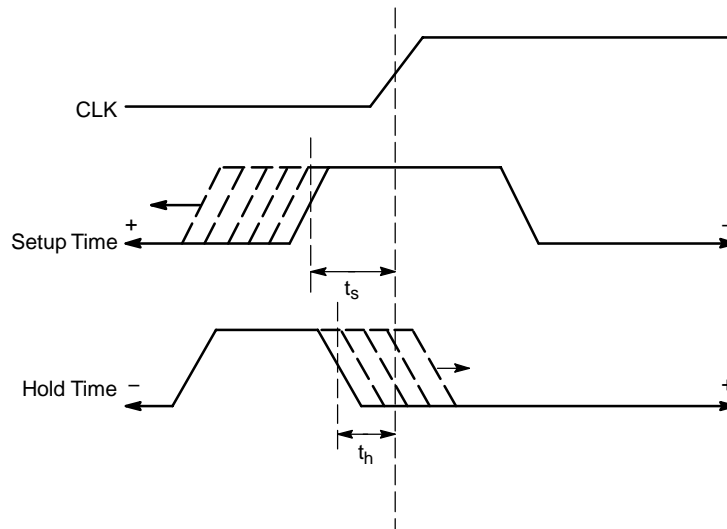


Figure 23. Setup and Hold Time

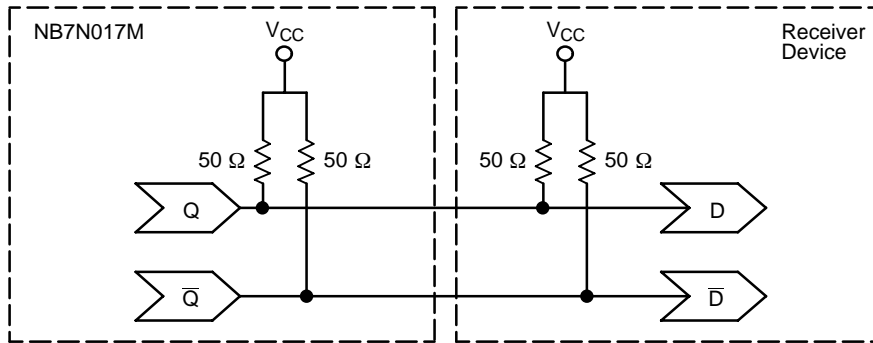


Figure 24. Typical Termination for 16 mA Output Drive and Device Evaluation

ORDERING INFORMATION

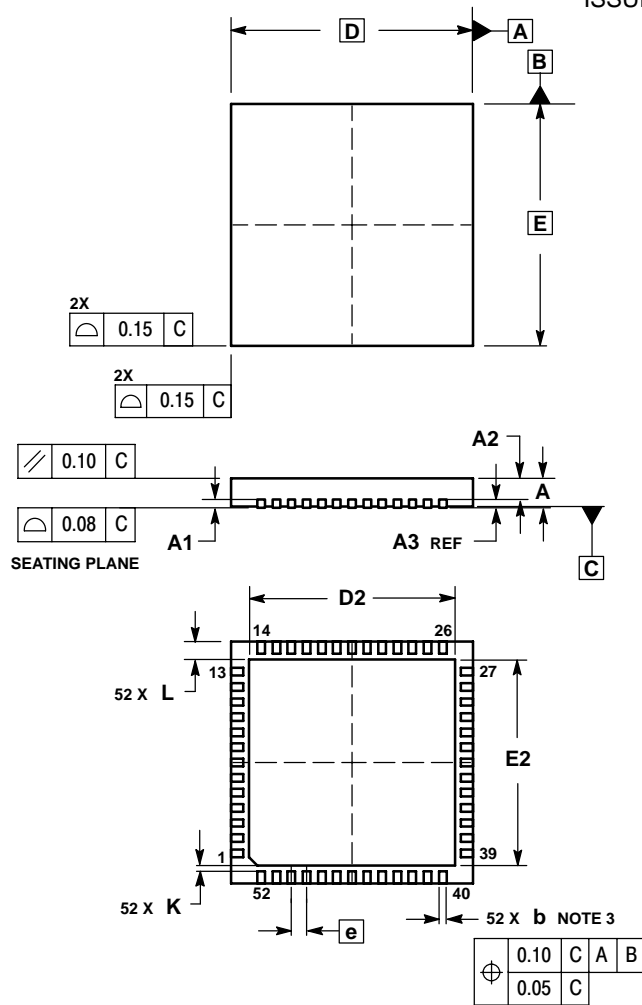
| Device | Package | Shipping† |
|---------------|---------------------|--------------------|
| NB7N017MMN | QFN-52 | 260 Units / Tray |
| NB7N017MMNG | QFN-52 (Pb-Free) | 260 Units / Tray |
| NB7N017MMNR2 | QFN-52 | 2000 / Tape & Reel |
| NB7N017MMNR2G | QFN-52 (Pb-Free) | 2000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7N017M

PACKAGE DIMENSIONS

52 PIN QFN 8x8
CASE 485M-01
ISSUE A



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.60 | 0.80 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 8.00 BSC | |
| D2 | 6.50 | 6.80 |
| E | 8.00 BSC | |
| E2 | 6.50 | 6.80 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

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