

**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

**Description**

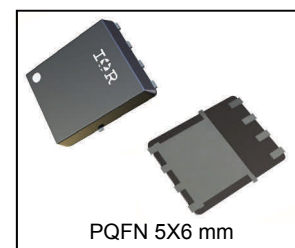
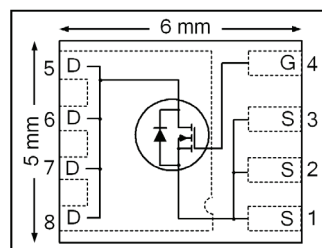
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this product an extremely efficient and reliable device for use in Automotive and wide variety of other applications.

**Applications**

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Converter

HEXFET® POWER MOSFET

<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>2.5mΩ</b>
<b>max</b>	<b>3.3mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>123A<sup>Ⓔ</sup></b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>95A</b>



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFN8403	PQFN 5mm x 6mm	Tape and Reel	4000	AUIRFN8403TR

**Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C(Bottom)</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	123 <sup>Ⓔ</sup>	A
I <sub>D</sub> @ T <sub>C(Bottom)</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	87 <sup>Ⓔ</sup>	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	95 <sup>Ⓔ</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	492	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation	4.3	W
P <sub>D</sub> @ T <sub>C(Bottom)</sub> = 25°C	Power Dissipation	94	
	Linear Derating Factor	0.029	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) <sup>②</sup>	100	mJ
E <sub>AS (Tested)</sub>	Single Pulse Avalanche Energy <sup>②</sup>	159	
I <sub>AR</sub>	Avalanche Current <sup>①</sup>	See Fig. 14, 15, 22a, 22b	A
E <sub>AR</sub>	Repetitive Avalanche Energy <sup>①</sup>		
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C

HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	1.6	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	31	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	23	


**Static Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

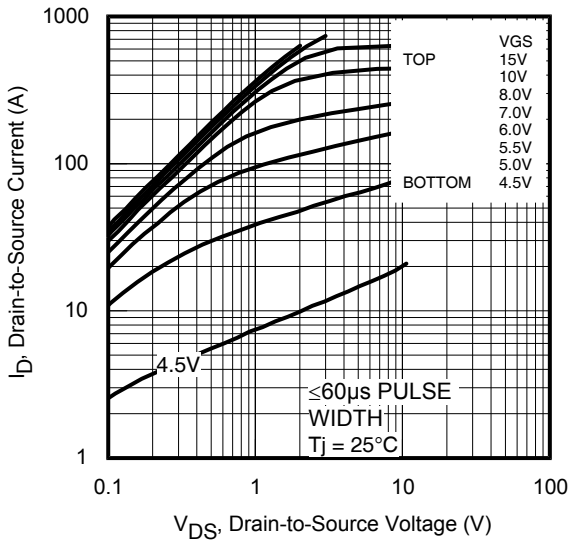
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	26	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 2.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.3	mΩ	$V_{GS} = 10V, I_D = 50A$
$V_{GS(th)}$	Gate Threshold Voltage	2.6	—	3.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	Ω	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Internal Gate Resistance	—	1.5	—		

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

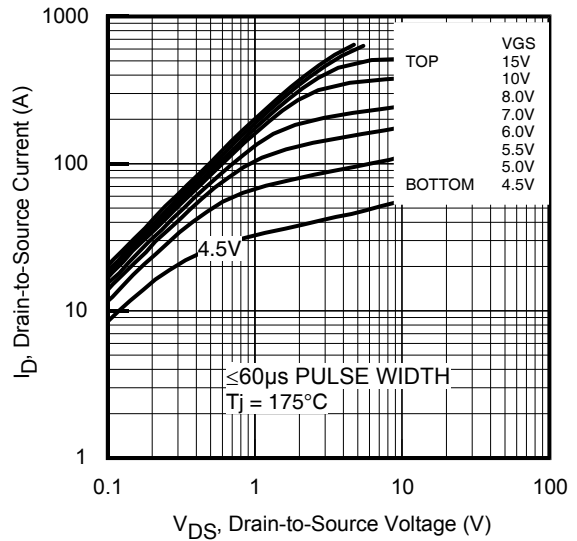
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	159	—	—	S	$V_{DS} = 10V, I_D = 50A$
$Q_g$	Total Gate Charge	—	65	98	nC	$I_D = 50A$ $V_{DS} = 20V$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source Charge	—	16	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	23	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	42	—		
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 20V$ $I_D = 30A$ $R_G = 2.7\Omega$ $V_{GS} = 10V$ ③
$t_r$	Rise Time	—	37	—		
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		
$t_f$	Fall Time	—	26	—		
$C_{iss}$	Input Capacitance	—	3174	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	479	—		
$C_{riss}$	Reverse Transfer Capacitance	—	332	—		
$C_{oss\ eff. (ER)}$	Effective Output Capacitance (Energy Related)	—	637	—		
$C_{oss\ eff. (TR)}$	Effective Output Capacitance (Time Related)	—	656	—		

**Diode Characteristics**

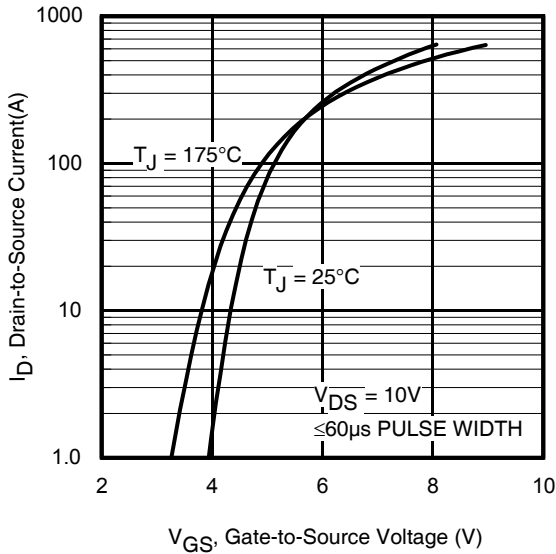
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	123⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	492	A	
$V_{SD}$	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
$dv/dt$	Peak Diode Recovery	—	2.4	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 50A, V_{DS} = 40V$
$t_{rr}$	Reverse Recovery Time	—	16	—	ns	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $V_R = 34V,$ $I_F = 50A$
		—	18	—		
$Q_{rr}$	Reverse Recovery Charge	—	5.0	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $di/dt = 100A/\mu s$ ③
		—	6.9	—		
$I_{RRM}$	Reverse Recovery Current	—	0.50	—	A	$T_J = 25^\circ\text{C}$



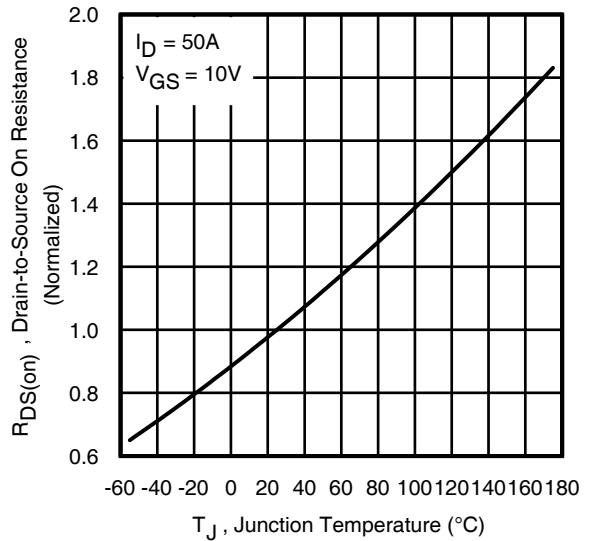
**Fig. 1** Typical Output Characteristics



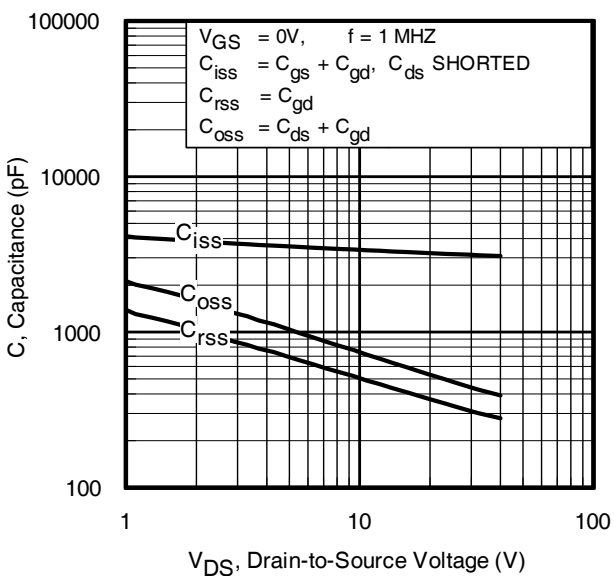
**Fig. 2** Typical Output Characteristics



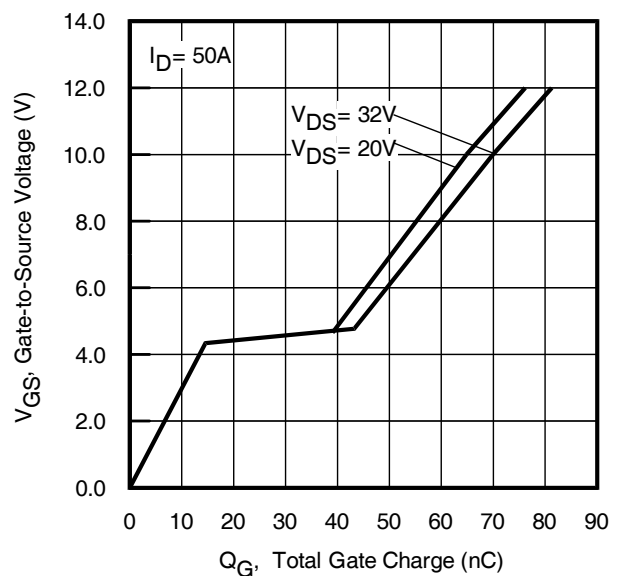
**Fig. 3** Typical Transfer Characteristics



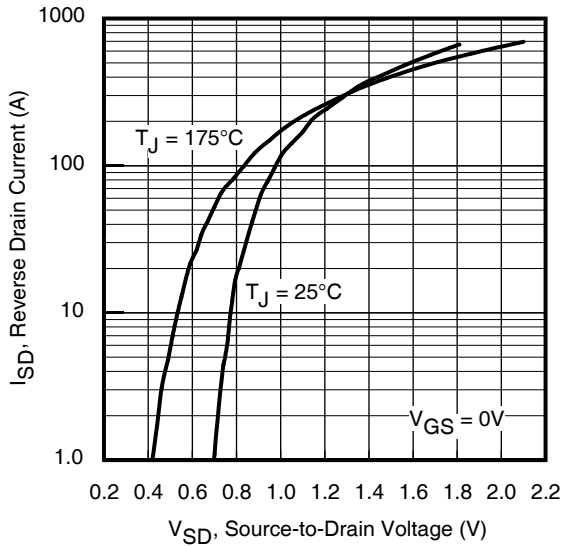
**Fig. 4** Normalized On-Resistance vs. Temperature



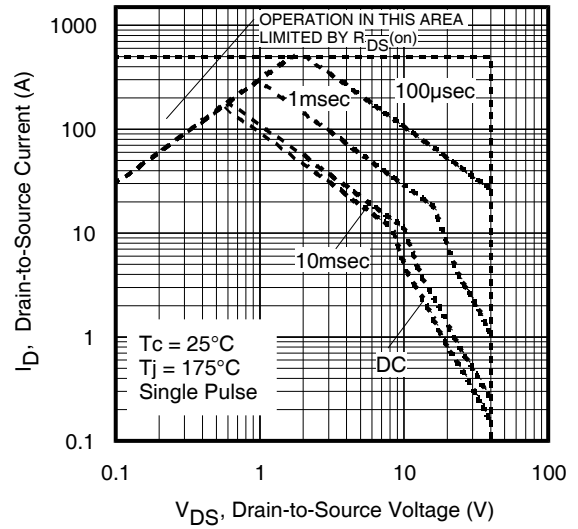
**Fig. 5.** Typical Capacitance vs. Drain-to-Source Voltage



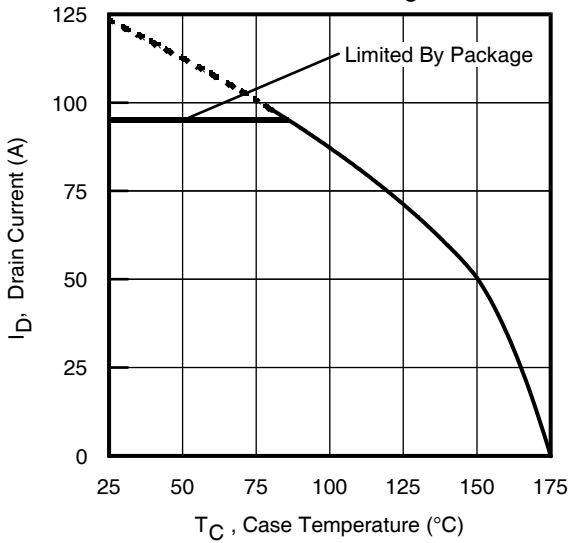
**Fig. 6.** Typical Gate Charge vs. Gate-to-Source Voltage



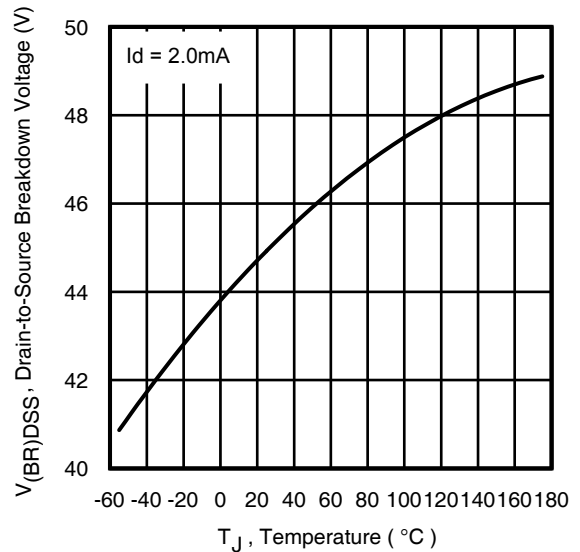
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



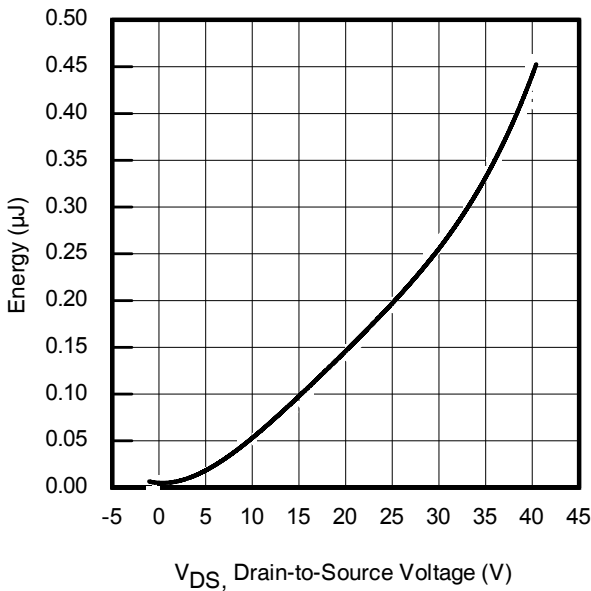
**Fig. 8.** Maximum Safe Operating Area



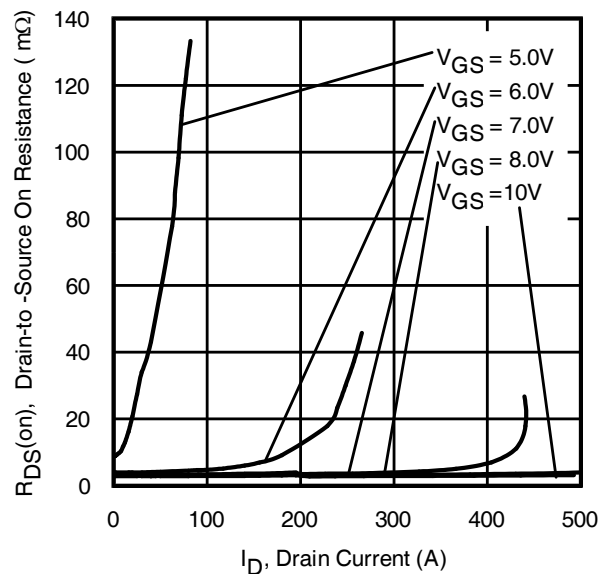
**Fig. 9.** Maximum Drain Current vs. Case Temperature



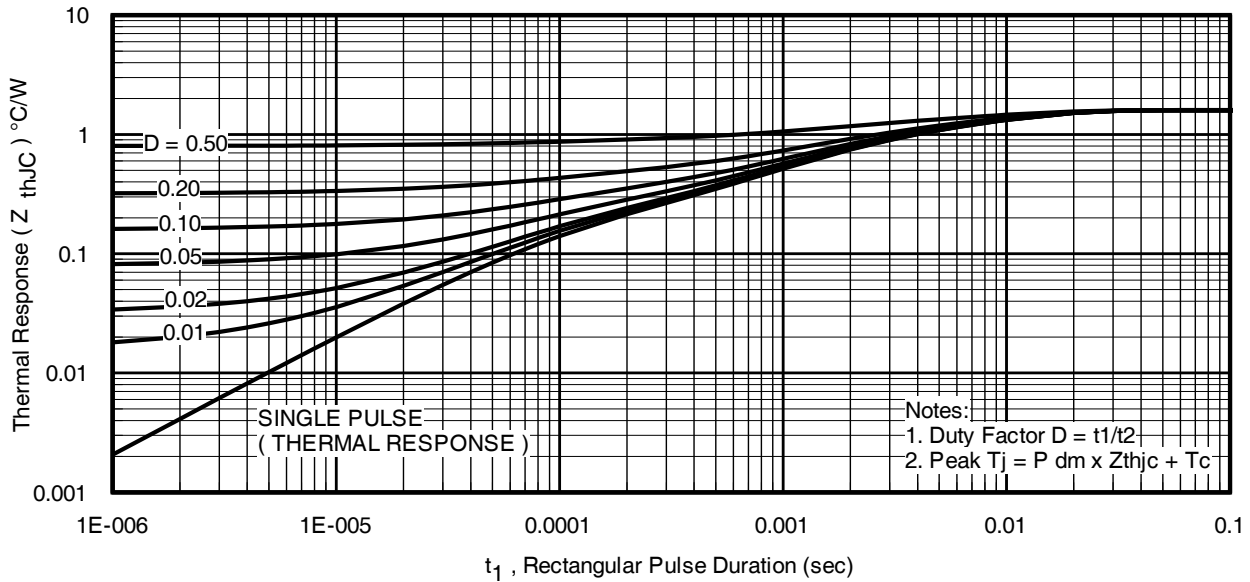
**Fig. 10.** Drain-to-Source Breakdown Voltage



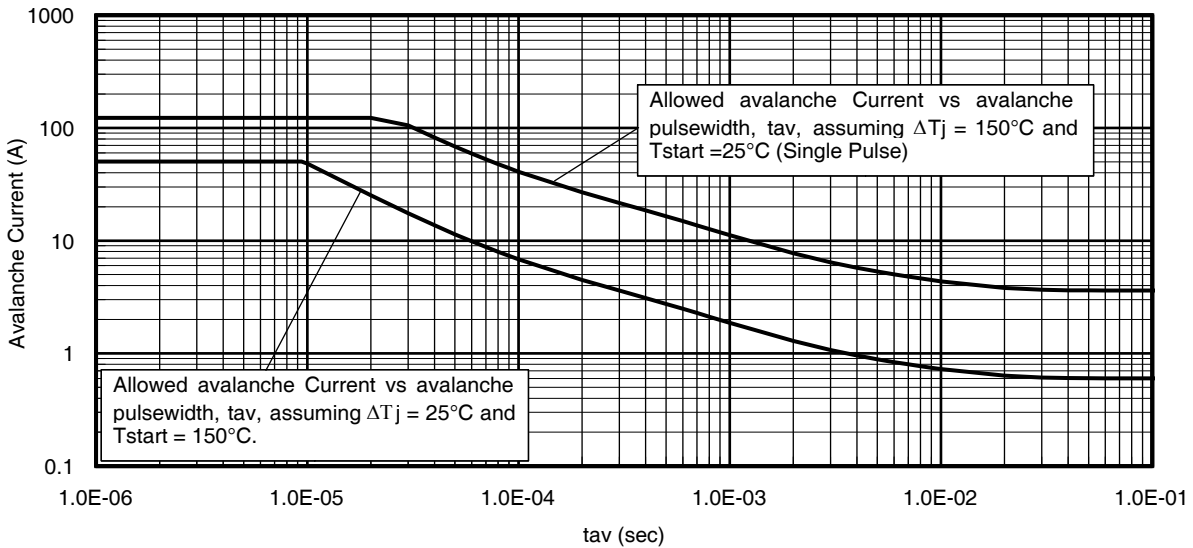
**Fig. 11.** Typical  $C_{oss}$  Stored Energy



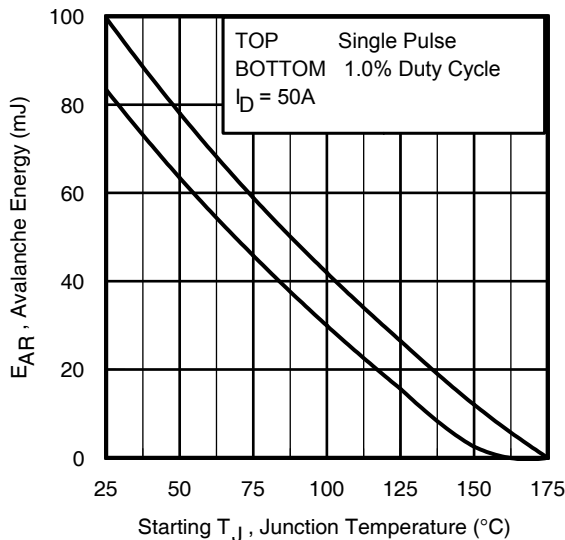
**Fig. 12.** Typical On-Resistance vs. Drain Current



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 14.** Typical Avalanche Current vs. Pulse Width



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

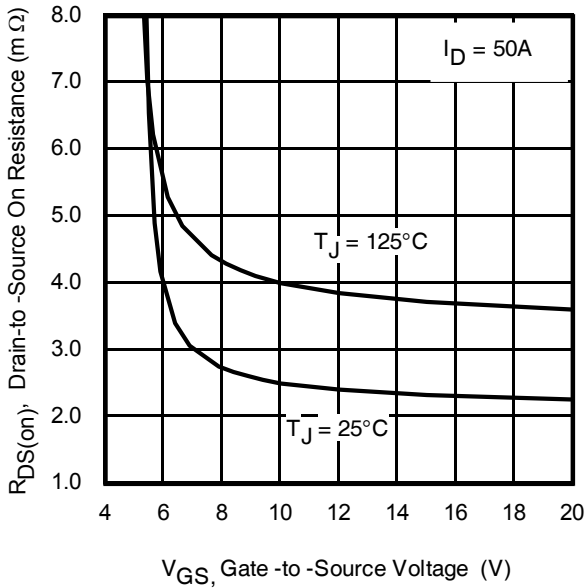


Fig 16. Typical On-Resistance vs. Gate Voltage

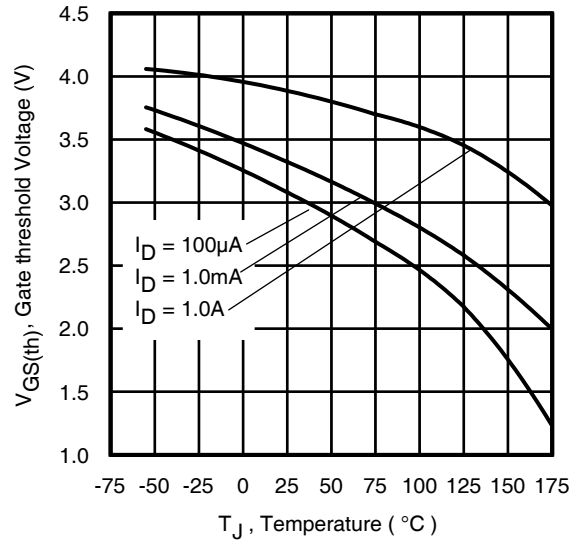


Fig 17. Threshold Voltage vs. Temperature

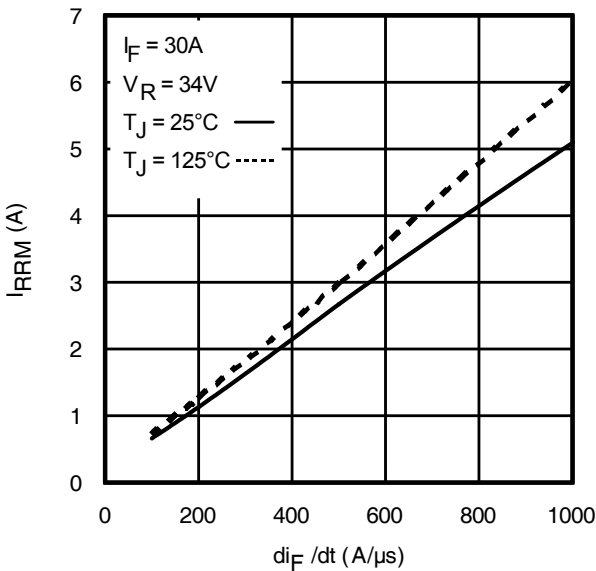


Fig 18 - Typical Recovery Current vs.  $di_F/dt$

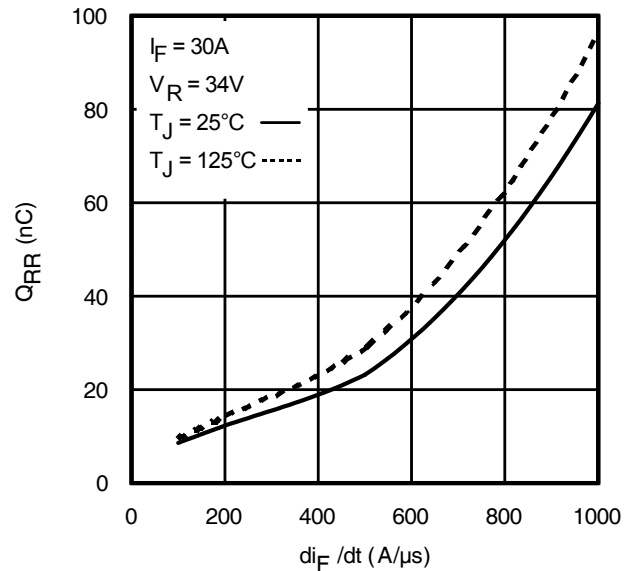


Fig. 19 - Typical Stored Charge vs.  $di_F/dt$

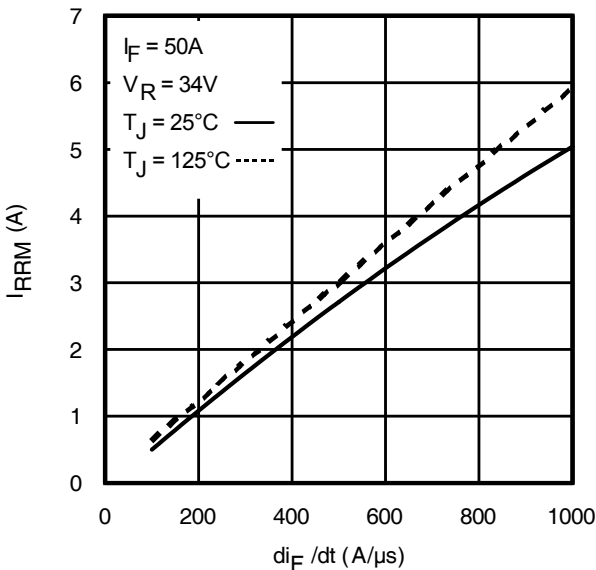


Fig. 20 - Typical Recovery Current vs.  $di_F/dt$

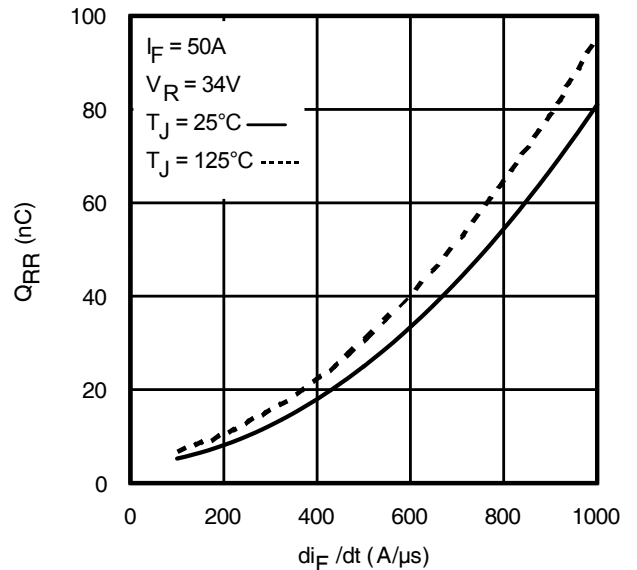


Fig. 21 - Typical Stored Charge vs.  $di_F/dt$

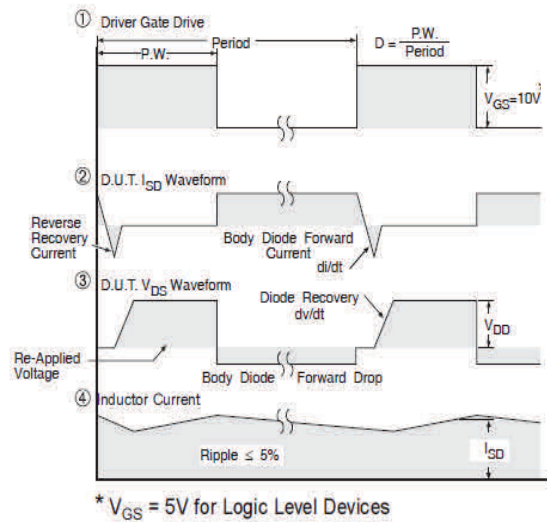
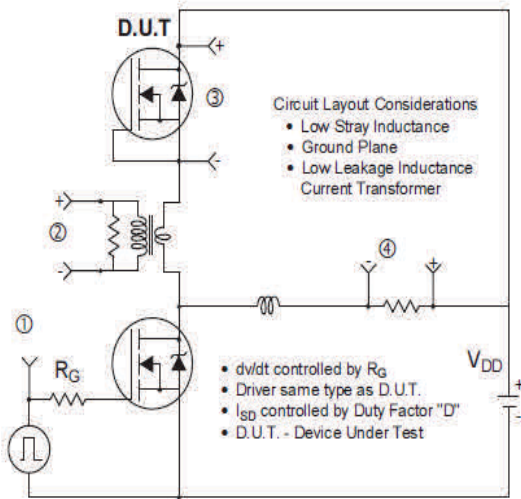


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

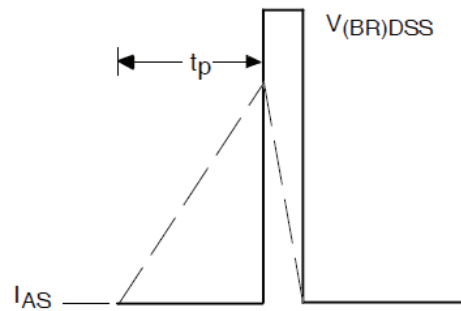
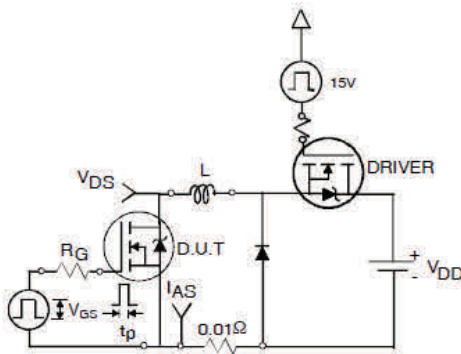


Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

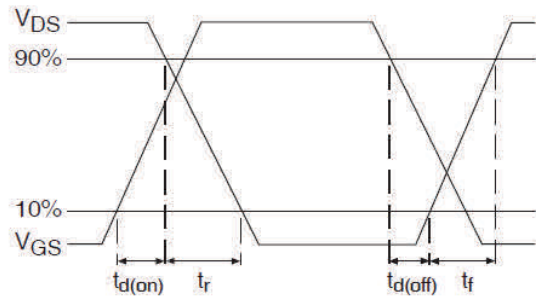
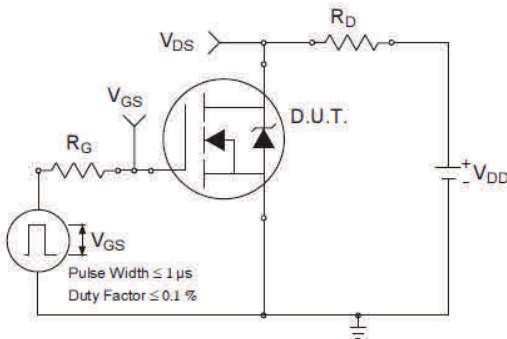


Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

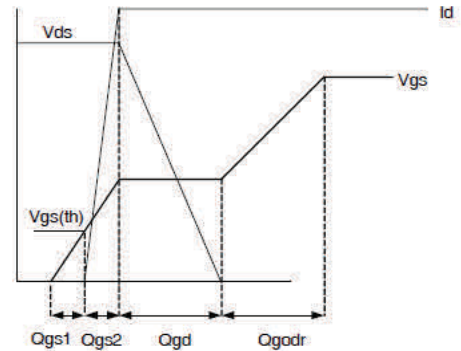
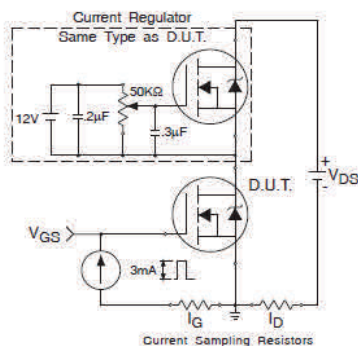
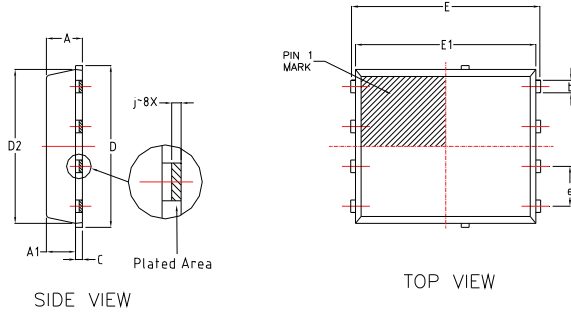


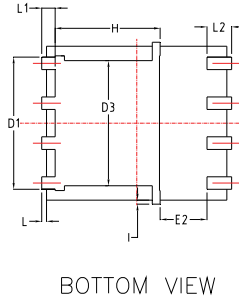
Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

**PQFN 5x6 Outline "E" Package Details**

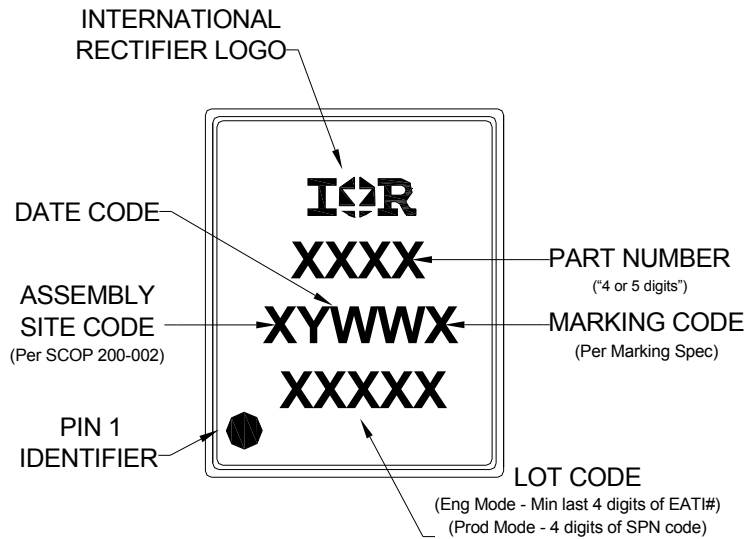


D I M	MM		
	MIN	NOM	MAX
A	0.90	1.10	1.17
A1	0.824	0.897	0.97
b	0.33	0.41	0.50
c	0.150	0.20	0.250
D	4.80	4.98	5.15
D1	3.91	4.22	4.36
D2	4.80	4.90	5.00
D3	3.85	4.00	4.15
E	5.90	6.05	6.15
E1	5.65	5.76	5.85
E2	1.10	/	/
e	1.27 BSC		
L	0.05	0.15	0.25
L1	0.38	0.425	0.50
L2	0.51	0.785	0.86
H	3.25	3.35	3.58
I	0	/	0.18
j	0.1015 BSC		



For footprint and stencil design recommendations, please refer to application note AN-1136 at <http://www.irf.com/technical-info/appnotes/an-1136.pdf>  
 For visual inspection recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

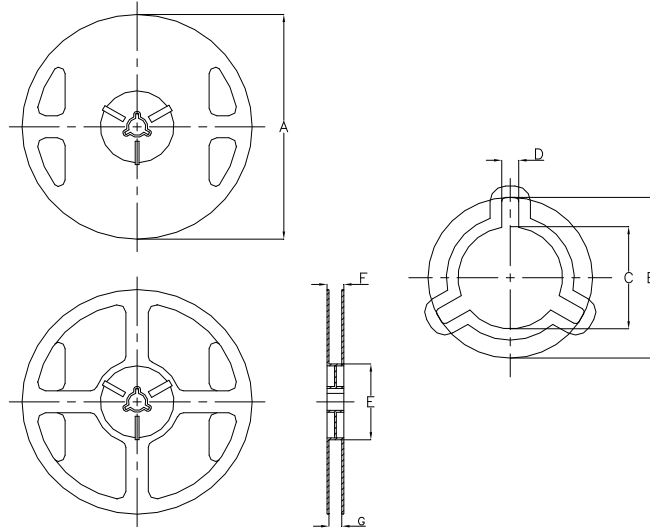
**PQFN 5x6 Outline "E" Part Marking**



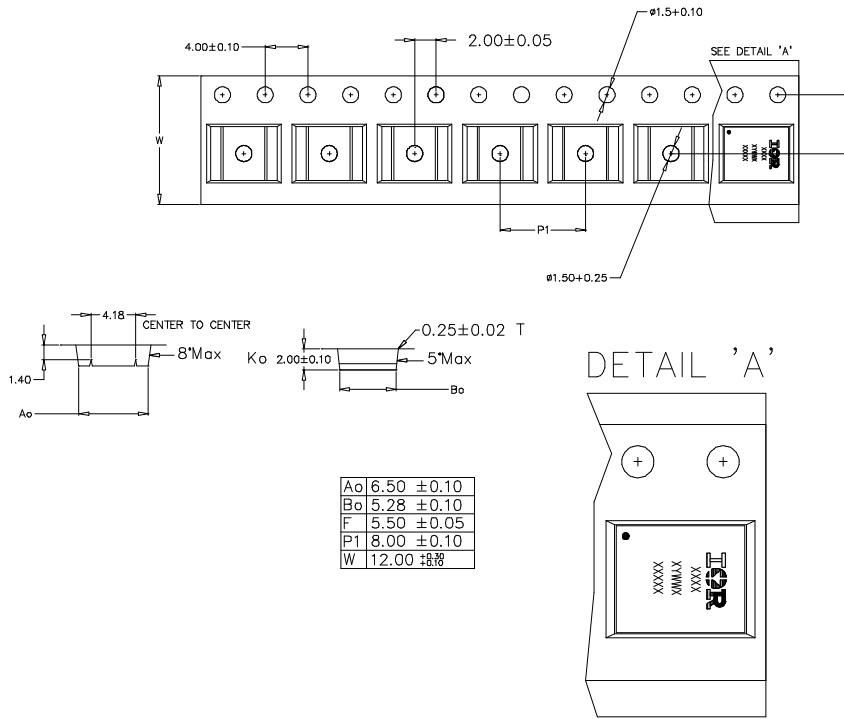
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**PQFN 5x6 Outline "E" Tape and Reel**



REEL DIMENSIONS				
STANDARD OPTION (QTY 4000) TR				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	329.5	330.5	12.972	13.011
B	20.9	21.5	0.823	0.846
C	12.8	13.5	0.504	0.532
D	1.7	2.3	0.067	0.091
E	97	99	3.819	3.898
F	Ref	17.4		
G	13	14.5	0.512	0.571



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

### Qualification Information<sup>†</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		PQFN 5mm x 6mm	MSL1
<b>ESD</b>	Machine Model	Class M3 (+/- 400V) <sup>††</sup>	
		AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) <sup>††</sup>	
		AEC-Q101-001	
Charged Device Model	Class C5 (+/- 2000V) <sup>††</sup>		
	AEC-Q101-005		
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Highest passing voltage.

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^{\circ}\text{C}$ ,  $L = 0.080\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^{\circ}\text{C}$ .
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 80% VDSS.
- ⑧ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 to 80% VDSS.

### Revision History

Date	Comments
05/08/2014	• Updated typo on "Description" on page 1.
07/08/2014	• Updated typo on Gate Charge units from "S" to "nC" on page 2. • Removed extra GFS from Electrical Table on page 2.
07/08/2015	• Corrected $V_{GS(th)}$ min from 2.2V to 2.6V on page 2. • Updated "IFX logo" on all pages.
09/01/2015	• Corrected dv/dt from "1.3V/ns" to "2.4V/ns" on page 2.

**IMPORTANT NOTICE**

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IR warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with IR's standard warranty. Testing and other quality control techniques are used to the extent IR deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

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**WORLD HEADQUARTERS:**

101 N. Sepulveda Blvd., El Segundo, California 90245

Tel: (310) 252-7105

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9