

## 18-Bit Analog-to-Digital Converter with I<sup>2</sup>C Interface and On-Board Reference

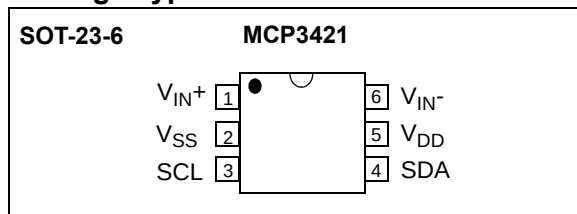
### Features

- 18-bit  $\Delta\Sigma$  ADC in a SOT-23-6 package
- Differential Input Operation
- Self Calibration of Internal Offset and Gain Per Each Conversion
- On-Board Voltage Reference:
  - Accuracy:  $2.048V \pm 0.05\%$
  - Drift: 15 ppm/°C
- On-Board Programmable Gain Amplifier (PGA):
  - Gains of 1, 2, 4 or 8
- On-Board Oscillator
- INL: 10 ppm of FSR (FSR = 4.096V/PGA)
- Programmable Data Rate Options:
  - 3.75 SPS (18 bits)
  - 15 SPS (16 bits)
  - 60 SPS (14 bits)
  - 240 SPS (12 bits)
- One-Shot or Continuous Conversion Options
- Low Current Consumption:
  - 145  $\mu A$  typical ( $V_{DD} = 3V$ , Continuous Conversion)
  - 39  $\mu A$  typical ( $V_{DD} = 3V$ , One-Shot Conversion with 1 SPS)
- Supports I<sup>2</sup>C Serial Interface:
  - Standard, Fast and High Speed Modes
- Single Supply Operation: 2.7V to 5.5V
- Extended Temperature Range: -40°C to +125°C

### Typical Applications

- Portable Instrumentation
- Weigh Scales and Fuel Gauges
- Temperature Sensing with RTD, Thermistor, and Thermocouple
- Bridge Sensing for Pressure, Strain, and Force.

### Package Types



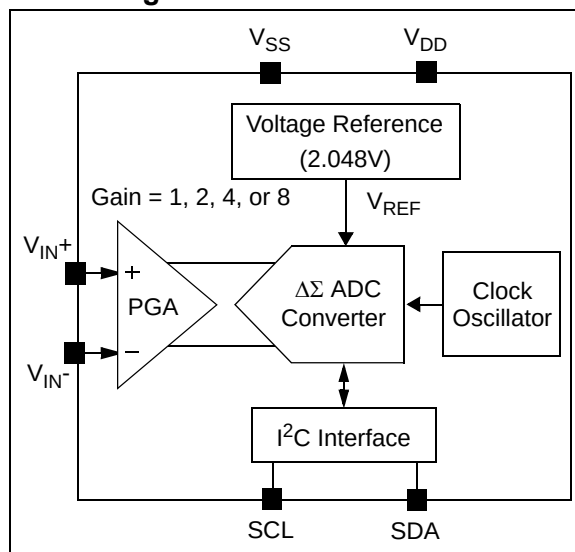
### Description

The MCP3421 is a single channel low-noise, high accuracy  $\Delta\Sigma$  A/D converter with differential inputs and up to 18 bits of resolution in a small SOT-23-6 package. The on-board precision 2.048V reference voltage enables an input range of  $\pm 2.048V$  differentially ( $\Delta$  voltage = 4.096V). The device uses a two-wire I<sup>2</sup>C compatible serial interface and operates from a single 2.7V to 5.5V power supply.

The MCP3421 device performs conversion at rates of 3.75, 15, 60, or 240 samples per second (SPS) depending on the user controllable configuration bit settings using the two-wire I<sup>2</sup>C serial interface. This device has an on-board programmable gain amplifier (PGA). The user can select the PGA gain of x1, x2, x4, or x8 before the analog-to-digital conversion takes place. This allows the MCP3421 device to convert a smaller input signal with high resolution. The device has two conversion modes: (a) Continuous mode and (b) One-Shot mode. In One-Shot mode, the device enters a low current standby mode automatically after one conversion. This reduces current consumption greatly during idle periods.

The MCP3421 device can be used for various high accuracy analog-to-digital data conversion applications where design simplicity, low power, and small footprint are major considerations.

### Block Diagram



# MCP3421

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NOTES:

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings†

|                                              |                                 |
|----------------------------------------------|---------------------------------|
| $V_{DD}$ .....                               | 7.0V                            |
| All inputs and outputs w.r.t $V_{SS}$ .....  | -0.3V to $V_{DD}+0.3V$          |
| Differential Input Voltage .....             | $ V_{DD} - V_{SS} $             |
| Output Short Circuit Current .....           | Continuous                      |
| Current at Input Pins .....                  | $\pm 2$ mA                      |
| Current at Output and Supply Pins .....      | $\pm 10$ mA                     |
| Storage Temperature .....                    | -65°C to +150°C                 |
| Ambient Temp. with power applied .....       | -55°C to +125°C                 |
| ESD protection on all pins .....             | $\geq 6$ kV HBM, $\geq 400V$ MM |
| Maximum Junction Temperature ( $T_J$ ) ..... | +150°C                          |

†**Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 1.2 Electrical Specifications

## ELECTRICAL CHARACTERISTICS

| <b>Electrical Specifications:</b> Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{DD} = +5.0V$ , $V_{SS} = 0V$ , $V_{IN+} = V_{IN-} = V_{REF}/2$ . All ppm units use $2 \times V_{REF}$ as full scale range. |               |              |                 |              |               |                                                                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------------|-----------------|--------------|---------------|---------------------------------------------------------------------|
| Parameters                                                                                                                                                                                                                                                               | Sym           | Min          | Typ             | Max          | Units         | Conditions                                                          |
| <b>Analog Inputs</b>                                                                                                                                                                                                                                                     |               |              |                 |              |               |                                                                     |
| Differential Input Range                                                                                                                                                                                                                                                 |               | —            | $\pm 2.048/PGA$ | —            | V             | $V_{IN} = V_{IN+} - V_{IN-}$                                        |
| Common-Mode Voltage Range (absolute) <b>(Note 1)</b>                                                                                                                                                                                                                     |               | $V_{SS}-0.3$ | —               | $V_{DD}+0.3$ | V             |                                                                     |
| Differential Input Impedance <b>(Note 2)</b>                                                                                                                                                                                                                             | $Z_{IND}$ (f) | —            | $2.25/PGA$      | —            | M $\Omega$    | During normal mode operation                                        |
| Common Mode input Impedance                                                                                                                                                                                                                                              | $Z_{INC}$ (f) | —            | 25              | —            | M $\Omega$    | $PGA = 1, 2, 4, 8$                                                  |
| <b>System Performance</b>                                                                                                                                                                                                                                                |               |              |                 |              |               |                                                                     |
| Resolution and No Missing Codes <b>(Note 8)</b>                                                                                                                                                                                                                          |               | 12           | —               | —            | Bits          | DR = 240 SPS                                                        |
|                                                                                                                                                                                                                                                                          |               | 14           | —               | —            | Bits          | DR = 60 SPS                                                         |
|                                                                                                                                                                                                                                                                          |               | 16           | —               | —            | Bits          | DR = 15 SPS                                                         |
|                                                                                                                                                                                                                                                                          |               | 18           | —               | —            | Bits          | DR = 3.75 SPS                                                       |
| Data Rate <b>(Note 3)</b>                                                                                                                                                                                                                                                | DR            | 176          | 240             | 328          | SPS           | S1,S0 = '00', (12 bits mode)                                        |
|                                                                                                                                                                                                                                                                          |               | 44           | 60              | 82           | SPS           | S1,S0 = '01', (14 bits mode)                                        |
|                                                                                                                                                                                                                                                                          |               | 11           | 15              | 20.5         | SPS           | S1,S0 = '10', (16 bits mode)                                        |
|                                                                                                                                                                                                                                                                          |               | 2.75         | 3.75            | 5.1          | SPS           | S1,S0 = '11', (18 bits mode)                                        |
| Output Noise                                                                                                                                                                                                                                                             |               | —            | 1.5             | —            | $\mu V_{RMS}$ | $T_A = +25^\circ\text{C}$ , DR = 3.75 SPS, $PGA = 1$ , $V_{IN} = 0$ |
| Integral Nonlinearity (Note 4)                                                                                                                                                                                                                                           | INL           | —            | 10              | 35           | ppm of FSR    | DR = 3.75 SPS <b>(Note 6)</b>                                       |
| Internal Reference Voltage                                                                                                                                                                                                                                               | $V_{REF}$     | —            | 2.048           | —            | V             |                                                                     |

- Note 1:** Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
- 2:** This input impedance is due to 3.2 pF internal input sampling capacitor.
- 3:** The total conversion speed includes auto-calibration of offset and gain.
- 4:** INL is the difference between the endpoints line and the measured code at the center of the quantization band.
- 5:** Includes all errors from on-board PGA and  $V_{REF}$ .
- 6:** Full Scale Range (FSR) =  $2 \times 2.048/PGA = 4.096/PGA$ .
- 7:** This parameter is ensured by characterization and not 100% tested.
- 8:** This parameter is ensured by design and not 100% tested.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| <b>Electrical Specifications:</b> Unless otherwise specified, all parameters apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{DD} = +5.0\text{V}$ , $V_{SS} = 0\text{V}$ , $V_{IN+} = V_{IN-} = V_{REF}/2$ . All ppm units use $2 \cdot V_{REF}$ as full scale range. |            |               |      |              |                         |                                                                                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------------|------|--------------|-------------------------|------------------------------------------------------------------------------------|
| Parameters                                                                                                                                                                                                                                                                                | Sym        | Min           | Typ  | Max          | Units                   | Conditions                                                                         |
| Gain Error (Note 5)                                                                                                                                                                                                                                                                       |            | —             | 0.05 | 0.35         | %                       | PGA = 1, DR = 3.75 SPS                                                             |
| PGA Gain Error Match (Note 5)                                                                                                                                                                                                                                                             |            | —             | 0.1  | —            | %                       | Between any 2 PGA gains                                                            |
| Gain Error Drift (Note 5)                                                                                                                                                                                                                                                                 |            | —             | 15   | —            | ppm/ $^{\circ}\text{C}$ | PGA=1, DR=3.75 SPS                                                                 |
| Offset Error                                                                                                                                                                                                                                                                              | $V_{OS}$   | —             | 15   | 40           | $\mu\text{V}$           | Tested at PGA = 1<br>$V_{DD} = 5.0\text{V}$ and DR = 3.75 SPS                      |
| Offset Drift vs. Temperature                                                                                                                                                                                                                                                              |            | —             | 50   | —            | nV/ $^{\circ}\text{C}$  | $V_{DD} = 5.0\text{V}$                                                             |
| Common-Mode Rejection                                                                                                                                                                                                                                                                     |            | —             | 105  | —            | dB                      | at DC and PGA =1,                                                                  |
|                                                                                                                                                                                                                                                                                           |            | —             | 110  | —            | dB                      | at DC and PGA =8,<br>$T_A = +25^{\circ}\text{C}$                                   |
| Gain vs. $V_{DD}$                                                                                                                                                                                                                                                                         |            | —             | 5    | —            | ppm/V                   | $T_A = +25^{\circ}\text{C}$ , $V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ ,<br>PGA = 1 |
| Power Supply Rejection at DC                                                                                                                                                                                                                                                              |            | —             | 100  | —            | dB                      | $T_A = +25^{\circ}\text{C}$ , $V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ ,<br>PGA = 1 |
| <b>Power Requirements</b>                                                                                                                                                                                                                                                                 |            |               |      |              |                         |                                                                                    |
| Voltage Range                                                                                                                                                                                                                                                                             | $V_{DD}$   | 2.7           | —    | 5.5          | V                       |                                                                                    |
| Supply Current during Conversion                                                                                                                                                                                                                                                          | $I_{DDA}$  | —             | 155  | 190          | $\mu\text{A}$           | $V_{DD} = 5.0\text{V}$                                                             |
|                                                                                                                                                                                                                                                                                           |            | —             | 145  | —            | $\mu\text{A}$           | $V_{DD} = 3.0\text{V}$                                                             |
| Supply Current during Standby Mode                                                                                                                                                                                                                                                        | $I_{DDs}$  | —             | 0.1  | 0.5          | $\mu\text{A}$           |                                                                                    |
| <b>I<sup>2</sup>C Digital Inputs and Digital Outputs</b>                                                                                                                                                                                                                                  |            |               |      |              |                         |                                                                                    |
| High level input voltage                                                                                                                                                                                                                                                                  | $V_{IH}$   | $0.7 V_{DD}$  | —    | $V_{DD}$     | V                       |                                                                                    |
| Low level input voltage                                                                                                                                                                                                                                                                   | $V_{IL}$   | —             | —    | $0.3 V_{DD}$ | V                       |                                                                                    |
| Low level output voltage                                                                                                                                                                                                                                                                  | $V_{OL}$   | —             | —    | 0.4          | V                       | $I_{OL} = 3 \text{ mA}$ , $V_{DD} = +5.0\text{V}$                                  |
| Hysteresis of Schmitt Trigger for inputs (Note 7)                                                                                                                                                                                                                                         | $V_{HYST}$ | $0.05 V_{DD}$ | —    | —            | V                       | $f_{SCL} = 100 \text{ kHz}$                                                        |
| Supply Current when I <sup>2</sup> C bus line is active                                                                                                                                                                                                                                   | $I_{DDB}$  | —             | —    | 10           | $\mu\text{A}$           |                                                                                    |
| Input Leakage Current                                                                                                                                                                                                                                                                     | $I_{ILH}$  | —             | —    | 1            | $\mu\text{A}$           | $V_{IH} = 5.5\text{V}$                                                             |
|                                                                                                                                                                                                                                                                                           | $I_{ILL}$  | -1            | —    | —            | $\mu\text{A}$           | $V_{IL} = \text{GND}$                                                              |
| <b>Pin Capacitance and I<sup>2</sup>C Bus Capacitance</b>                                                                                                                                                                                                                                 |            |               |      |              |                         |                                                                                    |
| Pin capacitance                                                                                                                                                                                                                                                                           | $C_{PIN}$  | —             | —    | 10           | pF                      |                                                                                    |
| I <sup>2</sup> C Bus Capacitance                                                                                                                                                                                                                                                          | $C_b$      | —             | —    | 400          | pF                      |                                                                                    |

- Note 1:** Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
- 2:** This input impedance is due to 3.2 pF internal input sampling capacitor.
- 3:** The total conversion speed includes auto-calibration of offset and gain.
- 4:** INL is the difference between the endpoints line and the measured code at the center of the quantization band.
- 5:** Includes all errors from on-board PGA and  $V_{REF}$ .
- 6:** Full Scale Range (FSR) =  $2 \times 2.048/\text{PGA} = 4.096/\text{PGA}$ .
- 7:** This parameter is ensured by characterization and not 100% tested.
- 8:** This parameter is ensured by design and not 100% tested.

**TEMPERATURE SPECIFICATIONS**

| <b>Electrical Characteristics:</b> Unless otherwise indicated, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{DD} = +5.0\text{V}$ , $V_{SS} = 0\text{V}$ . |               |     |       |      |                      |            |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----|-------|------|----------------------|------------|
| Parameters                                                                                                                                                             | Sym           | Min | Typ   | Max  | Units                | Conditions |
| <b>Temperature Ranges</b>                                                                                                                                              |               |     |       |      |                      |            |
| Specified Temperature Range                                                                                                                                            | $T_A$         | -40 | —     | +85  | $^{\circ}\text{C}$   |            |
| Operating Temperature Range                                                                                                                                            | $T_A$         | -40 | —     | +125 | $^{\circ}\text{C}$   |            |
| Storage Temperature Range                                                                                                                                              | $T_A$         | -65 | —     | +150 | $^{\circ}\text{C}$   |            |
| <b>Thermal Package Resistances</b>                                                                                                                                     |               |     |       |      |                      |            |
| Thermal Resistance, 6L SOT-23                                                                                                                                          | $\theta_{JA}$ | —   | 190.5 | —    | $^{\circ}\text{C/W}$ |            |

# MCP3421

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NOTES:

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{IN+} = V_{IN-} = V_{REF}/2$ .

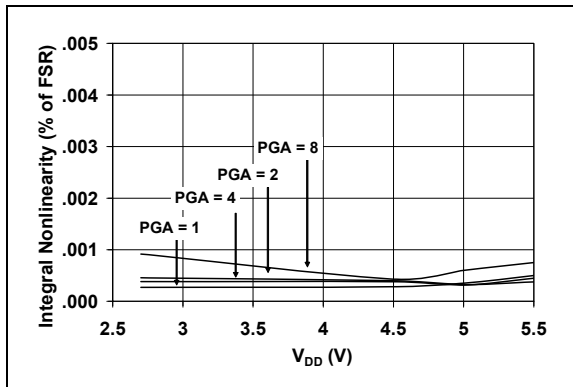


**FIGURE 2-1:** INL vs. Supply Voltage ( $V_{DD}$ ).

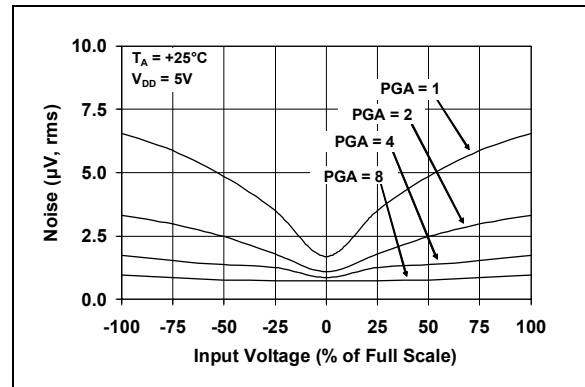


**FIGURE 2-4:** Output Noise vs. Input Voltage.

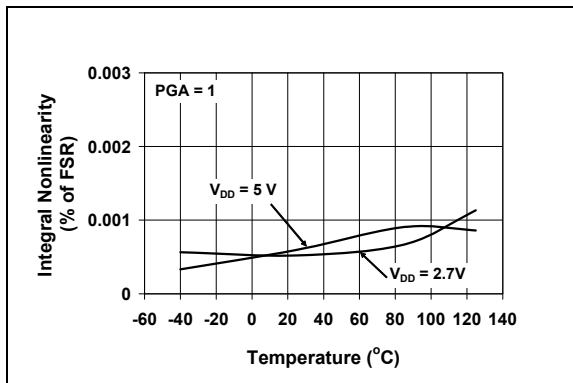


**FIGURE 2-2:** INL vs. Temperature.

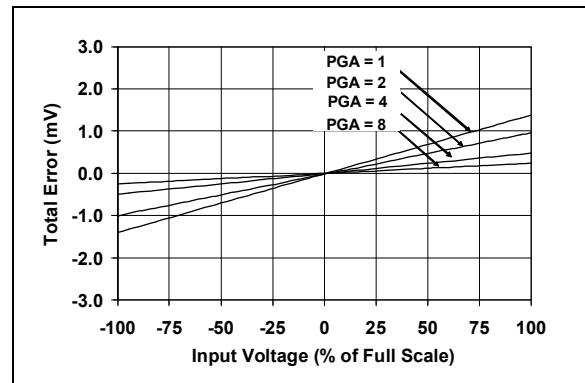


**FIGURE 2-5:** Total Error vs. Input Voltage.

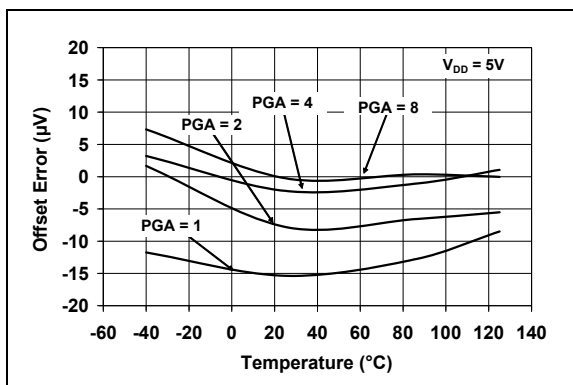


**FIGURE 2-3:** Offset Error vs. Temperature.

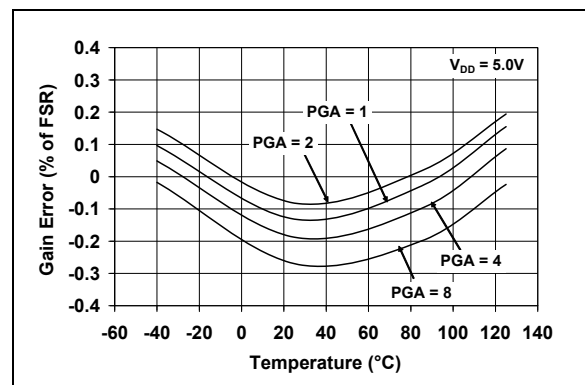


**FIGURE 2-6:** Gain Error vs. Temperature.

# MCP3421

**Note:** Unless otherwise indicated,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{IN+} = V_{IN-} = V_{REF}/2$ .

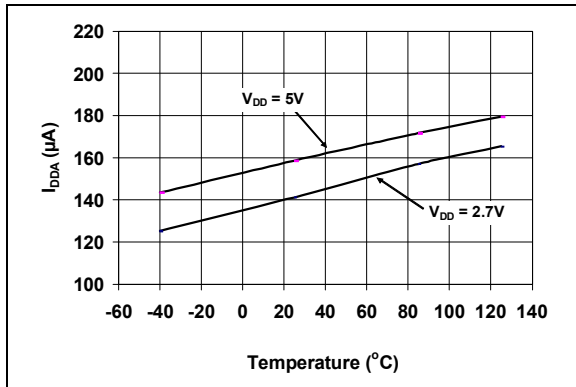


**FIGURE 2-7:**  $I_{DDA}$  vs. Temperature.

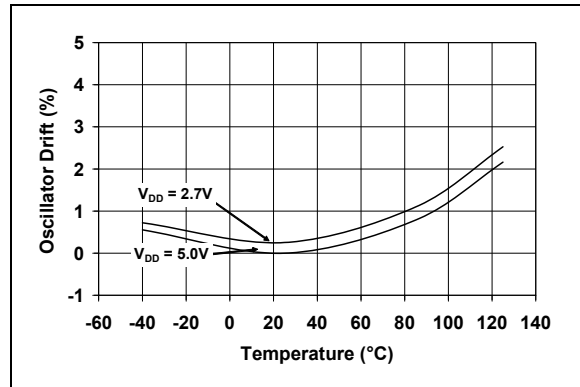


**FIGURE 2-10:** OSC Drift vs. Temperature.

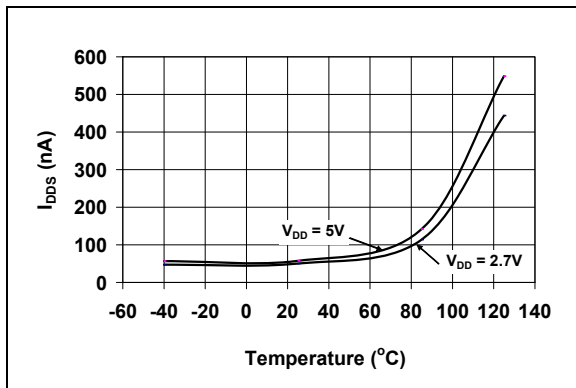


**FIGURE 2-8:**  $I_{DDS}$  vs. Temperature.

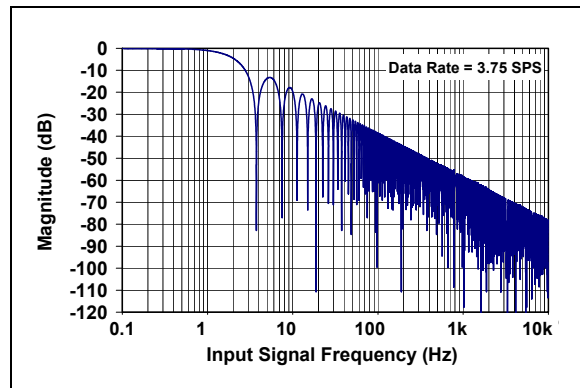


**FIGURE 2-11:** Frequency Response.

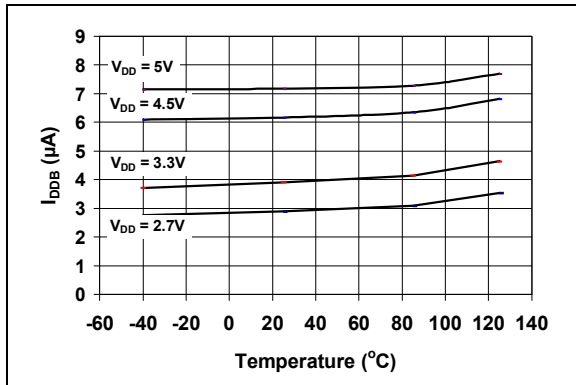


**FIGURE 2-9:**  $I_{DDB}$  vs. Temperature.

### 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP3421 | Symbol    | Description                                                     |
|---------|-----------|-----------------------------------------------------------------|
| 1       | $V_{IN+}$ | Positive Differential Analog Input Pin                          |
| 2       | $V_{SS}$  | Ground Pin                                                      |
| 3       | SCL       | Serial Clock Input Pin of the I <sup>2</sup> C Interface        |
| 4       | SDA       | Bidirectional Serial Data Pin of the I <sup>2</sup> C Interface |
| 5       | $V_{DD}$  | Positive Supply Voltage Pin                                     |
| 6       | $V_{IN-}$ | Negative Differential Analog Input Pin                          |

#### 3.1 Analog Inputs ( $V_{IN+}$ , $V_{IN-}$ )

$V_{IN+}$  and  $V_{IN-}$  are differential signal input pins. The MCP3421 device accepts a fully differential analog input signal which is connected on the  $V_{IN+}$  and  $V_{IN-}$  input pins. The differential voltage that is converted is defined by  $V_{IN} = (V_{IN+} - V_{IN-})$  where  $V_{IN+}$  is the voltage applied at the  $V_{IN+}$  pin and  $V_{IN-}$  is the voltage applied at the  $V_{IN-}$  pin. The user can also connect  $V_{IN-}$  pin to  $V_{SS}$  for a single-ended operation. See [Figure 6-4](#) for differential and single-ended connection examples.

The input signal level is amplified by the programmable gain amplifier (PGA) before the conversion. The differential input voltage should not exceed an absolute of  $(V_{REF}/PGA)$  for accurate measurement, where  $V_{REF}$  is the internal reference voltage (2.048V) and PGA is the PGA gain setting. The converter output code will saturate if the input range exceeds  $(V_{REF}/PGA)$ .

The absolute voltage range on each of the differential input pins is from  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$ . Any voltage above or below this range will cause leakage currents through the Electrostatic Discharge (ESD) diodes at the input pins. This ESD current can cause unexpected performance of the device. The common mode of the analog inputs should be chosen such that both the differential analog input range and the absolute voltage range on each pin are within the specified operating range defined in **Section 1.0 “Electrical Characteristics”** and **Section 4.0 “Description of Device Operation”**.

See **Section 4.5 “Input Voltage Range”** for more details of the input voltage range.

[Figure 3-1](#) shows the input structure of the device. The device uses a switched capacitor input stage at the front end.  $C_{PIN}$  is the package pin capacitance and typically about 4 pF.  $D_1$  and  $D_2$  are the ESD diodes.  $C_{SAMPLE}$  is the differential input sampling capacitor.

#### 3.2 Supply Voltage ( $V_{DD}$ , $V_{SS}$ )

$V_{DD}$  is the power supply pin for the device. This pin requires an appropriate bypass capacitor of about 0.1  $\mu F$  (ceramic) to ground. An additional 10  $\mu F$  capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in some application boards. The supply voltage ( $V_{DD}$ ) must be maintained in the 2.7V to 5.5V range for specified operation.

$V_{SS}$  is the ground pin and the current return path of the device. The user must connect the  $V_{SS}$  pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the  $V_{SS}$  pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

#### 3.3 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I<sup>2</sup>C interface. The MCP3421 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP3421 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the  $V_{DD}$  line to the SCL pin. Refer to **Section 5.3 “I<sup>2</sup>C Serial Communications”** for more details of I<sup>2</sup>C Serial Interface communication.

## 3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I<sup>2</sup>C interface. The SDA pin is used for input and output data. In read mode, the conversion result is read from the SDA pin (output). In write mode, the device configuration bits are written (input) through the SDA pin. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V<sub>DD</sub> line to the SDA pin. Except for start and stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 5.3 “I<sup>2</sup>C Serial Communications”** for more details of I<sup>2</sup>C Serial Interface communication.

Typical range of the pull-up resistor value for SCL and SDA is from 5 kΩ to 10 kΩ for standard (100 kHz) and fast (400 kHz) modes, and less than 1 kΩ for high speed mode (3.4 MHz). The High-Speed mode is not recommended for V<sub>DD</sub> less than 2.7V.

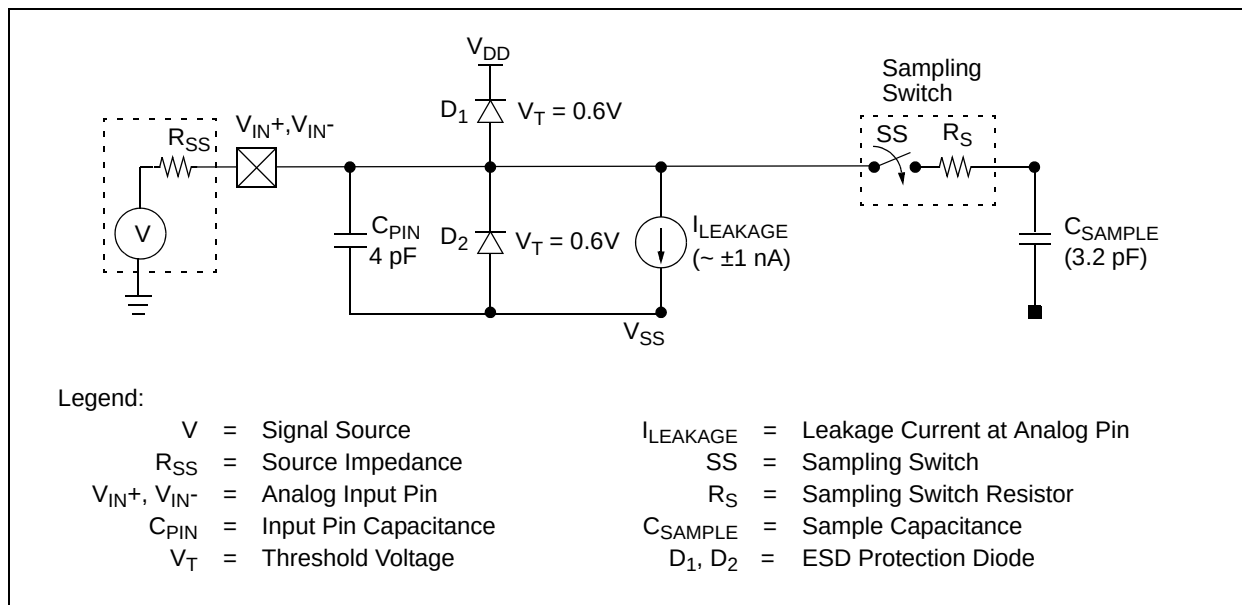


**FIGURE 3-1:** Equivalent Analog Input Circuit.

## 4.0 DESCRIPTION OF DEVICE OPERATION

### 4.1 General Overview

The MCP3421 is a low-power, 18-Bit Delta-Sigma A/D converter with an I<sup>2</sup>C serial interface. The device contains an on-board voltage reference (2.048V), programmable gain amplifier (PGA), and internal oscillator. When the device powers up (POR is set), it automatically resets the configuration bits to default settings.

#### Device default settings are:

- Conversion bit resolution: 12 bits (240 sps)
- PGA gain setting: x1
- Continuous conversion

Once the device is powered-up, the user can reprogram the configuration bits using I<sup>2</sup>C serial interface any time. The configuration bits are stored in volatile memory.

#### User selectable options are:

- Conversion bit resolution: 12, 14, 16, or 18 bits
- PGA Gain selection: x1, x2, x4, or x8
- Continuous or one-shot conversion

In the Continuous Conversion mode, the device converts the inputs continuously. While in the One-Shot Conversion mode, the device converts the input one time and stays in the low-power standby mode until it receives another command for a new conversion. During the standby mode, the device consumes less than 1  $\mu$ A maximum.

### 4.2 Power-On-Reset (POR)

The device contains an internal Power-On-Reset (POR) circuit that monitors power supply voltage ( $V_{DD}$ ) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The POR has built-in hysteresis and a timer to give a high degree of immunity to potential ripples and noises on the power supply. A 0.1  $\mu$ F decoupling capacitor should be mounted as close as possible to the  $V_{DD}$  pin for additional transient immunity.

The threshold voltage is set at 2.2V with a tolerance of approximately  $\pm 5\%$ . If the supply voltage falls below this threshold, the device will be held in a reset condition. The typical hysteresis value is approximately 200 mV.

The POR circuit is shut-down during the low-power standby mode. Once a power-up event has occurred, the device requires additional delay time (approximately 300  $\mu$ s) before a conversion can take place. During this time, all internal analog circuitries are settled before the first conversion occurs. Figure 4-1 illustrates the conditions for power-up and power-down events under typical start-up conditions.

When the device powers up, it automatically resets and sets the configuration bits to default settings. The default configuration bit conditions are a PGA gain of 1 V/V and a conversion speed of 240 SPS in Continuous Conversion mode. When the device receives an I<sup>2</sup>C General Call Reset command, it performs an internal reset similar to a Power-On-Reset event.

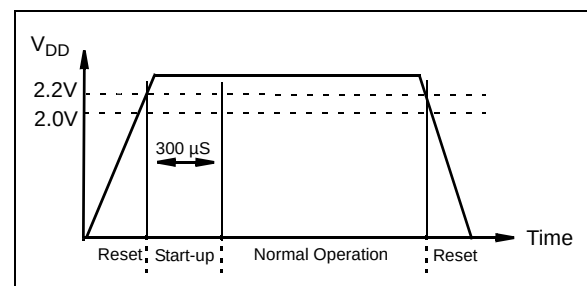


FIGURE 4-1: POR Operation.

### 4.3 Internal Voltage Reference

The device contains an on-board 2.048V voltage reference. This reference voltage is for internal use only and not directly measurable. The specifications of the reference voltage are part of the device's gain and drift specifications. Therefore, there is no separate specification for the on-board reference.

### 4.4 Analog Input Channel

The differential analog input channel has a switched capacitor structure. The internal sampling capacitor (3.2 pF for PGA = 1) is charged and discharged to process a conversion. The charging and discharging of the input sampling capacitor creates dynamic input currents at each input pin. The current is a function of the differential input voltages, and inversely proportional to the internal sampling capacitance, sampling frequency, and PGA setting.

## 4.5 Input Voltage Range

The differential ( $V_{IN}$ ) and common mode voltage ( $V_{INCOM}$ ) at the input pins without considering PGA setting are defined by:

$$V_{IN} = V_{IN+} - V_{IN-}$$

$$V_{INCOM} = \frac{V_{IN+} + V_{IN-}}{2}$$

The input signal levels are amplified by the internal programmable gain amplifier (PGA) at the front end of the  $\Delta\Sigma$  modulator.

The user needs to consider two conditions for the input voltage range: (a) Differential input voltage range and (b) Absolute maximum input voltage range.

### 4.5.1 DIFFERENTIAL INPUT VOLTAGE RANGE

The device performs conversions using its internal reference voltage ( $V_{REF} = 2.048V$ ). Therefore, the absolute value of the differential input voltage ( $V_{IN}$ ), with PGA setting is included, needs to be less than the internal reference voltage. The device will output saturated output codes (all 0s or all 1s except sign bit) if the absolute value of the input voltage ( $V_{IN}$ ), with PGA setting is included, is greater than the internal reference voltage ( $V_{REF} = 2.048V$ ). The input full-scale voltage range is given by:

#### EQUATION 4-1:

$$-V_{REF} \leq (V_{IN} \cdot PGA) \leq (V_{REF} - 1LSB)$$

Where:

$$V_{IN} = V_{IN+} - V_{IN-}$$

$$V_{REF} = 2.048V$$

If the input voltage level is greater than the above limit, the user can use a voltage divider and bring down the input level within the full-scale range. See [Figure 6-7](#) for more details of the input voltage divider circuit.

### 4.5.2 ABSOLUTE MAXIMUM INPUT VOLTAGE RANGE

The input voltage at each input pin must be less than the following absolute maximum input voltage limits:

- Input voltage  $< V_{DD} + 0.3V$
- Input voltage  $> V_{SS} - 0.3V$

Any input voltage outside this range can turn on the input ESD protection diodes, and result in input leakage current, causing conversion errors, or permanently damage the device.

Care must be taken in setting the input voltage ranges so that the input voltage does not exceed the absolute maximum input voltage range.

## 4.6 Input Impedance

The device uses a switched-capacitor input stage using a 3.2 pF sampling capacitor. This capacitor is switched (charged and discharged) at a rate of the sampling frequency that is generated by on-board clock. The differential input impedance varies with the PGA settings. The typical differential input impedance during a normal mode operation is given by:

$$Z_{IN}(f) = 2.25 M\Omega/PGA$$

Since the sampling capacitor is only switching to the input pins during a conversion process, the above input impedance is only valid during conversion periods. In a low power standby mode, the above impedance is not presented at the input pins. Therefore, only a leakage current due to ESD diode is presented at the input pins.

The conversion accuracy can be affected by the input signal source impedance when any external circuit is connected to the input pins. The source impedance adds to the internal impedance and directly affects the time required to charge the internal sampling capacitor. Therefore, a large input source impedance connected to the input pins can degrade the system performance, such as offset, gain, and Integral Non-Linearity (INL) errors. Ideally, the input source impedance should be zero. This can be achievable by using an operational amplifier with a closed-loop output impedance of tens of ohms.

## 4.7 Aliasing and Anti-aliasing Filter

Aliasing occurs when the input signal contains time-varying signal components with frequency greater than half the sample rate. In the aliasing conditions, the device can output unexpected output codes. For applications that are operating in electrical noise environments, the time-varying signal noise or high frequency interference components can be easily added to the input signals and cause aliasing. Although the device has an internal first order *sinc* filter, the filter response ([Figure 2-11](#)) may not give enough attenuation to all aliasing signal components. To avoid the aliasing, an external anti-aliasing filter, which can be accomplished with a simple RC low-pass filter, is typically used at the input pins. The low-pass filter cuts off the high frequency noise components and provides a band-limited input signal to the input pins.

## 4.8 Self-Calibration

The device performs a self-calibration of offset and gain for each conversion. This provides reliable conversion results from conversion-to-conversion over variations in temperature as well as power supply fluctuations.

## 4.9 Digital Output Codes and Conversion to Real Values

### 4.9.1 DIGITAL OUTPUT CODE FROM DEVICE

The digital output code is proportional to the input voltage and PGA settings. The output data format is a binary two's complement. With this code scheme, the MSB can be considered a sign indicator. When the MSB is a logic '0', the input is positive. When the MSB is a logic '1', the input is negative. The following is an example of the output code:

- for a negative full scale input voltage:  
100...000  
Example:  $(V_{IN+} - V_{IN-}) \cdot PGA = -2.048V$
- for a zero differential input voltage: 000...000  
Example:  $(V_{IN+} - V_{IN-}) = 0$
- for a positive full scale input voltage:  
011...111  
Example:  $(V_{IN+} - V_{IN-}) \cdot PGA = 2.048V$

The MSB (sign bit) is always transmitted first through the I<sup>2</sup>C serial data line. The resolution for each conversion is 18, 16, 14, or 12 bits depending on the conversion rate selection bit settings by the user.

The output codes will not roll-over even if the input voltage exceeds the maximum input range. In this case, the code will be locked at 0111...11 for all voltages greater than  $(V_{REF} - 1 \text{ LSB})/PGA$  and 1000...00 for voltages less than  $-V_{REF}/PGA$ . Table 4-2 shows an example of output codes of various input levels for 18 bit conversion mode. Table 4-3 shows an example of minimum and maximum output codes for each conversion rate option.

The number of output code is given by:

#### EQUATION 4-2:

$$\text{Number of Output Code} = (\text{Maximum Code} + 1) \times PGA \times \frac{(V_{IN+} - V_{IN-})}{2.048V}$$

Where:

See Table 4-3 for Maximum Code.

The LSB of the data conversion is given by:

#### EQUATION 4-3:

$$LSB = \frac{2 \times V_{REF}}{2^N} = \frac{2 \times 2.048V}{2^N}$$

Where:

N = User programmable bit resolution:  
12,14,16, or 18

Table 4-1 shows the LSB size of each conversion rate setting. The measured unknown input voltage is obtained by multiplying the output codes with LSB. See the following section for the input voltage calculation using the output codes.

**TABLE 4-1: RESOLUTION SETTINGS VS. LSB**

| Resolution Setting | LSB            |
|--------------------|----------------|
| 12 bits            | 1 mV           |
| 14 bits            | 250 $\mu$ V    |
| 16 bits            | 62.5 $\mu$ V   |
| 18 bits            | 15.625 $\mu$ V |

**TABLE 4-2: EXAMPLE OF OUTPUT CODE FOR 18 BITS (NOTE 1,NOTE 2)**

| Input Voltage:<br>[ $V_{IN+} - V_{IN-}$ ] $\cdot$ PGA | Digital Output Code |
|-------------------------------------------------------|---------------------|
| $\geq V_{REF}$                                        | 011111111111111111  |
| $V_{REF} - 1 \text{ LSB}$                             | 011111111111111111  |
| 2 LSB                                                 | 000000000000000010  |
| 1 LSB                                                 | 000000000000000001  |
| 0                                                     | 000000000000000000  |
| -1 LSB                                                | 111111111111111111  |
| -2 LSB                                                | 111111111111111110  |
| $-V_{REF}$                                            | 100000000000000000  |
| $< -V_{REF}$                                          | 100000000000000000  |

**Note 1:** MSB is a sign indicator:

- 0: Positive input ( $V_{IN+} > V_{IN-}$ )
- 1: Negative input ( $V_{IN+} < V_{IN-}$ )

**2:** Output data format is binary two's complement.

**TABLE 4-3: MINIMUM AND MAXIMUM OUTPUT CODES (NOTE)**

| Resolution Setting | Data Rate | Minimum Code | Maximum Code |
|--------------------|-----------|--------------|--------------|
| 12                 | 240 SPS   | -2048        | 2047         |
| 14                 | 60 SPS    | -8192        | 8191         |
| 16                 | 15 SPS    | -32768       | 32767        |
| 18                 | 3.75 SPS  | -131072      | 131071       |

**Note:** Maximum n-bit code =  $2^{N-1} - 1$   
Minimum n-bit code =  $-1 \times 2^{N-1}$

## 4.9.2 CONVERTING THE DEVICE OUTPUT CODE TO INPUT SIGNAL VOLTAGE

When the user gets the digital output codes from the device as described in **Section 4.9.1 “Digital output code from device”**, the next step is converting the digital output codes to a measured input voltage. [Equation 4-4](#) shows an example of converting the output codes to its corresponding input voltage.

If the sign indicator bit (MSB) is ‘0’, the input voltage is obtained by multiplying the output code with the LSB and divided by the PGA setting.

If the sign indicator bit (MSB) is ‘1’, the output code needs to be converted to two's complement before multiplied by LSB and divided by the PGA setting. [Table 4-4](#) shows an example of converting the device output codes to input voltage.

## EQUATION 4-4: CONVERTING OUTPUT CODES TO INPUT VOLTAGE

**If MSB = 0 (Positive Output Code):**

$$\text{Input Voltage} = (\text{Output Code}) \cdot \frac{\text{LSB}}{\text{PGA}}$$

**If MSB = 1 (Negative Output Code):**

$$\text{Input Voltage} = (2\text{'s complement of Output Code}) \cdot \frac{\text{LSB}}{\text{PGA}}$$

Where:

LSB = See [Table 4-1](#)

2's complement = 1's complement + 1

**TABLE 4-4: EXAMPLE OF CONVERTING OUTPUT CODE TO VOLTAGE (WITH 18 BIT SETTING)**

| Input Voltage<br>[V <sub>IN+</sub> - V <sub>IN-</sub> ] • PGA | Digital Output Code | MSB<br>(sign bit) | Example of Converting Output Codes to Input Voltage                                                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------|---------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ≥ V <sub>REF</sub>                                            | 0111111111111111    | 0                 | (2 <sup>16</sup> +2 <sup>15</sup> +2 <sup>14</sup> +2 <sup>13</sup> +2 <sup>12</sup> +2 <sup>11</sup> +2 <sup>10</sup> +2 <sup>9</sup> +2 <sup>8</sup> +2 <sup>7</sup> +2 <sup>6</sup> +2 <sup>5</sup> +2 <sup>4</sup> +2 <sup>3</sup> +2 <sup>2</sup> +2 <sup>1</sup> +2 <sup>0</sup> )x LSB(15.625μV)/PGA = 2.048 (V) for PGA = 1 |
| V <sub>REF</sub> - 1 LSB                                      | 0111111111111111    | 0                 | (2 <sup>16</sup> +2 <sup>15</sup> +2 <sup>14</sup> +2 <sup>13</sup> +2 <sup>12</sup> +2 <sup>11</sup> +2 <sup>10</sup> +2 <sup>9</sup> +2 <sup>8</sup> +2 <sup>7</sup> +2 <sup>6</sup> +2 <sup>5</sup> +2 <sup>4</sup> +2 <sup>3</sup> +2 <sup>2</sup> +2 <sup>1</sup> +2 <sup>0</sup> )x LSB(15.625μV)/PGA = 2.048 (V) for PGA = 1 |
| 2 LSB                                                         | 00000000000000010   | 0                 | (0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+2 <sup>1</sup> +0)x LSB(15.625μV)/PGA = 31.25 (μV) for PGA = 1                                                                                                                                                                                                                                     |
| 1 LSB                                                         | 00000000000000001   | 0                 | (0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+2 <sup>0</sup> )x LSB(15.625μV)/PGA = 15.625 (μV)for PGA = 1                                                                                                                                                                                                                                       |
| 0                                                             | 000000000000000000  | 0                 | (0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0)x LSB(15.625μV)/PGA = 0 V (V) for PGA = 1                                                                                                                                                                                                                                                        |
| -1 LSB                                                        | 1111111111111111    | 1                 | -(0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+2 <sup>0</sup> )x LSB(15.625μV)/PGA = - 15.625 (μV)for PGA = 1                                                                                                                                                                                                                                    |
| -2 LSB                                                        | 11111111111111110   | 1                 | -(0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+2 <sup>1</sup> +0)x LSB(15.625μV)/PGA = - 31.25 (μV)for PGA = 1                                                                                                                                                                                                                                   |
| - V <sub>REF</sub>                                            | 100000000000000000  | 1                 | -(2 <sup>17</sup> +0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0) x LSB(15.625μV)/PGA = - 2.048 (V) for PGA = 1                                                                                                                                                                                                                                   |
| ≤ -V <sub>REF</sub>                                           | 100000000000000000  | 1                 | -(2 <sup>17</sup> +0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0) x LSB(15.625μV)/PGA = - 2.048 (V) for PGA = 1                                                                                                                                                                                                                                   |

## 5.0 USING THE MCP3421 DEVICE

### 5.1 Operating Modes

The user operates the device by setting up the device configuration register using a write command (see Figure 5-2) and reads the conversion data using a read command (see Figure 5-3 and Figure 5-4). The device operates in two modes: (a) Continuous Conversion Mode or (b) One-Shot Conversion Mode (single conversion). This mode selection is made by setting the  $\overline{O/C}$  bit in the Configuration Register. Refer to **Section 5.2 “Configuration Register”** for more information.

#### 5.1.1 CONTINUOUS CONVERSION MODE ( $\overline{O/C}$ BIT = 1)

The device performs a Continuous Conversion if the  $\overline{O/C}$  bit is set to logic “high”. Once the conversion is completed,  $\overline{RDY}$  bit is toggled to ‘0’ and the result is placed at the output data register. The device immediately begins another conversion and overwrites the output data register with the most recent result. The device clears the data ready flag ( $\overline{RDY}$  bit = 0) when the conversion is completed. The device sets the ready flag bit ( $\overline{RDY}$  bit = 1), if the latest conversion result has been read by the Master.

- **When writing configuration register:**
  - Setting  $\overline{RDY}$  bit in continuous mode does not affect anything
- **When reading conversion data:**
  - $\overline{RDY}$  bit = 0 means the latest conversion result is ready
  - $\overline{RDY}$  bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the  $\overline{RDY}$  bit will be cleared when the new conversion result is ready

#### 5.1.2 ONE-SHOT CONVERSION MODE ( $\overline{O/C}$ BIT = 0)

Once the One-Shot Conversion (single conversion) Mode is selected, the device performs only one conversion, updates the output data register, clears the data ready flag ( $\overline{RDY}$  = 0), and then enters a low power standby mode. A new One-Shot Conversion is started again when the device receives a new write command with  $\overline{RDY}$  = 1.

- **When writing configuration register:**
  - The  $\overline{RDY}$  bit needs to be set to begin a new conversion in one-shot mode
- **When reading conversion data:**
  - $\overline{RDY}$  bit = 0 means the latest conversion result is ready
  - $\overline{RDY}$  bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the  $\overline{RDY}$  bit will be cleared when the new conversion is done

This One-Shot Conversion Mode is highly recommended for low power operating applications where the conversion result is needed by request on demand. During the low current standby mode, the device consumes less than 1  $\mu$ A maximum (or 300 nA typical). For example, if the user collects 18 bit conversion data once a second in One-Shot Conversion mode, the device draws only about one fourth of its total operating current. In this example, the device consumes approximately 39  $\mu$ A (145  $\mu$ A / 3.75 SPS = 39  $\mu$ A), if the device performs only one conversion per second (1 SPS) in 18-bit conversion mode with 3V power supply.

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## 5.2 Configuration Register

The device has an 8-bit wide configuration register to select for: input channel, conversion mode, conversion rate, and PGA gain. This register allows the user to change the operating condition of the device and check the status of the device operation.

The user can rewrite the configuration byte any time during the device operation. Register 5-1 shows the configuration register bits.

**REGISTER 5-1: CONFIGURATION REGISTER**

| R/W-1                   | R/W-0 | R/W-0 | R/W-1                   | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------------------------|-------|-------|-------------------------|-------|-------|-------|-------|
| $\overline{\text{RDY}}$ | C1    | C0    | $\overline{\text{O/C}}$ | S1    | S0    | G1    | G0    |
| 1 *                     | 0 *   | 0 *   | 1 *                     | 0 *   | 0 *   | 0 *   | 0 *   |
| bit 7                   |       |       |                         | bit 0 |       |       |       |

\* Default Configuration after Power-On Reset

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

### $\overline{\text{RDY}}$ : Ready Bit

This bit is the data ready flag. In read mode, this bit indicates if the output register has been updated with a latest conversion result. In One-Shot Conversion mode, writing this bit to "1" initiates a new conversion.

#### Reading $\overline{\text{RDY}}$ bit with the read command:

1 = Output register has not been updated.

0 = Output register has been updated with the latest conversion result.

#### Writing $\overline{\text{RDY}}$ bit with the write command:

Continuous Conversion mode: No effect

One-Shot Conversion mode:

1 = Initiate a new conversion.

0 = No effect.

bit 6-5

**C1-C0**: These bits are not effected for the MCP3421.

bit 4

### $\overline{\text{O/C}}$ : Conversion Mode Bit

1 = Continuous Conversion Mode (**Default**). The device performs data conversions continuously.

0 = One-Shot Conversion Mode. The device performs a single conversion and enters a low power standby mode until it receives another write or read command.

bit 3-2

### **S1-S0**: Sample Rate Selection Bit

00 = 240 SPS (12 bits) (**Default**)

01 = 60 SPS (14 bits)

10 = 15 SPS (16 bits)

11 = 3.75 SPS (18 bits)

bit 1-0

### **G1-G0**: PGA Gain Selection Bits

00 = x1 (**Default**)

01 = x2

10 = x4

11 = x8

If the configuration byte is read repeatedly by clocking continuously after reading the data bytes (i.e., after the 5th byte in the 18-bit conversion mode), the state of the RDY bit indicates whether the device is ready with new conversion result. When the Master finds the RDY bit is cleared, it can send a not-acknowledge (NAK) bit and a stop bit to exit the current read operation and send a new read command for the latest conversion data. Once the conversion data has been read, the ready bit toggles to '1' until the next new conversion data is ready. The conversion data in the output register is overwritten every time a new conversion is completed.

Figure 5-3 and Figure 5-4 show the examples of reading the conversion data. The user can rewrite the configuration byte any time for a new setting.

Table 5-1 and Table 5-2 show the examples of the configuration bit operation.

**TABLE 5-1: WRITE CONFIGURATION BITS**

| R/W | O/C | RDY | Operation                                                                                    |
|-----|-----|-----|----------------------------------------------------------------------------------------------|
| 0   | 0   | 0   | No effect if all other bits remain the same - operation continues with the previous settings |
| 0   | 0   | 1   | Initiate One-Shot Conversion                                                                 |
| 0   | 1   | 0   | Initiate Continuous Conversion                                                               |
| 0   | 1   | 1   | Initiate Continuous Conversion                                                               |

**TABLE 5-2: READ CONFIGURATION BITS**

| R/W | O/C | RDY | Operation                                                                                                                                                                    |
|-----|-----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | 0   | 0   | New conversion result in One-Shot conversion mode has just been read. The RDY bit remains low until set by a new write command.                                              |
| 1   | 0   | 1   | One-Shot Conversion is in progress. The conversion result is not updated yet. The RDY bit stays high until the current conversion is completed.                              |
| 1   | 1   | 0   | New conversion result in Continuous Conversion mode has just been read. The RDY bit changes to high after reading the conversion data.                                       |
| 1   | 1   | 1   | The conversion result in Continuous Conversion mode was already read. The next new conversion data is not ready. The RDY bit stays high until a new conversion is completed. |

## 5.3 I<sup>2</sup>C Serial Communications

The device communicates with Master (microcontroller) through a serial I<sup>2</sup>C (Inter-Integrated Circuit) interface and support standard (100 kbits/sec), fast (400 kbits/sec) and high-speed (3.4 Mbits/sec) modes.

**Note:** The High-Speed mode is not recommended for V<sub>DD</sub> less than 2.7V.

The serial I<sup>2</sup>C is a bidirectional 2-wire data bus communication protocol using open-drain SCL and SDA lines.

The device can only be addressed as a slave. Once addressed, it can receive configuration bits with a write command or transmit the latest conversion results with a read command. The serial clock pin (SCL) is an input only and the serial data pin (SDA) is bidirectional. The Master starts communication by sending a START bit and terminates the communication by sending a STOP bit. In read mode, the device releases the SDA line after receiving NAK and STOP bits.

An example of a hardware connection diagram is shown in Figure 6-1. More details of the I<sup>2</sup>C bus characteristic is described in Section 5.6 "I<sup>2</sup>C Bus Characteristics".

### 5.3.1 I<sup>2</sup>C DEVICE ADDRESSING

The first byte after the START bit is always the address byte of the device, which includes the device code (4 bits), address bits (3 bits), and R/W bit. The device code of the MCP3421 is **1101**, which is programmed at the factory. The device code is followed by three address bits (A2, A1, A0) which are also programmed at the factory. The three address bits allow up to eight MCP3421 devices on the same data bus line.

The (R/W) bit determines if the Master device wants to read the conversion data or write to the Configuration register. If the (R/W) bit is set (read mode), the device outputs the conversion data in the following clocks. If the (R/W) bit is cleared (write mode), the device expects a configuration byte in the following clocks. When the device receives the correct address byte, it outputs an acknowledge bit after the R/W bit.

Figure 5-1 shows the address byte. Figure 5-2 through Figure 5-4 show how to write the configuration register bits and read the conversion results.

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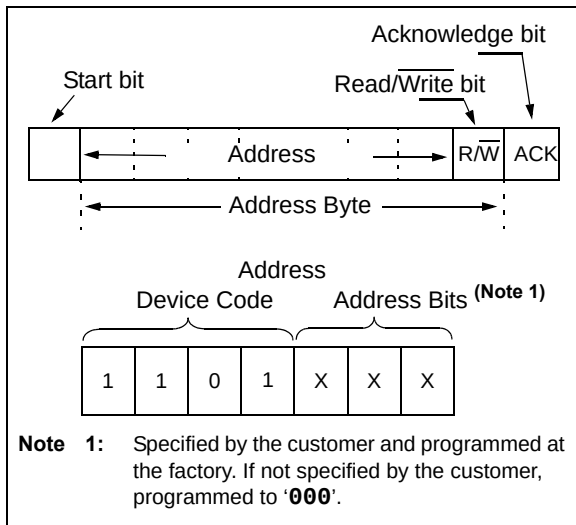


**FIGURE 5-1:** MCP3421 Address Byte.

## 5.3.2 WRITING A CONFIGURATION BYTE TO THE DEVICE

When the Master sends an address byte with the  $\overline{R/W}$  bit low ( $R/W = 0$ ), the MCP3421 expects one configuration byte following the address. Any byte sent after this second byte will be ignored. The user can change the operating mode of the device by writing the configuration register bits.

If the device receives a write command with a new configuration setting, the device immediately begins a new conversion and updates the conversion data.

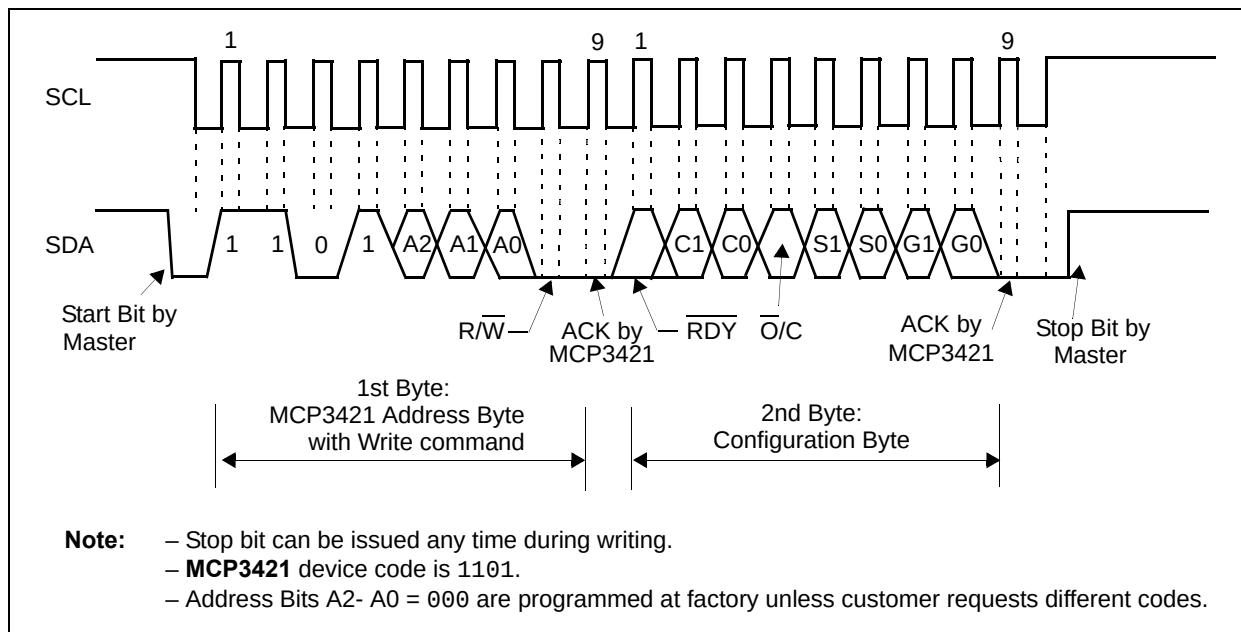


**FIGURE 5-2:** Timing Diagram For Writing To The MCP3421.

### 5.3.3 READING OUTPUT CODES AND CONFIGURATION BYTE FROM THE DEVICE

When the Master sends a read command ( $\overline{R/\overline{W}} = 1$ ), the device outputs both the conversion data and configuration bytes. Each byte consists of 8 bits with one acknowledge (ACK) bit. The ACK bit after the address byte is issued by the device and the ACK bits after each conversion data bytes are issued by the Master.

When the device is configured for 18-bit conversion mode, it outputs three data bytes followed by a configuration byte. The first 6 data bits in the first data byte are repeated MSB (= sign bit) of the conversion data. The user can ignore the first 6 data bits, and take the 7th data bit (D17) as the MSB of the conversion data. The LSB of the 3rd data byte is the LSB of the conversion data (D0).

If the device is configured for 12, 14, or 16 bit-mode, the device outputs two data bytes followed by a configuration byte. In 16 bit-conversion mode, the MSB (= sign bit) of the first data byte is D15. In 14-bit conversion mode, the first two bits in the first data byte are repeated MSB bits and can be ignored, and the 3rd bit (D13) is the MSB (=sign bit) of the conversion data. In 12-bit conversion mode, the first four bits are repeated MSB bits and can be ignored. The 5th bit (D11) of the byte represents the MSB (= sign bit) of the conversion data. [Table 5-3](#) summarizes the conversion data output of each conversion mode.

The configuration byte follows the output data bytes. The device repeatedly outputs the configuration byte only if the Master sends clocks repeatedly after the data bytes.

The device terminates the current outputs when it receives a Not-Acknowledge (NAK), a repeated start or a stop bit at any time during the output bit stream. It is not required to read the configuration byte. However, the Master may read the configuration byte to check the  $\overline{RDY}$  bit condition. The Master may continuously send clock (SCL) to repeatedly read the configuration byte (to check the  $\overline{RDY}$  bit status).

[Figures 5-3](#) and [5-4](#) show the timing diagrams of the reading.

**TABLE 5-3: OUTPUT CODES OF EACH RESOLUTION OPTION**

| Conversion Option | Digital Output Codes                                                                                                    |
|-------------------|-------------------------------------------------------------------------------------------------------------------------|
| 18-bits           | MMMMMMD17D16 (1st data byte) - D15 ~ D8 (2nd data byte) - D7 ~ D0 (3rd data byte) - Configuration byte. <b>(Note 1)</b> |
| 16-bits           | D15 ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 2)</b>                                |
| 14-bits           | MMD13D ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 3)</b>                             |
| 12-bits           | MMMMD11 ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 4)</b>                            |

**Note 1:** D17 is MSB (= sign bit), M is repeated MSB of the data byte.

**2:** D15 is MSB (= sign bit).

**3:** D13 is MSB (= sign bit), M is repeated MSB of the data byte.

**4:** D11 is MSB (= sign bit), M is repeated MSB of the data byte.



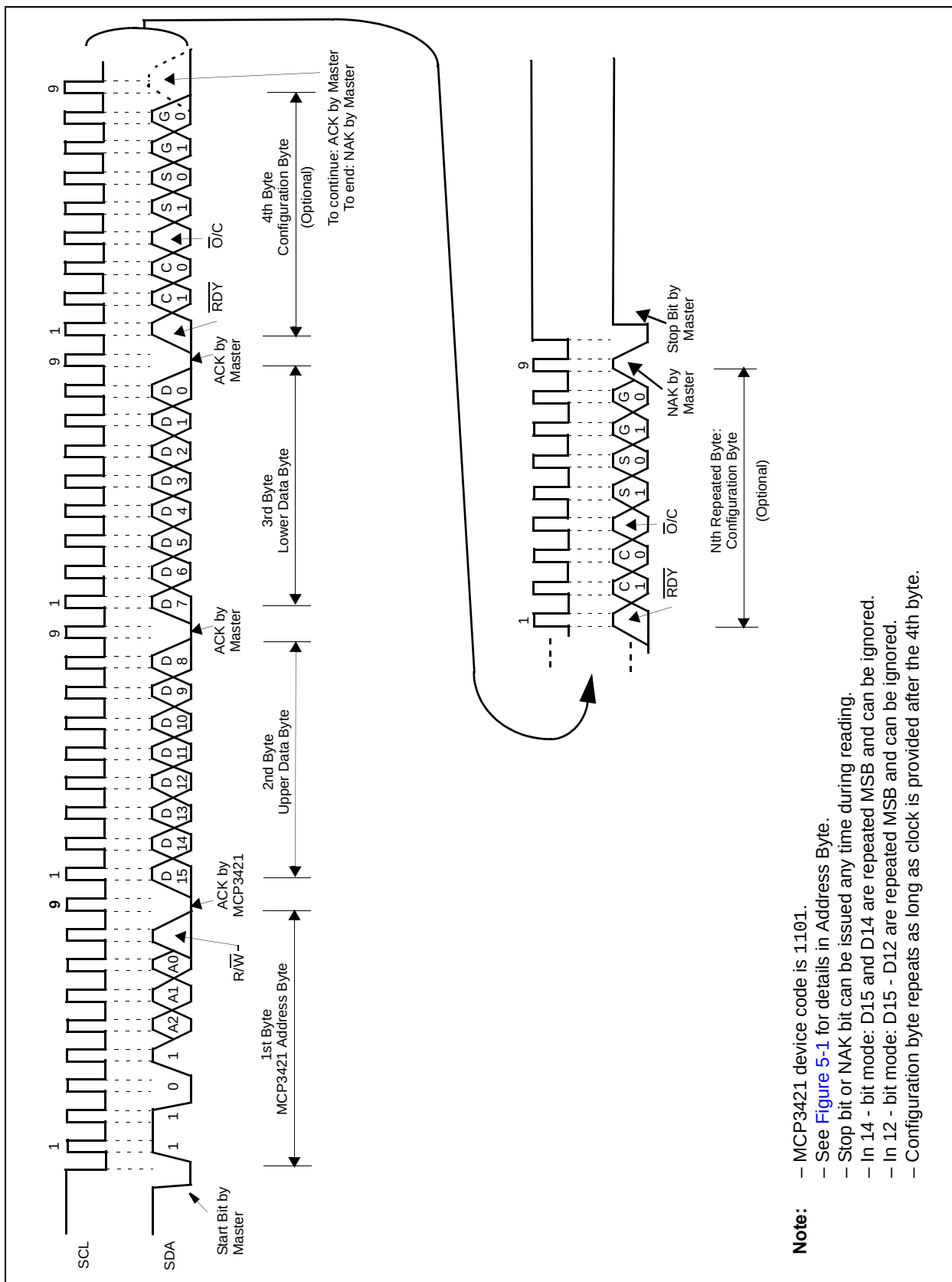


**FIGURE 5-4:** Timing Diagram For Reading From The MCP3421 With 12-Bit to 16-Bit Modes.

## 5.4 General Call

The device acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. Refer to [Figure 5-5](#). The device supports the following two general calls.

For more information on the general call, or other I<sup>2</sup>C modes, please refer to the Phillips I<sup>2</sup>C specification.

### 5.4.1 GENERAL CALL RESET

The general call reset occurs if the second byte is '00000110' (06h). At the acknowledgement of this byte, the device will abort current conversion and perform an internal reset similar to a Power-On-Reset (POR). All configuration and data register bits are reset to default values.

### 5.4.2 GENERAL CALL CONVERSION

The general call conversion occurs if the second byte is '00001000' (08h). All devices on the bus initiate a conversion simultaneously. When the device receives this command, the configuration will be set to the One-Shot Conversion mode and a single conversion will be performed. The PGA and data rate settings are unchanged with this general call.

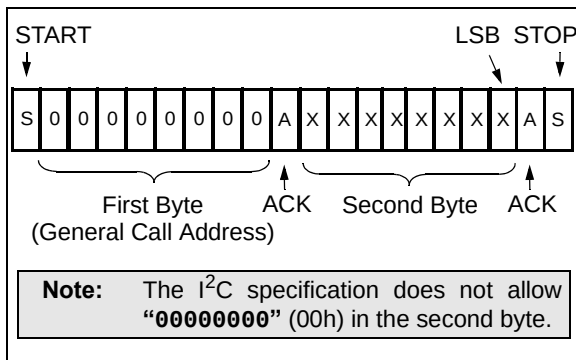


**FIGURE 5-5:** General Call Address Format.

## 5.5 High-Speed (HS) Mode

The I<sup>2</sup>C specification requires that a high-speed mode device must be 'activated' to operate in high-speed mode. This is done by sending a special address byte of "00001XXX" following the START bit. The "XXX" bits are unique to the High-Speed (HS) mode Master. This byte is referred to as the High-Speed (HS) Master Mode Code (HSMMC). The MCP3421 device does not acknowledge this byte. However, upon receiving this code, the device switches on its HS mode filters and communicates up to 3.4 MHz on SDA and SCL bus lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I<sup>2</sup>C modes, please refer to the Phillips I<sup>2</sup>C specification.

## 5.6 I<sup>2</sup>C Bus Characteristics

The I<sup>2</sup>C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition

Accordingly, the following bus conditions have been defined using [Figure 5-6](#).

### 5.6.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

### 5.6.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 5.6.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations can be ended with a STOP condition.

### 5.6.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

## 5.6.5 ACKNOWLEDGE AND NON-ACKNOWLEDGE

The Master (microcontroller) and the slave (MCP3421) use an acknowledge pulse as a hand shake of communication for each byte. The ninth clock pulse of each byte is used for the acknowledgement. The clock pulse is always provided by the Master (microcontroller) and the acknowledgement is issued by the receiving device of the byte (Note: The transmitting device must release the SDA line during the acknowledge pulse.). The acknowledgement is achieved by pulling-down the SDA line "LOW" during the 9th clock pulse by the receiving device.

During reads, the Master (microcontroller) can terminate the current read operation by not providing an acknowledge bit (not Acknowledge (NAK)) on the last byte. In this case, the MCP3421 device releases the SDA line to allow the Master (microcontroller) to generate a STOP or repeated START condition.

The non-acknowledgement (NAK) is issued by providing the SDA line to "HIGH" during the 9th clock pulse.

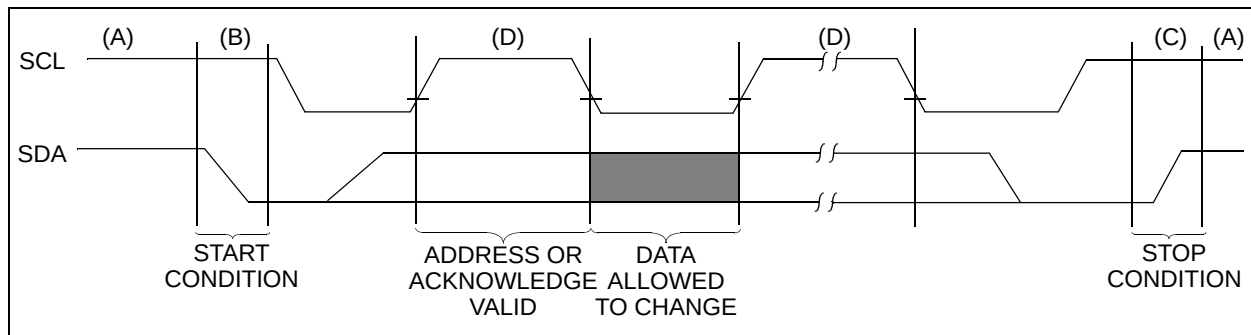


**FIGURE 5-6:** Data Transfer Sequence on I<sup>2</sup>C Serial Bus.

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**TABLE 5-4: I<sup>2</sup>C SERIAL TIMING SPECIFICATIONS**

| <b>Electrical Specifications:</b> Unless otherwise specified, all limits are specified for T <sub>A</sub> = -40 to +85°C, V <sub>IN+</sub> = V <sub>IN-</sub> = V <sub>REF</sub> /2, V <sub>SS</sub> = 0V, V <sub>DD</sub> = +2.7V to +5.0V. |                     |            |     |      |       |                                                           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------|-----|------|-------|-----------------------------------------------------------|
| Parameters                                                                                                                                                                                                                                   | Sym                 | Min        | Typ | Max  | Units | Conditions                                                |
| <b>Standard Mode (100 kHz)</b>                                                                                                                                                                                                               |                     |            |     |      |       |                                                           |
| Clock frequency                                                                                                                                                                                                                              | f <sub>SCL</sub>    | —          | —   | 100  | kHz   |                                                           |
| Clock high time                                                                                                                                                                                                                              | T <sub>HIGH</sub>   | 4000       | —   | —    | ns    |                                                           |
| Clock low time                                                                                                                                                                                                                               | T <sub>LOW</sub>    | 4700       | —   | —    | ns    |                                                           |
| SDA and SCL rise time                                                                                                                                                                                                                        | T <sub>R</sub>      | —          | —   | 1000 | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ( <b>Note 1</b> ) |
| SDA and SCL fall time                                                                                                                                                                                                                        | T <sub>F</sub>      | —          | —   | 300  | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ( <b>Note 1</b> ) |
| START condition hold time                                                                                                                                                                                                                    | T <sub>HD:STA</sub> | 4000       | —   | —    | ns    |                                                           |
| START (Repeated) condition setup time                                                                                                                                                                                                        | T <sub>SU:STA</sub> | 4700       | —   | —    | ns    |                                                           |
| Data hold time                                                                                                                                                                                                                               | T <sub>HD:DAT</sub> | 0          | —   | 3450 | ns    | ( <b>Note 3</b> )                                         |
| Data input setup time                                                                                                                                                                                                                        | T <sub>SU:DAT</sub> | 250        | —   | —    | ns    |                                                           |
| STOP condition setup time                                                                                                                                                                                                                    | T <sub>SU:STO</sub> | 4000       | —   | —    | ns    |                                                           |
| Output valid from clock                                                                                                                                                                                                                      | T <sub>AA</sub>     | 0          | —   | 3750 | ns    | ( <b>Note 2, Note 3</b> )                                 |
| Bus free time                                                                                                                                                                                                                                | T <sub>BUF</sub>    | 4700       | —   | —    | ns    | Time between START and STOP conditions.                   |
| <b>Fast Mode (400 kHz)</b>                                                                                                                                                                                                                   |                     |            |     |      |       |                                                           |
| Clock frequency                                                                                                                                                                                                                              | T <sub>SCL</sub>    | —          | —   | 400  | kHz   |                                                           |
| Clock high time                                                                                                                                                                                                                              | T <sub>HIGH</sub>   | 600        | —   | —    | ns    |                                                           |
| Clock low time                                                                                                                                                                                                                               | T <sub>LOW</sub>    | 1300       | —   | —    | ns    |                                                           |
| SDA and SCL rise time                                                                                                                                                                                                                        | T <sub>R</sub>      | 20 + 0.1Cb | —   | 300  | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ( <b>Note 1</b> ) |
| SDA and SCL fall time                                                                                                                                                                                                                        | T <sub>F</sub>      | 20 + 0.1Cb | —   | 300  | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ( <b>Note 1</b> ) |
| START condition hold time                                                                                                                                                                                                                    | T <sub>HD:STA</sub> | 600        | —   | —    | ns    |                                                           |
| START (Repeated) condition setup time                                                                                                                                                                                                        | T <sub>SU:STA</sub> | 600        | —   | —    | ns    |                                                           |
| Data hold time                                                                                                                                                                                                                               | T <sub>HD:DAT</sub> | 0          | —   | 900  | ns    | ( <b>Note 4</b> )                                         |
| Data input setup time                                                                                                                                                                                                                        | T <sub>SU:DAT</sub> | 100        | —   | —    | ns    |                                                           |
| STOP condition setup time                                                                                                                                                                                                                    | T <sub>SU:STO</sub> | 600        | —   | —    | ns    |                                                           |
| Output valid from clock                                                                                                                                                                                                                      | T <sub>AA</sub>     | 0          | —   | 1200 | ns    | ( <b>Note 2, Note 3</b> )                                 |
| Bus free time                                                                                                                                                                                                                                | T <sub>BUF</sub>    | 1300       | —   | —    | ns    | Time between START and STOP conditions.                   |

**Note 1:** This parameter is ensured by characterization and not 100% tested.

**2:** This specification is not a part of the I<sup>2</sup>C specification. This specification is equivalent to the Data Hold Time (T<sub>HD:DAT</sub>) plus SDA Fall (or rise) time: T<sub>AA</sub> = T<sub>HD:DAT</sub> + T<sub>F</sub> (OR T<sub>R</sub>).

**3:** If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time (T<sub>LOW</sub>) can be affected.

**4:** For Data Input: This parameter must be longer than t<sub>SP</sub>. If this parameter is too long, the Data Input Setup (T<sub>SU:DAT</sub>) or Clock Low time (T<sub>LOW</sub>) can be affected.

For Data Output: This parameter is characterized, and tested indirectly by testing T<sub>AA</sub> parameter.

TABLE 5-4: I<sup>2</sup>C SERIAL TIMING SPECIFICATIONS (CONTINUED)

| <b>Electrical Specifications:</b> Unless otherwise specified, all limits are specified for T <sub>A</sub> = -40 to +85°C, V <sub>IN+</sub> = V <sub>IN-</sub> = V <sub>REF</sub> /2, V <sub>SS</sub> = 0V, V <sub>DD</sub> = +2.7V to +5.0V. |                      |     |     |     |       |                                                                                                  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|-----|-----|-------|--------------------------------------------------------------------------------------------------|
| Parameters                                                                                                                                                                                                                                   | Sym                  | Min | Typ | Max | Units | Conditions                                                                                       |
| <b>High-Speed Mode (3.4 MHz): Not recommended for V<sub>DD</sub> &lt; 2.7V</b>                                                                                                                                                               |                      |     |     |     |       |                                                                                                  |
| Clock frequency                                                                                                                                                                                                                              | f <sub>SCL</sub>     | —   | —   | 3.4 | MHz   | C <sub>b</sub> = 100 pF                                                                          |
|                                                                                                                                                                                                                                              |                      | —   | —   | 1.7 | MHz   | C <sub>b</sub> = 400 pF                                                                          |
| Clock high time                                                                                                                                                                                                                              | T <sub>HIGH</sub>    | 60  | —   | —   | ns    | C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz                                              |
|                                                                                                                                                                                                                                              |                      | 120 | —   | —   | ns    | C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz                                              |
| Clock low time                                                                                                                                                                                                                               | T <sub>LOW</sub>     | 160 | —   | —   | ns    | C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz                                              |
|                                                                                                                                                                                                                                              |                      | 320 | —   | —   | ns    | C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz                                              |
| SCL rise time<br>(Note 1)                                                                                                                                                                                                                    | T <sub>R</sub>       | —   | —   | 40  | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ,<br>C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz |
|                                                                                                                                                                                                                                              |                      | —   | —   | 80  | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ,<br>C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz |
| SCL fall time<br>(Note 1)                                                                                                                                                                                                                    | T <sub>F</sub>       | —   | —   | 40  | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ,<br>C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz |
|                                                                                                                                                                                                                                              |                      | —   | —   | 80  | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ,<br>C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz |
| SDA rise time<br>(Note 1)                                                                                                                                                                                                                    | T <sub>R: DAT</sub>  | —   | —   | 80  | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ,<br>C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz |
|                                                                                                                                                                                                                                              |                      | —   | —   | 160 | ns    | From V <sub>IL</sub> to V <sub>IH</sub> ,<br>C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz |
| SDA fall time<br>(Note 1)                                                                                                                                                                                                                    | T <sub>F: DATA</sub> | —   | —   | 80  | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ,<br>C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz |
|                                                                                                                                                                                                                                              |                      | —   | —   | 160 | ns    | From V <sub>IH</sub> to V <sub>IL</sub> ,<br>C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz |
| Data hold time<br>(Note 4)                                                                                                                                                                                                                   | T <sub>HD: DAT</sub> | 0   | —   | 70  | ns    | C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz                                              |
|                                                                                                                                                                                                                                              |                      | 0   | —   | 150 | ns    | C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz                                              |
| Output valid from clock<br>(Notes 2 and 3)                                                                                                                                                                                                   | T <sub>AA</sub>      | —   | —   | 150 | ns    | C <sub>b</sub> = 100 pF, f <sub>SCL</sub> = 3.4 MHz                                              |
|                                                                                                                                                                                                                                              |                      | —   | —   | 310 | ns    | C <sub>b</sub> = 400 pF, f <sub>SCL</sub> = 1.7 MHz                                              |
| START condition hold time                                                                                                                                                                                                                    | T <sub>HD: STA</sub> | 160 | —   | —   | ns    |                                                                                                  |
| START (Repeated) condition<br>setup time                                                                                                                                                                                                     | T <sub>SU: STA</sub> | 160 | —   | —   | ns    |                                                                                                  |
| Data input setup time                                                                                                                                                                                                                        | T <sub>SU: DAT</sub> | 10  | —   | —   | ns    |                                                                                                  |
| STOP condition setup time                                                                                                                                                                                                                    | T <sub>SU: STO</sub> | 160 | —   | —   | ns    |                                                                                                  |

**Note 1:** This parameter is ensured by characterization and not 100% tested.

**2:** This specification is not a part of the I<sup>2</sup>C specification. This specification is equivalent to the Data Hold Time (T<sub>HD: DAT</sub>) plus SDA Fall (or rise) time: T<sub>AA</sub> = T<sub>HD: DAT</sub> + T<sub>F</sub> (OR T<sub>R</sub>).

**3:** If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time (T<sub>LOW</sub>) can be affected.

**4:** For Data Input: This parameter must be longer than t<sub>SP</sub>. If this parameter is too long, the Data Input Setup (T<sub>SU: DAT</sub>) or Clock Low time (T<sub>LOW</sub>) can be affected.  
For Data Output: This parameter is characterized, and tested indirectly by testing T<sub>AA</sub> parameter.

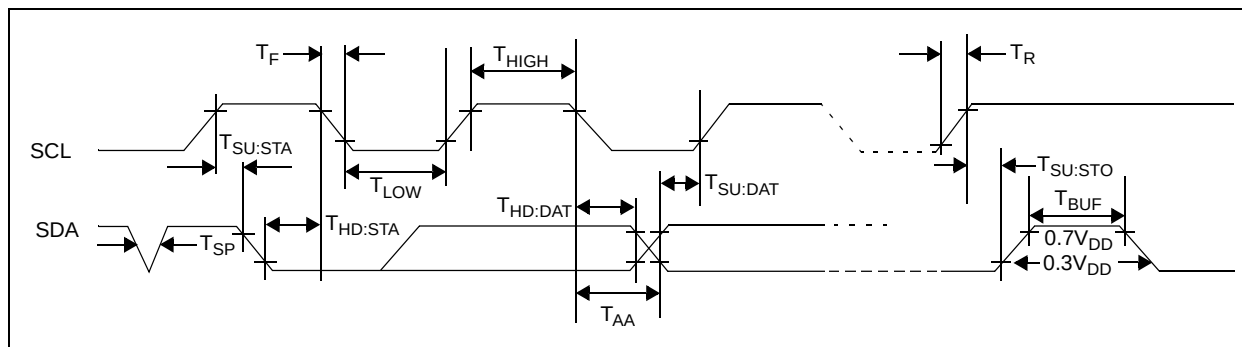


**FIGURE 5-7:** I<sup>2</sup>C Bus Timing Data.

## 6.0 BASIC APPLICATION CONFIGURATION

The MCP3421 can be used for various precision analog-to-digital converter applications. The device operates with very simple connections to the application circuit. The following sections discuss the examples of the device connections and applications.

### 6.1 Connecting to the Application Circuits

#### 6.1.1 BYPASS CAPACITORS ON $V_{DD}$ PIN

For an accurate measurement, the application circuit needs a clean supply voltage and must block any noise signal to the MCP3421 device. [Figure 6-1](#) shows an example of using two bypass capacitors (a 10  $\mu\text{F}$  tantalum capacitor and a 0.1  $\mu\text{F}$  ceramic capacitor) on the  $V_{DD}$  line of the MCP3421. These capacitors are helpful to filter out any high frequency noises on the  $V_{DD}$  line and also provide the momentary bursts of extra currents when the device needs from the supply. These capacitors should be placed as close to the  $V_{DD}$  pin as possible (within one inch). If the application circuit has separate digital and analog power supplies, the  $V_{DD}$  and  $V_{SS}$  of the MCP3421 device should reside on the analog plane.

#### 6.1.2 CONNECTING TO $I^2C$ BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP3421 are open-drain configurations. These pins require a pull-up resistor as shown in [Figure 6-1](#). The value of these pull-up resistors depends on the operating speed and loading capacitance of the  $I^2C$  bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus. Therefore, it can limit the bus operating speed. The lower value of resistor, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long bus line or high number of devices connected to the bus, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 5 k $\Omega$  and 10 k $\Omega$  ranges for standard and fast modes.

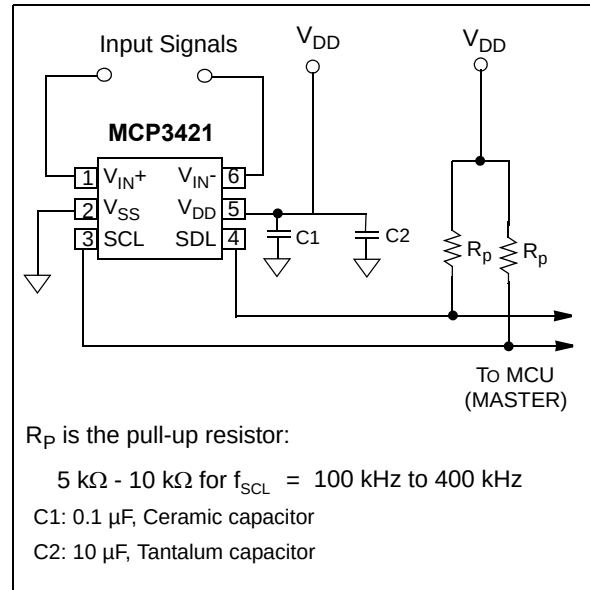


**FIGURE 6-1:** Typical Connection Example.

The number of devices connected to the bus is limited only by the maximum bus capacitance of 400 pF. The bus loading capacitance affects on the bus operating speed. [Figure 6-2](#) shows an example of multiple device connections.

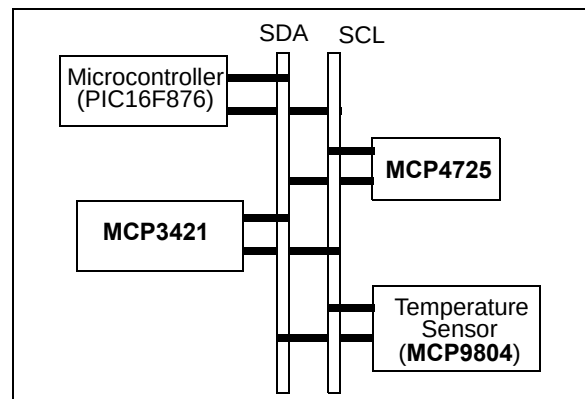


**FIGURE 6-2:** Example of Multiple Device Connection on  $I^2C$  Bus.

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## 6.1.3 DEVICE COMMUNICATION TEST

The user can test the communication between the Master (MCU) and the MCP3421 by simply checking an acknowledge response from the MCP3421 after sending a read or write command. Here is an example using [Figure 6-3](#):

- Set the  $\overline{R/W}$  bit "LOW" in the address byte.
- Check the ACK pulse after sending the address byte.

If the device acknowledges (ACK = 0), then the device is connected, otherwise it is not connected.

- Send a STOP bit.

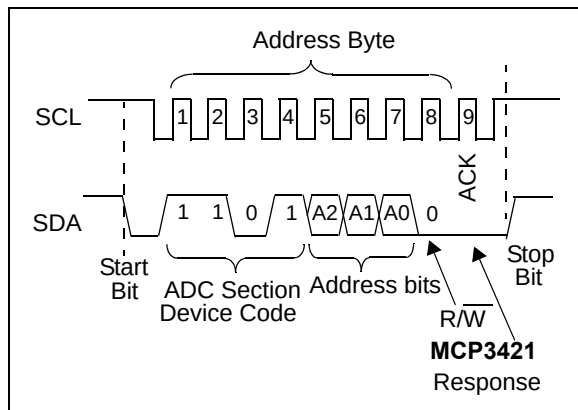


**FIGURE 6-3:** *I<sup>2</sup>C Bus Communications Test.*

## 6.1.4 DIFFERENTIAL AND SINGLE-ENDED CONFIGURATION

[Figure 6-4](#) shows typical connection examples for differential and single-ended inputs. Differential input signals are connected to the  $V_{IN+}$  and  $V_{IN-}$  input pins. For the single-ended input, the input signal is applied to one of the input pins (typically connected to the  $V_{IN+}$  pin) while the other input pin (typically  $V_{IN-}$  pin) is grounded. All device characteristics hold for the single-ended configuration, but this configuration loses one bit resolution because the input can only stand in positive half scale. Refer to **Section 4.9 "Digital Output Codes and Conversion to Real Values"**.

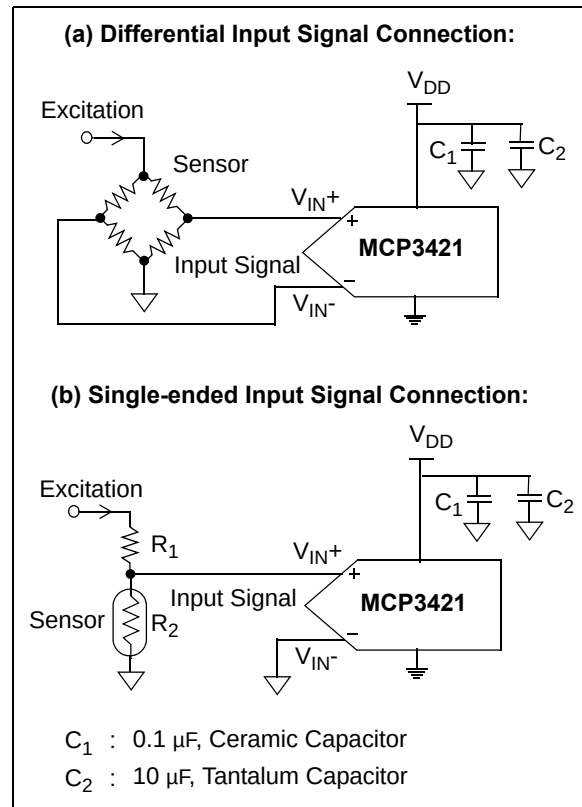


**FIGURE 6-4:** *Differential and Single-Ended Input Connections.*

## 6.2 Application Examples

### 6.2.1 VOLTAGE MEASUREMENT

The MCP3421 device can be used in a broad range of sensor and data acquisition applications.

Figure 6-5 shows a circuit example measuring the battery voltage. When the input voltage is greater than the internal reference voltage ( $V_{REF} = 2.048V$ ), it needs a voltage divider circuit to prevent the output code from being saturated. In the example,  $R_1$  and  $R_2$  form a voltage divider. The  $R_1$  and  $R_2$  are set to yield  $V_{IN}$  to be less than the internal reference voltage ( $V_{REF} = 2.048V$ ).

If the input voltage range is much less than the internal reference voltage, the voltage divider at the input pin is not needed, and the user may use the internal PGA with a gain of up to 8.

When the voltage divider or internal PGA is used for the input signal, these factor must be taken into account when the user converts the output codes to the actual input voltage.

Find the Microchip Application Note AN1156 for the input voltage and current measurement using the MCP342X device family. The MCU firmware is well documented in the reference.

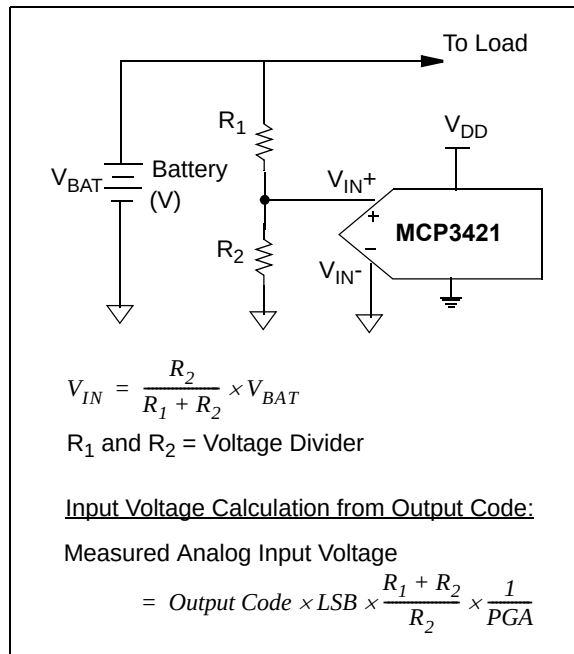


**FIGURE 6-5:** Battery Voltage Measurement.

### 6.2.2 CURRENT MEASUREMENT

Figure 6-6 shows a circuit example of current measurement. For the current measurement, the device measures the voltage across the current sensor, and converts it to current by dividing the measured voltage by a known resistance value of the current sensor. The voltage drops across the sensor is waste. Therefore, the current measurement often prefers to use a current sensor with smaller resistance value, which, in turn, requires high resolution ADC device. The high precision MCP342x devices from Microchip Technology Inc. are suitable for the current measurement with low resistive current sensors. These devices can measure the input voltage as low as  $2 \mu V$  range (or current in  $\sim \mu A$  range) with 18 bit resolution and  $\text{PGA} = 8$  settings. The MSB (= sign bit) of the output code indicates the direction of the current.

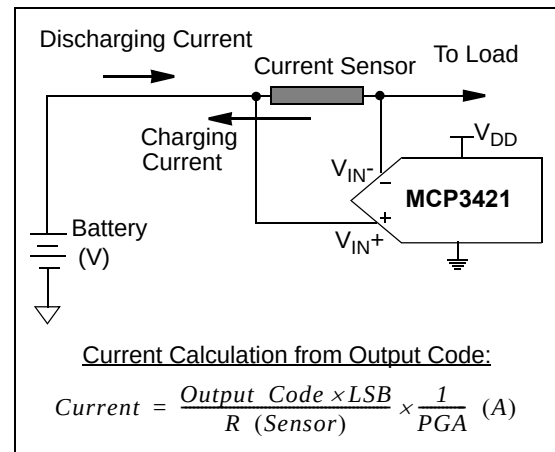


**FIGURE 6-6:** Battery Current Measurement.

# MCP3421

## 6.2.3 PRESSURE MEASUREMENT

Figure 6-7 shows an example of measuring the pressure using NPP301 (manufactured by GE NovaSensor). No external signal conditioning circuit is needed by utilizing its internal PGA. The pressure sensor output is 20 mV/V. This gives 100 mV of full scale output for  $V_{DD}$  of 5V (sensor excitation voltage). Equation 6-1 shows an example of calculating the number of output code for the full scale output of the NPP301.

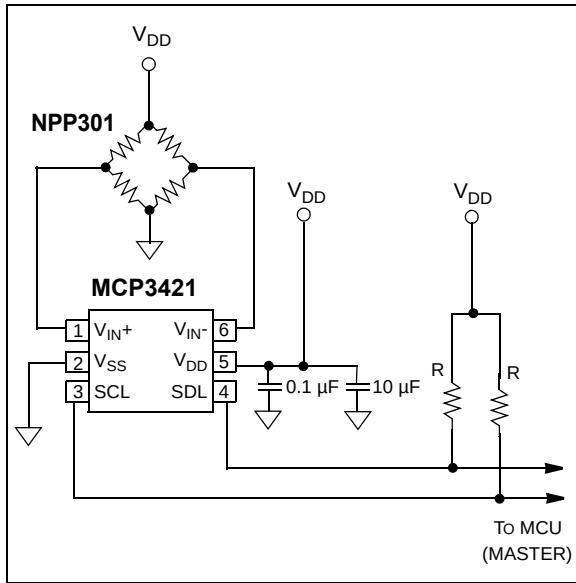


**FIGURE 6-7:** Example of Pressure Measurement.

### EQUATION 6-1: EXPECTED NUMBER OF OUTPUT CODE FOR NPP301 PRESSURE SENSOR

Expected Number of Output Code =  $\log_2 \left( \frac{100 \text{ mV}}{15.625 \mu\text{V}} \right)$

PGA

= 12.64 bits for PGA =1

= 13.64 bits for PGA =2

= 14.64 bits for PGA =4

= 15.64 bits for PGA =8

Where:

1 LSB = 15.625  $\mu\text{V}$  with 18 Bit configuration.

## 6.2.4 WHEATSTONE BRIDGE TYPE SENSORS WITH SIGNAL CONDITIONING

Wheatstone bridge is one of the most common configurations in the sensor applications. Strain gauges and pressure sensors are the common examples. When the sensor output signal is small and the common mode noise level is large, it needs a signal conditioning circuit between the sensor and the MCP3421. Figure 6-8 and Figure 6-9 show examples of using the MCP6V01 (high precision auto-zeroed Op Amp) for the sensor signal conditioning. Figure 6-8 shows the interface circuit with a minimum of components between the sensor and the MCP3421, but it is not symmetric, and therefore, the ADC input becomes a single ended. On the other hand, the Figure 6-9 has a symmetric and differential output, but requires more components.

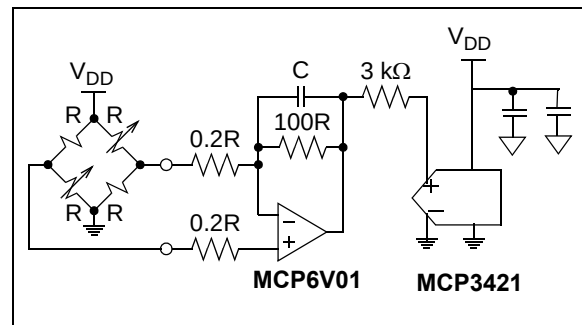


**FIGURE 6-8:** Simple Signal Conditioning Design with Asymmetric Circuit.

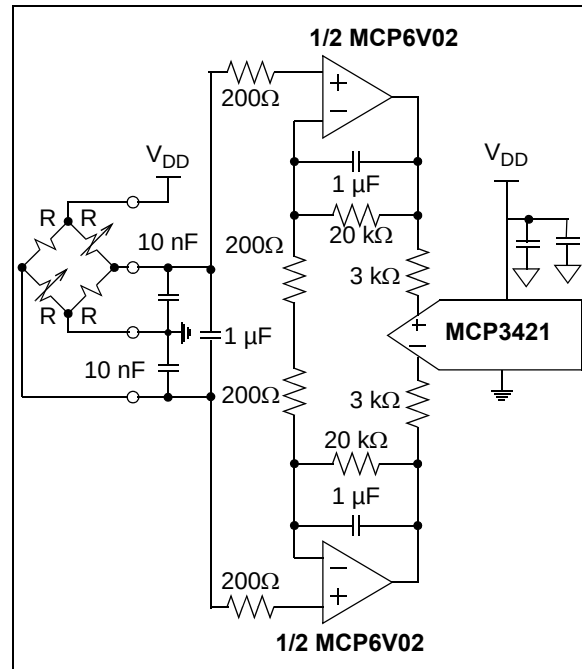


**FIGURE 6-9:** High Performance Signal Conditioning Design with Symmetric Circuit.

## 6.2.5 TEMPERATURE MEASUREMENT

Figure 6-10 shows an example of temperature measurement using a thermocouple sensor and the MCP9800 silicon temperature sensor. The MCP9800 is a high accuracy temperature sensor that can detect the temperature in the range of -55°C to 125°C with 1°C accuracy.

The type K thermocouple sensor senses the temperature at the hot junction ( $T_{HJ}$ ) with respect to the cold junction temperature (reference,  $T_{CJ}$ ). The temperature difference between the hot and cold junctions is represented by the voltage  $V_1$ . This voltage is then converted to digital codes by the MCP3421. In the circuit, the MCP9800 is used for cold junction compensation. The MCU computes the difference of the hot and cold junction temperatures, which is proportional to the hot junction temperature ( $T_{HJ}$ ).

With **Type K** thermocouple, it can measure temperature from 0°C to 1250°C degrees. The full scale output range of the **Type K** thermocouple is about 50 mV. This provides 40  $\mu\text{V}/^\circ\text{C}$  ( $= 50 \text{ mV}/1250^\circ\text{C}$ ) of measurement resolution. Equation 6-2 shows the measurement budget for thermocouple sensor signal using the MCP3421 device with 18 bits and PGA = 8 settings. With this configuration, it can detect the input signal level as low as approximately 2  $\mu\text{V}$ . The internal PGA boosts the input signal level eight times. The 40  $\mu\text{V}/^\circ\text{C}$  input from the thermocouple is amplified internally to 320  $\mu\text{V}/^\circ\text{C}$  before the conversion takes place. This results in 20.48 LSB/ $^\circ\text{C}$  output codes. This means there are about 20 LSB output codes (or about 4.32 bits) per 1°C of change in temperature.

### EQUATION 6-2: MEASUREMENT BUDGET FOR THERMOCOUPLE SENSOR

$$\begin{aligned} \text{Detectable Input Signal Level} &= 15.625 \mu\text{V}/\text{PGA} \\ &= 1.953125 \mu\text{V for PGA} = 8 \\ \text{Input Signal Level after gain of 8:} \\ &= (40 \mu\text{V}/^\circ\text{C}) \bullet 8 = 320 \mu\text{V}/^\circ\text{C} \\ \text{No. of LSB}/^\circ\text{C} &= \frac{320 \mu\text{V}/^\circ\text{C}}{15.625 \mu\text{V}} = 20.48 \text{ Codes}/^\circ\text{C} \\ \text{Where:} \\ 1 \text{ LSB} &= 15.625 \mu\text{V with 18-bit configuration} \end{aligned}$$

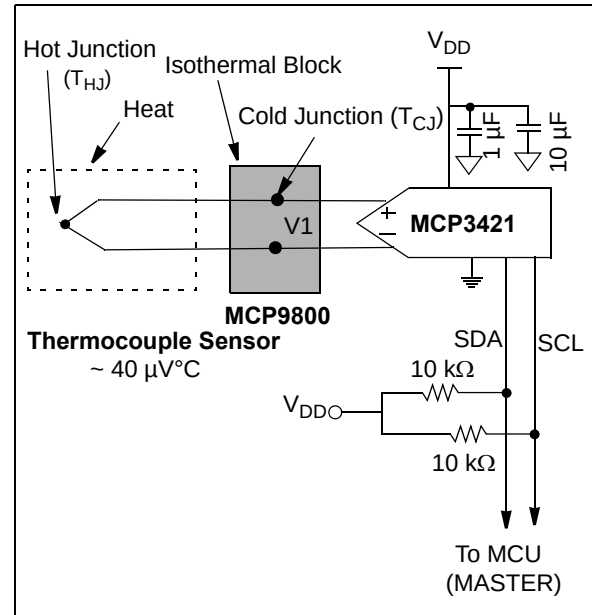


FIGURE 6-10: Example of Temperature Measurement.

Equation 6-3 shows an example of calculating the expected number of output code with various PGA gain settings for **Type K** thermocouple output.

### EQUATION 6-3: EXPECTED NUMBER OF OUTPUT CODE FOR TYPE K THERMOCOUPLE

$$\begin{aligned} \text{Expected Number of Output Code} &= \log_2 \left( \frac{50 \text{ mV}}{\frac{15.625 \mu\text{V}}{\text{PGA}}} \right) \\ &= 11.6 \text{ bits for PGA} = 1 \\ &= 12.6 \text{ bits for PGA} = 2 \\ &= 13.6 \text{ bits for PGA} = 4 \\ &= 14.6 \text{ bits for PGA} = 8 \end{aligned}$$

Where:

$$1 \text{ LSB} = 15.625 \mu\text{V with 18-bit configuration.}$$

NOTES:

## 7.0 DEVELOPMENT TOOL SUPPORT

### 7.1 MCP3421 Evaluation Boards

The MCP3421 Evaluation Board is available from Microchip Technology Inc. This board works with Microchip's PICKit™ Serial Analyzer. The user can simply connect any sensing voltage to the input test pads of the board and read conversion codes using the easy-to-use PICKit™ Serial Analyzer. Refer to [www.microchip.com](http://www.microchip.com) for further information on this product's capabilities and availability.

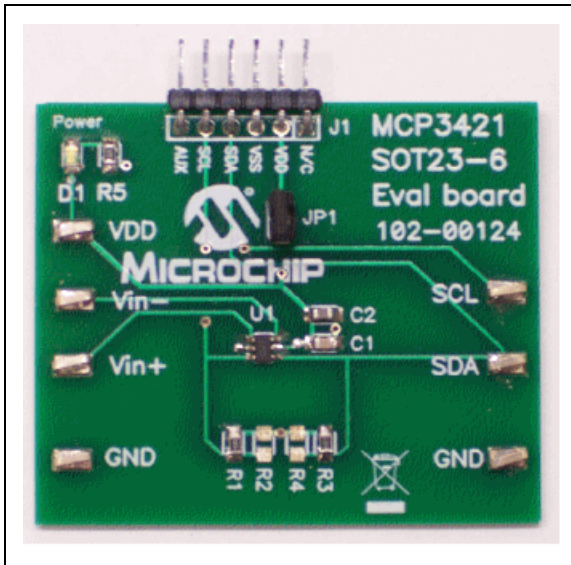


**FIGURE 7-1:** MCP3421 Evaluation Board.



**FIGURE 7-2:** Setup for the MCP3421 Evaluation Board with PICKit™ Serial Analyzer.

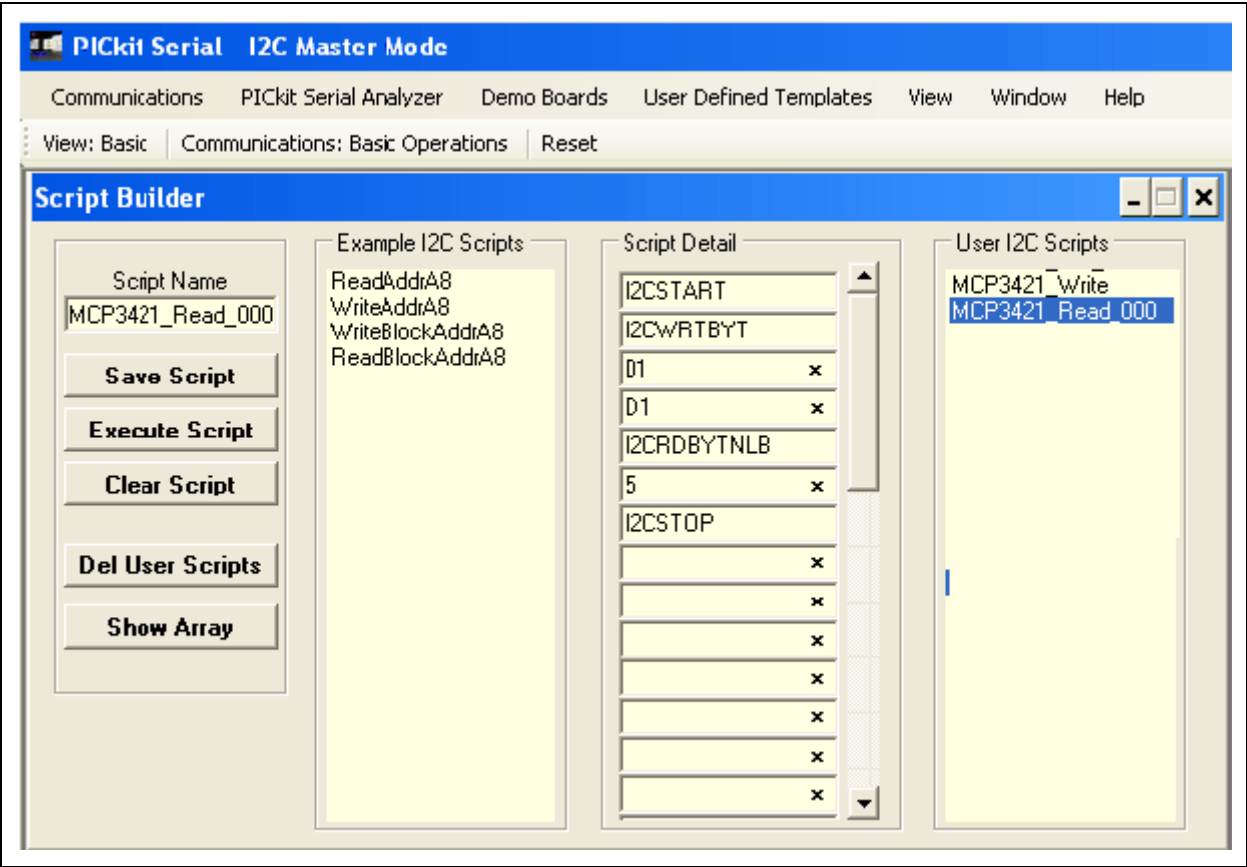
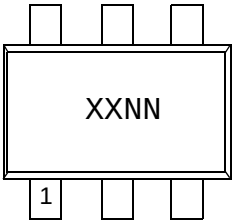


**FIGURE 7-3:** Example of PICKit™ Serial User Interface.

8.0 PACKAGING INFORMATION

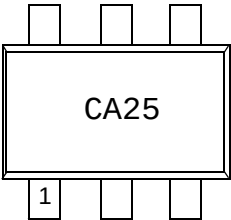
8.1 Package Marking Information

6-Lead SOT-23



| Part Number     | Address Option | Code |
|-----------------|----------------|------|
| MCP3421A0T-E/CH | A0 (000)       | CANN |
| MCP3421A1T-E/CH | A1 (001)       | CBNN |
| MCP3421A2T-E/CH | A2 (010)       | CCNN |
| MCP3421A3T-E/CH | A3 (011)       | CDNN |
| MCP3421A4T-E/CH | A4 (100)       | CENN |
| MCP3421A5T-E/CH | A5 (101)       | CFNN |
| MCP3421A6T-E/CH | A6 (110)       | CGNN |
| MCP3421A7T-E/CH | A7 (111)       | CHNN |

Example



**Legend:**

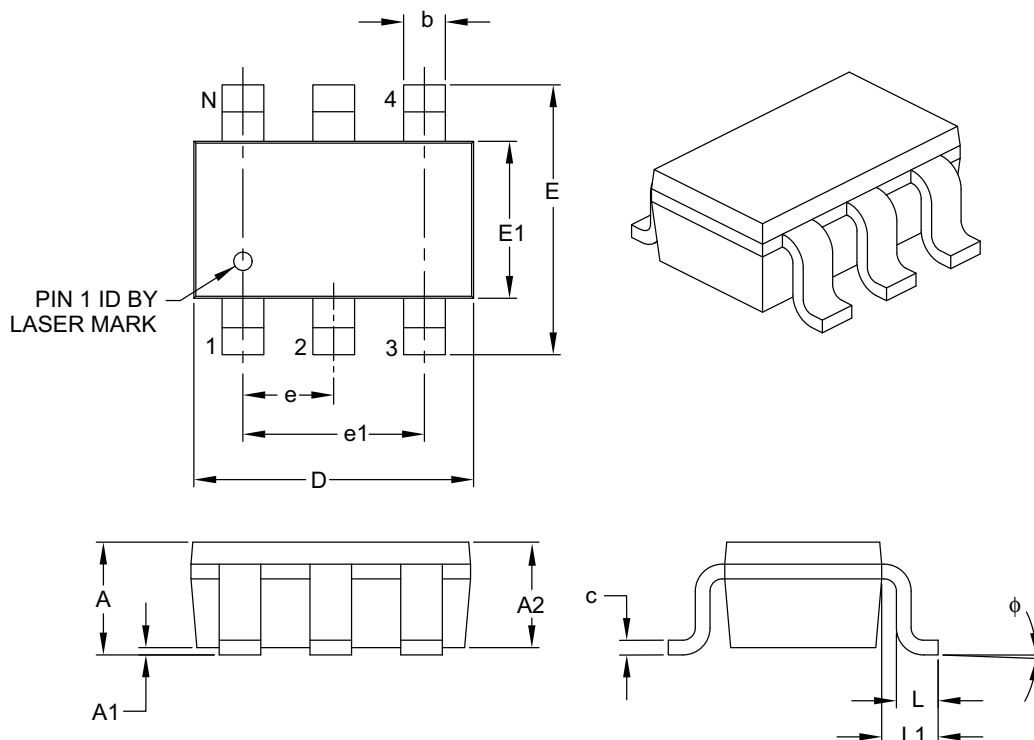
- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week '01')
- NNN Alphanumeric traceability code
- (e3) Pb-free JEDEC designator for Matte Tin (Sn)
- \* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# MCP3421

## 6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension                | Units | MILLIMETERS |     |      |
|--------------------------|-------|-------------|-----|------|
|                          |       | MIN         | NOM | MAX  |
| Number of Pins           | N     | 6           |     |      |
| Pitch                    | e     | 0.95 BSC    |     |      |
| Outside Lead Pitch       | e1    | 1.90 BSC    |     |      |
| Overall Height           | A     | 0.90        | —   | 1.45 |
| Molded Package Thickness | A2    | 0.89        | —   | 1.30 |
| Standoff                 | A1    | 0.00        | —   | 0.15 |
| Overall Width            | E     | 2.20        | —   | 3.20 |
| Molded Package Width     | E1    | 1.30        | —   | 1.80 |
| Overall Length           | D     | 2.70        | —   | 3.10 |
| Foot Length              | L     | 0.10        | —   | 0.60 |
| Footprint                | L1    | 0.35        | —   | 0.80 |
| Foot Angle               | φ     | 0°          | —   | 30°  |
| Lead Thickness           | c     | 0.08        | —   | 0.26 |
| Lead Width               | b     | 0.20        | —   | 0.51 |

### Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

## APPENDIX A: REVISION HISTORY

### Revision E (August 2009)

The following is the list of modifications:

1. Updated **Section 4.1 “General Overview”**.
2. Added new section: **Section 4.5 “Input Voltage Range”**.
3. Restructured information in **Section 4.9 “Digital Output Codes and Conversion to Real Values”**.
4. Updated information in [Table 5-4](#) in **Section 5.0 “Using the MCP3421 Device”**.
5. Updated section **Section 6.0 “Basic Application Configuration”**.
6. Added new **Section 7.0 “Development Tool Support”**.
7. Updated drawings in **Section 8.0 “Packaging Information”**.

### Revision D (November 2007)

The following is the list of modifications:

1. Section 1.0 Electrical Characteristics: Changed Gain Error Drift typical from 5 to 15, and Maximum from 40 to —.

### Revision C (October 2007)

The following is the list of modifications:

1. Figure 5-4: Changed  $\overline{O/C}$  designation to  $\overline{O}/C$ .
2. Updated package outline drawing.
3. Updated revision history.

### Revision B (December 2006)

The following is the list of modifications:

1. Changes to Electrical Characteristics tables
2. Added characterization data
3. Changes to I<sup>2</sup>C Serial Timing Specification table
4. Change to Figure 5-7.
5. Updated package outline drawings

### Revision A (August 2006)

- Original Release of this Document.

NOTES:



# MCP3421

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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