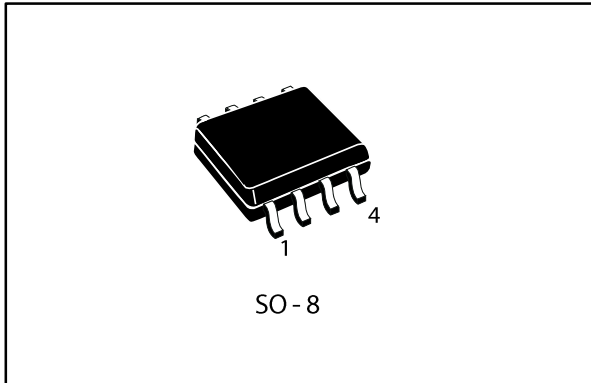


0.5 A high-side driver intelligent power switch

Datasheet - production data



- Output status LED driver
- Immunity against burst transient (IEC 61000-4-4)
- ESD protection (human body model ± 2 kV)

Description

The L6375S is a monolithic intelligent power switch in multipower BCD technology to drive inductive, capacitive or resistive loads with controlled output voltage slew rate and short-circuit protection. An internal clamping diode enables the fast demagnetization of inductive loads. Diagnostic for CPU feedback and extensive use of electrical protections make this device robust and suitable for industrial automation applications.

Features

- 0.5 A output current
- 8 to 35 V supply voltage range
- Internal current limit
- Non-dissipative short-circuit protection
- Thermal shutdown
- Undervoltage lockout with hysteresis
- Internal negative voltage clamping for fast demagnetization
- Differential inputs with large common mode range and threshold hysteresis
- Open load detection
- Two diagnostic outputs
- Open ground protection

Table 1: Device summary

| Order code | Temperature range | Package | Packing |
|------------|-------------------|---------|---------------|
| L6375S | -25 to +125 °C | SO-8 | Tube |
| L6375STR | | | Tape and reel |

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1 Pin connections

Figure 1: Pin connections (top view)

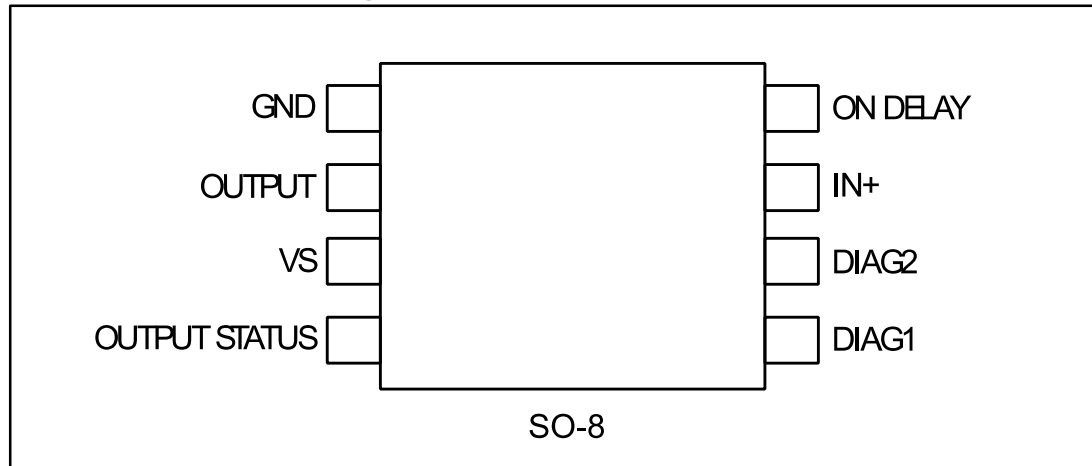


Table 2: Pin description

| Pin | Pin name | Function |
|-----|---------------|---|
| 1 | GND | Ground |
| 2 | OUTPUT | High-side output with built-in current limitation |
| 3 | VS | Supply voltage range with undervoltage monitoring |
| 4 | Output status | This current source output can drive a LED to signal the status of the output pin. The pin is active (source current) when the output pin is high |
| 5 | DIAG1 | Diagnostic1 output. This open drain reports the IC working conditions |
| 6 | DIAG2 | Diagnostic2 output. This open drain reports the IC working conditions |
| 7 | IN+ | Comparator inverting input |
| 8 | ON DELAY | Programmable ON time interval duration during short-circuit operation |

2 Maximum ratings

Table 3: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------------------------|---|----------------------------|------|
| V _s | Supply voltage (tw ≤ 10 ms) | 50 | V |
| | Supply voltage (DC) | 40 | V |
| V _{S- V_{OUT}} | Supply to output differential voltage | Internally limited | V |
| V _{od} | ON DELAY pin voltage | -0.3 to 7 | V |
| I _{od} | ON DELAY pin current | ± 1 | mA |
| I _{out} | Output current | Internally limited | A |
| V _{out} | Output voltage | Internally limited | V |
| E _i | Energy inductive load: T _J = 85 °C | 200 | mJ |
| P _{tot} | Power dissipation | Internally limited | W |
| V _{diag} | DIAGx pin voltage | -0.3 to 40 | V |
| I _{diag} | DIAGx pin current | -10 to 10 | mA |
| I _i | IN+ pin current | 20 | mA |
| V _i | IN+ pin voltage | -10 to V _s +0.3 | V |
| T _{op} | Ambient temperature, operating range | -25 to 85 | °C |
| T _J | Junction tmperature, operating range | -25 to 125 | °C |
| T _{stg} | Storage temperature | -55 to 150 | °C |

Table 4: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|-------------------------------------|-------------------------|------|
| R _{th(JA)} | Thermal resistance junction-ambient | 100 max. ⁽¹⁾ | °C/W |
| R _{th(JP)} | Thermal resistance junction-pins | 15 max. | |

Notes:

⁽¹⁾When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35 μm thick) connected to all VCC pins. Horizontal mounting and no artificial air flow.

3 Electrical characteristics

$V_S = 24\text{ V}$; $T_J = -25\text{ to }125\text{ }^\circ\text{C}$, unless otherwise specified.

Table 5: Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|--|--|------|------|-----------|---------------|
| V_{smin} | Supply voltage for valid diagnostic | $I_{diag} \geq 0.5\text{ mA}$; $V_{diag} = 1.5\text{ V}$ | 4 | | 35 | V |
| V_S | Operative supply voltage | | 8 | 24 | 35 | V |
| V_{sth1} | Undervoltage threshold 1 | | 7 | 7.5 | 8 | V |
| V_{sth2} | Undervoltage threshold 2 | | 6.5 | 7 | 7.5 | V |
| V_{shys} | Undervoltage hysteresis | | 300 | 500 | 700 | mV |
| I_q | Quiescent current | Output open | | 800 | | μA |
| I_{qo} | | Output on | | 1.6 | | mA |
| V_{ith} | IN+ pin threshold voltage | | 0.8 | 1.3 | 2 | V |
| V_{iths} | IN+ pin threshold hysteresis | | 50 | | 400 | mV |
| V_{il} | IN+ pin low level voltage | | -7 | | 0.8 | V |
| V_{ih} | IN+ pin high level voltage | $V_S < 18\text{ V}$ | 2 | | $V_S - 3$ | V |
| | | $V_S > 18\text{ V}$ | 2 | | 15 | |
| I_{ib} | IN+ pin bias current | $V_i = -7\text{ to }15\text{ V}$ | -250 | | 250 | μA |
| I_{dch} | Delay capacitor charging current | ON DELAY pin shorted-to-ground | | 2.5 | | μA |
| V_{don} | Output voltage drop | $I_{out} = 500\text{ mA}$; $T_J = 25\text{ }^\circ\text{C}$ | | 200 | 280 | mV |
| | | $T_J = 125\text{ }^\circ\text{C}$ | | 320 | 440 | |
| | | $I_{out} = 625\text{ mA}$; $T_J = 25\text{ }^\circ\text{C}$ | | 250 | 350 | |
| | | $T_J = 125\text{ }^\circ\text{C}$ | | 400 | 550 | |
| I_{olk} | Output leakage current | $V_i = \text{low}$; $V_{out} = 0$ | | | 100 | μA |
| V_{ol} | Output low-state voltage | $V_i = \text{high}$; pin floating | | 0.8 | 1.5 | V |
| V_{cl} | Internal voltage clamp ($V_S - V_{out}$) | $I_o = 200\text{ mA}$ single Pulsed = 300 ms | 48 | 53 | 58 | V |
| I_{sc} | Short-circuit output current | $V_S = 8\text{ to }35\text{ V}$; $R_l = 2\text{ }\Omega$ | 0.75 | 1.1 | 1.5 | A |
| I_{old} | Open load detection current | $V_i = V_{ih}$; $T_A = 0\text{ to }+85\text{ }^\circ\text{C}$ | 1 | 3 | 6 | mA |
| V_{oth1} | Output status threshold 1 voltage | | 4.5 | 5 | 5.5 | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|--|--|------|------|------|------------|
| V_{oth2} | Output status threshold 2 voltage | | 4 | 4.5 | 5 | V |
| V_{ohys} | Output status threshold hysteresis | | 300 | 500 | 700 | mV |
| I_{osd} | Output status source current | $V_{out} > V_{oth1}$; $V_{OS} = 2.5$ V | 2 | | 4 | mA |
| V_{osd} | Active output status driver drop voltage | $V_S - V_{OS}$; $I_{OS} = 2$ mA; $T_A = 0$ to $+85$ °C | | 1.5 | 3 | V |
| I_{oslk} | Output status driver leakage current | $V_{out} < V_{oth2}$; $V_{OS} = 0$ V; $V_S = 18$ to 35 V | | | 25 | μ A |
| V_{dgl} | Diagnostic drop voltage | D1 / D2 = L; $I_{diag} = 0.5$ mA | | 40 | | mV |
| | | D1 / D2 = L; $I_{diag} = 3$ mA | | 250 | | |
| I_{dglk} | Diagnostic leakage current | D1 / D2 = H; $0 < V_{dg} < V_S$ $V_S = 15.6$ to 35 V | | | 5 | μ A |
| $T_{max.}$ | Overtemperature upper threshold | | | 150 | | °C |
| T_{hys} | Overtemperature hysteresis | | | 20 | | °C |
| AC operation | | | | | | |
| t_r - t_f | Rise or fall time | $V_S = 24$ V; $R_i = 70$ Ω ; R_i to ground | | 20 | | μ s |
| t_d | Delay time | | | 5 | | |
| dV/dt | Slew rate (rising and falling edge) | | 0.7 | 1 | 1.5 | V/ μ s |
| t_{ON} | On-time during short-circuit condition | 50 pF $< C_{DON} < 2$ nF | | 1.28 | | μ s/pF |
| t_{OFF} | Off-time during short-circuit condition | | | 64 | | t_{ON} |
| $f_{max.}$ | Maximum operating frequency | | | 25 | | kHz |
| Source drain NDMOS diode | | | | | | |
| V_{fsd} | Forward on voltage | $I_{fsd} = 625$ mA | | 1 | 1.5 | V |
| I_{fp} | Forward peak current | $t_p = 10$ ms; duty cycle = 20% | | | 2 | A |
| t_{rr} | Reverse recovery time | $I_{fsd} = 625$ mA; $dI_{fsd}/dt = 25$ A/ μ s | | 200 | | ns |
| t_{fr} | Forward recovery time | | | 50 | | ns |

3.1 Schematic diagram

Figure 2: Block diagram

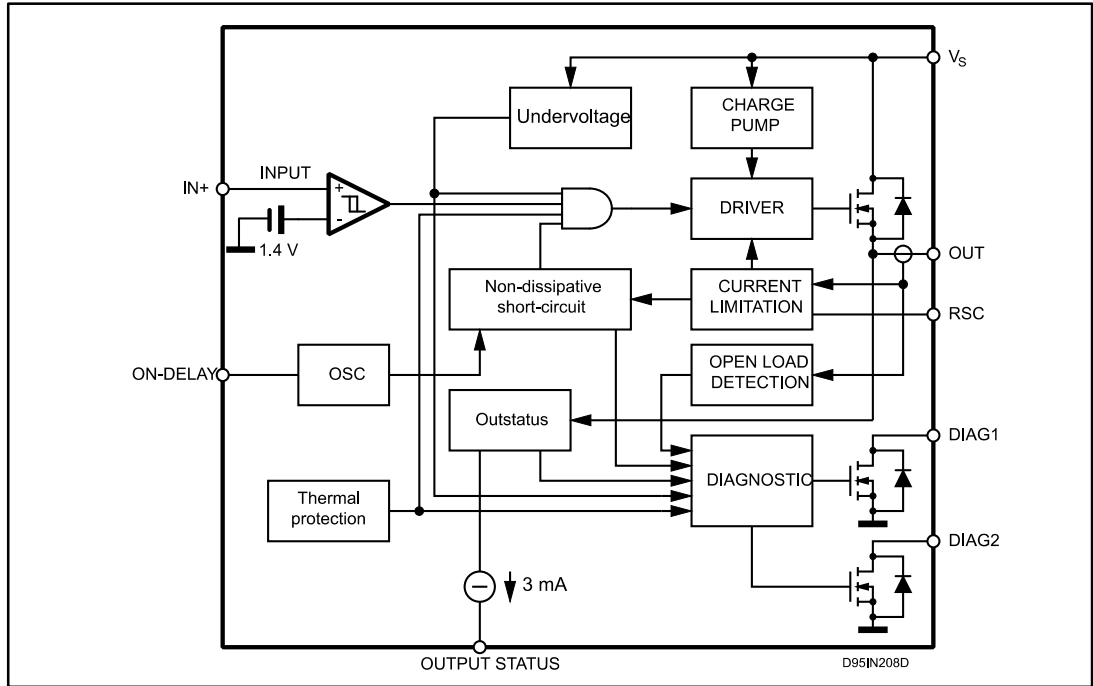
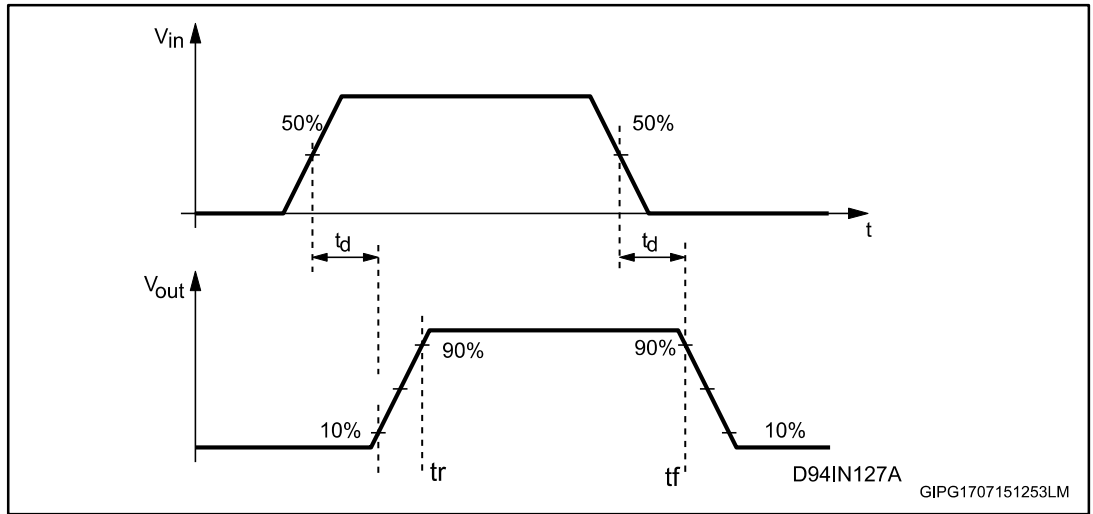


Figure 3: Switching waveforms



3.2 Input section

A single ended input TTL/CMOS compatible with a wide voltage range and high noise immunity (thanks to a built-in hysteresis) is available.

3.3 Overtemperature protection

On-chip overtemperature protection provides an excellent protection of the device in extreme conditions. Whenever the temperature, measured on a central portion of the chip, exceeds $T_{max.} = 150\text{ °C}$ (typical value) the device shuts down, and the DIAG2 output goes low. Normal operation is resumed as the chip temperature (normally after few seconds) falls below $T_{max.} - T_{hys} = 130\text{ °C}$ (typical value). The hysteresis avoids that an intermittent behavior occurs.

3.4 Undervoltage protection

The supply voltage operates correctly in a range from 8 to 35 V. Below 8 V the overall system has to be considered not reliable. To avoid any malfunctioning, the supply voltage is continuously monitored to provide an undervoltage protection. As V_s falls below $V_{sth} - V_{shys}$ (typically 7.5 V) the output power MOSFET switches off and DIAG1 and DIAG2 output go low. Normal operation is resumed as soon as V_s exceeds V_{sth} . The hysteretic behavior prevents intermittent operation at low supply voltage.

3.5 Overcurrent operation

In order to implement a short-circuit protection, the output power MOSFET is driven to linear mode to limit the output current to the I_{sc} value (1.1 A typical value).

This condition (current limited to the I_{sc} value) lasts for a T_{ON} time interval that can be set by a capacitor (C_{DON}) connected to the ON DELAY pin according to the following formula:

Equation 1:

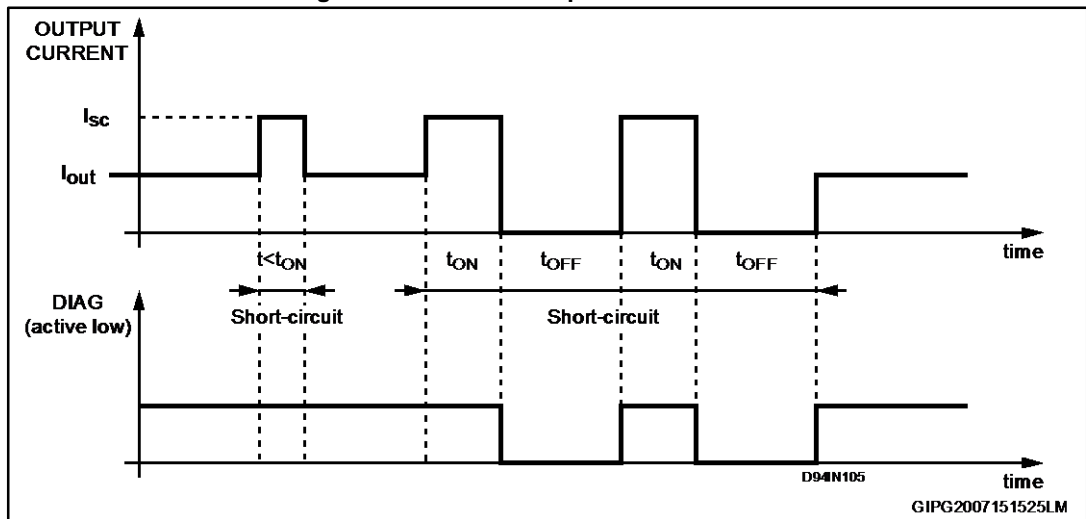
$$t_{ON} = 1.28 \mu\text{s/pF for } 50 \text{ pF} < C_{DON} < 2 \text{ nF}$$

After the t_{ON} interval has expired the output power MOSFET switches off for the t_{OFF} time interval:

Equation 2:

$$t_{OFF} = 64 \cdot t_{ON}$$

Figure 4: Short-circuit operation waveforms



When the t_{OFF} interval has expired, the output power MOSFET switches on. In this manner two conditions may occur:

- the overload is still present. In this case, the output power MOSFET is again driven to linear mode (limiting the output current to I_{SC}) for another t_{ON} , starting a new cycle
- the overload condition is removed, and the output power MOSFET is no longer driven to linear mode

Please, see the DIAG pin (see [Figure 4: "Short-circuit operation waveforms"](#)). This unique feature is called no-dissipative short-circuit protection and it ensures a very safe operation even in permanent overload conditions. The choice of the most appropriate value for the t_{ON} interval (the value of the C_{DON} capacitor) is very important, a delay (the t_{ON} itself) prevents the misleading short-circuit information is presented on the DIAG output, when capacitive loads are driven or incandescent lamp, a cold filament, has a very low resistive value. The non-dissipative short-circuit protection can be disabled (keeping $t_{ON} = 0$ but with the output current still limited to I_{SC} , and diagnostic disabled) by shorting to ground the ON DELAY pin.

3.6 Diagnostic logic

The operating conditions of the device are permanently monitored and the following occurrences are indicated by DIAG1/DIAG2 open drain output pins.

- Short-circuit vs. ground
- Short-circuit vs. V_S
- Undervoltage (UV)
- Overtemperature (OVT)
- Open load, if the output current is less than 3 mA (typical value)

3.7 Demagnetization of inductive loads

An internal Zener diode, limiting the voltage across the power MOSFET between 50 and 60 V (V_{cl}), provides safe and fast demagnetization of inductive loads without the external clamping devices. The maximum energy absorbed by an inductive load is specified as 200 mJ (at $T_J = 85\text{ }^\circ\text{C}$).

3.8 Diagnostic truth table

Table 6: Diagnostic truth table

| Diagnostic conditions | Input | Output | DIAG1 | DIAG2 |
|---|-------|--------|-------|-------|
| Normal operation | L | L | H | H |
| | H | H | H | H |
| Open load condition ($I_o < I_{old}$) | L | L | H | H |
| | H | H | L | H |
| Short to V_S | L | H | L | H |
| | H | H | L | H |
| Short-circuit to ground ($I_o = I_{sc}$) ^a (ON DELAY pin grounded) | H | X | H | H |
| | L | L | H | H |
| Output DMOS open | L | L | H | H |
| | H | L | L | H |
| Overtemperature | L | L | H | L |
| | H | L | H | L |
| Supply undervoltage ($V_S < V_{sth2}$) | L | L | L | L |
| | H | L | L | L |

^a A cold lamp filament or a capacitive load activates the current limiting circuit of the IPS, when the IPS is initially turned on.

4 Application circuits

Figure 5: Input comparator hysteresis

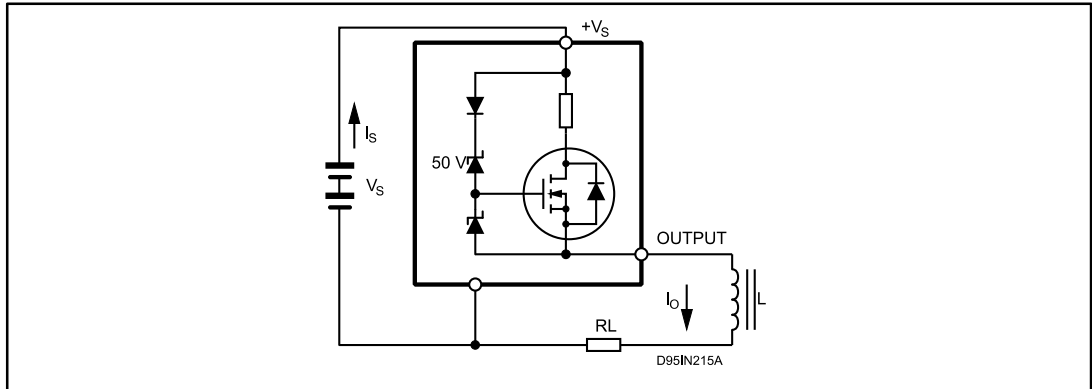


Figure 6: External demagnetization circuit (versus ground)

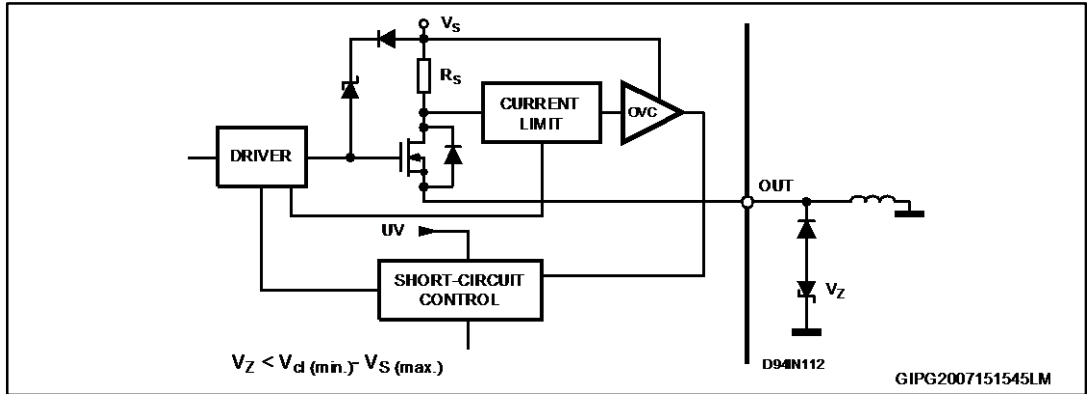


Figure 7: External demagnetization circuit (versus VS)

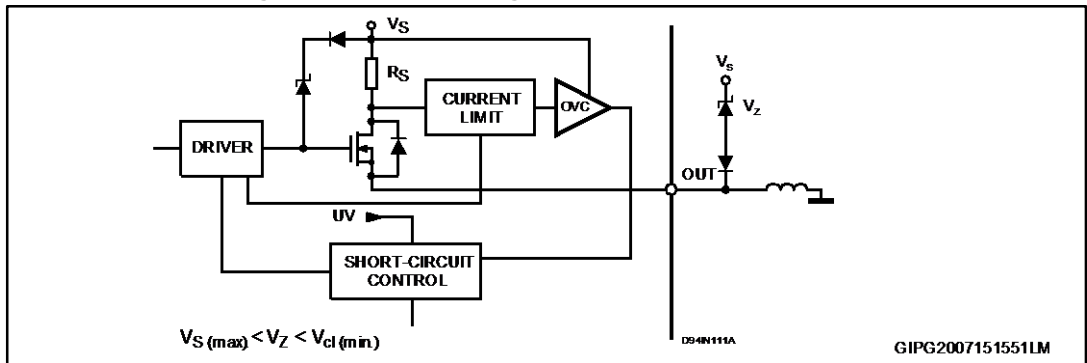
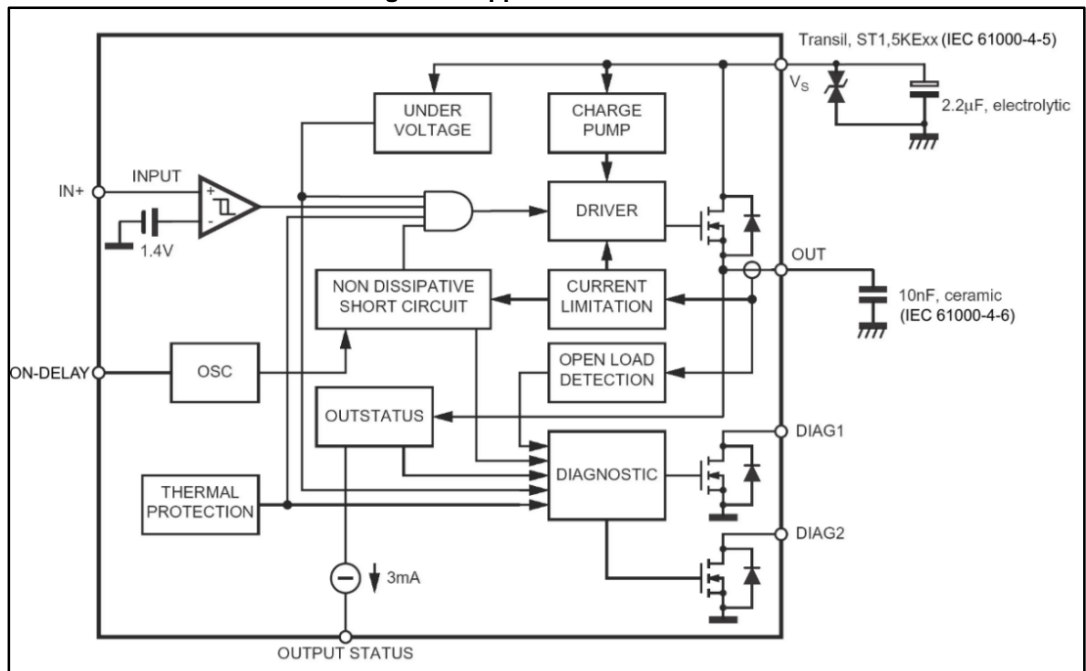


Figure 8: Application schematic



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 SO-8 package information

Figure 9: SO-8 package outline

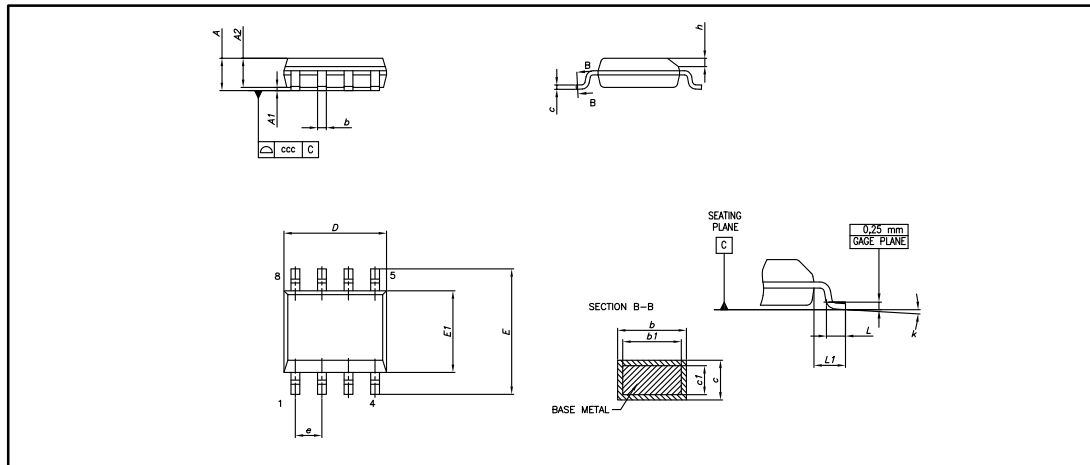
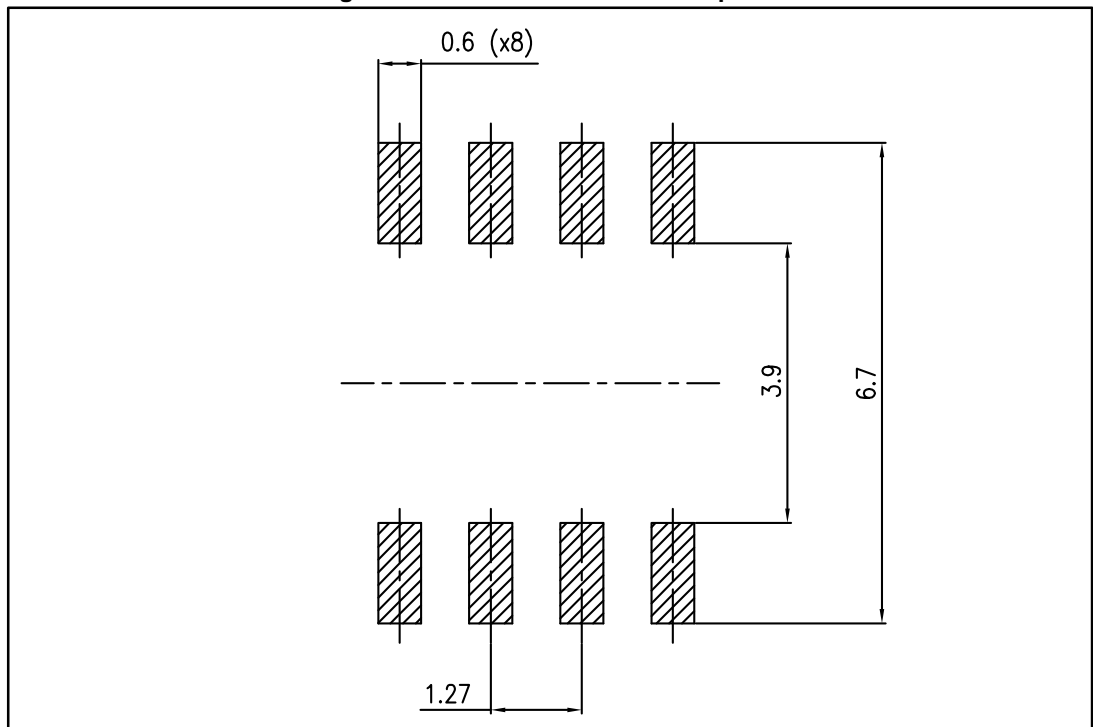


Table 7: SO-8 package mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

Figure 10: SO-8 recommended footprint



5.2 SO-8 packing information

Figure 11: SO-8 tape and reel outline

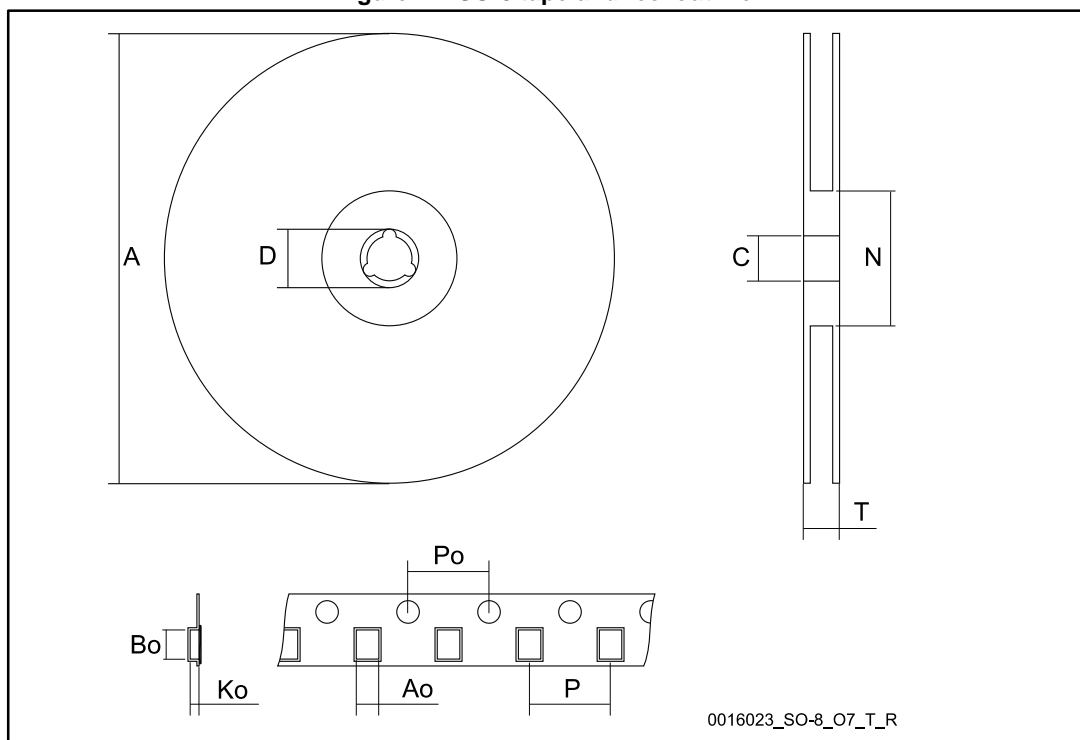


Table 8: SO-8 tape and reel mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 8.1 | | 8.5 |
| Bo | 5.5 | | 5.9 |
| Ko | 2.1 | | 2.3 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

Figure 12: SO-8 tube outline

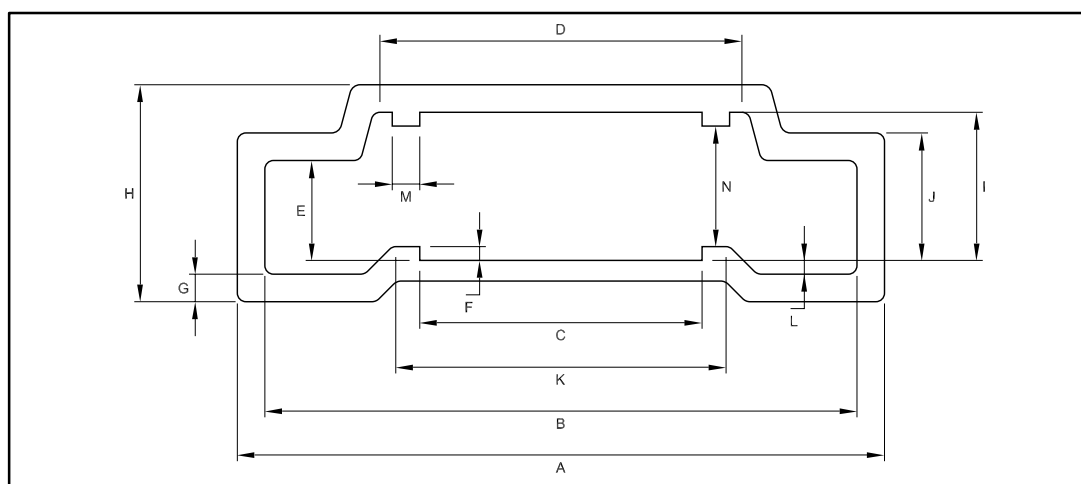


Table 9: SO-8 tube mechanical data

| Dim. | mm |
|------|-------------|
| A | 18.80 |
| B | 17.2 ± 0.2 |
| C | 8.20 ± 0.2 |
| D | 10.90 ± 0.2 |
| E | 2.90 ± 0.2 |
| F | 0.40 |
| G | 0.80 |
| H | 6.30 |
| I | 4.30 ± 0.2 |
| J | 3.7 ± 0.2 |
| K | 9.4 |
| L | 0.40 |
| M | 0.80 |
| N | 3.50 ± 0.2 |

6 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 18-Sep-2006 | 1 | Initial release. |
| 19-Jun-2007 | 2 | Truth table updated |
| 05-Jul-2007 | 3 | Typo in Table 5 |
| 16-Jul-2007 | 4 | Updated pinout |
| 15-Oct-2007 | 5 | Updated table 4 |
| 29-Jun-2009 | 6 | Updated table 5 |
| 12-Mar-2010 | 7 | Updated table 5 |
| 20-Dec-2011 | 8 | Updated table 5 |
| 23-Feb-2016 | 9 | Changed <i>Figure 1: "Pin connections (top view)"</i> . Updated <i>Table 3: "Absolute maximum ratings"</i> and <i>Table 5: "Electrical characteristics"</i> . |

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