Voltage Detector (Reset) IC Series for Automotive Application

Free Time Delay Setting CMOS Voltage Detector (Reset) IC

BD52xx-2M Series and BD53xx-2M Series

General Description

ROHM's BD52xx-2M and BD53xx-2M series are highly accurate, low current consumption Voltage Detector ICs with a capacitor controlled time delay. The lineup includes N-channel open drain output (BD52xx-2M) and CMOS output (BD53xx-2M) so that the users can select depending on the application. The devices are available for specific detection voltage ranging from 0.9V to 5.0V with 0.1V increment.
The time delay has ±30% accuracy in the overall operating temperature range of -40°C to 105°C.

Special Features

- AEC-Q100 Qualified (Note1)
- Nano Energy
- Delay Time Setting controlled by external capacitor
- Two output types (Nch open drain and CMOS output)
- Very small, lightweight and thin package
- Package SSOP5 is similar to SOT-23-5 (JEDEC)

(Note1: Grade 1)

Key Specifications

- Detection Voltage: 0.9V to 5.0V (Typ.) 0.1V step
- Ultra-Low Current Consumption: 270nA (Typ.)
- Time Delay Accuracy: ±30% (-40°C to +105°C,) (CT pin capacitor ≥ 1nF)

Special Characteristics

- Detection Voltage Accuracy:
  ±2.0%±12mV (V_{DET}=0.9V to 1.6V)
  ±2.5% (V_{DET}=1.7V to 5.0V)

Package

SSOP5: W(typ) x D(typ) x H(max) 2.90mm x 2.80mm x 1.25mm

Application

- Automotive (audio system, navigation system, etc.)

Application Circuit

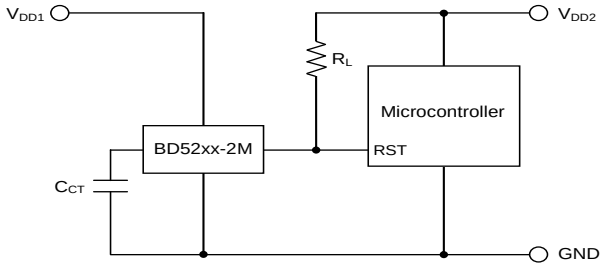


Figure 1. Open Drain Output Type
BD52xx-2M Series

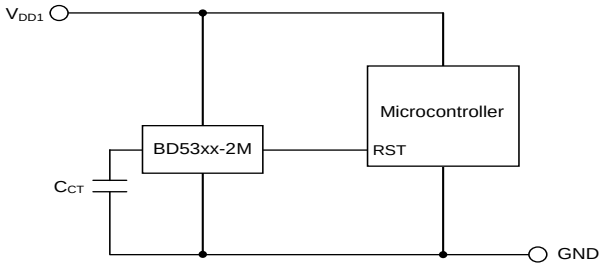
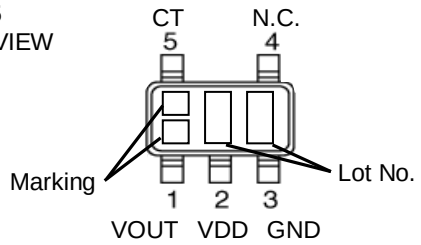


Figure 2. CMOS Output Type
BD53xx-2M Series

Pin Configuration

SSOP5
TOP VIEW



Pin Description

SSOP5		
PIN No.	Symbol	Function
1	VOUT	Output pin
2	VDD	Power supply voltage
3	GND	GND
4	N.C.	No connection pin
5	CT	Capacitor connection pin for output delay time setting

N.C. pin is electrically open and can be connected to either VDD or GND.

Nano Energy is a combination of technologies which realizes ultra low quiescent current operation.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Ordering Information

B D x x x x x - 2 M T R

- Part Number
- Output Type: 52 : Open Drain; 53 : CMOS
- Detection Voltage: 09 : 0.9V ⇩ 0.1V step 50 : 5.0V
- Package: G : SSOP5
- Product Rank: M : for Automotive
- Packaging and forming specification: TR : Embossed tape and reel

Lineup

Output Type	Open Drain		CMOS	
Detection Voltage	Marking	Part Number	Marking	Part Number
5.0V	1Z	BD5250	90	BD5350
4.9V	1Y	BD5249	89	BD5349
4.8V	1X	BD5248	88	BD5348
4.7V	1W	BD5247	87	BD5347
4.6V	1V	BD5246	86	BD5346
4.5V	1U	BD5245	85	BD5345
4.4V	1T	BD5244	84	BD5344
4.3V	1S	BD5243	83	BD5343
4.2V	1R	BD5242	82	BD5342
4.1V	1Q	BD5241	81	BD5341
4.0V	1P	BD5240	80	BD5340
3.9V	1N	BD5239	79	BD5339
3.8V	08	BD5238	78	BD5338
3.7V	07	BD5237	77	BD5337
3.6V	06	BD5236	76	BD5336
3.5V	05	BD5235	75	BD5335
3.4V	04	BD5234	74	BD5334
3.3V	03	BD5233	73	BD5333
3.2V	02	BD5232	72	BD5332
3.1V	01	BD5231	71	BD5331
3.0V	5G	BD5230	70	BD5330
2.9V	Z9	BD5229	69	BD5329
2.8V	Z8	BD5228	68	BD5328
2.7V	Z7	BD5227	67	BD5327
2.6V	XS	BD5226	66	BD5326
2.5V	XR	BD5225	65	BD5325
2.4V	24	BD5224	64	BD5324
2.3V	23	BD5223	63	BD5323
2.2V	22	BD5222	62	BD5322
2.1V	21	BD5221	61	BD5321
2.0V	20	BD5220	60	BD5320
1.9V	19	BD5219	59	BD5319
1.8V	18	BD5218	58	BD5318
1.7V	17	BD5217	57	BD5317
1.6V	16	BD5216	56	BD5316
1.5V	15	BD5215	55	BD5315
1.4V	14	BD5214	54	BD5314
1.3V	13	BD5213	53	BD5313
1.2V	12	BD5212	52	BD5312
1.1V	11	BD5211	51	BD5311
1.0V	10	BD5210	5F	BD5310
0.9V	09	BD5209	5E	BD5309

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Absolute Maximum Ratings (Ta=+25°C)

Parameter		Symbol	Limit	Unit
Power Supply Voltage		V_{DD}-GND	-0.3 to +7	V
Output Voltage	Nch Open Drain Output	V_{OUT}	GND-0.3 to +7	V
	CMOS Output		GND-0.3 to V_{DD}+0.3	
Output Current		Io	70	mA
Operating Temperature Range		Topr	-40 to +105	°C
Maximum Junction Temperature		Tjmax	+150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP5				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	40	30	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air).

*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Electrical Characteristics (Unless otherwise specified Ta=-40°C to +105°C, VDD=0.8V to 6V)

Parameter	Symbol	Condition	Limit			Unit
			Min	Typ	Max	
Detection Voltage	V_{DET}	V_{DET}=0.9V to 1.6V, V_{DD}=H→L, R_L=100kΩ	V_{DET}(T) ×0.98 -0.012	V_{DET}(T)	V_{DET}(T) ×1.02 +0.012	V
		V_{DET}=1.7V to 5.0V, V_{DD}=H→L, R_L=100kΩ	V_{DET} (T) ×0.975	V_{DET}(T)	V_{DET}(T) ×1.025	
Hysteresis Voltage	ΔV_{DET}	V_{DD}=L→H→L, R_L=100kΩ	V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.07	V
Circuit Current when ON	I_{DD1}	V_{DD}= V_{DET}-0.2V	-	0.23	1.00	µA
Circuit Current when OFF	I_{DD2}	V_{DD}= V_{DET}+0.5V	-	0.27	1.10	µA
Operating Voltage Range	V_{OPL}	V_{OL}≤0.4V, Ta=-40°C to 105°C, R_L=100kΩ	0.80	-	-	V
"Low" Output Voltage (Nch)	V_{OL}	V_{DD}=0.8V, ISINK = 0.17mA, V_{DET}=0.9V to 1.6V	-	-	0.4	V
		V_{DD}=1.2V, ISINK = 1.0mA, V_{DET}=1.7V to 5.0V	-	-	0.4	
		V_{DD}=2.4V, ISINK = 2.0mA, V_{DET}=2.7V to 5.0V	-	-	0.4	
"High" Output Voltage (Pch)	V_{OH}	V_{DD}=4.8V, ISOURCE=2.0mA, V_{DET}(0.9V to 4.2V)	V_{DD}-0.4	-	-	V
		V_{DD}=6.0V, ISOURCE=2.5mA, V_{DET}(0.9V to 5.0V)	V_{DD}-0.4	-	-	
Output Leak Current (BD52xx)	I_{LEAK}	V_{DD}= V_{DS}=6V	-	-	1.0	µA
Delay Time (L → H)	t_{PLH}	V_{OUT}＝GND→50%, CT=0.01µF Note 1 Note 2	38.9	55.5	72.1	ms

V_{DET}(T) : Standard Detection Voltage(0.9V to 5.0V, 0.1V step)
R_L: Pull-up resistor to be connected between V_{OUT} and power supply.
Note 1 t_{PLH} : V_{DD}=(V_{DET}(T)–0.1V) → (V_{DET}(T)+0.5V) for V_{DET}=0.9V to 1.2V
t_{PLH} : V_{DD}=(V_{DET}(T)–0.5V) → (V_{DET}(T)+0.5V) for V_{DET}=1.3V to 5.0V
Note 2 CT delay capacitor range: open to 4.7µF.

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Block Diagram

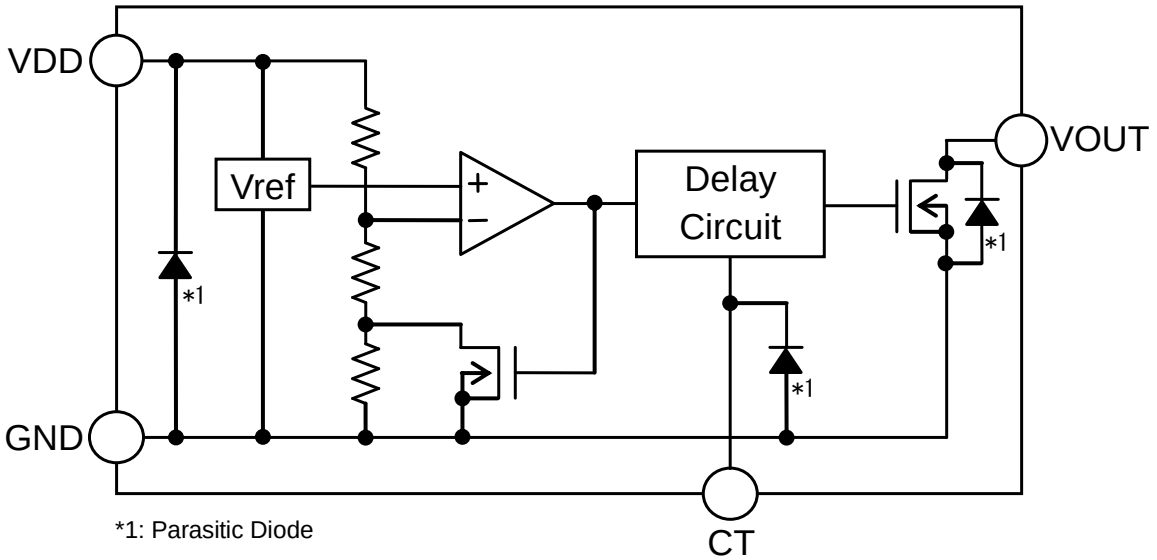

Figure 3. BD52xx-2M Series

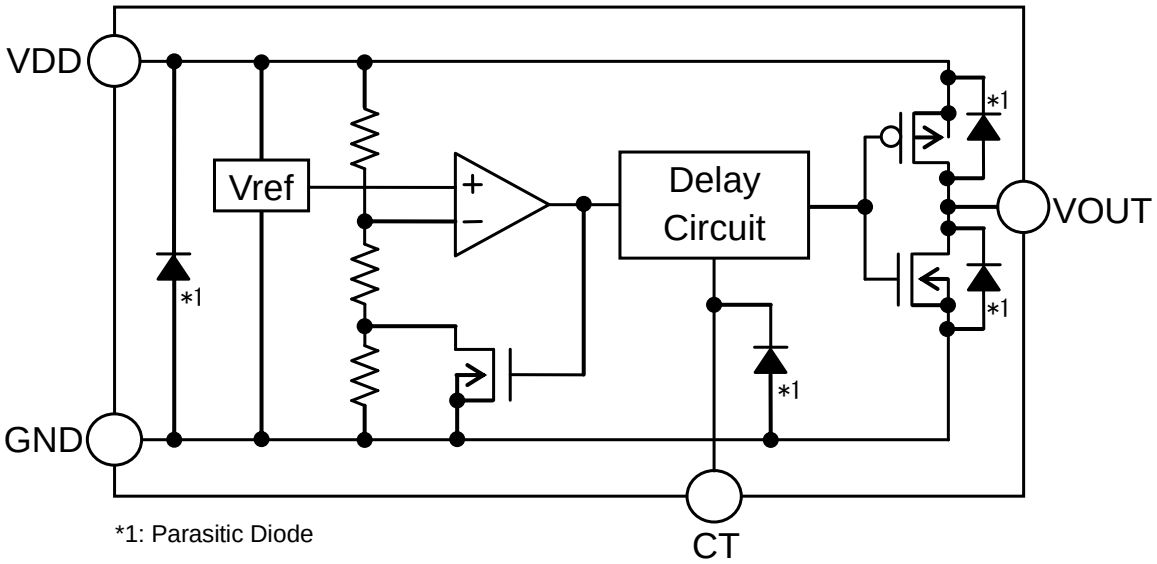

Figure 4. BD53xx-2M Series

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Typical Performance Curves

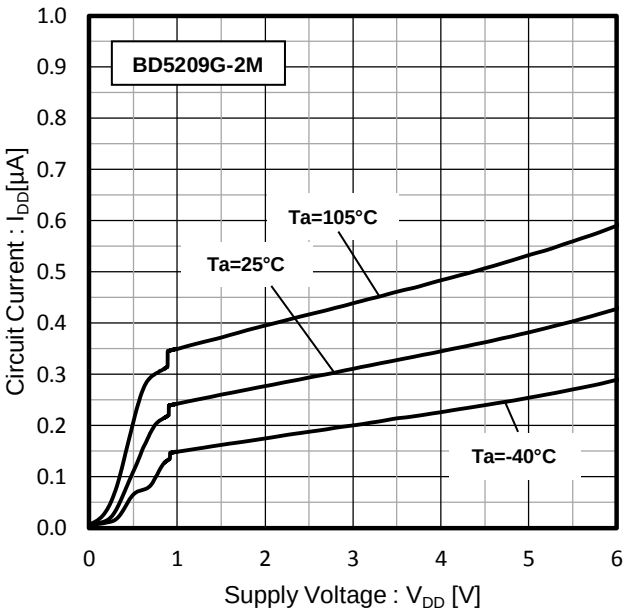

Figure 5. Circuit Current vs. V_{DD}

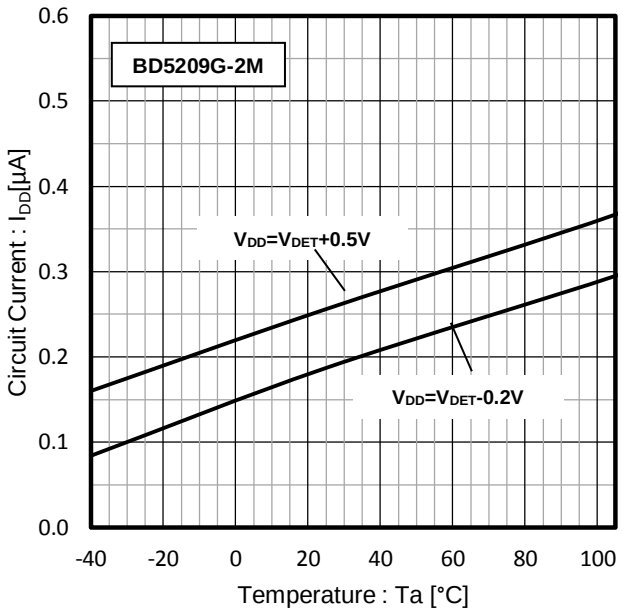

Figure 6. Circuit Current vs. Temp

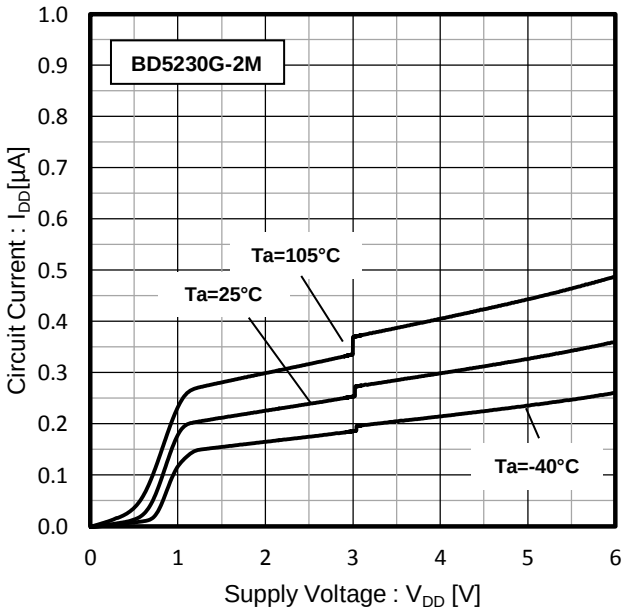

Figure 7. Circuit Current vs. V_{DD}

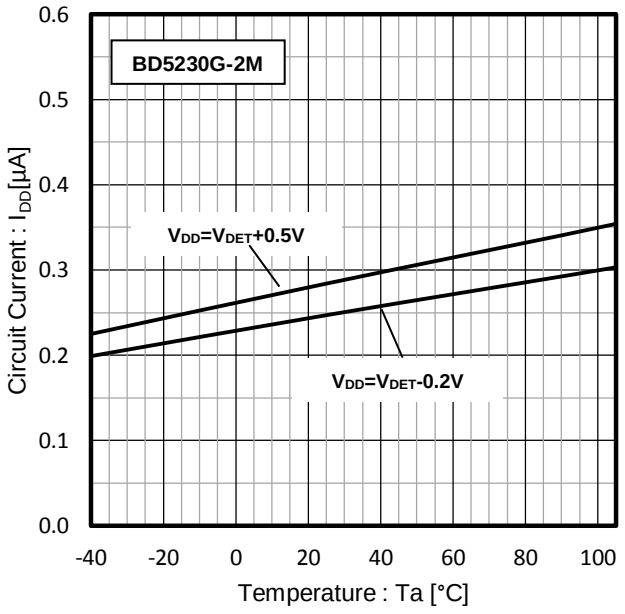

Figure 8. Circuit Current vs. Temp

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Typical Performance Curves - continued

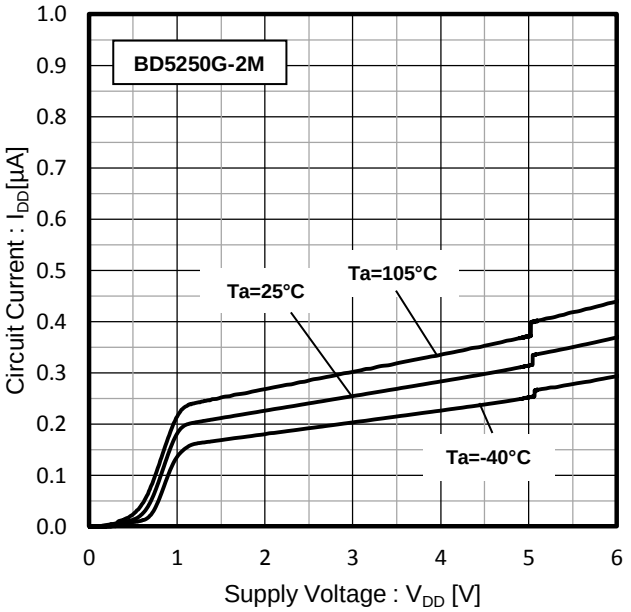

Figure 9. Circuit Current vs. V_{DD}

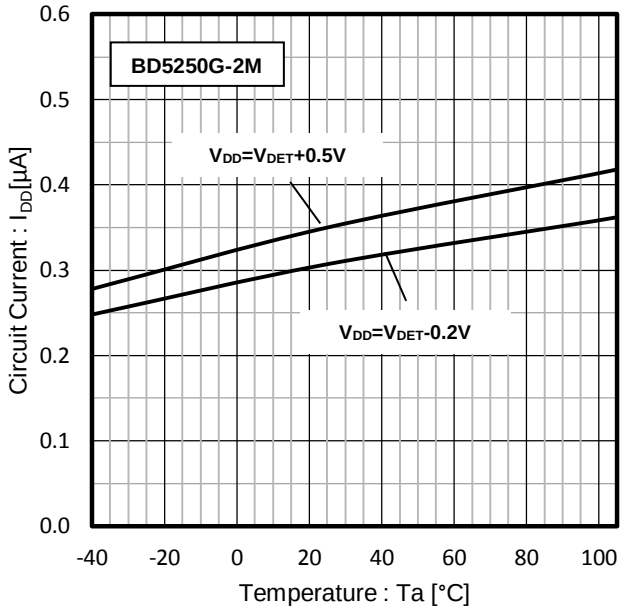

Figure 10. Circuit Current vs. Temp

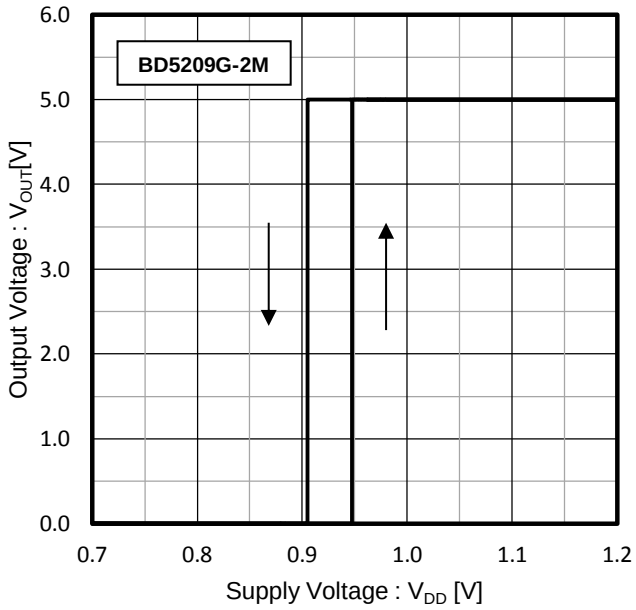

Figure 11. Detection Voltage

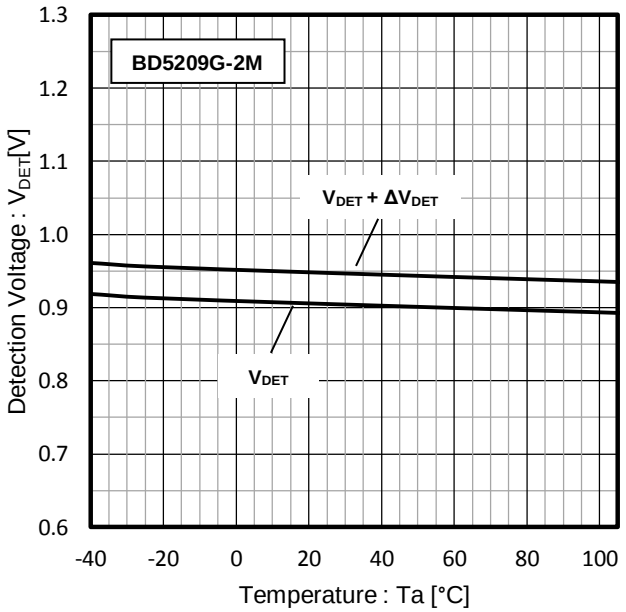

Figure 12. Detection Voltage and Release Voltage

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Typical Performance Curves - continued

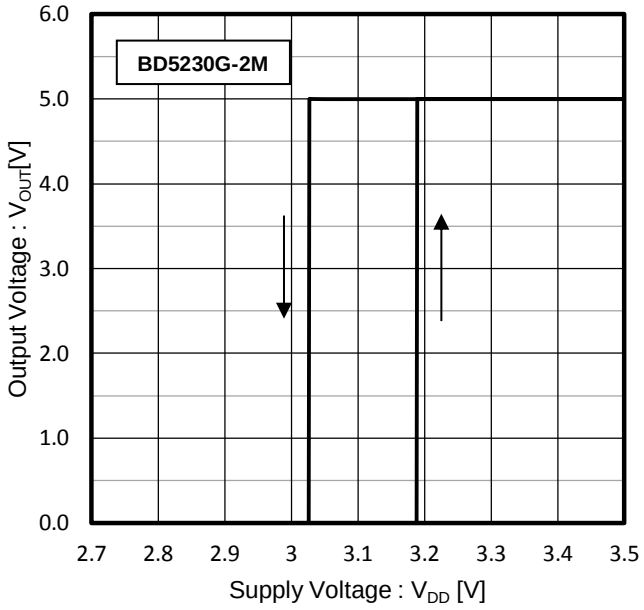

Figure 13. Detection Voltage

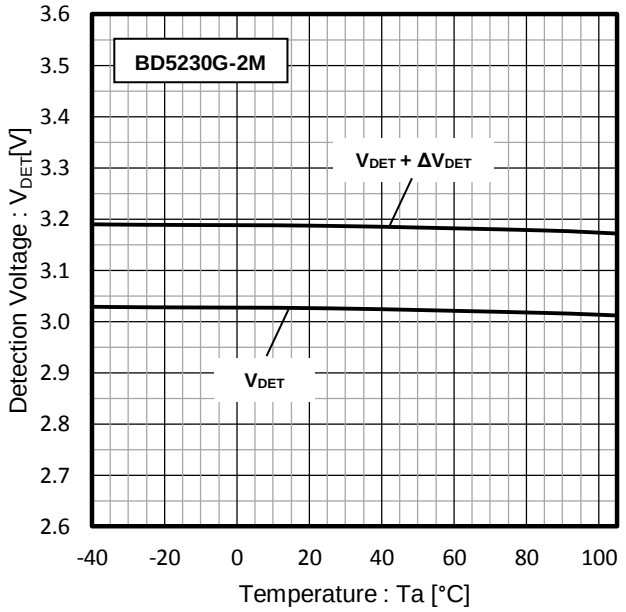

Figure 14. Detection Voltage and Release Voltage

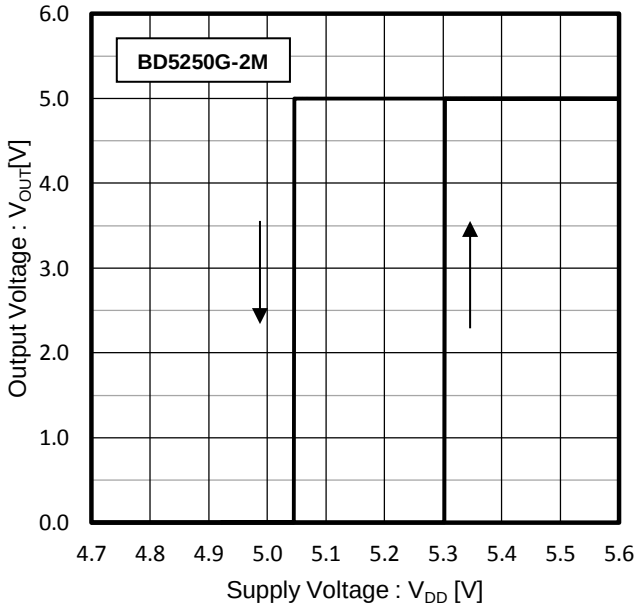

Figure 15. Detection Voltage

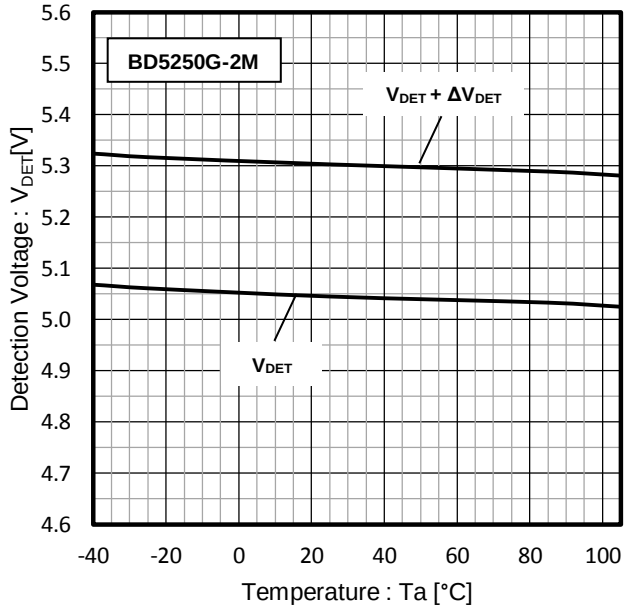

Figure 16. Detection Voltage and Release Voltage

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Typical Performance Curves - continued

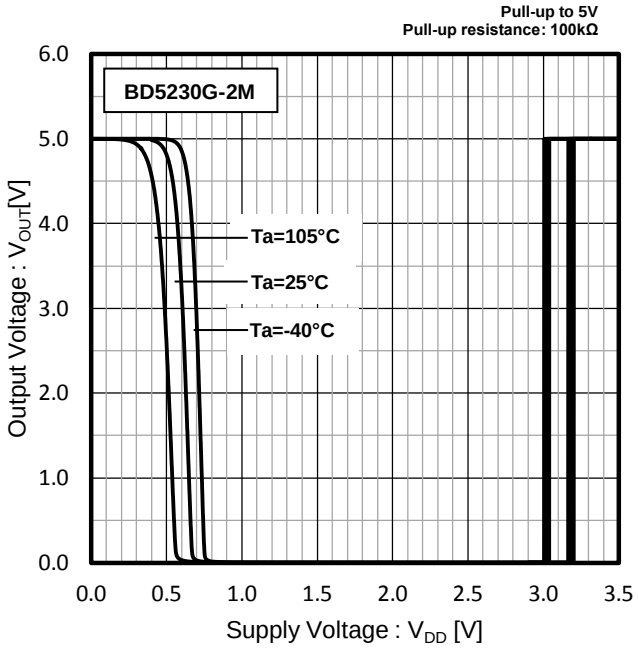

Figure 17. I/O Characteristics

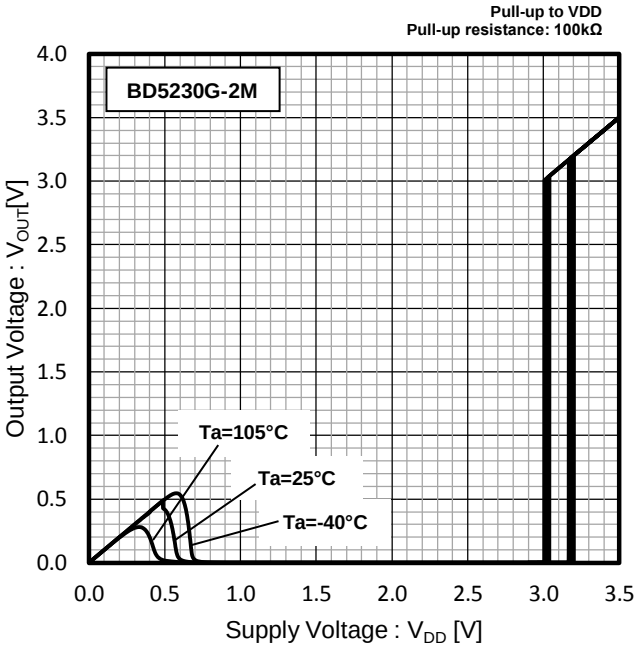

Figure 18. I/O Characteristics

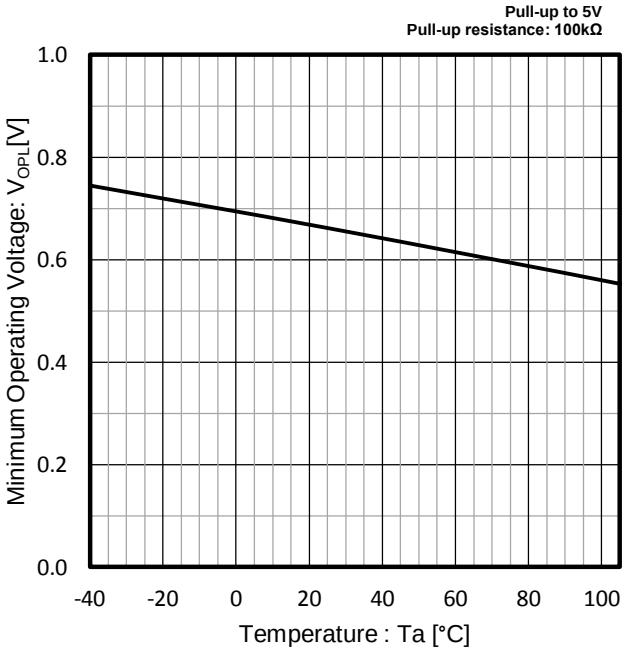

Figure 19. Operating Limit Voltage

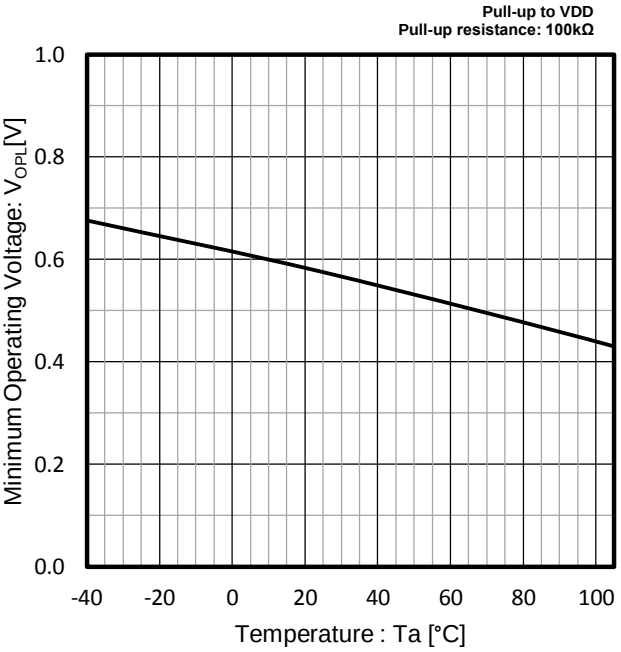

Figure 20. Operating Limit Voltage

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Typical Performance Curves - continued

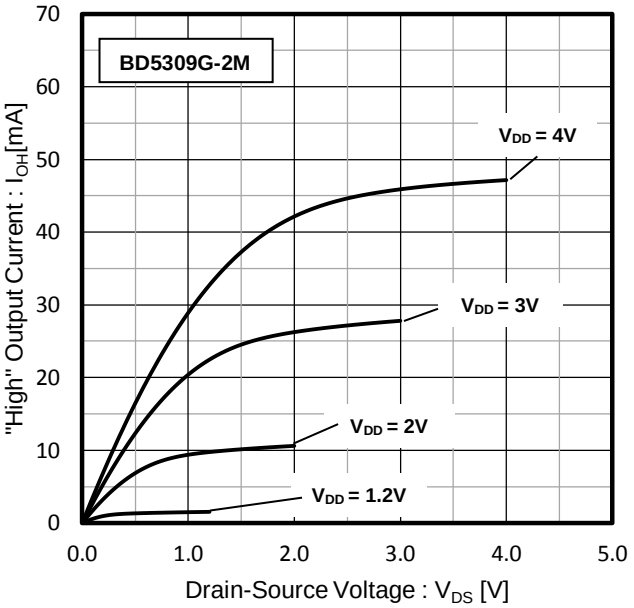

Figure 21. “High” Output Current

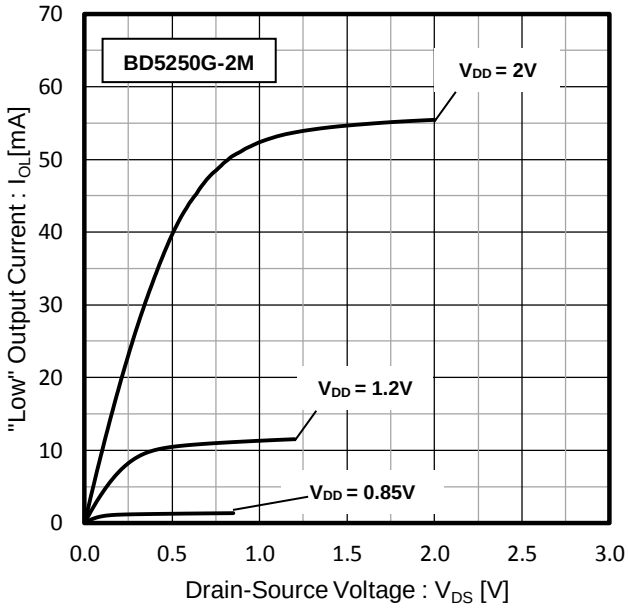

Figure 22. “Low” Output Current

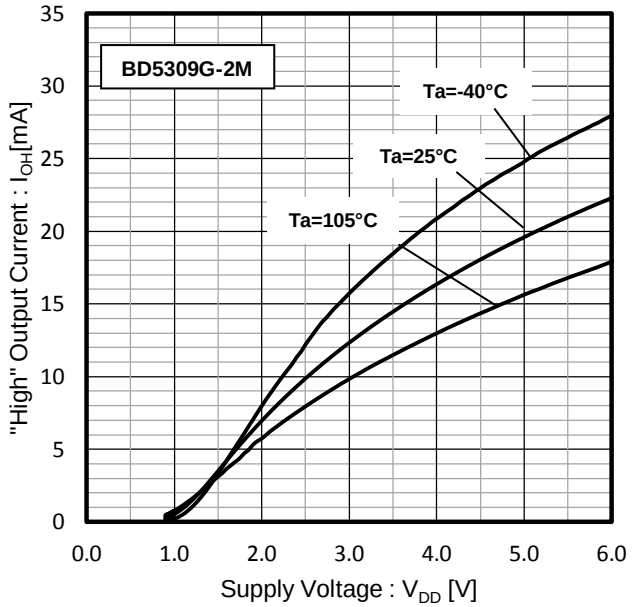

Figure 23. “High” Output Current (V_{DS}=0.5V)

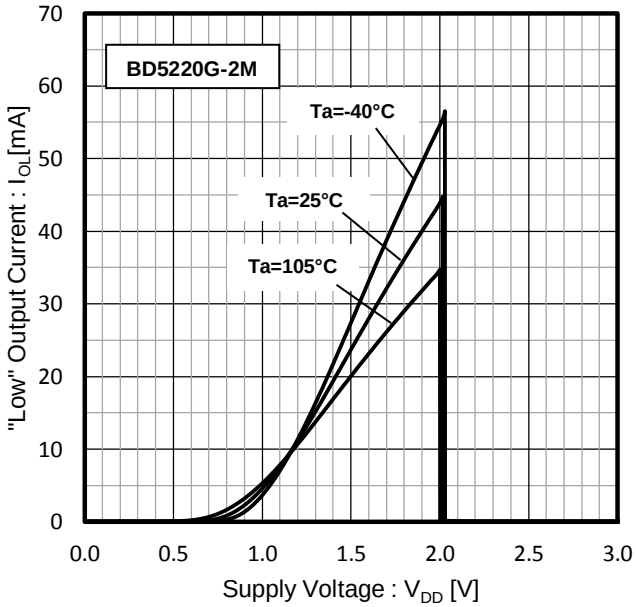

Figure 24. “Low” Output Current (V_{DS}=0.5V)

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Typical Performance Curves - continued

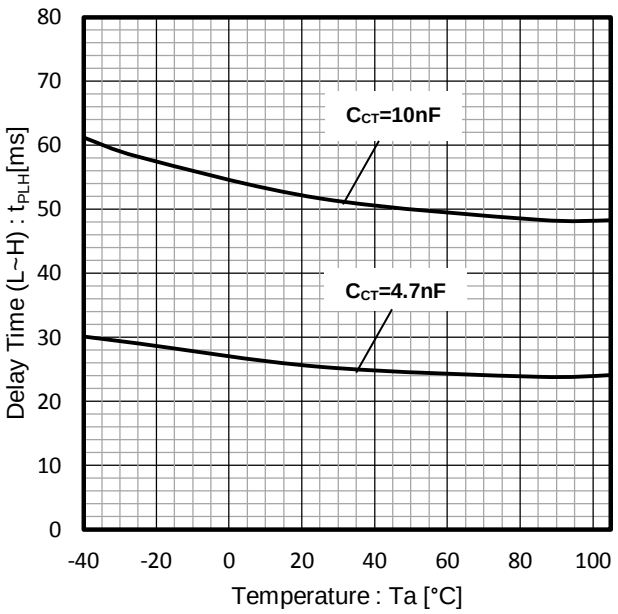

Figure 25. Output Delay Time (L to H)

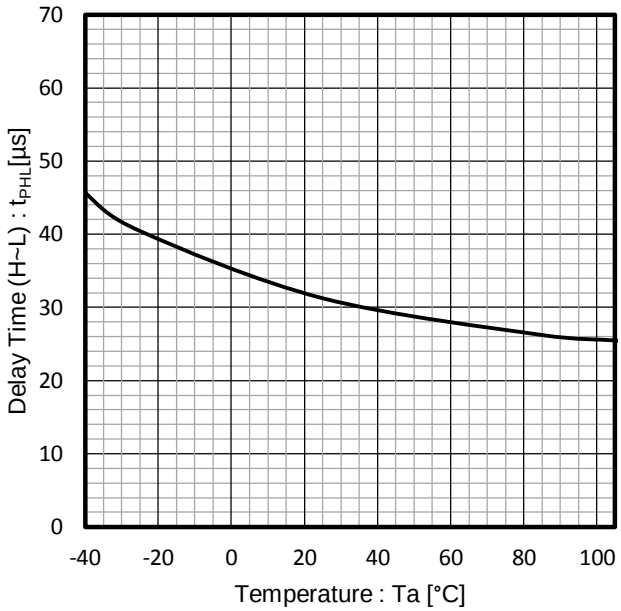

Figure 26. Output Delay Time (H to L)

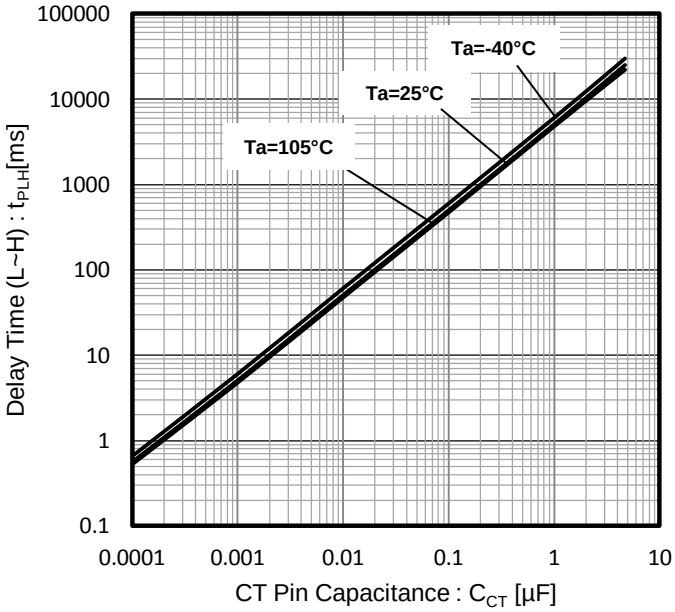

Figure 27. Output Delay Time (L to H)

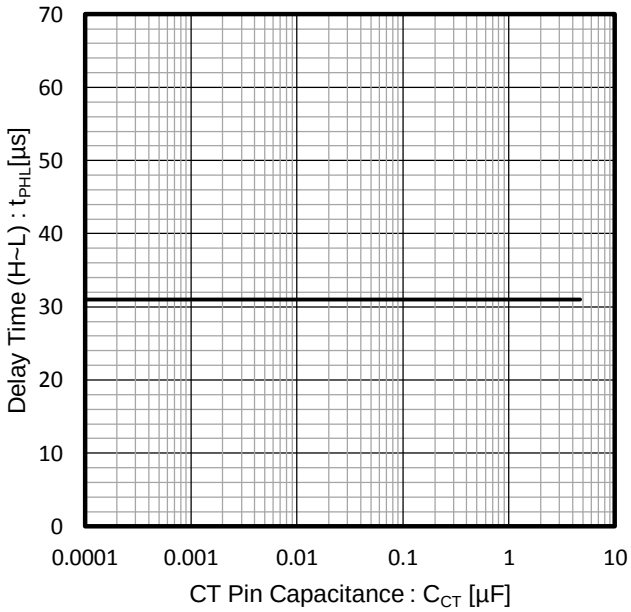

Figure 28. Output Delay Time (H to L)

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Application Information

1. Explanation of Operation

For both the open drain type (Figure 29) and the CMOS output type (Figure 30), the detection and release voltages are used as threshold voltages. When the voltage applied to the VDD pin reaches the applicable threshold voltage, the VOUT pin voltage switches from either "High" to "Low" or from "Low" to "High". BD52xx-2M series and BD53xx-2M series have delay time function which set t_{PLH} (output "Low" to "High") using an external capacitor connected in CT pin (C_{CT}). Because the BD52xx-2M series uses an open drain output type, it is necessary to connect a pull up resistor to V_{DD} or another power supply if needed [The output "High" voltage (V_{OUT}) in this case becomes V_{DD} or the voltage of the other power supply].

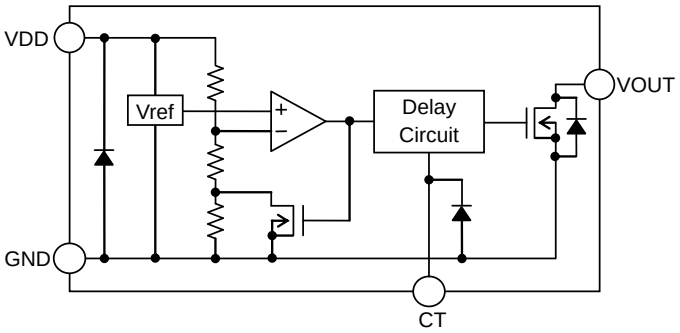

Figure 29. (BD52xx-2M type internal block diagram)

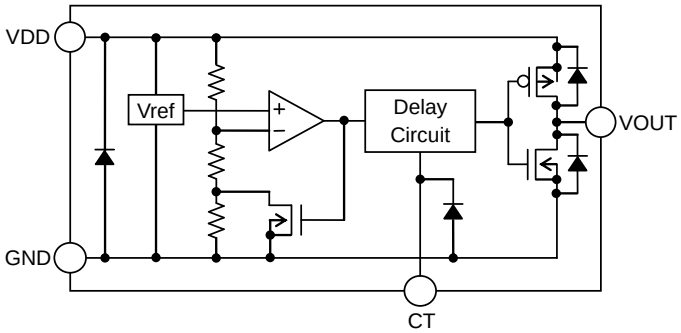

Figure 30. (BD53xx-2M type internal block diagram)

2. Setting of Detector Delay Time

Delay time L to H (t_{PLH}) is the time when V_{OUT} rises to 1/2 of V_{DD} after V_{DD} rises up and beyond the release voltage ($V_{DET}+\Delta V_{DET}$). The delay time (t_{PLH}) at the rise of V_{DD} is determined by delay coefficient, CT capacitor and delay time when CT pin is open (t_{CTO}) and calculated from the following formula. When CT capacitor ≥ 1nF, t_{CTO} has less effect and t_{PLH} computation is shown on Example No.2. The result has ±30% tolerance within the operating temperature range of -40°C to +105°C

Formula: (Ta=25°C)

$$t_{PLH} = C_{CT} \times Delay\ Coefficient + t_{CTO} \quad [s]$$

where:
C_{CT} is the CT pin external capacitor
Delay Coefficient is equal to 5.55 x 10^6
t_{CTO} is the delay time when CT=open *Note1*

Temperature	Delay Time (t_{CTO})		
	Min	Typ	Max
Ta = -40°C to +105°C	15µs	50µs	150µs

Note1: t_{CTO} is design guarantee only; outgoing inspection is not done on all products.

Example No.1:
CT capacitor = 100pF

$$t_{PLH_min} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 0.7 + 15 \times 10^{-6} = 403\mu s$$

$$t_{PLH_typ} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 1.0 + 50 \times 10^{-6} = 605\mu s$$

$$t_{PLH_max} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 1.3 + 150 \times 10^{-6} = 872\mu s$$

Example No.2:
CT capacitor = 1nF

$$t_{PLH_typ} = 1 \times 10^{-9} \times 5.55 \times 10^{6} = 5.55ms$$

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3. Timing Waveform

The following shows the relationship between the input voltage V_{DD} and the output voltage V_{OUT} when the power supply voltage V_{DD} is sweep up and sweep down.

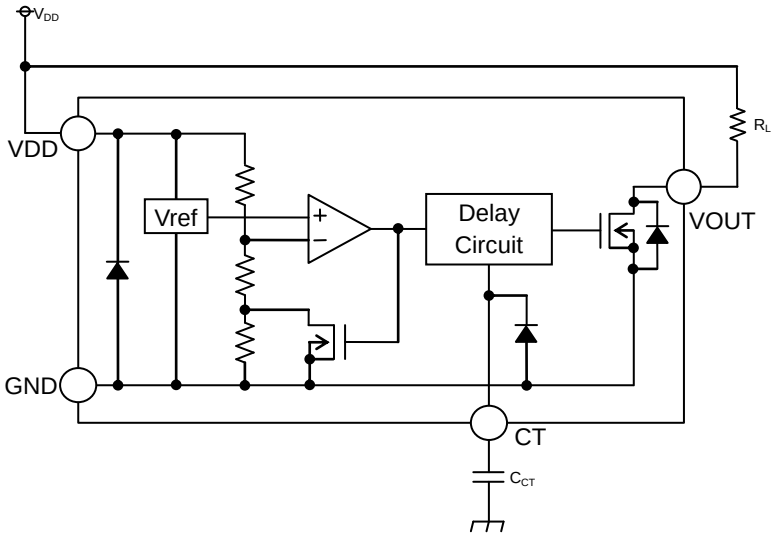

Figure 31. BD52xx-2M Set-up

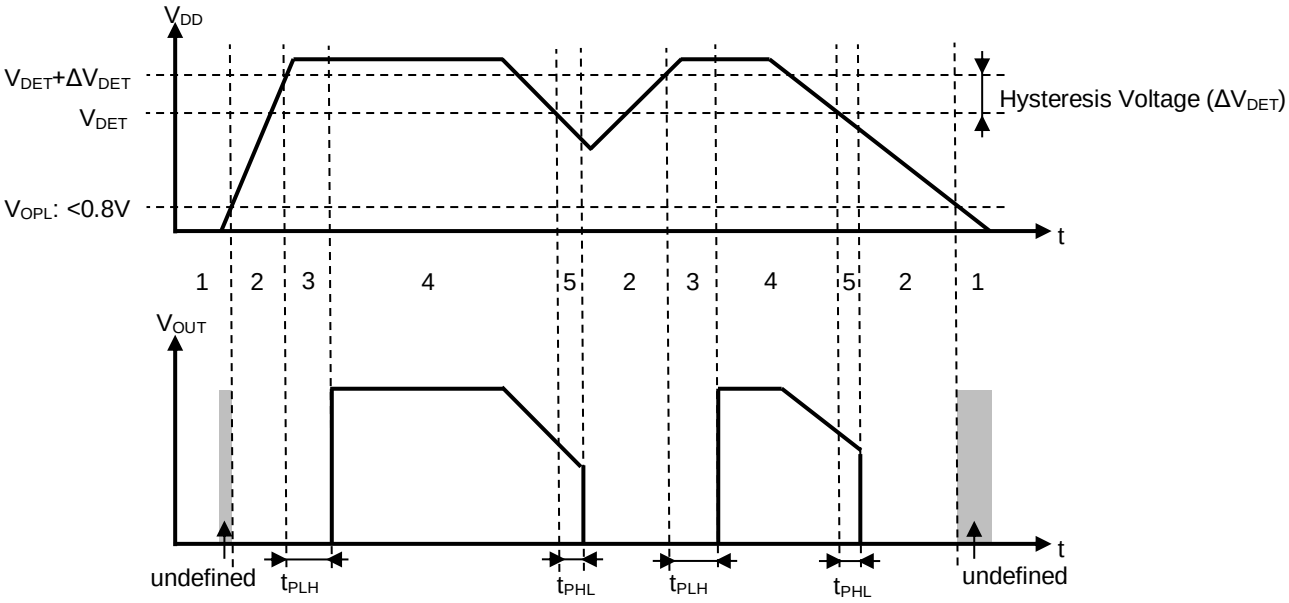

Figure 32. Timing Diagram

1. When the power supply turns on, the Output Voltage (V_{OUT}) is undefined until V_{DD} overcomes the Operating Voltage Limit (V_{OPL}).

2. V_{OUT} will turn to "Low" as V_{DD} increases above V_{OPL} but less than the Release Voltage ($V_{DET}+\Delta V_{DET}$),

3. When V_{DD} exceeds the Release Voltage ($V_{DET}+\Delta V_{DET}$), delay time (t_{PLH}) set by capacitor at CT pin (C_{CT}) will happen then V_{OUT} will switch from "Low" to "High".

4. V_{OUT} will remain "High" until V_{DD} do not fall below the Detection Voltage (V_{DET}).

5. When V_{DD} drops below V_{DET}, V_{OUT} will switch from "High" to "Low" with a delay of t_{PHL}.

*The potential difference between the detection voltage and the release voltage is known as the Hysteresis Voltage width (ΔV_{DET}). The system is designed such that the output will not toggle with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

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4. Circuit Applications

(1) Examples of common application circuits

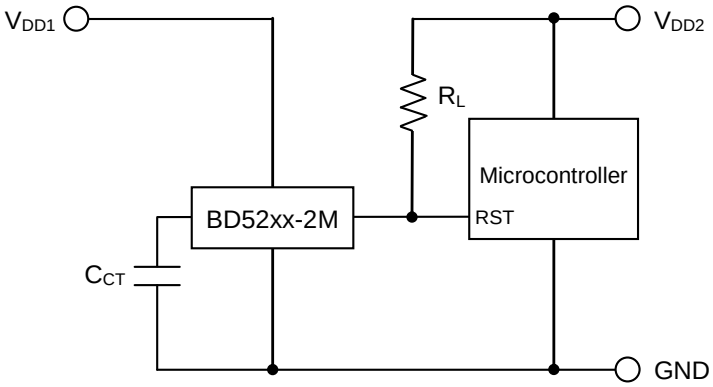

Figure 33. Open Drain Output Type

Application examples of BD52xx-2M series (Open-drain output type) and BD53xx-2M series (CMOS output type) are shown below.

CASE1: Power supply of the microcontroller (V_{DD2}) differs from the power supply of the reset detection (V_{DD1}).
Use an open drain output type (BD52xx-2M) device with a load resistance R_L attached as shown in Figure33.

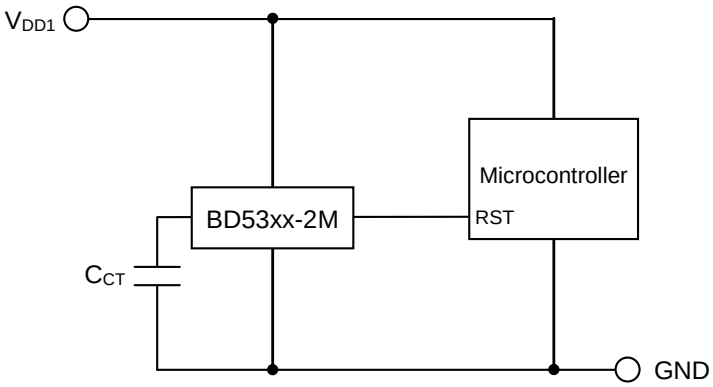

Figure 34. CMOS Output type

CASE2: Power supply of the microcontroller (V_{DD1}) is the same as the power supply of the reset detection (V_{DD1}).
Use a CMOS output type (BD53xx-2M) device or an open-drain output type (BD52xx-2M) device with a pull-up resistor between the output and V_{DD1}.

(2) The following is an example of circuit application in which an OR connection between two types of detection voltage resets the microcontroller.

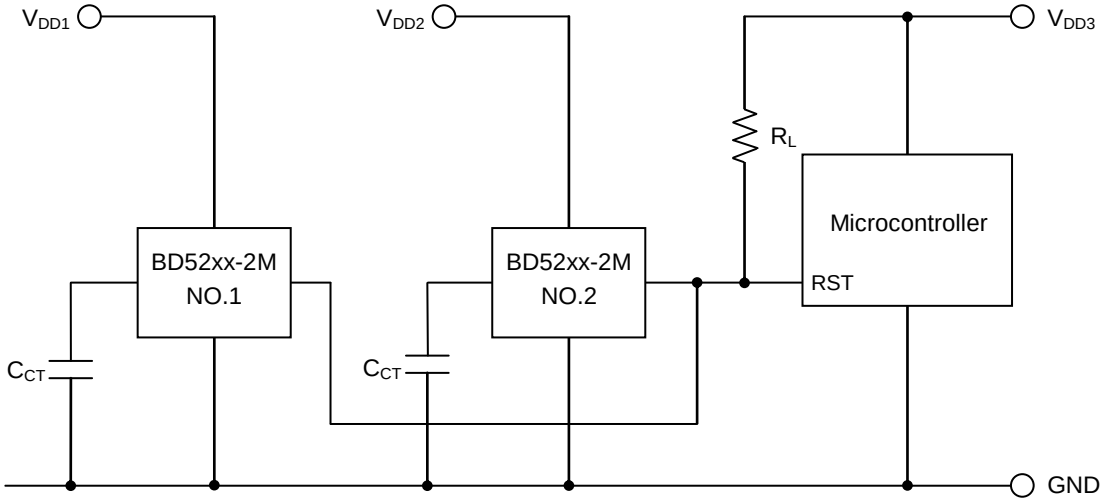

Figure 35. OR Circuit Connection Application

To reset the microcontroller when many independent power supplies are used in the system, OR connect an open drain output type (BD52xx-2M series) to the microcontroller's input with pull-up resistor to the supply voltage of the microcontroller (V_{DD3}) as shown in Figure 35. By pulling-up to V_{DD3}, output "High" voltage of micro-controller power supply is possible.

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Circuit Applications (continued)

(3) Examples of the power supply with resistor dividers

In applications wherein the power supply voltage of an IC comes from a resistor divider circuit, an inrush current will flow into the circuit when the output level switches from “Low” to “High” or vice versa. Inrush current is a sudden surge of current that flows from the power supply (V_{DD}) to ground (GND) as the output logic changes its state. This current flow may cause malfunction in the systems operation such as output oscillations, etc.

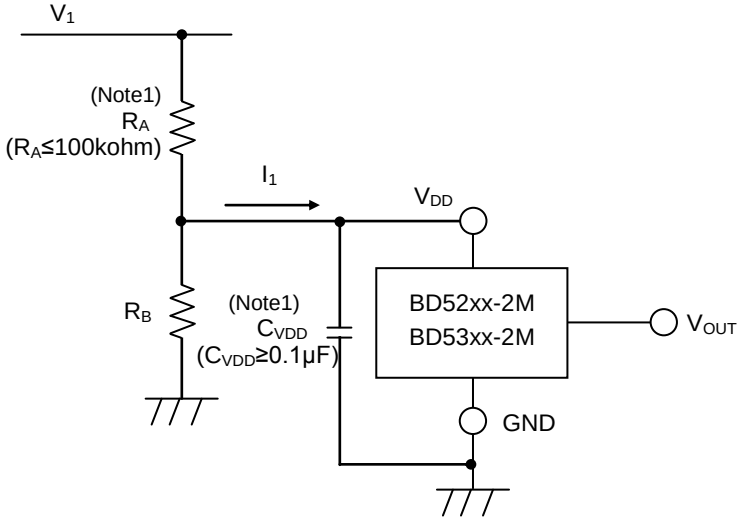

Figure 36. Resistor Divider Connection Application

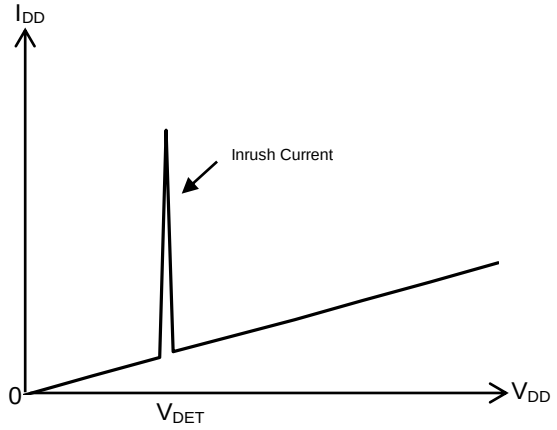

Figure 37. V_{DD} Voltage vs. Current Consumption

A voltage drop [Inrush current (I_1)] × [input resistor (R_A)] is caused by the inrush current, and causes the input voltage to drop when the output switches from “Low” to “High”. When the input voltage decreases and falls below the detection voltage, the output voltage switches from “High” to “Low”. At this time, the inrush current stops flowing through output “Low”, and the voltage drop is reduced. As a result, the output switches from “Low” to “High”, which again causes the inrush current to flow and the voltage to drop. This operation repeats and will result to oscillation. In case resistor divider will not use and only R_A will use, same response will happen.

Note1: The circuit connection mentioned above does not guarantee successful operation.
Please perform thorough evaluation using the actual application and set countermeasures

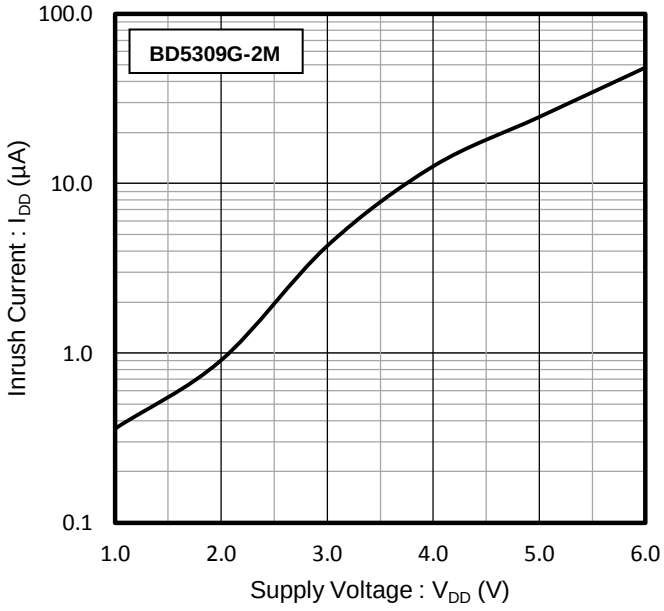

Figure 38. I_{DD} Inrush Current Ta=25°C

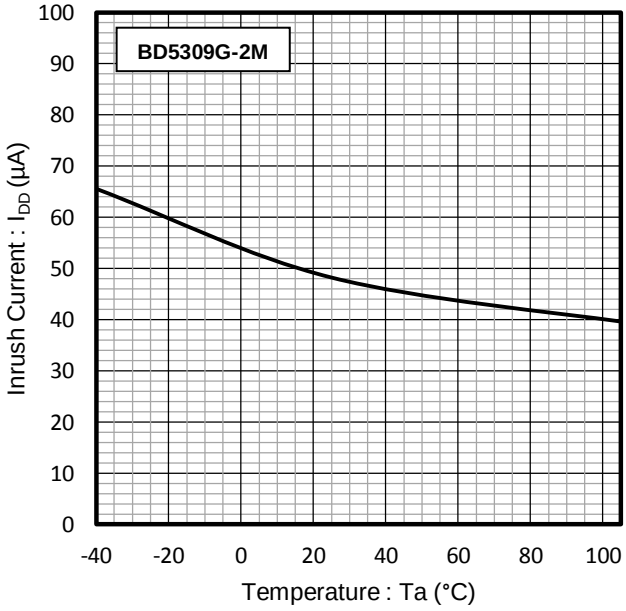

Figure 39. I_{DD} Inrush Current V_{DD}=6V

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Circuit Applications (continued)

Depending on the application set-up, there are times that V_{DD} voltage is always below the Release Voltage (V_{DET}+ΔV_{DET}) because of the effect of inrush current as shown in Figure 40.

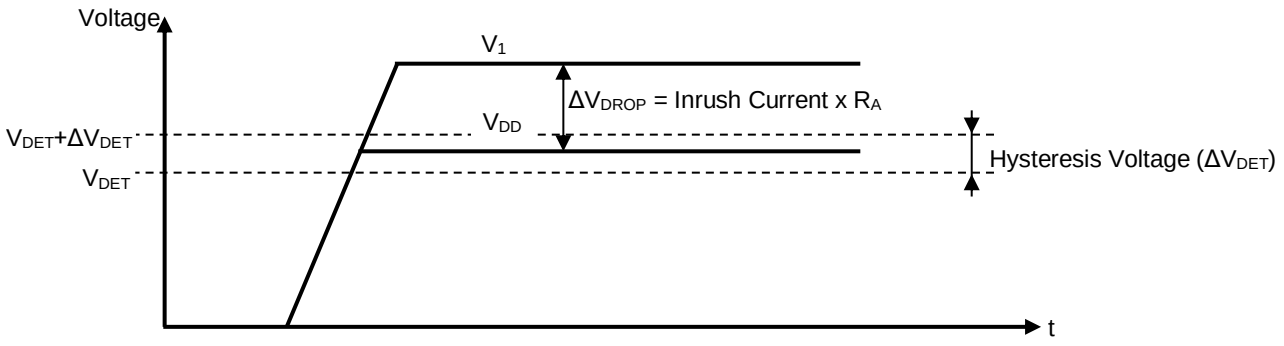

Figure 40. V_{DD} Drop Caused by Inrush Current

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Line**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line

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Operational Notes – continued

12. **Regarding Input Pins of the IC**
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC

13. **Ceramic Capacitor**
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others

14. **Area of Safe Operation (ASO)**
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. **Bypass Capacitor for Noise Rejection**
To help reject noise, put more than 0.1µF capacitor between VDD pin and GND. Be careful when using extremely big capacitor as transient response will be affected.

16. The V_{DD} line impedance might cause oscillation because of the detection current.

17. A V_{DD} to GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

18. **External Parameters**
The recommended value of C_T Capacitor is from open to 4.7µF and pull-up resistance value is 50kΩ to 1MΩ. There are many factors (board layout, etc) that can affect characteristics. Operating beyond the recommended values does not guarantee correct operation. Please verify and confirm using practical applications.

19. When V_{DD} falls below the minimum operating voltage, output will be open. When output is connected to pull-up voltage, output will be equivalent to pull-up voltage.

20. **Power-on Reset Operation**
Please note that the power on reset output varies with the V_{DD} rise time. Please verify the behavior in the actual operation.

21. **CT Pin Discharge**
Due to the capabilities of the CT pin discharge transistor, the CT pin may not completely discharge when a short input pulse is applied, and in this case the delay time may not be controlled. Please verify the actual operation.

22. This IC has extremely high impedance pins. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the CT and GND pin, it is recommended to insert 1MΩ resistor between CT and VDD pin. However, delay time will change when resistor is connected externally to CT pin so verify the delay time requirements when using this set-up. Also, when similar leakage is assumed between VOUT and GND pin, consider to set the value of pull up resistor lower than 1/10 of the impedance of assumed leakage route.

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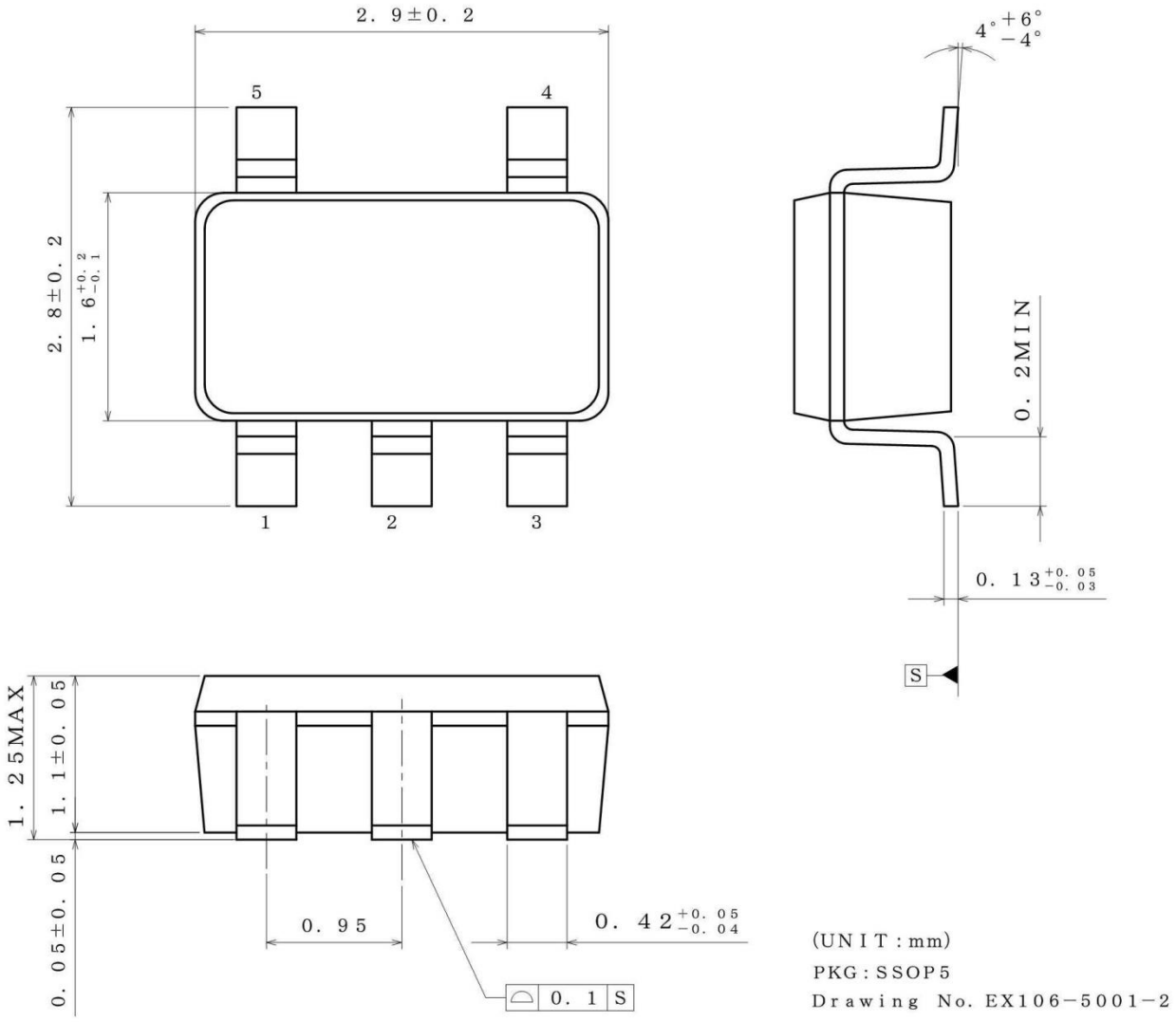
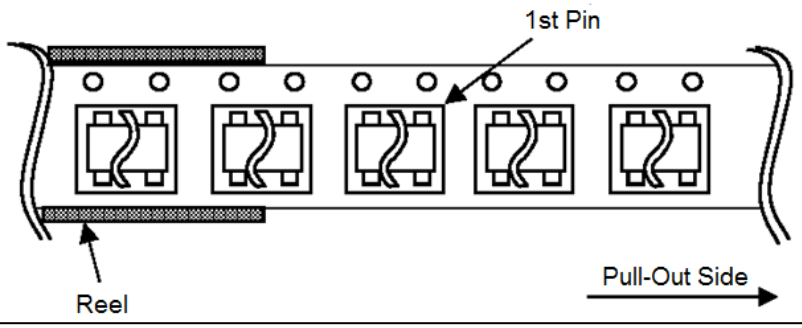
External Dimension Diagram, Packaging and Forming Specification

Package Name	SSOP5



<Packing Condition, Packing qty and Packing Direction>

Packing Condition	Emboss Taping
Packing Qty	3000pcs
Packing Direction	TR (When reel is held at left hand and pulled at right hand, the 1st pin of the product will come to top right direction.)



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Revision History

Date	Revision	Changes
2017/05/12	001	New
2018/07/05	002	Add notation of “Nano Energy”

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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