EVALUATION KIT AVAILABLE

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MAX9985

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

General Description

The MAX9985 high-linearity, dual-channel downconversion mixer is designed to provide approximately 6dB gain, +28.5dBm of IIP3, and 10.5dB of noise figure (NF) ideal for diversity receiver applications. With a 700MHz to 1000MHz RF frequency range and a 570MHz to 865MHz LO frequency range, this mixer is ideal for low-side LO injection architectures. In addition, the broad frequency range makes the MAX9985 ideal for GSM 850/950, 2G/2.5G EDGE, WCDMA, cdma2000®, and iDEN® base-station applications.

The MAX9985 dual-channel downconverter achieves a high level of component integration. The MAX9985 integrates two double-balanced active mixer cores, two LO buffers, a dual-input LO selectable switch, and a pair of differential IF output amplifiers. In addition, integrated on-chip baluns at the RF and LO ports allow for single-ended RF and single-ended LO inputs. The MAX9985 requires a typical 0dBm LO drive. Supply current is adjustable up to 400mA.

The MAX9985 is available in a 36-pin thin QFN package (6mm x 6mm) with an exposed paddle. Electrical performance is guaranteed over the extended temperature range, from T_C = -40°C to +100°C.

Applications

850MHz WCDMA Base Stations

GSM 850/GSM 950, 2G/2.5G EDGE Base Stations

cdmaOne™ and cdma2000 Base Stations

iDEN Base Stations

Fixed Broadband Wireless Access

Wireless Local Loop

Private Mobile Radios

Military Systems

Digital and Spread-Spectrum Communication Systems

Microwave Links

cdma2000 is a registered trademark of Telecommunications Industry Association.

iDEN is a registered trademark of Motorola, Inc.

cdmaOne is a trademark of CDMA Development Group.

Features

- **700MHz to 1000MHz RF Frequency Range**
- **570MHz to 865MHz LO Frequency Range**
- **50MHz to 250MHz IF Frequency Range**
- **6dB Typical Conversion Gain**
- **10.5dB Typical Noise Figure**
- **+28.5dBm Typical Input IP3**
- **+16.2dBm Typical Input 1dB Compression Point**
- **77dBc Typical 2RF-2LO Spurious Rejection at P_{RF} = -10dBm**
- **Dual Channels Ideal for Diversity Receiver Applications**
- **47dB Typical Channel-to-Channel Isolation**
- **-3dBm to +3dBm LO Drive**
- **Integrated LO Buffer**
- **Internal RF and LO Baluns for Single-Ended Inputs**
- **Built-In SPDT LO Switch with 43dB LO1-to-LO2 Isolation and 50ns Switching Time**
- **Pin-Compatible with MAX9995 1700MHz to 2200MHz Mixer**
- **Lead(Pb)-Free Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9985ETX+	-40°C to +100°C	36 Thin QFN-EP* (6mm x 6mm), lead free, bulk	T3666-2
MAX9985ETX+T	-40°C to +100°C	36 Thin QFN-EP* (6mm x 6mm), lead free, T/R	T3666-2

**EP = Exposed paddle.*

T = Tape-and-reel package.

+Denotes lead(Pb)-free and RoHS compliant.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +5.5V
LO1, LO2 to GND ....±0.3V
Any Other Pins to GND..........-0.3V to (V_{CC} + 0.3V)
RFMAIN, RFDIV, and LO_ Input Power ....+20dBm
RFMAIN, RFDIV Current (RF is DC shorted to GND through balun) 50mA
Continuous Power Dissipation (Note 1) 6.75W
Operating Case Temperature Range (Note 2)......-40°C to +100°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to PCB. See the Application Information section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

PACKAGE THERMAL CHARACTERISTICS

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Notes 3, 4)..........38°C/W
Junction-to-Board Thermal Resistance (θ_{JB})..........12.2°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Notes 1, 4)..........7.4°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Using the *Typical Application Circuit*, no input RF or LO signals applied, V_{CC} = 4.75V to 5.25V, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Total supply current (see Table 1 for lower current settings)		400	440	mA
		V_{CC} (pin 16)		80		
		V_{CC} (pin 30)		80		
		IFM+/IFM- (total of both)		105		
		IFD+/IFD- (total of both)		105		
LOSEL Input High Voltage	V_{IH}		2			V
LOSEL Input Low Voltage	V_{IL}				0.8	V
LOSEL Input Current	I_{IH} and I_{IL}		-10		+10	μA

AC ELECTRICAL CHARACTERISTICS

(Using the *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 820MHz to 920MHz, f_{LO} = 670MHz to 865MHz, f_{IF} = 100MHz, $f_{RF} > f_{LO}$, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 870MHz, f_{LO} = 770MHz, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 6)		700		1000	MHz
LO Frequency	f_{LO}	(Note 6)		570		865	MHz
IF Frequency	f_{IF}	IF matching components affect the IF frequency range (Note 6)		50		250	MHz
LO Drive	P_{LO}	(Note 7)		-3		+3	dBm
Conversion Gain	G_C	(Note 8)		4.5	6	7.5	dB
		T_C = +100°C			5.4		
Gain Variation over Temperature					-0.012		dB/°C
Conversion Gain Flatness		Flatness over any one of three frequency bands: f_{RF} = 824MHz to 849MHz, f_{RF} = 869MHz to 894MHz, f_{RF} = 880MHz to 915MHz			±0.1		dB
Noise Figure, Single Sideband	NF	f_{IF} = 190MHz, no blockers present (Note 7)			10.5	13	dB
Noise Figure under Blocking Condition		+11dBm blocker tone applied to RF port at 961MHz, f_{RF} = 860MHz, f_{LO} = 670MHz, $f_{IFDESIRED}$ = 190MHz, $f_{BLOCKER}$ = 291MHz (Notes 7, 9)			21	26	dB
Input Compression Point	P_{1dB}				16.2		dBm
Output Compression Point	OP_{1dB}			18.5	21.2		dBm
Small-Signal Compression under Blocking Conditions		P_{RF} = -5dBm, f_{RF} = 870MHz, $f_{BLOCKER}$ = 871MHz	$P_{BLOCKER}$ = +8dBm		0.1		dB
			$P_{BLOCKER}$ = +11dBm		0.25		
Third-Order Input Intercept Point	IIP3	f_{RF1}-f_{RF2} = 1MHz, f_{IF} = 100MHz, P_{RF} = -5dBm/tone			28.5		dBm
			T_C = +100°C		28.8		
Third-Order Input Intercept Point Variation over Temperature					-0.01		dB/°C
Third-Order Output Intercept Point	OIP3	P_{RF} = -5dBm/tone, f_{IF} = 100MHz, f_{RF1}-f_{RF2} = 1MHz (Note 7)		32.0	34.5		dBm
2RF-2LO Spur	2 x 2	f_{RF} = 870MHz, f_{LO} = 770MHz, f_{SPUR} = 820MHz	P_{RF} = -10dBm (Note 7)	63	77		dBc
			P_{RF} = -10dBm, T_C = +100°C		78		
			P_{RF} = -5dBm (Note 7)	58	72		
			P_{RF} = -5dBm, T_C = +100°C		73		
3RF-3LO Spur	3 x 3	f_{RF} = 870MHz, f_{LO} = 770MHz, f_{SPUR} = 803.3MHz	P_{RF} = -10dBm (Note 7)	70	85		dBc
			P_{RF} = -10dBm, T_C = +100°C		87.3		
			P_{RF} = -5dBm (Note 7)	60	75		
			P_{RF} = -5dBm, T_C = +100°C		77.3		

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AC ELECTRICAL CHARACTERISTICS (continued)

(Using the *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 820MHz to 920MHz, f_{LO} = 670MHz to 865MHz, f_{IF} = 100MHz, $f_{RF} > f_{LO}$, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 870MHz, f_{LO} = 770MHz, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.) (Note 5)

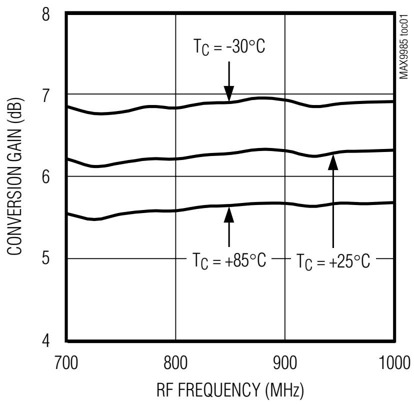
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LO1-to-LO2 Port Isolation		P_{LO1} = +3dBm, P_{LO2} = +3dBm, f_{LO1}-f_{LO2} = 1MHz, P_{RF} = -5dBm, f_{IF} = 100MHz (Notes 7, 10)	39	43		dB
Maximum LO Leakage at RF Port				-40	-30	dBm
Maximum 2LO Leakage at RF Port				-45	-20	dBm
Maximum LO Leakage at IF Port				-30	-20	dBm
		T_C = +100°C		-30.3		
Minimum RF-to-IF Isolation			30	45		dB
		T_C = +100°C		49.5		
Minimum Channel-to-Channel Isolation		P_{RF} = -10dBm, RFMAIN (RFDIV) power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω	40	47		dB
		T_C = +100°C		47.5		
LO Switching Time		50% of LOSEL to IF settled within 2 degrees (Note 7)		0.05	1	µs
RF Input Impedance				50		Ω
LO Input Impedance				50		Ω
IF Output Impedance		Differential		200		Ω
RF Input Return Loss		LO on and IF terminated		24		dB
LO Input Return Loss		LO port selected		35		dB
		LO port unselected		36		
IF Return Loss		RF terminated in 50Ω		20		dB

Note 5: All limits reflect losses of external components. Output measurements taken at IF outputs of the *Typical Application Circuit*.
Note 6: Performance is guaranteed for f_{RF} = 820MHz to 920MHz, f_{LO} = 670MHz to 865MHz, and f_{IF} = 100MHz. Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*.
Note 7: Guaranteed by design and characterization.
Note 8: Performance at T_C = -40°C is guaranteed by design.
Note 9: Measured with external LO source noise filtered so the noise floor is -174dBm/Hz. This specification reflects the effects of all SNR degradations in the mixer including the LO noise, as defined in Maxim Application Note 2021.
Note 10: Measured at IF port at IF frequency. LOSEL may be in any logic state.

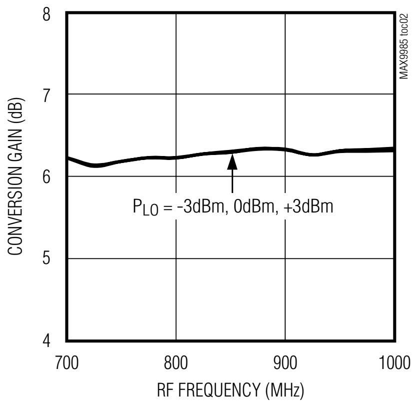
Typical Operating Characteristics

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, $f_{RF} > f_{LO}$, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)

CONVERSION GAIN vs. RF FREQUENCY



CONVERSION GAIN vs. RF FREQUENCY



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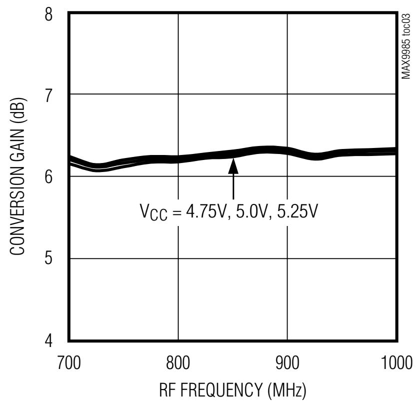
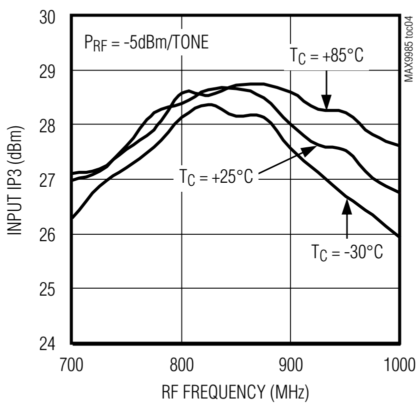


INPUT IP3 vs. RF FREQUENCY



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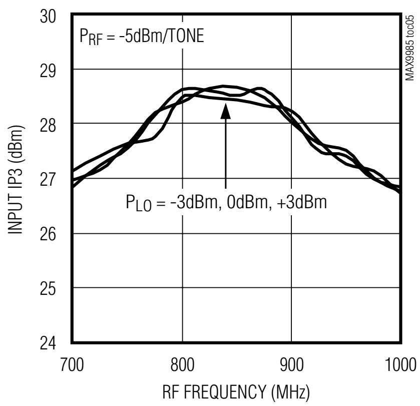

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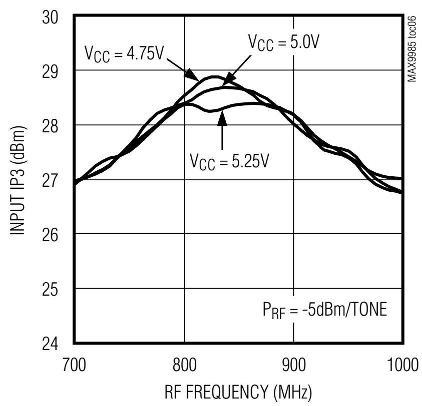
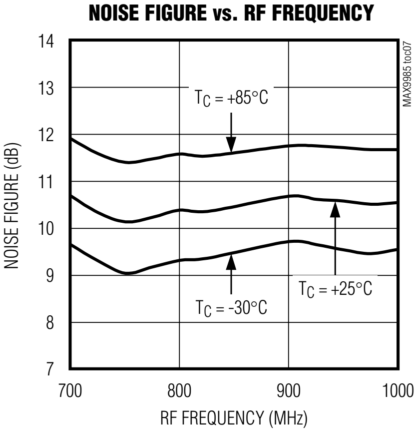


NOISE FIGURE vs. RF FREQUENCY



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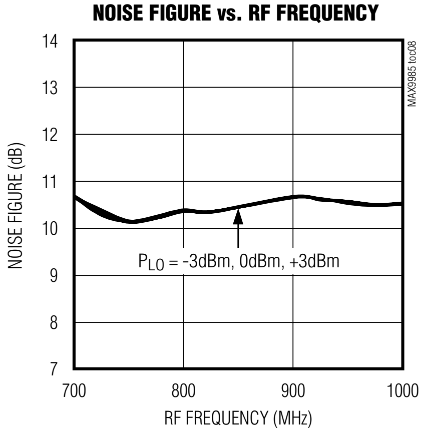

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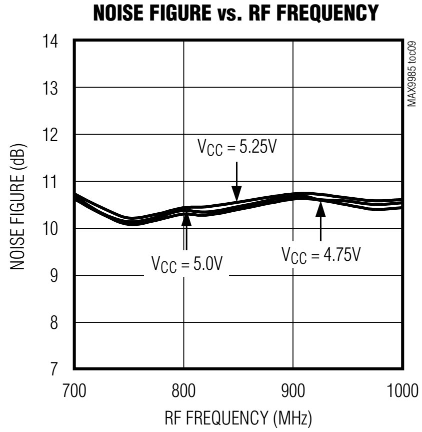
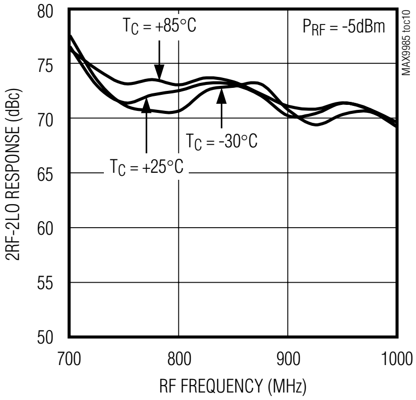


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

Typical Operating Characteristics (continued)

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, $f_{RF} > f_{LO}$, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)

2RF-2LO RESPONSE vs. RF FREQUENCY



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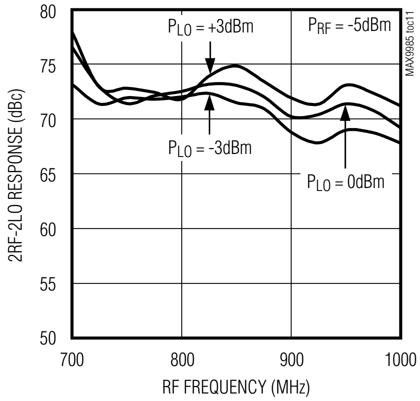

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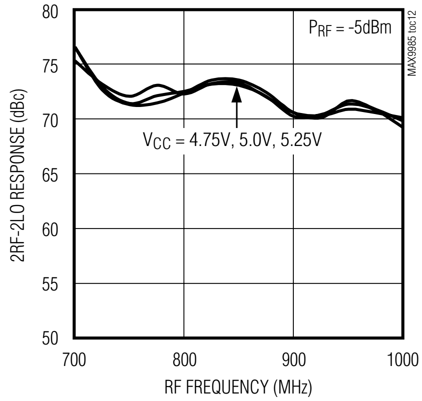
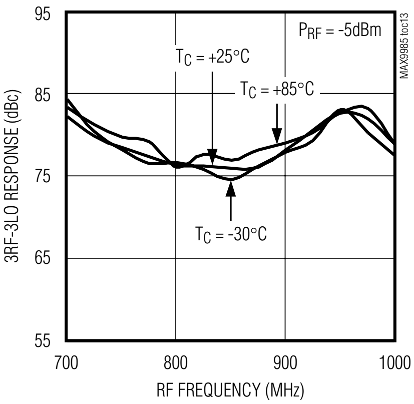
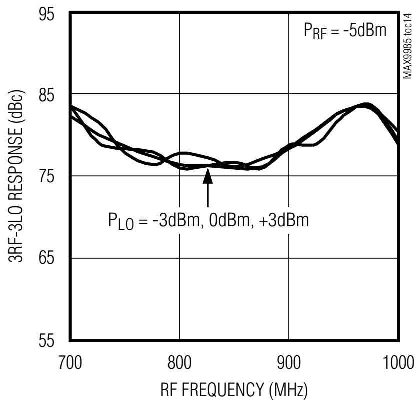


3RF-3LO RESPONSE vs. RF FREQUENCY



3RF-3LO RESPONSE vs. RF FREQUENCY



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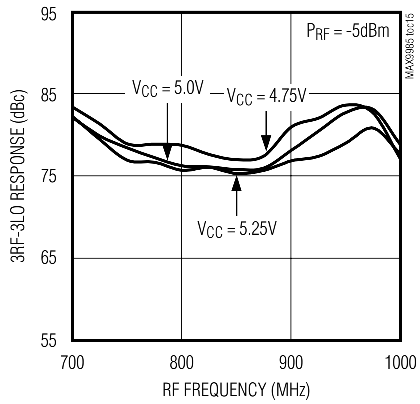
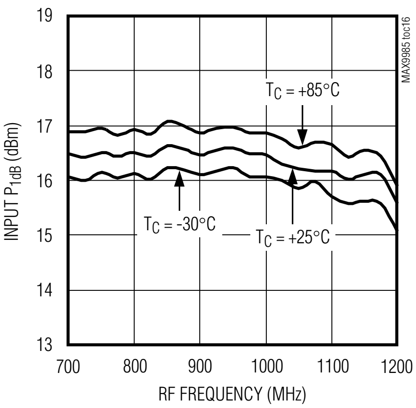


INPUT P_{1dB} vs. RF FREQUENCY



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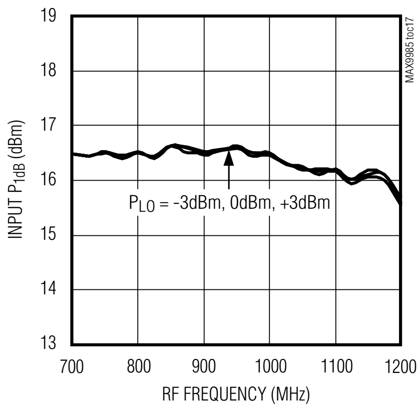

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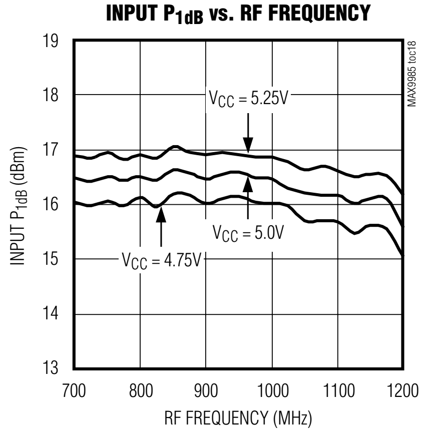
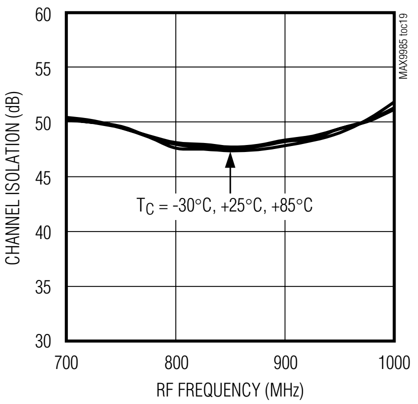


Typical Operating Characteristics (continued)

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, $f_{RF} > f_{LO}$, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)

CHANNEL ISOLATION vs. RF FREQUENCY



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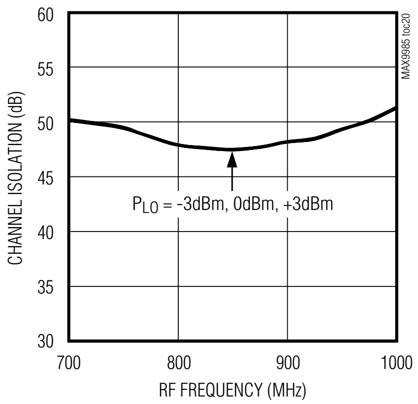

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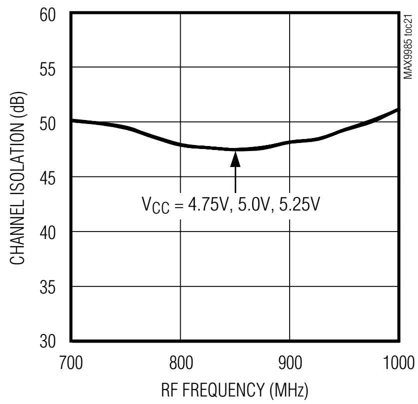
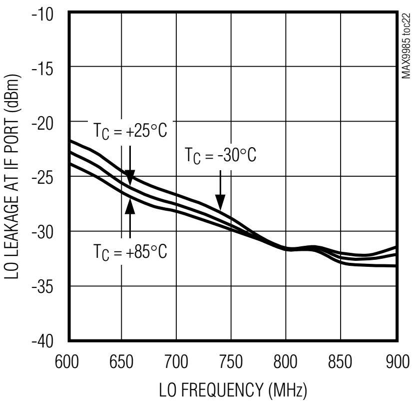


LO LEAKAGE AT IF PORT vs. LO FREQUENCY



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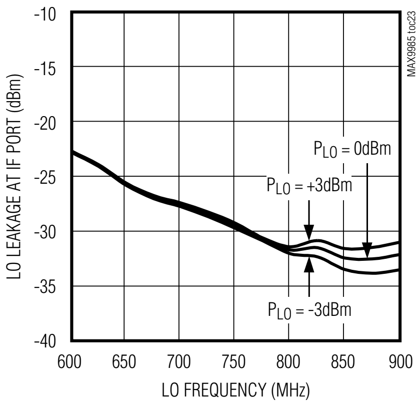
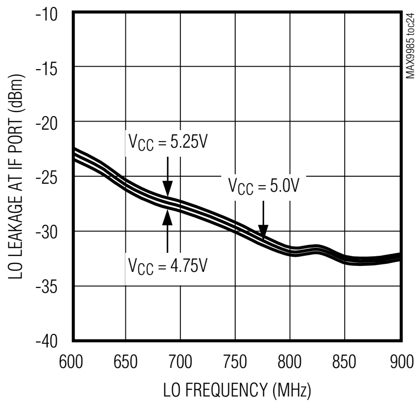
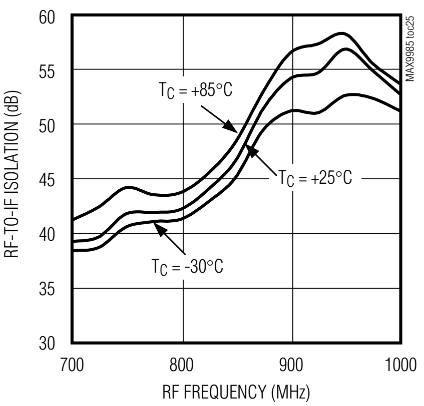


LO LEAKAGE AT IF PORT vs. LO FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY



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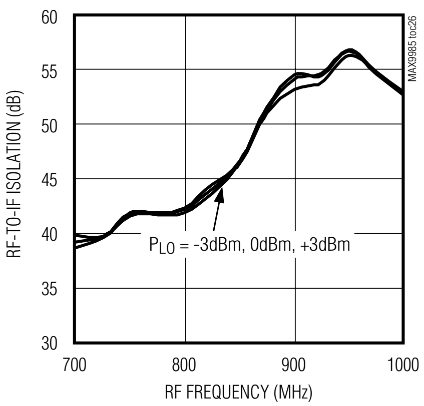

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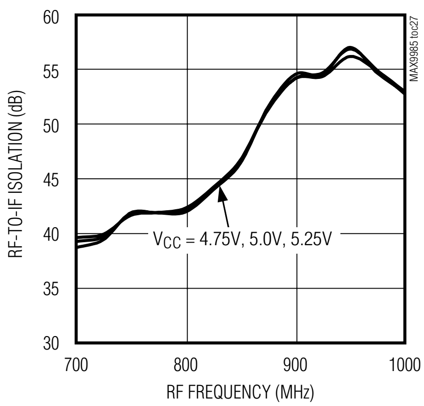
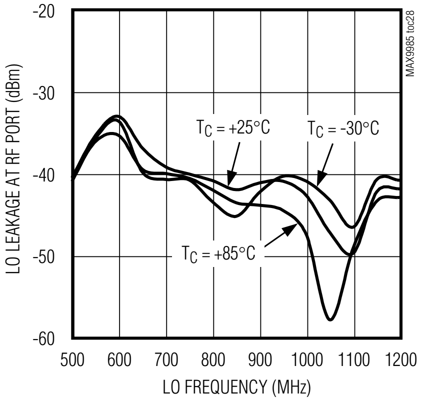


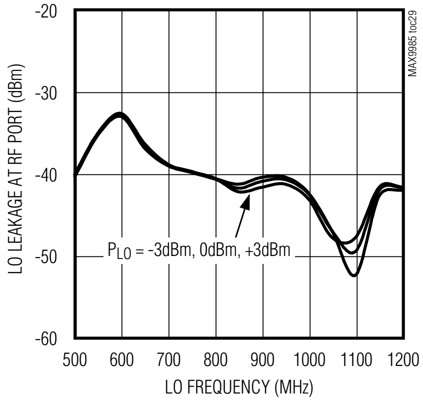
Typical Operating Characteristics (continued)

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, f_{RF} > f_{LO}, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)

LO LEAKAGE AT RF PORT vs. LO FREQUENCY



LO LEAKAGE AT RF PORT vs. LO FREQUENCY



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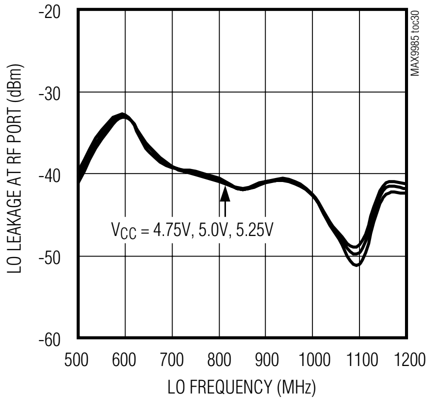
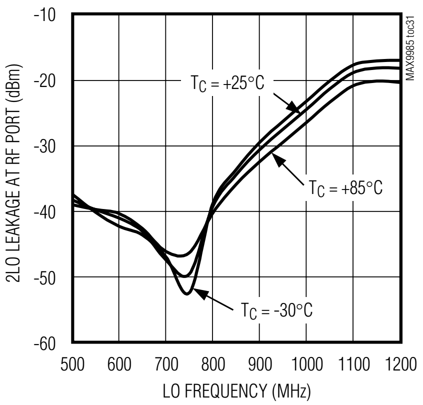


2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



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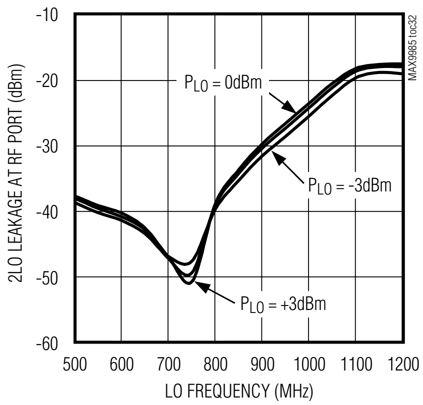
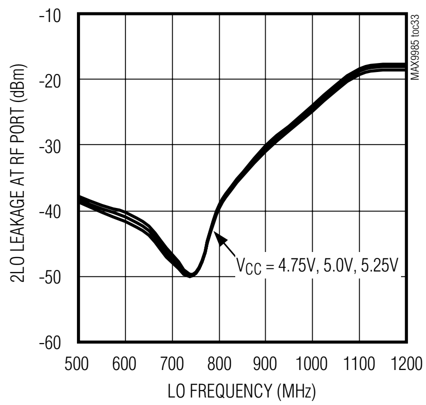
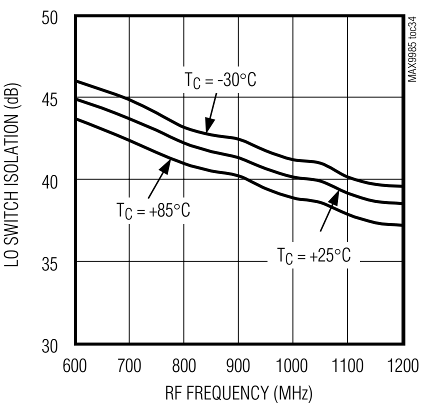


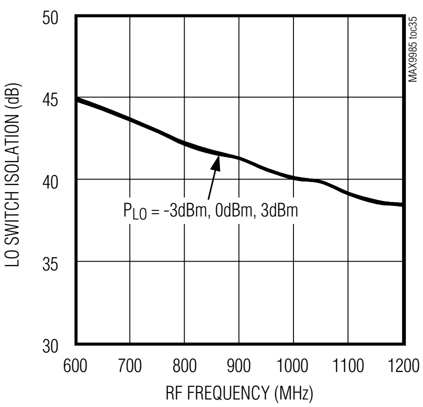
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



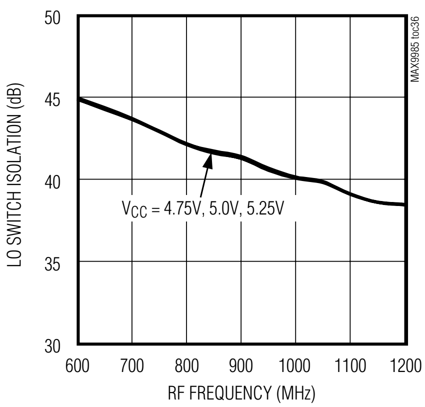
LO SWITCH ISOLATION vs. RF FREQUENCY



LO SWITCH ISOLATION vs. RF FREQUENCY



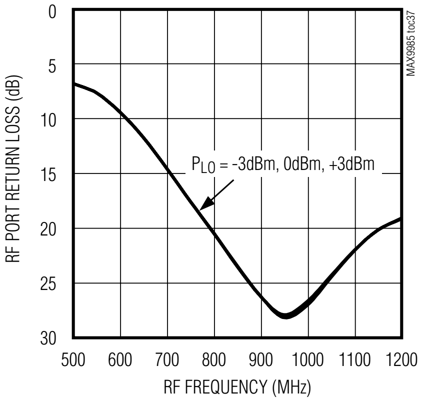
LO SWITCH ISOLATION vs. RF FREQUENCY



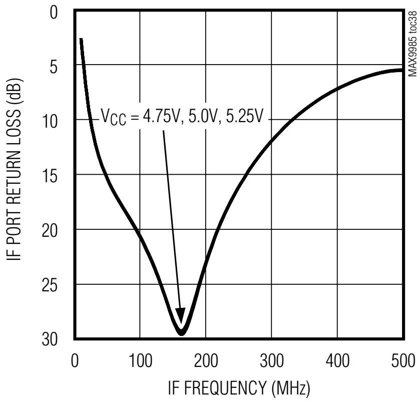
Typical Operating Characteristics (continued)

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, $f_{RF} > f_{LO}$, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)

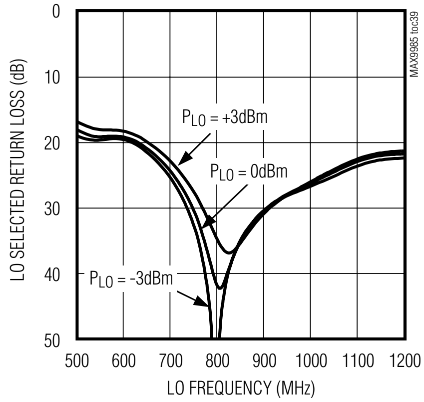
RF PORT RETURN LOSS vs. RF FREQUENCY



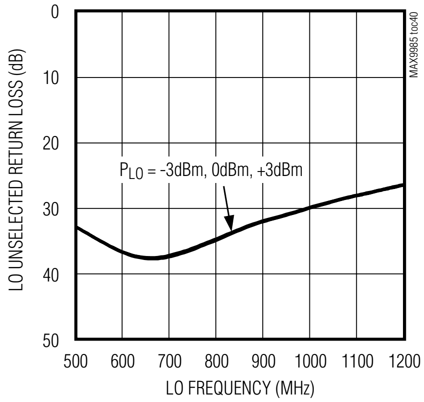
IF PORT RETURN LOSS vs. IF FREQUENCY



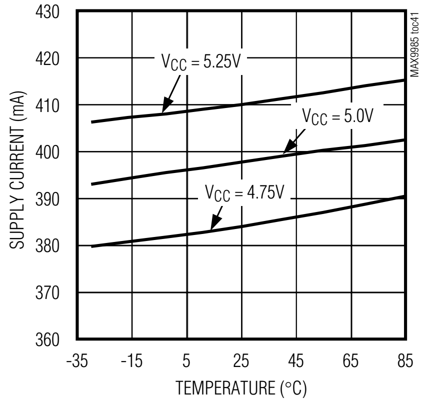
LO SELECTED RETURN LOSS vs. LO FREQUENCY



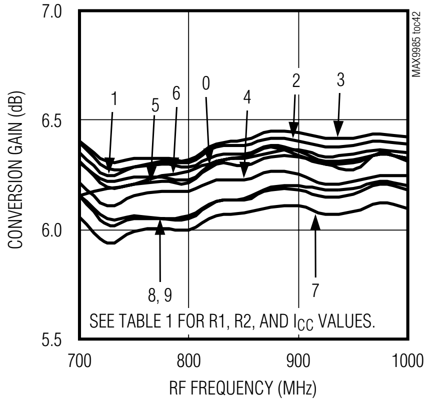
LO UNSELECTED RETURN LOSS vs. LO FREQUENCY



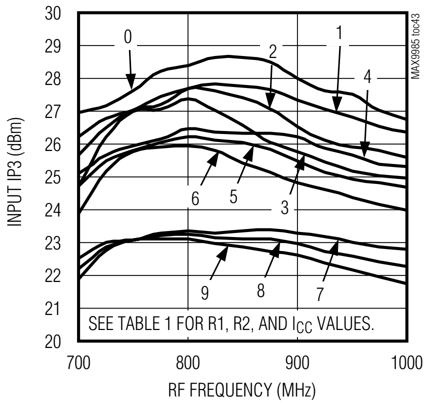
SUPPLY CURRENT vs. TEMPERATURE (T_C)



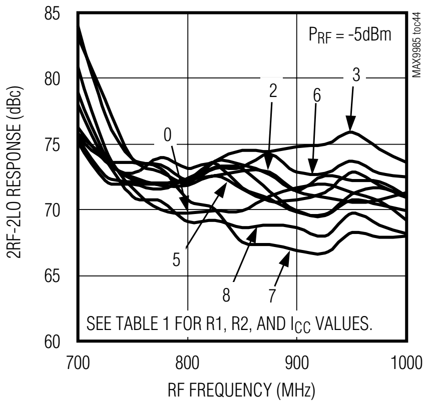
CONVERSION GAIN vs. RF FREQUENCY (VARIOUS LO AND IF BUFFER BIAS)



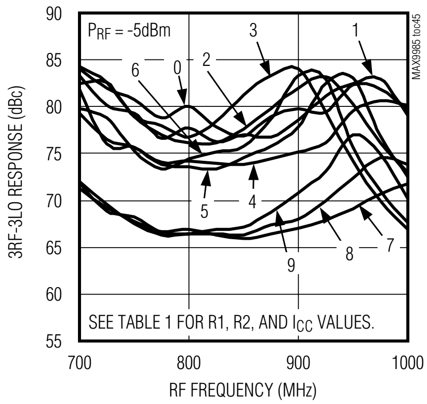
INPUT IP3 vs. RF FREQUENCY (VARIOUS LO AND IF BUFFER BIAS)



2RF-2LO RESPONSE vs. RF FREQUENCY (VARIOUS LO AND IF BUFFER BIAS)

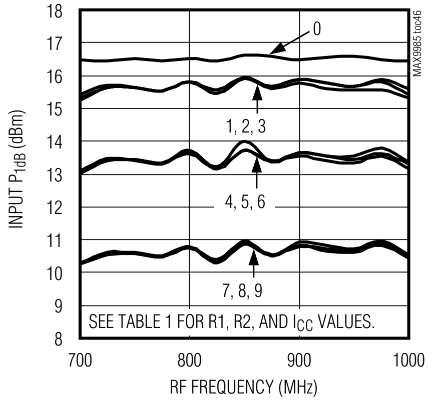


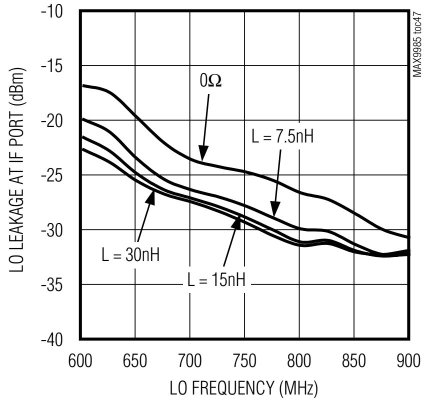
3RF-3LO RESPONSE vs. RF FREQUENCY (VARIOUS LO AND IF BUFFER BIAS)



Typical Operating Characteristics (continued)

(Using the *Typical Application Circuit*, V_{CC} = 5.0V, P_{LO} = 0dBm, P_{RF} = -5dBm, $f_{RF} > f_{LO}$, f_{IF} = 100MHz, T_C = +25°C, unless otherwise noted.)





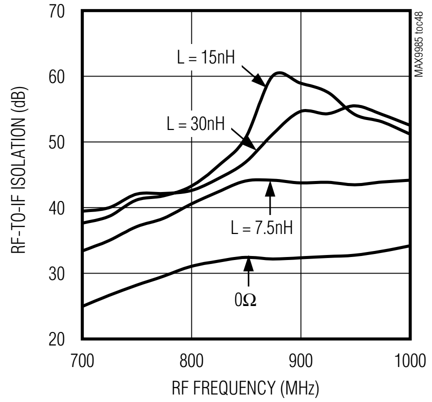


Table 1. DC Current vs. Bias Resistor Settings

BIAS CONDITION	DC CURRENT (mA)	R1 AND R4 VALUES (Ω)	R2 AND R5 VALUES (Ω)
0	397.8	1070	1100
1	345.0	1400	1100
2	316.5	1400	1620
3	297.5	1400	2210
4	301.2	1910	1100
5	271.7	1910	1620
6	252.2	1910	2210
7	260.1	2800	1100
8	230.5	2800	1620
9	211.5	2800	2210

Pin Description

PIN	NAME	FUNCTION
1	RFMAIN	Main Channel RF input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
2	TAPMAIN	Main Channel Balun Center Tap. Bypass to GND with capacitors close to the pin.
3, 5, 7, 12, 20, 22, 24, 25, 26, 34	GND	Ground
4, 6, 10, 16, 21, 30, 36	V_{CC}	Power Supply. Connect bypass capacitors as close to the pin as possible (see the *Typical Application Circuit*).
8	TAPDIV	Diversity Channel Balun Center Tap. Bypass to GND with capacitors close to the pin.
9	RFDIV	Diversity Channel RF Input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
11	IFDBIAS	IF Diversity Amplifier Bias Control. Connect a 1.07kΩ resistor from this pin to ground to set the bias current for the diversity IF amplifier (see the *Typical Operating Characteristics* for typical performance versus resistor value).
13, 14	IFD+, IFD-	Diversity Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
15	LEXTD	Connect a 30nH inductor from this pin to ground to increase the RF-to-IF and LO-to-IF isolation. Connect this pin to ground if isolations can be degraded (see the *Typical Operating Characteristics* for typical degradation).
17	LODBIAS	LO Diversity Amplifier Bias Control. Connect a 1.1kΩ resistor from this pin to ground to set the bias current for the diversity LO amplifier (see the *Typical Operating Characteristics* for typical performance versus resistor value).
18, 28	N.C.	No Connection. Not internally connected.
19	LO1	Local Oscillator 1 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
23	LOSEL	Local Oscillator Select. Set this pin to high to select LO1. Set low to select LO2.
27	LO2	Local Oscillator 2 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
29	LOMBIAS	LO Main Amplifier Bias Control. Connect a 1.1kΩ resistor from this pin to ground to set the bias current for the main LO amplifier (see the *Typical Operating Characteristics* for typical performance versus resistor value).
31	LEXTM	Connect a 30nH inductor from this pin to ground to increase the RF-IF and LO-IF isolation. Connect this pin to ground if isolations can be degraded (see the *Typical Operating Characteristics* for typical degradation).
32, 33	IFM-, IFM+	Main Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
35	IFMBIAS	IF Main Amplifier Bias Control. Connect a 1.07kΩ resistor from this pin to ground to set the bias current for the main IF amplifier (see the *Typical Operating Characteristics* for typical performance vs. resistor value).
—	EP	Exposed Paddle. Solder the exposed paddle to the ground plane using multiple vias. This paddle affects RF performance and provides heat dissipation.

Detailed Description

The MAX9985 is a dual-channel downconverter designed to provide 6dB of conversion gain, +28.5dBm input IP3, and +16.2dBm 1dB input compression point, with a 10.5dB NF.

In addition to its high-linearity performance, the MAX9985 achieves a high level of component integration. The device integrates two double-balanced active mixers for two-channel downconversion. Both the main and diversity channels include a balun and matching circuitry to allow 50Ω single-ended interfaces to the RF ports and the two LO ports. An integrated single-pole, double-throw (SPDT) switch provides 50ns switching time between the two LO inputs with 43dB of LO-to-LO isolation and a -40dBm of LO leakage at the RF port. Furthermore, the integrated LO buffers provide a high drive level to each mixer core, reducing the LO drive required at the MAX9985's inputs to a -3dBm to +3dBm range. The IF ports for both channels incorporate differential outputs for downconversion, which is ideal for providing enhanced IIP2 performance.

Dual-channel downconversion makes the MAX9985 ideal for diversity receiver applications. In addition, specifications are guaranteed over broad frequency ranges to allow for use in GSM 850/950, 2G/2.5G EDGE, WCDMA, cdma2000, and iDEN base stations. The MAX9985 is specified to operate over a 700MHz to 1000MHz RF input range, a 570MHz to 865MHz LO range, and a 50MHz to 250MHz IF range. The external IF components set the lower frequency range (see the *Typical Operating Characteristics* for details).

RF Port and Balun

The RF input ports to both the main and diversity channels are internally matched to 50Ω, requiring no external matching components. A DC-blocking capacitor is required as the input is internally DC-shorted to ground through the on-chip balun. The RF port return loss is typically 15dB over the entire 700MHz to 1000MHz RF frequency range.

LO Inputs, Buffer, and Balun

The MAX9985 is optimized for a 570MHz to 865MHz LO frequency range. As an added feature, the MAX9985 includes an internal LO SPDT switch for use in frequency-hopping applications. The switch selects one of the two single-ended LO ports, allowing the external oscillator to settle on a particular frequency before it is switched in. LO switching time is typically less than 50ns, which is more than adequate for typical GSM applications. If frequency hopping is not employed, simply set the switch to either of the LO inputs. The switch is controlled by a digital input (LOSEL), where logic-high selects LO1 and logic-low selects LO2. LO1 and LO2 inputs are internally matched to 50Ω, requiring only an 82pF DC-blocking capacitor. To avoid damage to the part, voltage **MUST** be applied to V_{CC} before digital logic is applied to LOSEL. Alternatively, a 1kΩ resistor can be placed in series at the LOSEL to limit the input current in applications where LOSEL is applied before V_{CC}.

The main and diversity channels incorporate a two-stage LO buffer that allows for a wide-input power range for the LO drive. All guaranteed specifications are for an LO signal power from -3dBm to +3dBm. The on-chip low-loss baluns, along with LO buffers, drive the double-balanced mixers. All interfacing and matching components from the LO inputs to the IF outputs are integrated on-chip.

High-Linearity Mixer

The core of the MAX9985 dual-channel downconverter consists of two double-balanced, high-performance passive mixers. Exceptional linearity is provided by the large LO swing from the on-chip LO buffers. When combined with the integrated IF amplifiers, the cascaded IIP3, 2RF-2LO rejection, and NF performance are typically +28.5dBm, 77dBc, and 10.5dB, respectively.

Differential IF

The MAX9985 has a 50MHz to 250MHz IF frequency range, where the low-end frequency depends on the frequency response of the external IF components. Note that these differential ports are ideal for providing enhanced IIP2 performance. Single-ended IF applications require a 4:1 (impedance ratio) balun to transform the 200Ω differential IF impedance to a 50Ω single-ended system. After the balun, the IF return loss is better than 20dB. The user can use a differential IF amplifier on the mixer IF ports, but a DC block is required on both IFD+/IFD- and IFM+/IFM- ports to keep external DC from entering the IF ports of the mixer.

Applications Information

Input and Output Matching

The RF and LO inputs are internally matched to 50Ω. No matching components are required. Return loss at the RF port is typically 15dB over the entire input range and return loss at the LO ports are typically 25dB. RF and LO inputs require only DC-blocking capacitors for interfacing.

The IF output impedance is 200Ω (differential). For evaluation, an external low-loss 4:1 (impedance ratio) balun transforms this impedance to a 50Ω single-ended output (see the *Typical Application Circuit*).

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

LO Buffer Bias Resistors

Bias currents for the two on-chip LO buffers is optimized by fine-tuning the off-chip resistors on LODBIAS (pin 17) and LOMBIAS (pin 29). The current in the buffer amplifiers is reduced by increasing the value of these resistors, but performance may degrade. See the *Typical Operating Characteristics* for key performance parameters versus this resistor value. Doubling the value of these resistors reduces the total chip current by approximately 50mA (see Table 1).

IF Amplifier Bias Resistors

Bias currents for the two on-chip IF amplifiers are optimized by fine-tuning the off-chip resistors on IFDBIAS (pin 11) and IFMBIAS (pin 35). The current in the IF amplifiers is decreased by raising the value of these resistors, but performance may degrade. See the *Typical Operating Characteristics* for key performance parameters versus this resistor value. Doubling the value of this resistor reduces the current in each IF amplifier from 100mA to approximately 50mA (see Table 1).

LEXT Inductor

Short LEXT_ to ground using a 0Ω resistor. For applications requiring improved RF-to-IF and LO-to-IF isolation, LEXT_ can be used by connecting a low-ESR inductor from LEXT_ to GND. See the *Typical Operating Characteristics* on RF-to-IF port isolation and LO-to-IF port leakage for various inductor values. The load impedance presented to the mixer must be such that any capacitance from both IF- and IF+ to ground do not exceed several picofarads to ensure stable operating conditions.

Approximately 100mA flows through LEXT_, so it is important to use a low-DCR wire-wound inductor.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For the best performance, route the ground pin traces directly to the exposed paddle under the package. The PCB exposed paddle **MUST** be connected to the ground plane of the PCB. It is suggested that multiple vias be used to connect this paddle to the lower-level ground planes. This method provides a good RF/thermal-conduction path for the device. Solder the exposed paddle on the bottom of the device package to the PCB. Refer to the *MAX9985 Evaluation Kit* as a reference for board layout. Gerber files are available upon request at www.maxim-ic.com.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin and TAPMAIN/TAPDIV with the capacitors shown in the *Typical Application Circuit* (see Table 2 for component values). Place the TAPMAIN/TAPDIV bypass capacitor to ground within 100 mils of the pin.

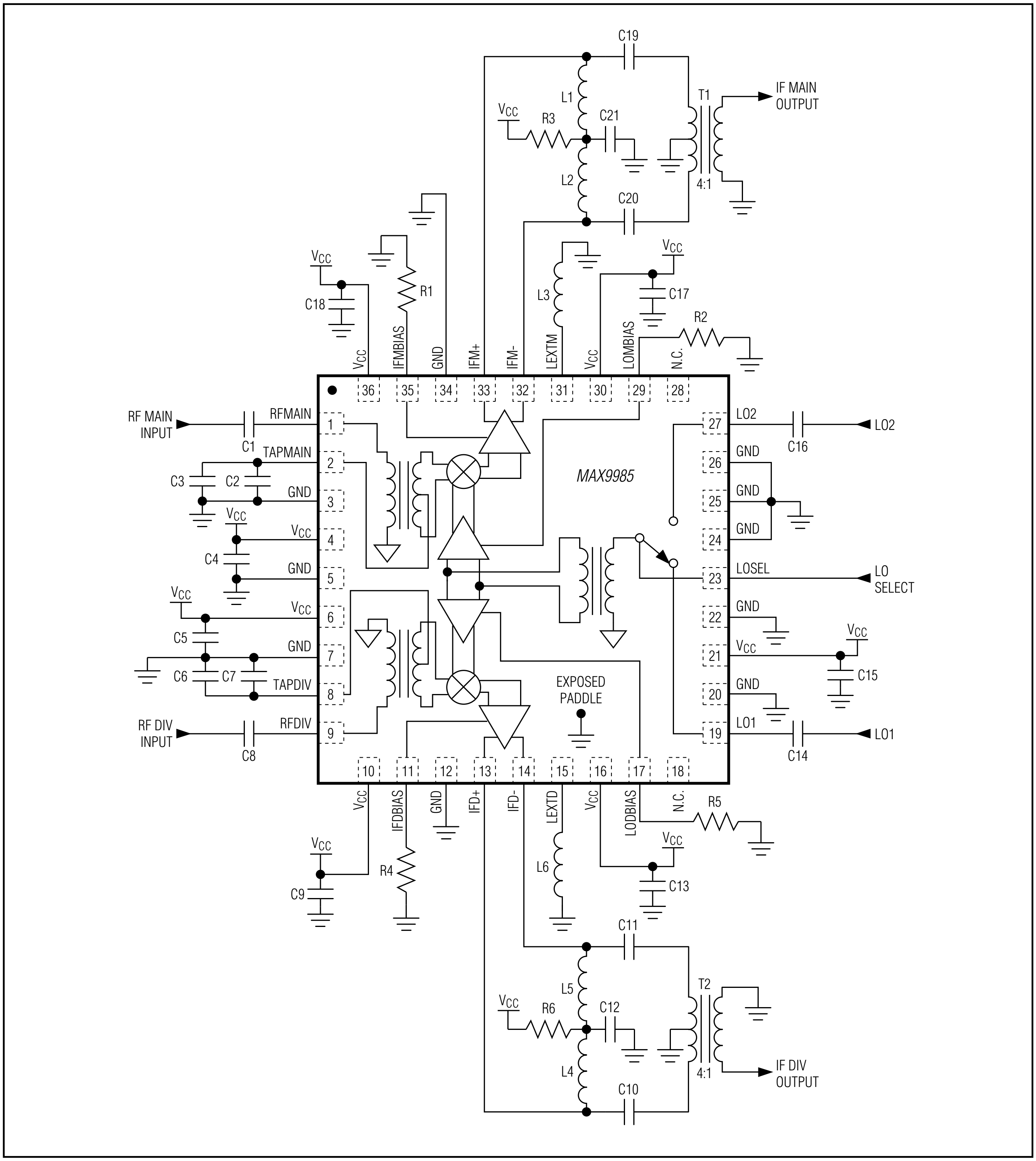
Table 2. Component Values

COMPONENT	VALUE	DESCRIPTION
C1, C2, C7, C8	39pF	Microwave capacitors (0402)
C3, C6	0.033µF	Microwave capacitors (0603)
C4, C5	—	Not used
C9, C13, C15, C17, C18	0.01µF	Microwave capacitors (0402)
C10, C11, C12, C19, C20, C21	150pF	Microwave capacitors (0603)
C14, C16	82pF	Microwave capacitors (0402)
L1, L2, L4, L5	560nH	Wire-wound high-Q inductors (0805)
L3, L6	30nH	Wire-wound high-Q inductors (0603)
R1, R4	1.07kΩ	±1% resistors (0402)
R2, R5	1.1kΩ	±1% resistors (0402)
R3, R6	0Ω	Resistors (1206)
T1, T2	4:1	Transformers (200:50) Mini-Circuits TC4-1W-7A
U1	—	MAX9985 IC

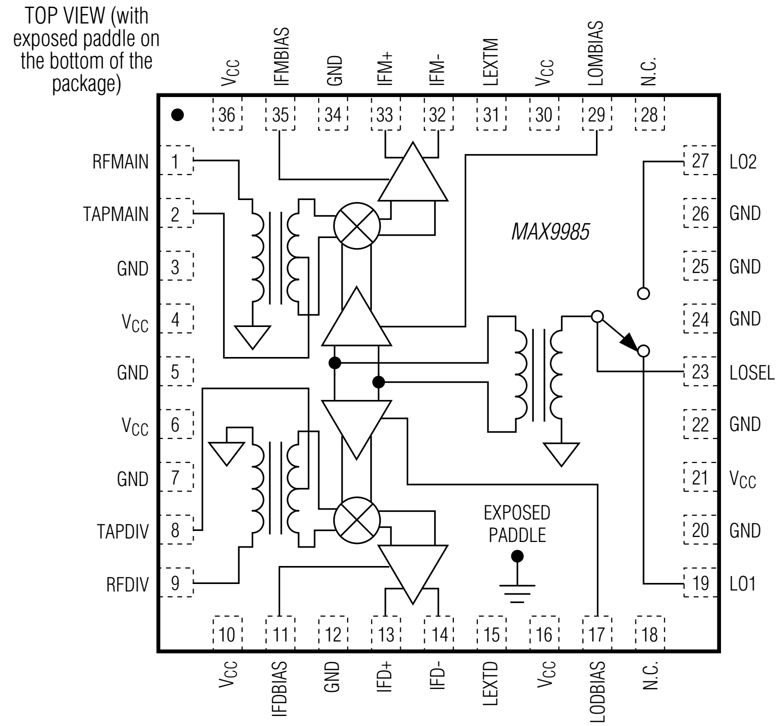
Exposed Paddle RF/Thermal Considerations

The exposed paddle (EP) of the MAX9985's 36-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX9985 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Typical Application Circuit



Pin Configuration/Functional Diagram



THIN QFN
6mm x 6mm

Chip Information

PROCESS: SiGe BiCMOS

Lead-Free/RoHS Considerations

http://www.maximintegrated.com/emmi/faq.cfm

Reliability Information:

http://www.maximintegrated.com/reliability/product/MAX9985.pdf

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/06	Initial release	—
1	1/07	Updated *Electrical Characteristics* table	2, 3
2	12/12	Updated *Electrical Characteristics* table, *Absolute Maximum Ratings*, and *Ordering Information*	1–4, 15

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