# THL3501

## 16-channel LED Driver with LVDS Interface

## Descriptions

The THL3501 is an LED driver with 16 channel open-drain outputs.

The embedded oscillator and PWM controller individually generates 256-step brightness set by the dedicated registers for each channel.

The serial interface of 2-pair LVDS lines (clock and data) features high-level noise tolerance, high-speed, and long-distance transmission.

The LVDS allowing cascaded and multidrop connection offers the maximum flexibility for designers to place and connect LED drivers.

The simple and one-way communication protocol is easily-controlled and requires less CPU resources.

## Applications

Amusement
LED Backlight
LED Display
Digital Signage
Illumination

## Features

< Driver part >
- Open-Drain Output: 16 channels
- Output Sink Current: up to 100mA/ch
- Output voltage: up to 40V
- Individual Brightness Control: 256 steps
- Group Brightness Control: 64 steps
- Output disable/enable

< Serial interface part >
- 2-pair Serial LVDS Input or 3-wire Serial CMOS Input up to 10Mbps
- Bridge Function Converting 3-wire Serial CMOS Input to 2-pair Serial LVDS Output
- Repeater function of 2-pair Serial LVDS Input / Output with Waveform and Timing Correction
- Device Address Selection up to 62 addresses
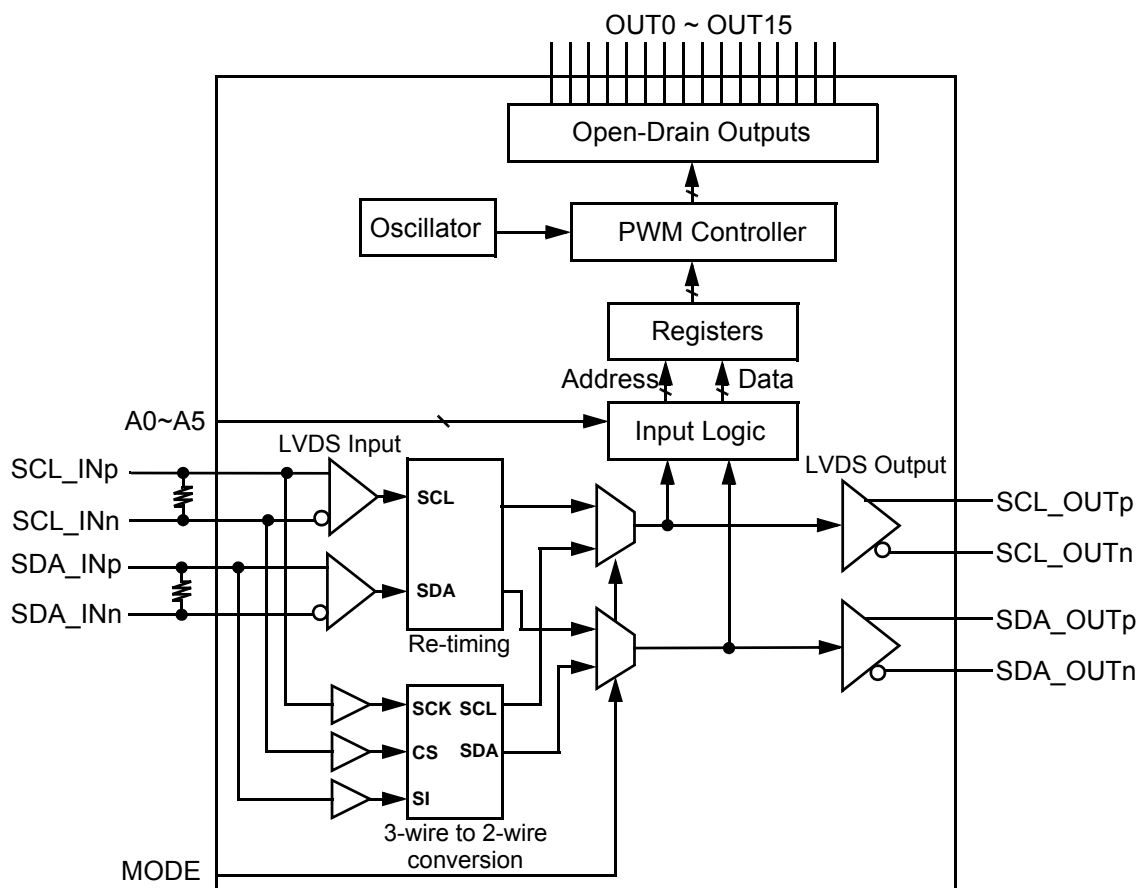- General call to all devices

Protection Circuits
  UVLO, Overcurrent Protection, Thermal Shutdown
Supply Voltage: 3.0~5.5V
Package: QFN 40-pin Exposed Pad

## Block Diagram

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD Supply Voltage | | -0.4 | | 6.0 | V |
| Digital Input Voltage *Note 1 | | -0.5 | | 6.0 | V |
| LED Driver Output Voltage | | | | 40 | V |
| Storage Temperature | | -55 | | 150 | °C |
| Junction Temperature, Tj | | | | 150 | °C |

*Note1: As for the A0 pin, the maximum value is VDD+0.5V. While power supply is not applied,
 voltage to the A0 pin must be lower than 0.5V.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD Supply Voltage | | 3.0 | | 5.5 | V |
| LED Driver Output Voltage | | | | 35 | V |
| LED Driver Output Current (Continuos) | | | | 100 | mA/ch |
| Operating Ambient Temperature, Ta | | -40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

| Parameter | Condtion | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD Supply Current *Note1 | VDD=3.3V, without LVDS output termination resistors | | 7 | | mA |
| | VDD=3.3V, with LVDS output termination resistors 100Ω | | 14 | | mA |
| | VDD=5.0V, without LVDS output termination resistors | | 10 | | mA |
| | VDD=5.0V, with LVDS output termination resistors 100Ω | | 18 | | mA |
| | VDD=5.5V, with LVDS output termination resistors 100Ω | | | 25 | mA |
| Osillator Frequency(fosc) | | | 10 | | MHz |
| UVLO Threshold Voltage (VDD Rising) | | | 2.5 | | V |
| UVLO Hysteresis | | | 0.1 | | V |
| LED Driver Output ON Resistance | VDD=3.0V | | | 4 | Ω |
| | VDD=3.3V | | 2 | | Ω |
| | VDD=5.0V | | 1.7 | | Ω |
| LED Driver Output Leakage Current | | | | 10 | µA |
| Digital Input, High Level Voltage (VIH) | | 0.7VDD | | | V |
| Digital Input, Low Level Voltage (VIL) | | | | 0.3VDD | V |
| Digital Input, Hysteresis | | 0.05VDD | | | V |
| Digital Input, Leakage Current | | | | ±10 | µA |
| LVDS Input, Differential Voltage (VID) | VIC=1.2V | ±100 | | | mV |
| LVDS Input, Leakage Current | | | | ±30 | µA |
| LVDS Output, Differential Voltage (VOD) | VDD=3.0V | 240 | | | mV |
| | VDD=3.3V | | 350 | | mV |
| | VDD=5.0V | | 420 | | mV |
| | VDD=5.5V | | | 480 | mV |
| LVDS Output, Common Mode Voltage (VOC) | | 1.1 | 1.25 | 1.4 | V |

3-wire Serial CMOS Level Input (MODE=High)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| fSCK | SCK Frequency | | | | 10 | MHz |
| tCH | SCK High Time | | 40 | | | ns |
| tCL | SCK Low Time | | 40 | | | ns |
| tDVCH | SI Setup Time | | 10 | | | ns |
| tCHDX | SI Hold Time | | 10 | | | ns |
| tCHSL | CSn Not Active Hold Time | | 40 | | | ns |
| tSLCH | CSn Active Setup Time | | 40 | | | ns |
| tCHSH | CSn Active Hold Time | | 40 | | | ns |
| tSHCH | CSn Not Active Setup Time | | 40 | | | ns |
| tSHSL | CSn Not Active Time | | 200 | | | ns |

2-pair Serial LVDS Output

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| tr, tf | SCL, SDA Transition Time | *2 | | | 10 | ns |
| tSTAH | Header Condition Hold Time | | 6 | 10 | 20 | ns |
| tDSU | SDA Setup Time | | 6 | 10 | 20 | ns |
| tDHO | SCL Falling Edge Hold Time | | 5 | | | ns |
| tPWE | End Pulse Width | | 25 | 40 | 70 | ns |
| tPD | SCL Propagation Delay | | | | 30 | ns |

2-pair Serial LVDS Input (MODE=Low)

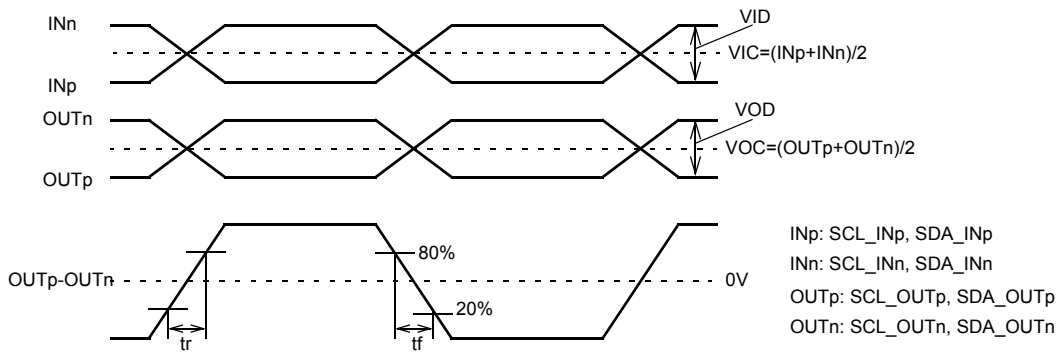| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| fSCL | SCL Frequency | | | | 10 | MHz |
| tDAH | SCL High Time | | 25 | | | ns |
| tDAL | SCL Low Time | | 25 | | | ns |
| tSTAH | Header Condition Hold Time | | 4 | | | ns |
| tDSU | SDA Setup Time | | 4 | | | ns |
| tDHO | SCL Falling Edge Hold Time | | 3 | | | ns |

*1. In cascading connection, termination resistors are necessary for LVDS outputs. In this case, 2.4mA to 4.8mA current flows at each resistor depending on the power supply voltage. Therefore, the current consumption is larger than the case without the termination resistors.

< With termination resistors >          < Without termination resistors >
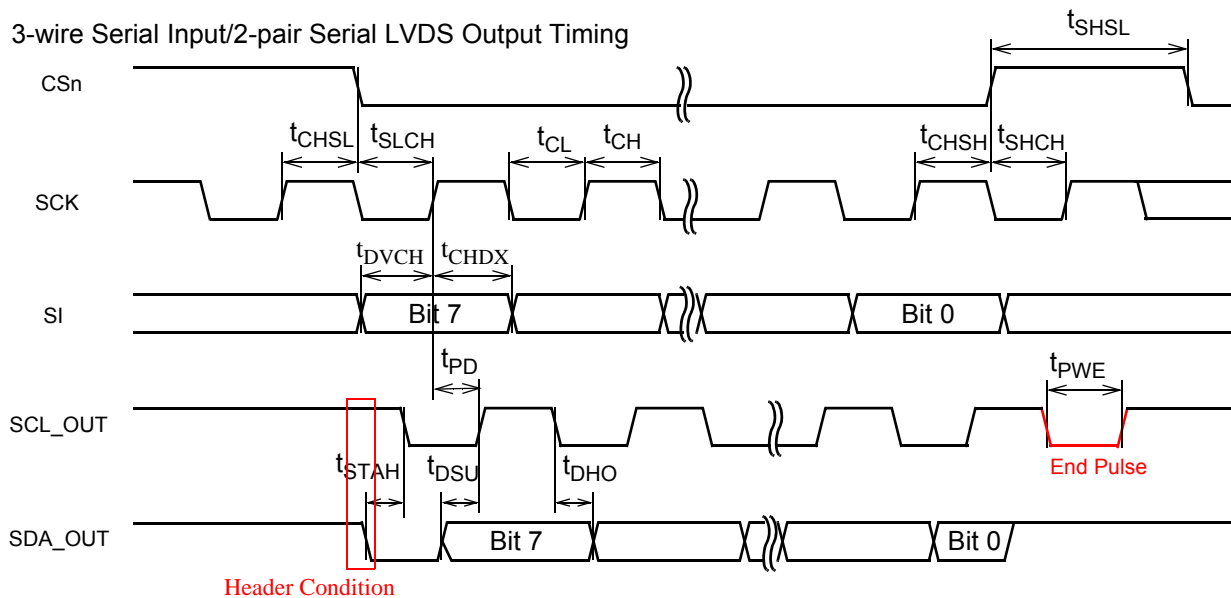
SCL_OUTp
SCL_OUTn          100Ω          Open

SDA_OUTp
SDA_OUTn          100Ω          Open
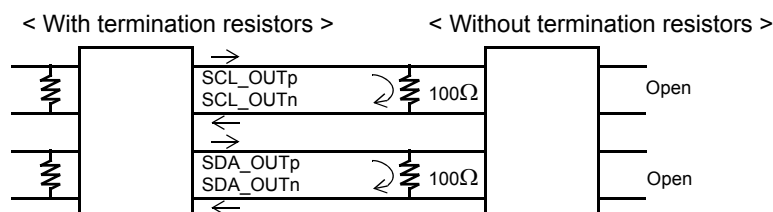
*2. SCL, SDATransition Time Measurement Condition

OUTp          Load Capacitance:50pF
              Termination Resistor:100Ω
OUTn

## LVDS Spec



```
INn
INp                                    VID
                                       VIC=(INp+INn)/2
OUTn
                                       VOD
OUTp                                   VOC=(OUTp+OUTn)/2

                        80%
OUTp-OUTn                              0V
                        20%
         tr        tf

INp: SCL_INp, SDA_INp
INn: SCL_INn, SDA_INn
OUTp: SCL_OUTp, SDA_OUTp
OUTn: SCL_OUTn, SDA_OUTn
```
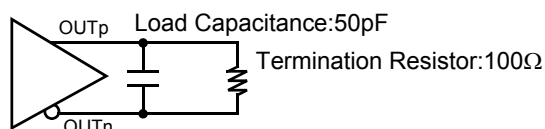
## Timing Diagram

3-wire Serial Input/2-pair Serial LVDS Output Timing



2-pair Serial LVDS Input/Output Timing
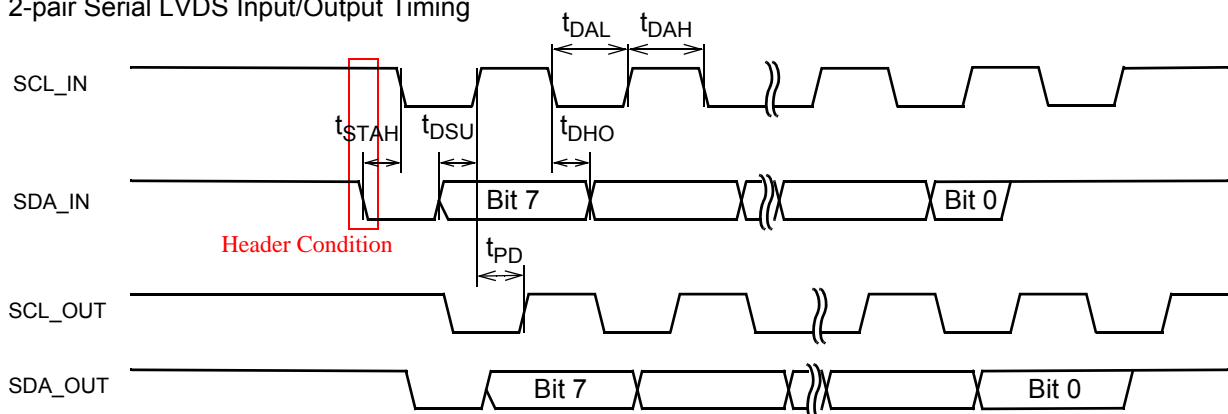


* Abbreviation

This documents refers to the differential signals in unipolar shorthand; for example, SCL_IN, SDA_IN, SCL_OUT, and SDA_OUT mean (SCL_INp - SCL_INn), (SDA_INp - SDA_INn), (SCL_OUTp - SCL_OUTn), and (SDA_OUTp - SDA_OUTn) respectively.

* A falling transition of the SDA_IN while the SCL_IN is high is defined as "Header Condition". Please refer to the section "2-pair Serial LVDS Input" for details.

## PIN CONFIGURATIONS

(Top View)
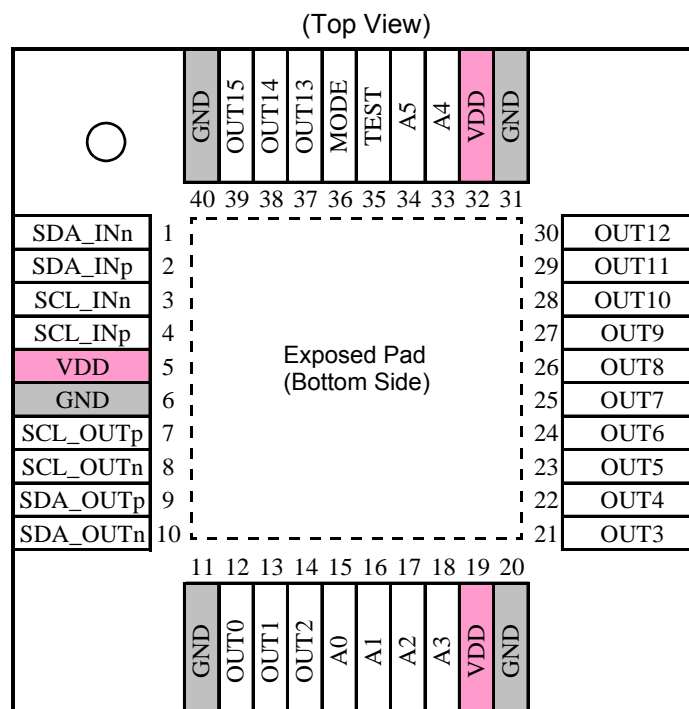


* The exposed pad is connected to GND inside the device.
  The exposed pad should be soldered to GND on the PCB.

## PIN DESCRIPTION

| Pin Name | Type | Description |
|---|---|---|
| MODE | Digital Input | Serial Interface Input Mode Select<br>Low: 2-pair Serial LVDS Input<br>High: 3-wire Serial CMOS Input |
| SCL_INp(SCK) | LVDS Input/<br>Digital Input | MODE=Low: 2-pair Serial LVDS Clock Input - Positive<br>MODE=High: 3-wire Serial Clock Input (SCK) |
| SCL_INn(CSn) | LVDS Input/<br>Digital Input | MODE=Low: 2-pair Serial LVDS Clock Input - Negative<br>MODE=High: 3-wire Serial Chip Select Input (CSn) |
| SDA_INp(SI) | LVDS Input/<br>Digital Input | MODE=Low: 2-pair Serial LVDS Data Input - Positive<br>MODE=High: 3-wire Serial Data Input (SI) |
| SDA_INn | LVDS Input/<br>Digital Input | MODE=Low: 2-pair Serial LVDS Data Input - Negative<br>MODE=High: Reserved (Connect to Low) |
| SCL_OUTp | LVDS Output | 2-pair Serial LVDS Clock Output - Positive |
| SCL_OUTn | LVDS Output | 2-pair Serial LVDS Clock Output - Negative |
| SDA_OUTp | LVDS Output | 2-pair Serial LVDS Data Output - Positive |
| SDA_OUTn | LVDS Output | 2-pair Serial LVDS Data Output - Negative |
| OUT0-OUT15 | Open-Drain<br>Output | LED Driver Output Channel 0 - 15 |
| TEST | Digital Input | Test Pin (Connect to Low) |
| A0-A5 | Digital Input | Device address input Bit0 - 5 |
| VDD | — | Power supply |
| GND | — | Ground |

## REGISTER NOTATION

Address is noted in hex with the prefix "R".     For example, R00 is a register of address 00.
Bit location is noted by "[]".     For example, R00[5:0] is bit 5 down to bit 0 of address 00.
Register value is noted in binary with the suffix "b".     For example, R00[5:0]=000000b
Register value is noted in decimal without a suffix.     For example, R04[7:0]=160
Register value is noted in hex with the suffix "h".     For example, R04=A0h

## REGISTER MAP

| Address | Default | Function | Description |
|---|---|---|---|
| R00[7] | 0 | PWM Phase Control Mode | 0: Normal Mode<br>1: Group Control Mode |
| R00[6] | 0 | LED Output Enable | 0: Output Disable<br>1: Output Enable |
| R00[5:0] | 000000b | Global Brightness | Global Brightness=(Value+1)/64 |
| R01[7:0] | 00h | Reserved | Set to 00h |
| R02[7:0] | 00h | Reserved | |
| R03[7:0] | 00h | Reserved | |
| R04[7:0] | 00h | Individual Brightness - OUT0 | Individual Brightness=Value/256 |
| R05[7:0] | 00h | Individual Brightness - OUT1 | |
| R06[7:0] | 00h | Individual Brightness - OUT2 | |
| R07[7:0] | 00h | Individual Brightness - OUT3 | |
| R08[7:0] | 00h | Individual Brightness - OUT4 | |
| R09[7:0] | 00h | Individual Brightness - OUT5 | |
| R0A[7:0] | 00h | Individual Brightness - OUT6 | |
| R0B[7:0] | 00h | Individual Brightness - OUT7 | |
| R0C[7:0] | 00h | Reserved | Set to 00h |
| R0D[7:0] | 00h | Reserved | |
| R0E[7:0] | 00h | Individual Brightness - OUT8 | Individual Brightness=Value/256 |
| R0F[7:0] | 00h | Individual Brightness - OUT9 | |
| R10[7:0] | 00h | Individual Brightness - OUT10 | |
| R11[7:0] | 00h | Individual Brightness - OUT11 | |
| R12[7:0] | 00h | Individual Brightness - OUT12 | |
| R13[7:0] | 00h | Individual Brightness - OUT13 | |
| R14[7:0] | 00h | Individual Brightness - OUT14 | |
| R15[7:0] | 00h | Individual Brightness - OUT15 | |
| R16[7:0] | 00h | Reserved | Set to 00h |
| R17[7:0] | 00h | Reserved | |
| R18[7:0] | 00h | Reserved | |

# FUNCTIONAL DESCRIPTION

## Writing to registers

The device includes 25-byte registers (R00-R18) for setting. Writing to registers is executed through the serial interface and the value is maintained as long as power is applied. The register value can not be read.

Writing to registers should be invoked after the power supply (VDD) of all the devices in cascading and multidrop connection gets stable above 3.0V.

Then after power-up, if using 2-pair serial LVDS input, initialization of 2-pair serial LVDS input must be done before writing to registers. Writing to registers. However, in case all the registers are continuously rewritten, in other words repeatedly refreshed, the initialization of 2-pair serial LVDS input is not necessary after power-up and instantaneous interruption.

Please refer to the section "Initialization of 2-pair Serial LVDS Input" for details.

## UVLO

The device has an internal UVLO (Under-Voltage Locked-Out) circuit to prevent the device from malfunction at low supply voltage. Until power supply (VDD) has reached 2.5V (typical value), the UVLO holds the internal logic circuit in a reset condition, and keeps the LED driver outputs and LVDS outputs in Hi-Z state. The UVLO circuit has hysteresis. If power supply falls below 2.4V (typical value), the device gets into the above UVLO state in which the internal logic circuit is reset and the regsiters are reset to default value.
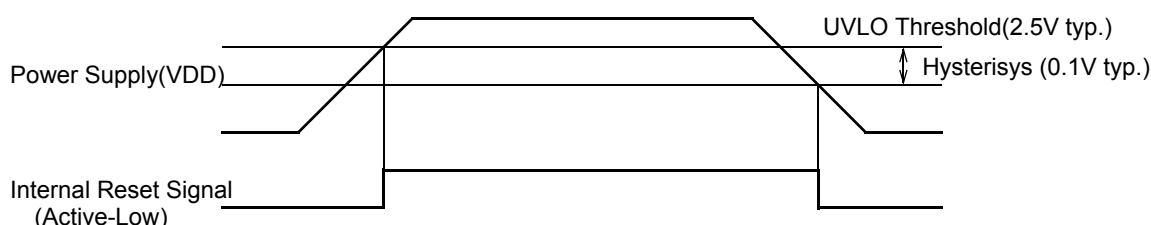


## Overcurrent Protection

The device includes overcurrent protection circuits for each LED output pin to prevent the LED driver outputs from driving excessive current.

If LED driver outputs turn on with the pins shorted to power supply, overcurrent flowing in output transistors may causes permanent damage to the device. The overcurrent protection is a function to shutdown outputs immediately when the device detects overcurrent condition on output pins. If short circuit condition is resolved, normal operation automatically resumes.

However, this function can not always prevent breakdown or damage to the device depending on usage situation and duration of abnormality.

## Thermal Shutdown

The device includes thermal shutdown circuit to prevent damages caused by excessive heat. If the junction temperature exceeds the absolute maximum rating (Tj=150°C), the thermal shutdown circuit turn off all LED driver outputs. The Thermal shutdown circuits has hysteresis. If Tj falls enough, normal operation automatically resumes.
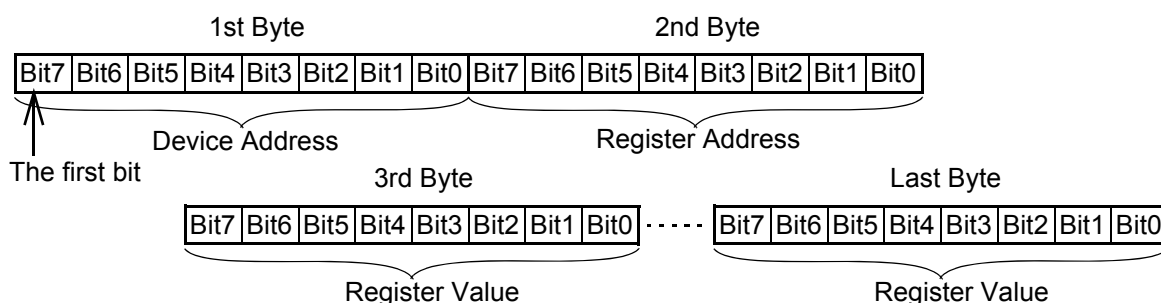
However, this function can not always prevent breakdown or damage to the device depending on usage situation and duration of abnormality.

## Serial Communication Protocol

2-pair serial LVDS input or 3-wire serial CMOS level input is selected as a serial interface for register setting by the MODE pin. The 2-pair serial LVDS input and 3-wire serial CMOS level input share input pins (SCL_INp/SCL_INn, SDA_INp/SDA_INn) which are used as 2-pair serial LVDS input when the MODE pin is set to low, and used as 3-wire serial CMOS level input when the MODE pin is set to high.

- The serial interface is clock synchronous and used only for writing to registers (one-way communication).
- The data length is 8-bit in MSB first bit order. As for how to recognize the first bit, please refer to the section "2-pair serial LVDS input" and "3-wire serial CMOS level input".
- The first 8 bits that includes the first bit is defined as "1st byte" and the next 8 bits as "2nd byte" and so on.
- "1st Byte" is assigned to the device address. If device address is set to 00h, all the devices are selected to be written except the device which has a device address 00111111 by the A5-A0 pins.
- "2nd Byte" is assigned to the register address.
- The bytes after "3rd Byte" is assigned to register values to write. The register address is incremented every time 8-bit register value is written. For example, the value of "3rd Byte" is written to the register at the address indicated in "2nd byte", and the value of "4th byte" is written to the register at the address ("2nd byte"+1).
- Don't write except the registers R00-R18

**< Serial Data >**

```
          1st Byte                         2nd Byte
 Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0
  ^
  |          Device Address                   Register Address
The first bit        3rd Byte                        Last Byte
          Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 ····· Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0
                  Register Value                          Register Value
```

## Device Address Setting

The lower 6 bits out of 8-bit serial interface device address are set by the A0-A5 pin.The higher 2 bits are fixed at 00. For example,
 in case A5=Low, A4=Low, A3=Low, A2=Low, A1=Low, A0=High,
 the device address is set to 00000001 (01h).

- If the A0-A5 pins are all set to high, the register of the device can not be written. Please set all the A0-A5 pins to high in order to use only 2-pair to 2-pair repeater function or 3-wire to 2-pair bridge function without using LED driver outputs.
- Since the device address 00000000 (00h) is the one to be used for writing to all devices, basically don't use it.
- Please set device addresses within the range from 00000001 (01h) to 00111110 (3Eh).

## Serial Interface Connection

THL3501 (16-channel open-drain outputs), THL3502(24-channel open-drain outputs), THL3503(16-channel constant-current outputs), and THL3504(24-channel constant-current outputs) are all communication protocol compatible with each other so that they can be mixed in cascade and multidrop connection scheme (Please note that multiple LVDS outputs can not be connected to each other.).

\* THL3501, THL3502, THL3503, and THL3504 are collectively referred to as THL350X hereafter.

## Cascade Connection by 2-pair serial LVDS

The THL350X can convert 3-wire serial output from the host such as micro-controller or CPU to 2-pair serial LVDS, which is connected to the 2-pair serial LVDS input of a following device in a point-to-point topology. As for the maximum number of devices to be cascaded, please refer to an application note.
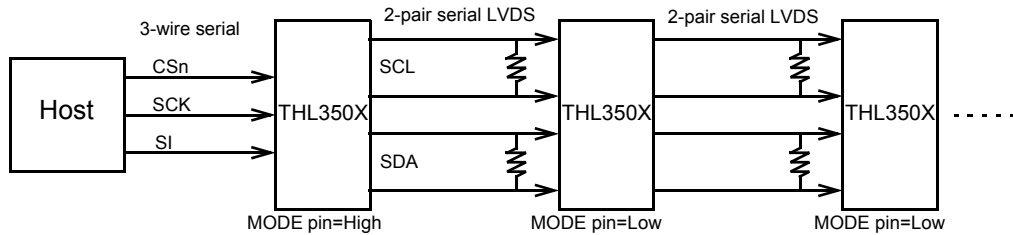


## Multidrop Connection by 2-pair serial LVDS

The THL350X can convert 3-wire serial output from the host such as micro-controller or CPU to 2-pair serial LVDS, which is connected to the 2-pair serial LVDS input of following multiple devices in a multidrop topology. As for the maximum number to devices to be multidropped, please refer to an application note.
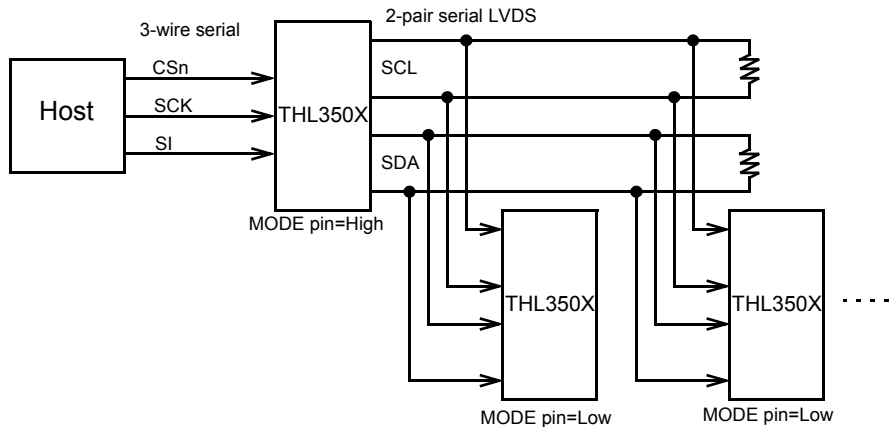


## Multidrop Connection by 3-wire serial

3-wire serial output from the host such as micro-controller or CPU to 2-pair serial LVDS is connected to following multiple devices in a multidrop topology.
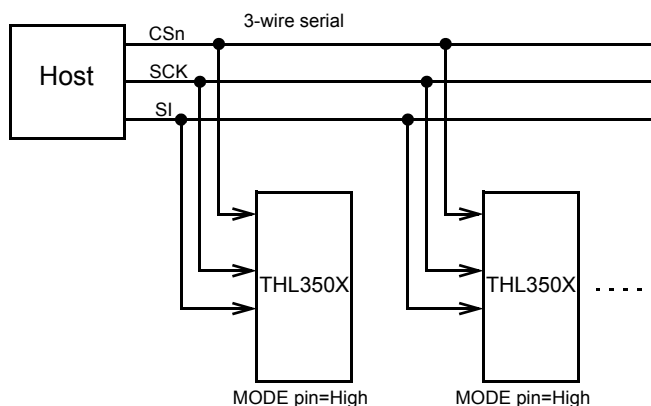
## 3-wire Serial CMOS Level Input

When the MODE pin is set to high, the serial interface for writing to registers becomes 3-wire serial CMOS level input. The chip select (CSn), serial clock (SCK), serial data (SI) of 3-wire serial CMOS level input are input to the SCL_INn pin, the SCL_INp pin, the SDA_IN pin respectively. The SDA_INn must be tied to low.

- While the CSn stays low, the data input SI is latched by rising edges of the clock input SCK.
- The data latched by the first clock rising edge after the CSn falls is assigned the "first bit".
- The "Last Byte" is written to a register when the CSn rises after Bit0 (in other words, "Last Byte" will not be written to a register until the CSn rises).
- If the CSn rises in the middle of a byte, the byte is not written to a register, then the communication resumes from "1st Byte" when the CSn falls next.

**< 3-wire Serial CMOS Level Input >**
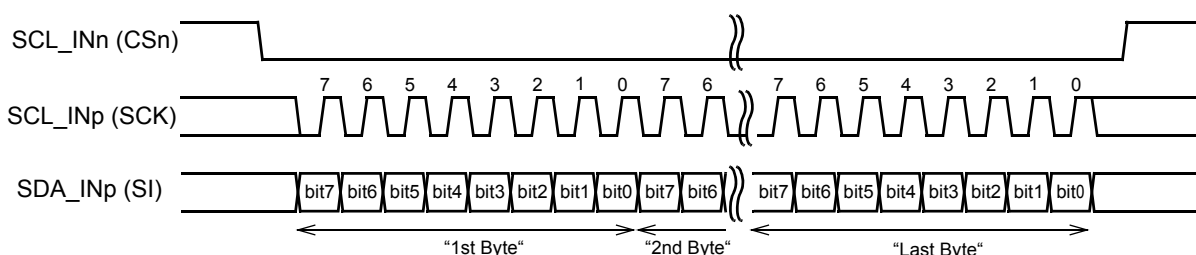


## 2-pair serial LVDS

When the MODE pin is set to low, the serial interface for writing to registers becomes 2-pair serial LVDS input (SCL_INp/SCL_INn, SDA_INp/SDA_INn).

- The data input SDA_IN is latched by rising edges of the clock input SCL_IN.
- A falling transition of the SDA_IN while the SCL_IN is high is defined as "Header Condition", and the data latched by the first clock rising edge after the "Header Condition" is assigned the "first bit". Except "Header Condition", the transitions of the data input SDA_IN are allowed while the clock input SCL_IN is low.
- The "Last Byte" is written to a register at the reception of an active-low pulse "End Pulse" (actually, "Last Byte" is written to a register at the rising edge of the "End Pulse"). When the "End Pulse" rises, the data output SDA_OUT must be high.
- If the "Header Condition" is received in the middle of a byte, the byte is not written to a register, then the communication resumes from "1st Byte".
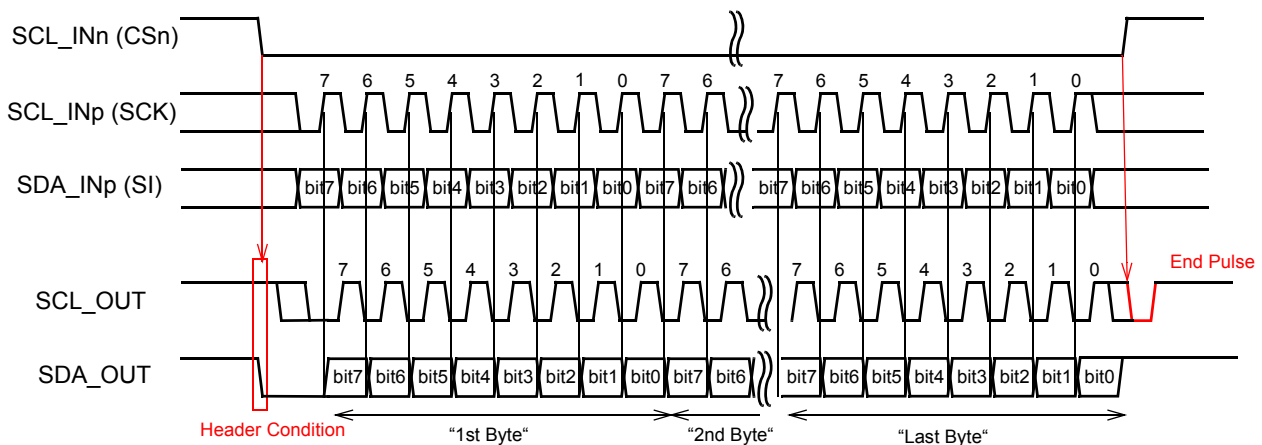
**< 2-pair serial LVDS input >**
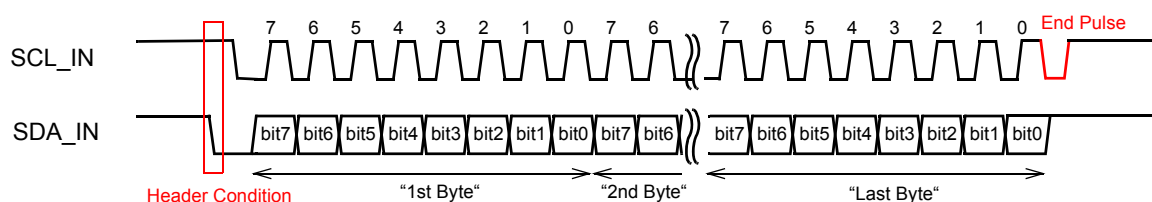


* The 3-wire to 2-pair bridge function can convert 3-wire serial output from the host such as micro-controller or CPU to 2-pair sereal LVDS. Please refer to the section "3-wire to 2-pair bridge function" for details.

## 3-wire to 2-pair bridge function

When the MODE pin is set to high, the serial interface for writing to registers becomes 3-wire serial CMOS level input (CSn, CK, SI), which is converted to 2-wire serial and transferred to the LVDS output pins.

- While the CSn is active low, the data input SI is latched and transferred to the LVDS output SDA_OUT on the rising edges of the clock input SCK. There is about 10ns setup time between the clock output SCL_OUT and the data output SDA_OUT.
- When the CSn falls, "Header Condition" is generated on 2-pair LVDS output.
- After the CSn rises, an active-low pulse "End Pulse" (the pulse width: 40ns typ) is added on the clock output SCL_OUT.
- When the CSn rises, the data output SDA_OUT is forced high. In the result, the low to high transition of the clock output SCL_OUT "End Pulse" occurs while the data output SDA_OUT is high

**< 3-wire to 2-pair bridge >**



## 2-pair to 2-pair repeater function

When the MODE pin is set to low, the serial interface for writing to registers becomes 2-pair serial LVDS input (SCL_INp/SCL_INn, SDA_INp/SDA_INn). The timing between the clock and the data is compensated and then they are transferred to the LVDS output pins.

- The data input SCL_IN is latched and transferred to the LVDS output SDA_OUT on the rising edges of the clock input SCL_IN. There is about 10ns setup time between the clock output SCL_OUT and the data output SDA_OUT.
- The "Header Condition" is regenerated and transferred to the output.
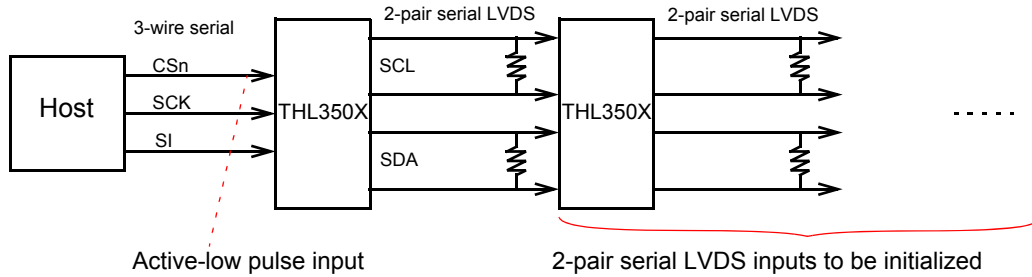
**< 2-pair to 2-pair repeater function >**
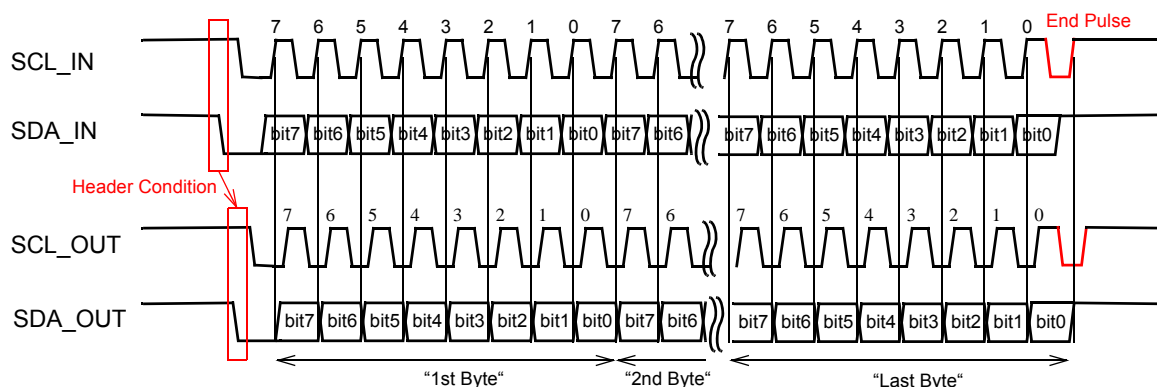
# Initialization of 2-pair Serial LVDS Input

After power-up, if using 2-pair serial LVDS input, initialization of 2-pair serial LVDS input must be done before writing to registers. Without the initialization of 2-pair serial LVDS input, the first writing to registers ("1st Byte"-"Last Byte") may possibly fail. However, the initialization of 2-pair serial LVDS input is not necessary in case failure in the first writing to registers can be allowed; for example, in case all the registers (R00-R18) are continuously rewritten, in other words repeatedly refreshed.

In order to initialize 2-pair serial LVDS input, please input active-low pulse (pulse width: 200ns min.) of the CSn into 3-wire serial CMOS level input of the first device which converts 3-wire to 2-pair. In consequence, the 2-pair serial LVDS input of all the following devices are initialized. In cascading connection, it takes the propagation delay of all stages in cascaded chain to finish the initialization of 2-pair serial LVDS input.
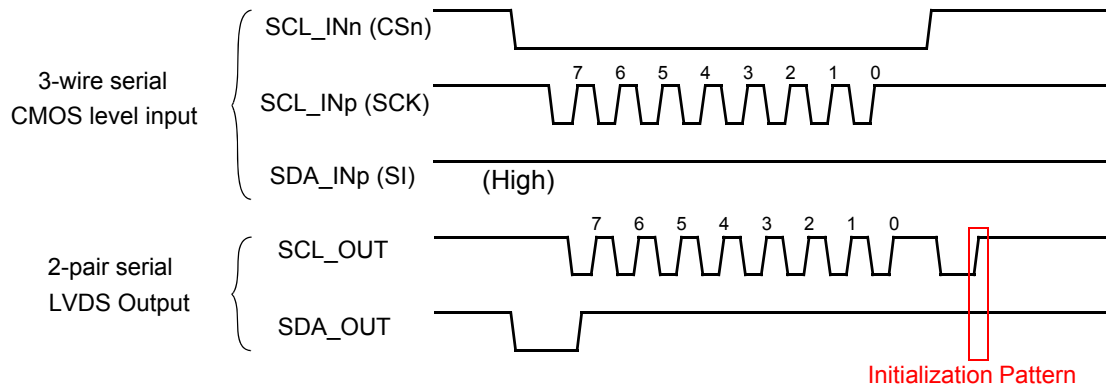


**< Initialization of 2-pair Serial LVDS Input >**

Initialization Pattern Example 1

Input active-low pulse input to the CSn
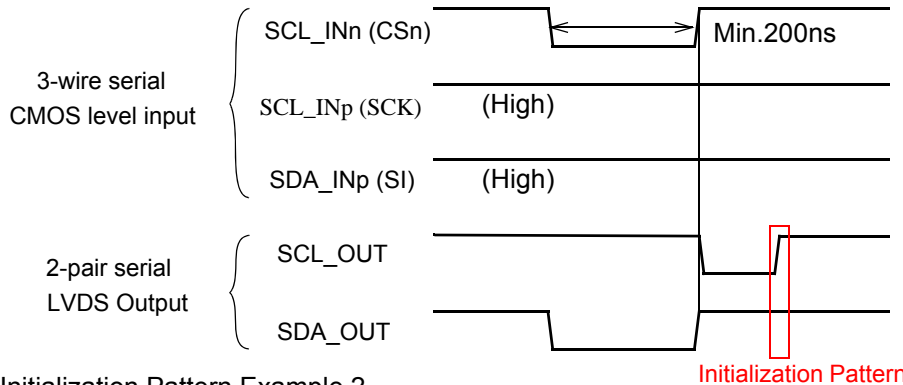


Initialization Pattern Example 2

Input 1st Byte (Device Address)=FFh

## Individual Brightness Control

The Brightness for each LED output channel (OUT0-OUT15) are individually programmable in 256 steps by the register configuration (R01-R15). The individual Brightness is controlled by PWM duty cycle.
The ratio of ON time for the open-drain outputs is expressed in the following equation.

ON time ratio = Individual Brightness Control Register Value / 256

The bigger setting value results in the larger ON time ratio, therefore higher brightness. When the register value is 0, the output current sink is held OFF, therefore the LED turns off.
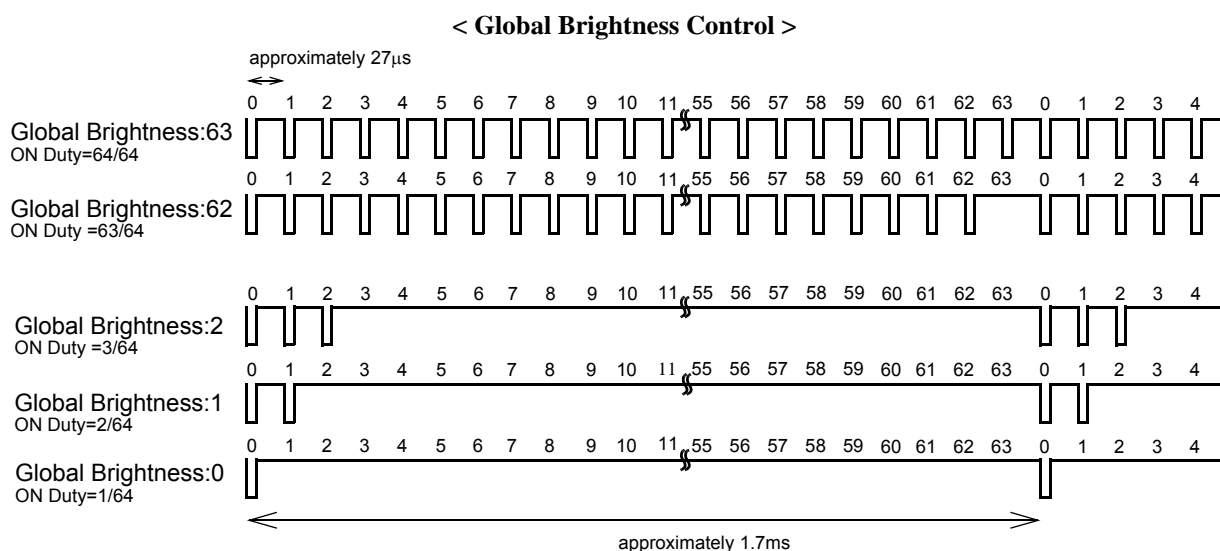
**< Individual Brightness Control >**
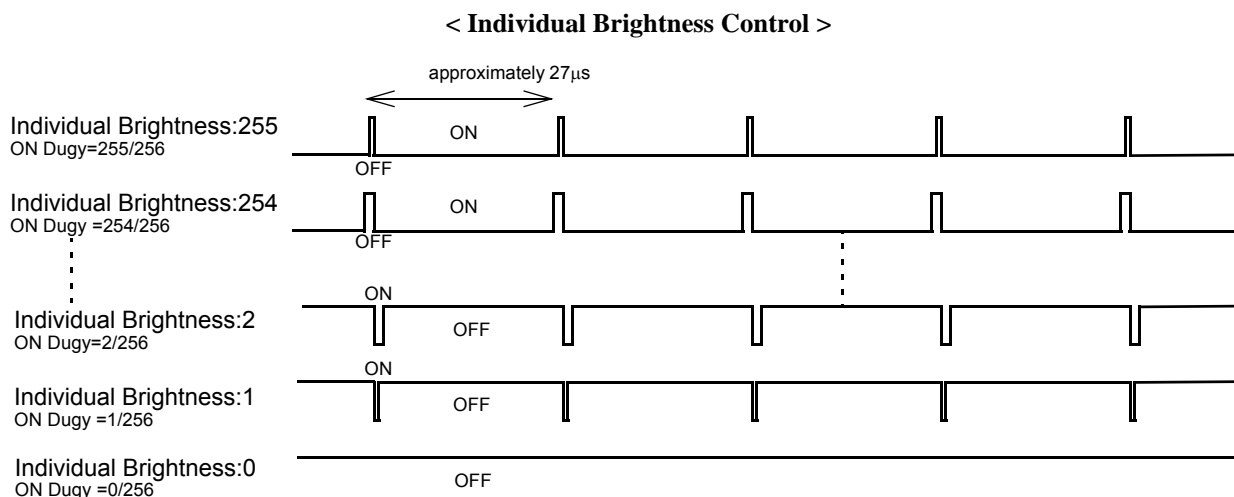


## Global Brightness Control

In addition to the individual brightness control for each LED driver output channels, the brightness of all channels is globally programmable in 64 steps by the register configuration (R00[5:0]). The global brightness controller partially masks pulses generated by the individual brightness controller.
The ratio of ON time for the open-drain outputs which is totally set by both the individual brightness control and global brightness control is expressed in the following equation.

ON time ratio = (Individual Brightness Control register value/256) x (Global Brightness Control register value+1)/64
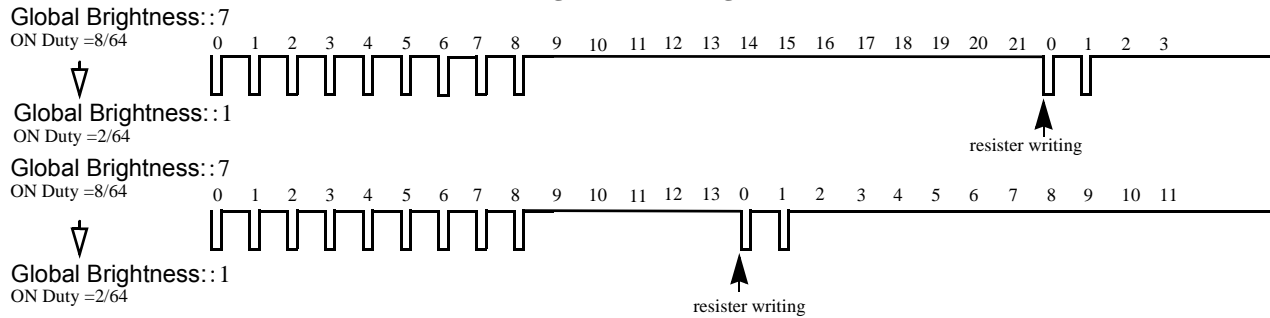
The bigger setting value results in the larger ON time ratio, therefore higher brightness.

**< Global Brightness Control >**

## Increment timing of Global Brightness Control

Global brightness control is started soon at the timing of incremented.new resister data and previous data is destructed.
Therefore, please be careful about brightness changes for short periods depending on the timing of incremented new data.

**< Increment timing of Global Brightness Control>**



Global Brightness::7
ON Duty =8/64

Global Brightness::1
ON Duty =2/64

resister writing

Global Brightness::7
ON Duty =8/64

Global Brightness::1
ON Duty =2/64

resister writing

## PWM Phase Control Mode

The PWM pulse start position of each channel is controlled in different phases to reduce switching noise.
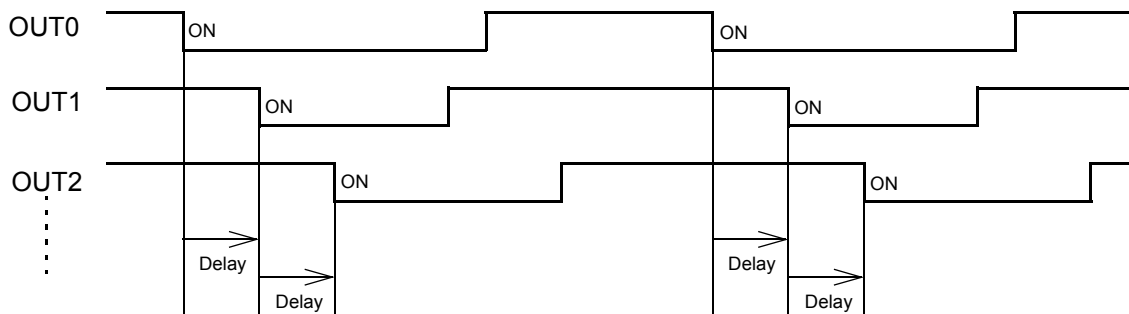The phase control mode is selectable in 2 ways by the register configuration (R00[7]).
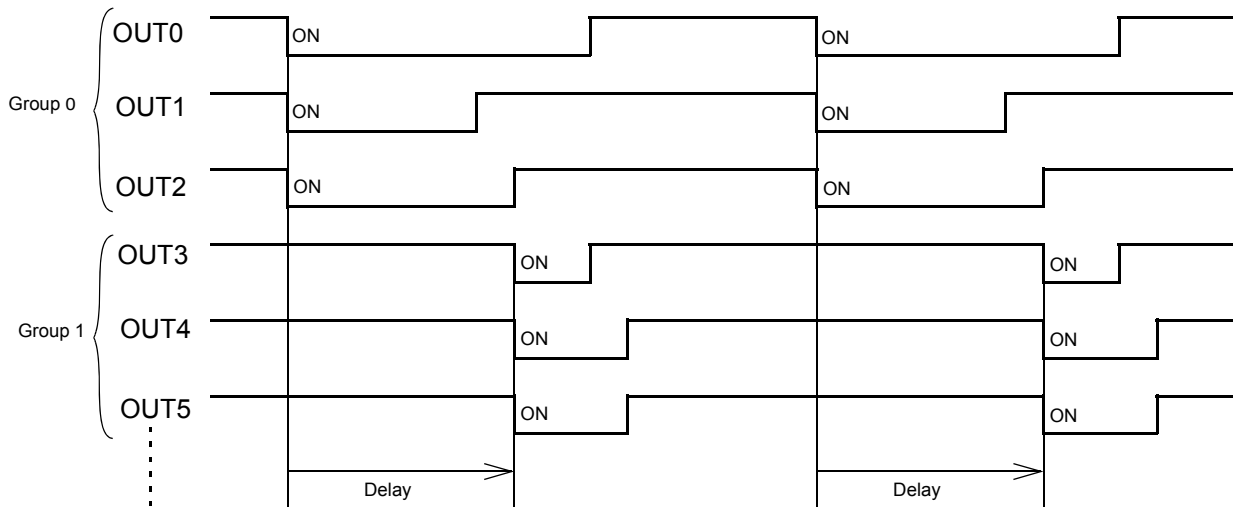In normal mode (R00[7]=0), the PWM pulse start positions of all channels are different from each other.
In group control mode (R00[7]=1), the PWM pulse start positions of 2 or 3 channel groups are different from each other.

**< PWM Phase Control Mode >**



Normal Mode(R00[7]=0)

Group Control Mode(R00[7]=1)

When multiple LED output channels need to be connected in parallel to drive, the PWM phase control mode must be set to group control mode (R00[7]=1), and the channels in the same group must be connected in parallel to drive.

< Grouping of Group Control Mode >

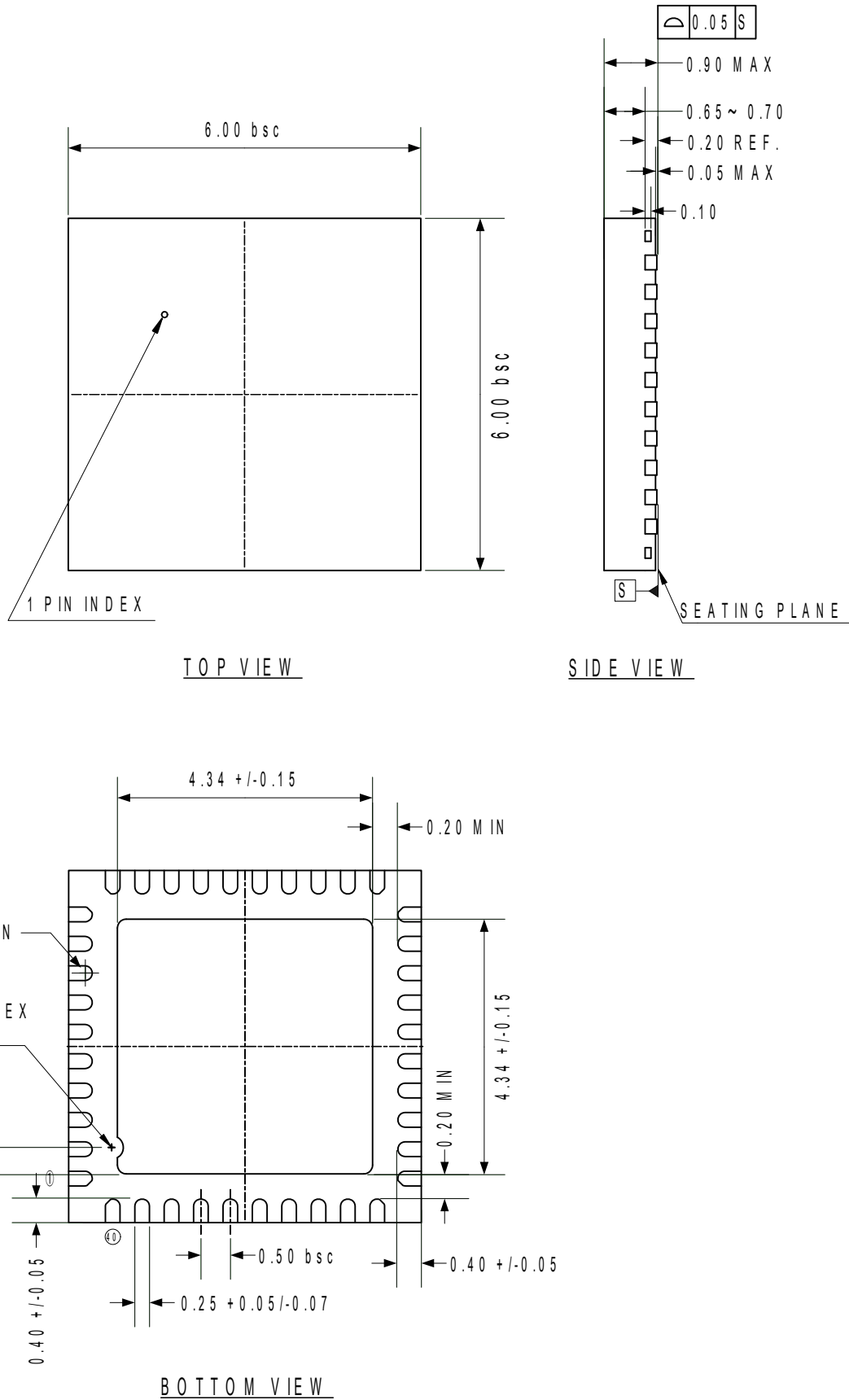| Group | Output Channel |
|-------|----------------|
| Group0 | OUT0, OUT1, OUT2 |
| Group1 | OUT3, OUT4, OUT5 |
| Group2 | OUT6, OUT7 |
| Group3 | OUT8, OUT9 |
| Group4 | OUT10, OUT11, OUT12 |
| Group5 | OUT13, OUT14, OUT15 |
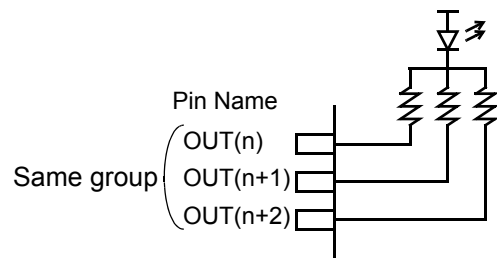


## LED Driver Output Enable

All of the LED driver outputs can be disabled by register configuration (R00[6]). When disabled (R00[6]=0), all of the LED driver outputs go into OFF (Hi-Z) state, LEDs turn off.

Package Dimensions

QFN 40-pin



0.05 S

0.90 MAX

0.65 ~ 0.70

0.20 REF.

0.05 MAX

0.10

6.00 bsc

6.00 bsc

1 PIN INDEX

TOP VIEW

S   SEATING PLANE

SIDE VIEW

4.34 +/-0.15

0.20 MIN

0.09 MIN

1 PIN INDEX
0.20 R

0.45

4.34 +/-0.15

0.20 MIN

40

0.50 bsc

0.40 +/-0.05

0.40 +/-0.05

0.25 +0.05/-0.07

BOTTOM VIEW

Unit:mm

## *Notices and Requests*

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
9. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damage s may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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### Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

Вы  можете разместить у нас заказ  для любого Вашего  проекта, будь то серийное   производство  или  разработка единичного прибора.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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