

Infrared Encoder/Decoder

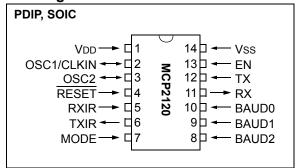
Features

- Supports with IrDA[®] Physical Layer Specification (version 1.3)
- · UART to IR Encoder/Decoder
 - Interfaces with IrDA Compliant Transceivers
 - Used with any UART, including standard 16550 UART and microcontroller UART
- · Transmit/Receive formats supported:
 - 1.63 µs
- · Hardware or Software Baud rate selection
 - Up to IrDA standard 115.2 kbaud operation
 - Up to 312.5 kbaud operation (at 20 MHz)
 - Low power mode
- · Pb-free packaging

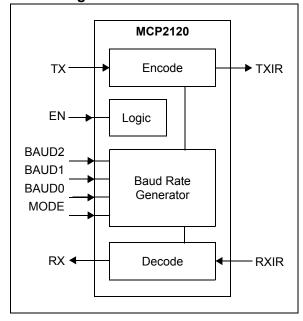
CMOS Technology

- · Low-power, high-speed CMOS technology
- · Fully static design
- · Low voltage operation
- Commercial and Industrial temperature ranges
- · Low power consumption
 - < 1 mA @ 3.3V, 8 MHz (typical)
 - 3 mA typical @ 5.0V when disabled

Pin Diagrams



Block Diagram



NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the following device:

MCP2120

This device is a low-cost, high-performance, fully-static infrared encoder/decoder. This device sits between a UART and an infrared (IR) optical transceiver.

The data received from a standard UART is encoded (modulated), and output as electrical pulses to the IR Transceiver. The IR Transceiver also receives data which it outputs as electrical pulses. The MCP2120 decodes (demodulates) these electrical pulses and then the data is transmitted by the MCP2120 UART. This modulation and demodulation method is performed in accordance with the IrDA standard.

Typically a microcontroller interfaces to the IR encoder/decoder.

Infrared communication is a wireless two-way data connection using infrared light generated by low-cost transceiver signaling technology. This provides reliable communication between two devices.

Infrared technology offers:

- Universal standard for connecting portable computing devices
- · Easy, effortless implementation
- Economical alternative to other connectivity solutions
- · Reliable, high speed connection
- Safe to use in any environment; can even be used during air travel
- · Eliminates the hassle of cables
- Allows PC's and non-PC's to communicate to each other
- Enhances mobility by allowing users to easily connect

1.1 Applications

The MCP2120 is a stand—alone IrDA Encoder/Decoder product. Figure 1-1 shows a typical application block diagram. Table 1-2 shows the pin definitions in the user (normal) mode of operation.

TABLE 1-1: MCP2120 FEATURES OVERVIEW

Features	MCP2120
Serial Communications:	UART, IR
Baud Rate Selection:	Hardware/Software
Low Power Mode:	Yes
Resets: (and Delays)	Wake-up (DRT)
Packages:	14-pin DIP 14-pin SOIC



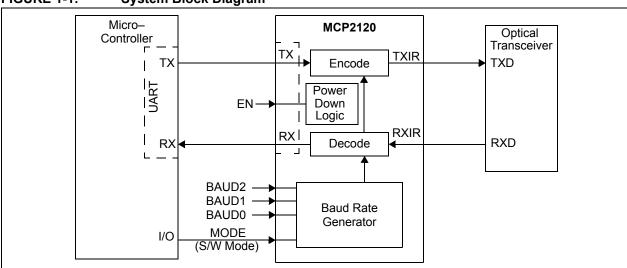


TABLE 1-2: PIN DESCRIPTION USER MODE

Pin Name	Pin N	umber	Pin	Buffer	
Pili Naille	PDIP	SOIC	Type Type		Description
VDD	1	1		Р	Positive supply for logic and I/O pins
OSC1/CLKIN	2	2	- 1	CMOS	Oscillator crystal input/external clock source input
OSC2	3	3	0	_	Oscillator crystal Output
RESET	4	4	1	ST	Resets the Device
RXIR	5	5	I	ST	Asynchronous receive from infrared transceiver
TXIR	6	6	0	_	Asynchronous transmit to infrared transceiver
MODE	7	7	I	TTL	Selects the device mode (Data/Command) for Software Baud Rate operation. For more information see Section 2.4.1.2 "Software Selection".
BAUD2	8	8	I	TTL	BAUD2:BAUD0 specify the Baud rate of the device, or if the
BAUD1	9	9	1	TTL	device operates in Software Baud Rate mode. For more informa-
BAUD0	10	10	- 1	TTL	tion see Section 2.4.1 "Baud Rate".
RX	11	11	0	_	Asynchronous transmit to controller UART
TX	12	12	- 1	TTL	Asynchronous receive from controller UART
EN	13	13	I	_	Device Enable.
Vss	14	14	_	Р	Ground reference for logic and I/O pins

Legend: TTL = TTL compatible input

I = Input P = Power ST = Schmitt Trigger input with CMOS levels

O = Output

CMOS = CMOS compatible input

2.0 DEVICE OPERATION

The MCP2120 is a low cost infrared Encoder/Decoder. The baud rate is user selectable to standard IrDA baud rates between 9600 baud to 115.2 kbaud. The maximum baud rate is 312.5 kbaud.

2.1 Power-up

Any time that the device is powered up, the Device Reset Timer delay (parameter 32) must occur before any communication with the device is initiated. This is from both the infrared transceiver side as well as the controller UART interface.

2.2 Device Reset

The MCP2120 is forced into the reset state when the RESET pin is in the low state. After the RESET pin is brought to a high state, the Device Reset Timer occurs. Once the DRT times out, normal operation occurs.

2.3 Bit Clock

The device crystal is used to derive the communication bit clock (BITCLK). There are 16 BITCLKs for each bit time. The BITCLKs are used for the generation of the Start bit and the eight data bits. The Stop bit uses the BITCLK when the data is transmitted (not for reception).

This clock is a fixed frequency, and has minimal variation in frequency (specified by crystal manufacturer).

2.4 UART Interface

The UART interface communicates with the "controller". This interface is a Half duplex interface, meaning that the system is either transmitting or receiving, but not both at the same time.

2.4.1 BAUD RATE

The baud rate for the MCP2120 can be configured either by the state of three hardware pins (BAUD2, BAUD1, and BAUD0) or through software selection.

2.4.1.1 Hardware Selection

Three device pins are used to select the baud rate that the MCP2120 will transmit and receive data. These pins are called BAUD2, BAUD1, and BAUD0. There is one pin state (device mode) where the application software can specify the baud rate. Table 2-1 shows the baud rate configurations.

TABLE 2-1: HARDWARE BAUD RATE SELECTION VS. FREQUENCY

BAUD2:BAUD0	0.6144 ⁽¹⁾	$0.6144^{(1)}$ 2.000 3.6864 4.9152 7.3728 $14.7456^{(2)}$ 20.000 ⁽²⁾									
000	800	2604	4800	6400	9600	19200	26042	Fosc / 768			
001	1600	5208	9600	12800	19200	38400	52083	Fosc / 384			
010	3200	10417	19200	25600	38400	78600	104167	Fosc / 192			
011	4800	15625	28800	38400	57600	115200	156250	Fosc / 128			
100	9600	31250	57600	78600	115200	230400	312500	Fosc / 64			

Note 1: An external clock is recommended for frequencies below 2 MHz.

2: For frequencies above 7.5 MHz, the TXIR pulse width (parameter IR121) will be shorter than the minimum pulse width of 1.6 µs in the IrDA standard specification.

2.4.1.2 Software Selection

When the BAUD2:BAUD0 pins are configured as '111' the MCP2120 defaults to a baud rate of Fosc / 768.

To place the MCP2120 into Command Mode, the MODE pin must be at a low level. When in this mode, any data that is received by the MCP2120's UART is "echoed" back to the controller and no encoding/ decoding occurs. The echoed data will be skewed less than 1 bit time (see parameter IR141). When the MODE pin goes high, the device is returned to Data Mode where the encoder/decoder is in operation.

Table 2-2 shows the software hex commands to configure the MCP2120's baud rate.

The MCP2120 receives data bytes at the existing baud rate. When the change baud rate command (0x11) is received, the last valid baud rate value received becomes the new baud rate. The new baud rate is effective after the stop bit of the echoed data. Figure 2-2 shows this sequence.

2.4.2 TRANSMITTING

When the controller sends serial data to the MCP2120, the baud rates are required to match.

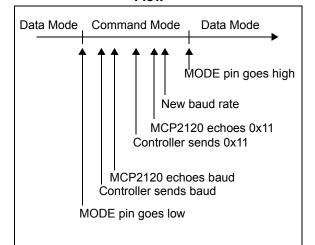
There will be some jitter on the detection of the high to low edge of the start bit. This jitter will affect the placement of the encoded start bit. All subsequent bits will be 16 BITCLK times later.

2.4.3 RECEIVING

When the controller receives serial data from the MCP2120, the baud rates are required to match.

There will be some jitter on the detection of the high to low edge of the start bit. This jitter will affect the placement of the decoded Start bit. All subsequent bits will be 16 BITCLK times later.

FIGURE 2-1: Data/Command Mode Flow



When echoing the Data, once the first bit is detected, it is echoed back. This means that the echoed data is skewed no more than 1 bit time.

The new baud rate can occur once the echoed stop bit completes.

TABLE 2-2: SOFTWARE BAUD RATE SELECTION VS. FREQUENCY

Hex									
Command ^(3, 4)	0.6144 ⁽¹⁾	0.6144 ⁽¹⁾ 2.000 3.6864 4.9152 7.3728 14.7456 ⁽²⁾ 20.000 ⁽²⁾							
0x87	800	2604	4800	6400	9600	19200	26042	Fosc / 768	
0x8B	1600	5208	9600	12800	19200	38400	52083	Fosc / 384	
0x85	3200	10417	19200	25600	38400	78600	104167	Fosc / 192	
0x83	4800	15625	28800	38400	57600	115200	156250	Fosc / 128	
0x81	9600	31250	57600	78600	115200	230400	312500	Fosc / 64	

Note 1: An external clock is recommended for frequencies below 2 MHz.

- 2: For frequencies above 7.3728 MHz, the TXIR pulse width (parameter IR121) will be shorter than the 1.6 μs IrDA standard specification.
- 3: Command 0x11 is used to change to the new baud rate.
- **4:** All other command codes are reserved for possible future use.

2.5 Modulation

When the UART receives data to be transmitted, the data needs to be modulated. This modulated signal drives the IR transceiver module. Figure 2-2 shows the encoding of the modulated signal.

Each bit time is comprised of 16-bit clocks. If the value to be transmitted (as determined by the TX pin) is a logic low, then the TXIR pin will output a low level for 7-bit clock cycles, a logic high level for 3-bit clock cycles, and then the remaining 6-bit clock cycles will be low. If the value to transmit is a logic high, then the TXIR pin will output a low level for the entire 16-bit clock cycles.

2.6 Demodulation

The modulated signal from the IR transceiver module needs to be demodulated to form the received data. As demodulation occurs, the bit value is placed on the RX pin in UART format. Figure 2-3 shows the decoding of the modulated signal.

Each bit time is comprised of 16 bit clocks. If the value to be received is a logic low, then the RXIR pin will be a low level for the first 3-bit clock cycles, and then the remaining 13-bit clock cycles will be high. If the value to be received is a logic high, then the RXIR pin will be a high level for the entire 16-bit clock cycles. The level on the RX pin will be in the appropriate state for the entire 16 clock cycles.

FIGURE 2-2: Encoding

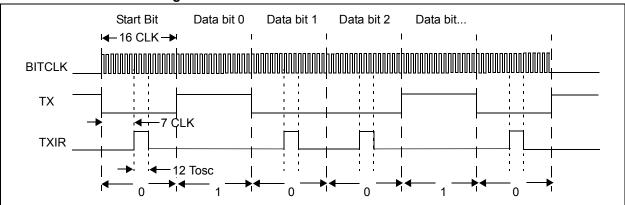
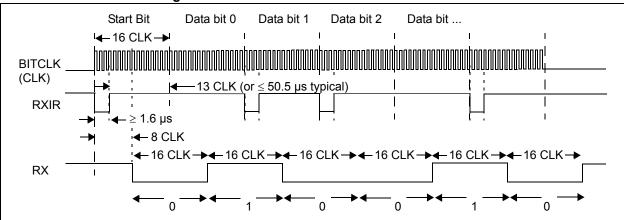


FIGURE 2-3: Decoding



2.7 Encoding/Decoding Jitter and Offset

Figure 2-4 shows the jitter and offset that is possible on the RX pin and the TXIR pin.

Jitter is the possible variation of the desired edge.

Offset is the propagation delay of the input signal (RXIR or TX) to the output signal (RX or TXIR).

The first bit on the output pin (on RX or TXIR) will show jitter compared to the input pin (RXIR or TX), but all remaining bits will be a constant distance.

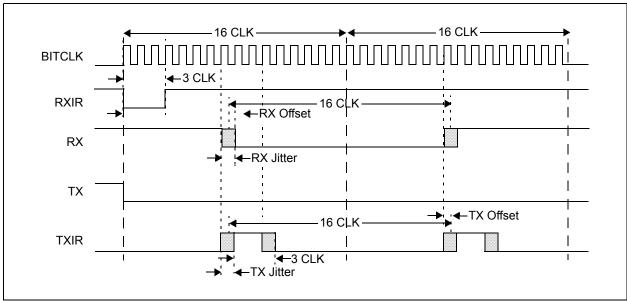
2.8 Minimizing Power

The device can be placed in a low power mode by disabling the device (holding the EN pin at the low state). The internal state machine is monitoring this pin for a low level, and once this is detected the device is disabled and enters into a low power state.

2.8.1 RETURNING TO OPERATION

When the device is disabled, the device is in a low power state. When the EN pin is brought to a high level, the device will return to the operating mode. The device requires a delay of 1000 Tosc before data may be transmitted or received.





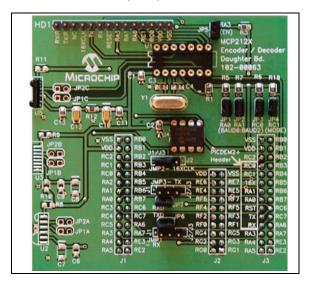
3.0 DEVELOPMENT TOOLS

The MCP212X Developer's Daughter Board is used to evaluate and demonstrate the MCP2122 or the MCP2120 IrDA® Standard Encoder/Decoder devices.

A header allows the MCP212X Developer's Daughter Board to be jumpered easily into systems for development purposes.

The MCP212X Developer's Daughter Board is designed to interface to several of the "new" low cost PIC® Demo Boards. These include the PICDEM HPC Explorer Demo board, the PICDEM FS USB Demo board, and the PICDEM LCD Demo board.

When the MCP212X Developer's Daughter Board is used in conjunction with the PICDEM HPC Explorer Demo board, the MCP212x can be connected to either of the PIC18F8772's two UARTs or the RX and TX signals can be "crossed" so the MCP212x device can communicate directly out the PICDEM HPC Explorer Demo Board's UART (DB-9).



Features:

- 8-pin socket for installation of MCP2122 (installed) and 14-pin socket for installation of MCP2120
- · Three Optical Transceiver circuits (1 installed)
- Headers to interface to low cost PICDEM Demo Boards, including:
 - • PICDEM™ HPC Explorer Demo Board
 - • PICDEM™ LCD Demo Board
 - • PICDEM™ FS USB Demo Board
 - • PICDEM™ 2 Plus Demo Board
- Headers to easily connect to the user's embedded system
- Jumpers to select routing of MCP212X signals to the PICDEM™ Demo Board Headers
- Jumpers to configure the operating mode of the board

The MCP2120/MCP2150 Developer's Kit has been obsoleted but if you have access to one of these kits, it can be used to demonstrate the operation of the MCP2120.

NOTES:

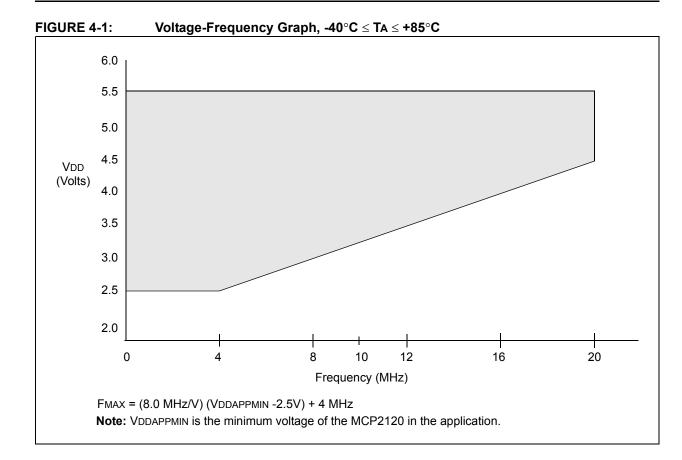
4.0 **ELECTRICAL CHARACTERISTICS**

Absolute Maximum Ratings†

Ambient Temperature under bias	40°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7V
Voltage on RESET with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	
Total Power Dissipation (1)	700 mW
Max. Current out of Vss pin	150 mA
Max. Current into VDD pin	125 mA
Input Clamp Current, liκ (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, Ιοκ (V0 < 0 or V0 > VDD)	±20 mA
Max. Output Current sunk by any Output pin	25 mA
Max. Output Current sourced by any Output pin	25 mA
Note 1: Power Dissipation is calculated as follows:	

PDIS = VDD x {IDD - \sum IOH} + \sum {(VDD-VOH) x IOH} + \sum (VOL x IOL)

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



4.1 DC Characteristics

DC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ (industrial)				
Param. No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
D001	Vdd	Supply Voltage	2.5	_	5.5	V	See Figure 4-1	
D002	VDR	RAM Data Retention Voltage ⁽²⁾	2.5	_	_	V	Device Oscillator/Clock stopped	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	_	Vss	_	V		
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05	_	_	V/ms		
D010	IDD	Supply Current ⁽³⁾	_ _ _ _ _	0.8 0.6 0.4 3 4 4.5	1.4 1.0 0.8 7 12 16	mA mA mA mA mA	Fosc = 4 MHz, VDD = 5.5V Fosc = 4 MHz, VDD = 3.0V Fosc = 4 MHz, VDD = 2.5V Fosc = 10 MHz, VDD = 3.0V Fosc = 20 MHz, VDD = 4.5V Fosc = 20 MHz, VDD = 5.5V	
D020	IPD	Device Disabled Current ^(3, 4)	_ _ _	0.25 0.25 0.4 3	4 3 5.5 8	μΑ μΑ μΑ μΑ	$\begin{split} &V_{DD} = 3.0 \text{V}, 0^{\circ}\text{C} \leq \text{Ta} \leq +70^{\circ}\text{C} \\ &V_{DD} = 2.5 \text{V}, 0^{\circ}\text{C} \leq \text{Ta} \leq +70^{\circ}\text{C} \\ &V_{DD} = 4.5 \text{V}, 0^{\circ}\text{C} \leq \text{Ta} \leq +70^{\circ}\text{C} \\ &V_{DD} = 5.5 \text{V}, -40^{\circ}\text{C} \leq \text{Ta} \leq +85^{\circ}\text{C} \end{split}$	

Note 1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered without losing RAM data.
- **3:** The supply current is mainly a function of the operating voltage and frequency. Pin loading, pin rate, and temperature have an impact on the current consumption.
 - a) The test conditions for all IDD measurements are made when device is enabled (EN pin is high):
 OSC1 = external square wave, from rail-to-rail; all input pins pulled to Vss, RXIR = VDD,
 RESET = VDD;
 - b) When device is disabled (EN pin is low), the conditions for current measurements are the same.
- **4:** When the device is disabled (EN pin is low), current is measured with all input pins tied to VDD or VSS and the output pins driving a high or low level into infinite impedance.

DC Characteristics (Continued)

DC CHA	RACTERI	STICS	Standard Operating Conditions (unless otherwise specified) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ (industrial) Operating voltage VDD range as described in DC spec Section 4.1 "DC Characteristics".					
Param No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions	
		Input Low Voltage						
	VIL	Input pins						
D030		with TTL buffer	Vss	_	0.8V	V	For all 4.5 ≤ V _{DD} ≤ 5.5V	
D030A			Vss	_	0.15VDD	V	otherwise	
D031		with Schmitt Trigger buffer	Vss	_	0.2VDD	V		
D032		RESET, RXIR	Vss	_	0.2VDD	V		
D033		OSC1	Vss	_	0.3VDD	V		
		Input High Voltage						
	VIH	Input pins		_				
D040		with TTL buffer	2.0	_	VDD	V	$4.5 \leq V_{DD} \leq 5.5V$	
D040A			0.25VDD + 0.8VDD	_	VDD	V	otherwise	
D041		with Schmitt Trigger buffer	0.8VDD	_	VDD	V	For entire VDD range	
D042		RESET, RXIR	0.8VDD	_	VDD	V		
D043		OSC1	0.7VDD	_	VDD	V		
		Input Leakage Current ^(1, 2)						
D060	lıL	Input pins	_	_	±1	μΑ	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance	
D061		RESET	_	_	±30	μΑ	VSS ≤ VPIN ≤ VDD	
D063		OSC1	_	_	±5	μΑ	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration	
D070	lpur	weak pull-up current	50	250	400	μA	VDD = 5V, VPIN = VSS	

Note 1: The leakage current on the RESET pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{2:} Negative current is defined as coming out of the pin.

DC Characteristics (Continued)

DC CHA	RACTERI	STICS	Standard Operating Conditions (unless otherwise specified) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (industrial) Operating voltage VDD range as described in DC spec Section 4.1 "DC Characteristics"					
Param No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions	
D080	Vol	Output Low Voltage TXIR, RX	_	_	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C	
D083		OSC2	_	_	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C	
D090	Vон	Output High Voltage TXIR, RX ⁽¹⁾	VDD - 0.7	_	_	٧	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C	
D092		OSC2	VDD - 0.7	_	_	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C	
		Capacitive Loading Specs on Output Pins						
D100	Cosc2	OSC2 pin	_	_	15	pF	when external clock is used to drive OSC1.	
D101	Сю	All Input or Output pins	_	_	50	pF		

Note 1: Negative current is defined as coming out of the pin.

4.2 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

4.2.1 TIMING CONDITIONS

The temperature and voltages specified in Table 4-2 apply to all timing specifications unless otherwise noted. Figure 4-2 specifies the load conditions for the timing specifications.

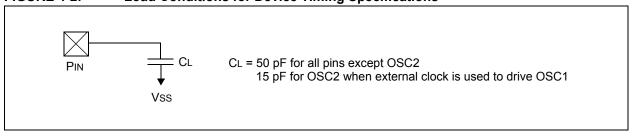
TABLE 4-1: SYMBOLOGY

1	TppS2pp	S	2. Tpps	8
T				
	F	Frequency	Т	Time
	Е	Error		
Lov	wercase	letters (pp) and their meanings:		
pp				
	io	Input or Output pin	osc	Oscillator
	rx	Receive	tx	Transmit
	bitclk	RX/TX BITCLK	RST	Reset
	drt	Device Reset Timer		
Up	percase	letters and their meanings:		
S				
	F	Fall	Р	Period
	Н	High	R	Rise
	1	Invalid (Hi-impedance)	V	Valid
	L	Low	Z	Hi-impedance

TABLE 4-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature —40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 4.1 "DC Characteristics".
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FIGURE 4-2: Load Conditions for Device Timing Specifications



4.3 Timing Diagrams and Specifications

FIGURE 4-3: External Clock Timing

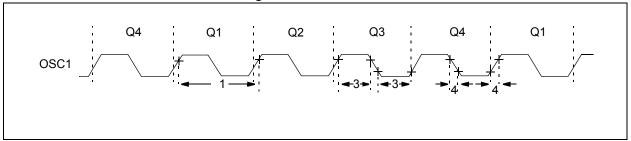


TABLE 4-3: EXTERNAL CLOCK TIMING REQUIREMENTS

AC Chai	racteristic	s	Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"					
Param. No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
1	Tosc	External CLKIN Period (2,3)	50	_	_	ns		
		Oscillator Period (2)	50	_	500	ns		
1A	Fosc	External CLKIN Frequency ^(2,3)	DC	_	20	MHz		
		Oscillator Frequency (2)	2	_	20	MHz		
1C	Eclk	Clock Error	_	_	0.01	%		
3	TosL,	Clock in (OSC1)	10	_	_	ns		
	TosH	Low or High Time						
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_	_	15	ns		

- **Note 1:** Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
 - 2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

 When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - 3: A duty cycle of no more than 60/40 (High Time / Low Time or Low Time / High Time) is recommended for external clock inputs.

FIGURE 4-4: I/O Waveform

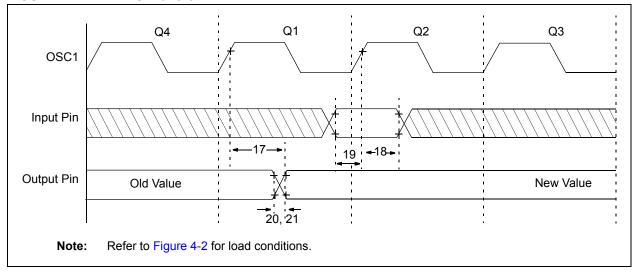


TABLE 4-4: I/O TIMING REQUIREMENTS

AC Cha	racteristic	s	Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"					
Param. No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Output valid ⁽²⁾	_	_	100	ns		
18	TosH2ioI	OSC1↑ (Q2 cycle) to Input invalid (I/O in hold time)	200	_		ns		
19	TioV2osH	Input valid to OSC1↑ (I/O in setup time)	0	_	_	ns		
20	ToR	RX and TXIR pin rise time (2)	_	10	25	ns		
21	ToF	RX and TXIR pin fall time (2)		10	25	ns		

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated.

2: See Figure 4-2 for loading conditions.

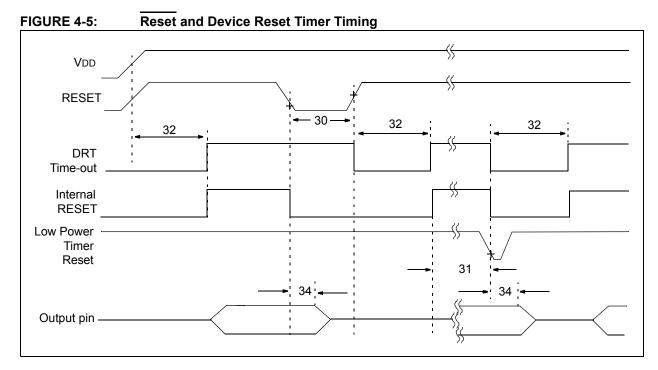


TABLE 4-5: RESET AND DEVICE RESET TIMER REQUIREMENTS

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"						
Param. No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions		
30	TRSTL	RESET Pulse Width (low)	2000	_	_	ns	VDD = 5.0 V		
31	TLPT	Low Power Time-out Period	9	18	30	ms	VDD = 5.0 V		
32	TDRT	Device Reset Timer Period	9	18	30	ms	V _{DD} = 5.0 V		
34	Tioz	Output Hi-impedance from RESET Low or device Reset	_	_	2	μs			

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated.

FIGURE 4-6: USART ASynchronous Transmission Waveform

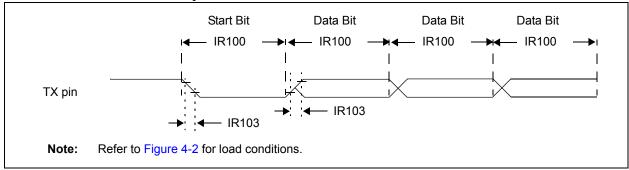


TABLE 4-6: USART ASYNCHRONOUS TRANSMISSION REQUIREMENTS

AC Cha	racteristi	cs	Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"					
Param. No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions	
IR100	Ттхвіт	Transmit Baud rate					Hardware Selection	
			768	_	768	Tosc	BAUD2:BAUD0 = 000	
			384	_	384	Tosc	BAUD2:BAUD0 = 001	
			192	_	192	Tosc	BAUD2:BAUD0 = 010	
			128	_	128	Tosc	BAUD2:BAUD0 = 011	
			64	_	64	Tosc	BAUD2:BAUD0 = 100	
							Software Selection BAUD2:BAUD0 = 111	
			768	_	768	Tosc	Hex Command = 0x87	
			384	_	384	Tosc	Hex Command = 0x8B	
			192	_	192	Tosc	Hex Command = 0x85	
			128	_	128	Tosc	Hex Command = 0x83	
			64	_	64	Tosc	Hex Command = 0x81	
IR101	Етхвіт	Transmit (TX pin) Baud rate Error (into MCP2120)	_	_	1	%		
IR102	ETXIRBIT	Transmit (TXIR pin) Baud rate Error (out of MCP2120) ⁽¹⁾	_	_	1	%		
IR103	TTXRF	TX pin rise time and fall time	_		25	ns		

Note 1: This error is not additive to IR101 parameter.

FIGURE 4-7: USART ASynchronous Receive Timing

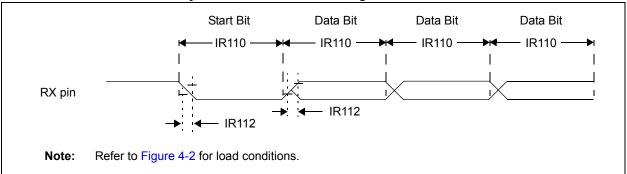


TABLE 4-7: USART ASYNCHRONOUS RECEIVE REQUIREMENTS

AC Cha	racteristi	cs	Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"					
Param. No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions	
IR110	TRXBIT	Receive Baud Rate					Hardware Selection	
			768	_	768	Tosc	BAUD2:BAUD0 = 000	
			384	_	384	Tosc	BAUD2:BAUD0 = 001	
			192	_	192	Tosc	BAUD2:BAUD0 = 010	
			128	_	128	Tosc	BAUD2:BAUD0 = 011	
			64	_	64	Tosc	BAUD2:BAUD0 = 100	
							Software Selection BAUD2:BAUD0 = 111	
			768	_	768	Tosc	Hex Command = 0x87	
			384	_	384	Tosc	Hex Command = 0x8B	
			192	_	192	Tosc	Hex Command = 0x85	
			128	_	128	Tosc	Hex Command = 0x83	
			64	_	64	Tosc	Hex Command = 0x81	
IR111	ERXBIT	Receive (RXIR pin) Baud rate Error (into MCP2120)	_	_	1	%		
IR112	ERXBIT	Receive (RX pin) Baud rate Error (out of MCP2120) ⁽¹⁾	_	_	1	%		
IR113	TTXRF	RX pin rise time and fall time		_	25	ns		

Note 1: This error is not additive to IR111 parameter.

FIGURE 4-8: TX and TXIR Waveforms

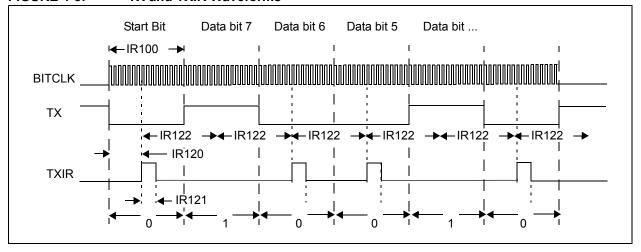


TABLE 4-8: TX AND TXIR REQUIREMENTS

AC Cha	racteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"						
Param. No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions		
IR100	Ттхвіт	Transmit Baud Rate					Hardware Selection		
			768	_	768	Tosc	BAUD2:BAUD0 = 000		
			384		384	Tosc	BAUD2:BAUD0 = 001		
			192		192	Tosc	BAUD2:BAUD0 = 010		
			128	1	128	Tosc	BAUD2:BAUD0 = 011		
			64		64	Tosc	BAUD2:BAUD0 = 100		
					8		Software Selection BAUD2:BAUD0 = 111		
			768	_	768	Tosc	Hex Command = 0x87		
			384	_	384	Tosc	Hex Command = 0x8B		
			192	-	192	Tosc	Hex Command = 0x85		
			128	_	128	Tosc	Hex Command = 0x83		
			64	_	64	Tosc	Hex Command = 0x81		
IR120	TTXL2TXIRH	TX falling edge (↓) to TXIR rising edge (↑) ⁽¹⁾	7ΤΒΙΤCLK - 8.34 μs	7	7ΤΒΙΤCLK + 8.34 μs	Твітськ			
IR121	TTXIRPW	TXIR pulse width	12	_	12	Tosc			
IR122	TTXIRP	TXIR bit period (1)	_	16	_	TBITCLK			

Note 1: TBITCLK = TTXBIT/16

FIGURE 4-9: RXIR and RX Waveforms

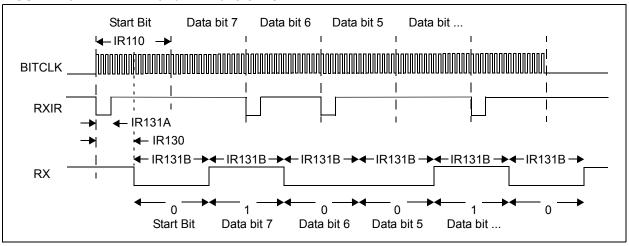


TABLE 4-9: RXIR REQUIREMENTS

AC Cha	AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"					
Param. No. Sym Characteristic		Characteristic	Min Ty		Max	Units	Conditions		
IR110	TRXBIT	Receive Baud Rate					Hardware Selection		
			768	_	768	Tosc	BAUD2:BAUD0 = 000		
			384	_	384	Tosc	BAUD2:BAUD0 = 001		
			192	_	192	Tosc	BAUD2:BAUD0 = 010		
			128	_	128	Tosc	BAUD2:BAUD0 = 011		
			64	_	64	Tosc	BAUD2:BAUD0 = 100		
							Software Selection BAUD2:BAUD0 = 111		
			768	_	768	Tosc	Hex Command = 0x87		
			384	_	384	Tosc	Hex Command = 0x8B		
			192	_	192	Tosc	Hex Command = 0x85		
			128	_	128	Tosc	Hex Command = 0x83		
			64	_	64	Tosc	Hex Command = 0x81		
IR130	TRXIRL2RXH	RXIR falling edge (\downarrow) to RX falling edge (\downarrow) (1)	8ΤΒΙΤCLK - 8.34 μs	8	8ΤΒΙΤCLK + 8.34 μs	Твітськ			
IR131A	TRXIRPW	RXIR pulse width	3	_	3	Tosc			
IR132	TRXIRP	RXIR bit period (1)	_	16	_	TBITCLK			

Note 1: TBITCLK = TRXBIT/16

FIGURE 4-10: Command Mode: TX and RX Waveforms

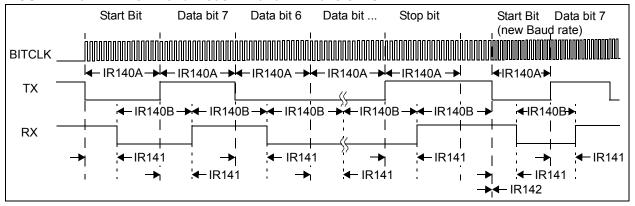


TABLE 4-10: TX AND TXIR REQUIREMENTS

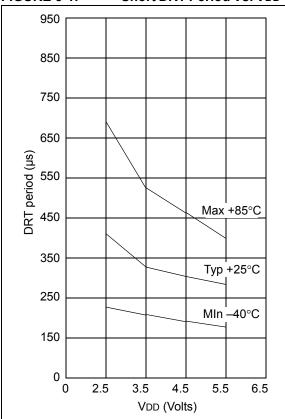
AC Characteristics Op				Tempera	ture /DD rang	-40°C ≤	s otherwise specified) TA \leq +85°C (industrial) ibed in Section 4.1
Param. No.	Sym	Characteristic	Min	Тур	Max	Units	Conditions
IR140A	Втх	Transmit Baud Rate	16		16	TBITCLK	
IR140B	Brx	Receive Baud Rate	16	-	16	TBITCLK	
IR141	TTXE2RXE	TX edge to RX edge (delay)	5.5	8	10.5	TBITCLK	_
IR142	TrxP2txS	Delay from RX Stop bit complete to TX Start bit (new baud rate)	_		0	Tosc	

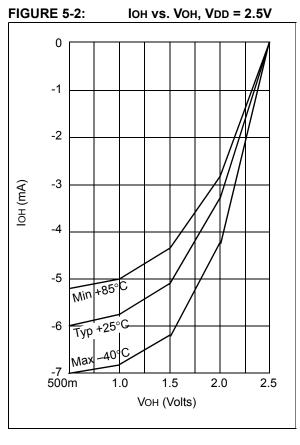
5.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

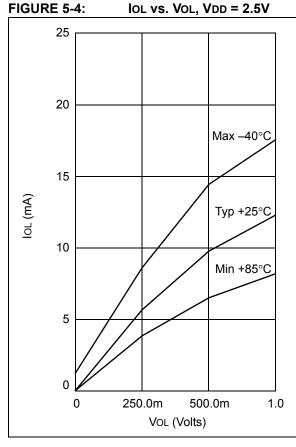
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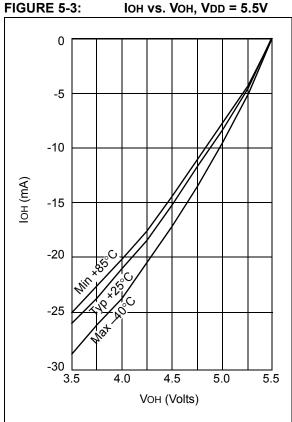
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3s) and (mean - 3s) respectively, where s is standard deviation.

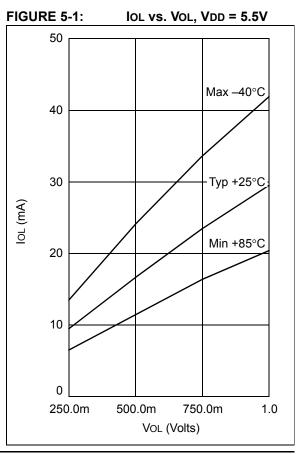
FIGURE 5-1: Short DRT Period Vs. VDD











6.0 PACKAGING INFORMATION

6.1 **Package Marking Information**

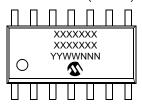
14-Lead PDIP (300 mil)



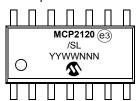
Example:



14-Lead SOIC (150 mil)



Example:



Legend: XX...X Customer-specific information

Υ Year code (last digit of calendar year) ΥY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01')

Alphanumeric traceability code NNN

(e3) Pb-free JEDEC designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator (@3)

can be found on the outer packaging for this package.

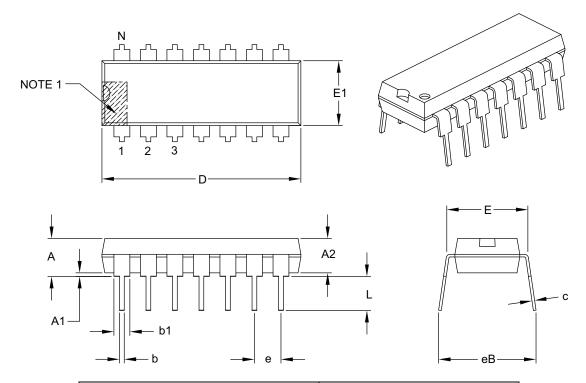
In the event the full Microchip part number cannot be marked on one line, it will

be carried over to the next line, thus limiting the number of available

characters for customer-specific information.

14-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimension	on Limits	MIN	NOM	MAX
Number of Pins	N		14	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	_	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	_
Shoulder to Shoulder Width	Е	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB		_	.430

Notes:

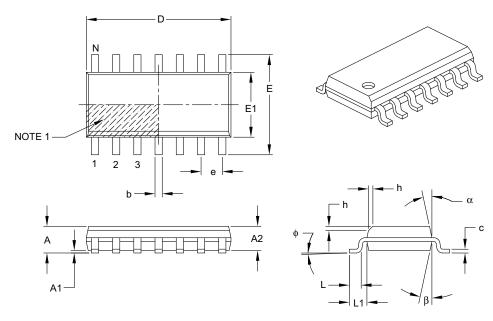
- 1. Pin 1 visual index feature may vary, but must be located with the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLMETERS	}
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		14	
Pitch	е		1.27 BSC	
Overall Height	A	_	-	1.75
Molded Package Thickness	A2	1.25	_	_
Standoff §	A1	0.10	_	0.25
Overall Width	Е	6.00 BSC		
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	ф	0°	_	8°
Lead Thickness	С	0.17	-	0.25
Lead Width	b	0.31	_	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

FIGURE 6-1: EMBOSSED CARRIER DIMENSIONS (16 MM TAPE)

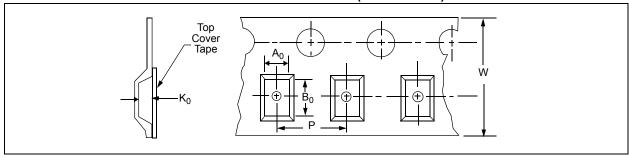
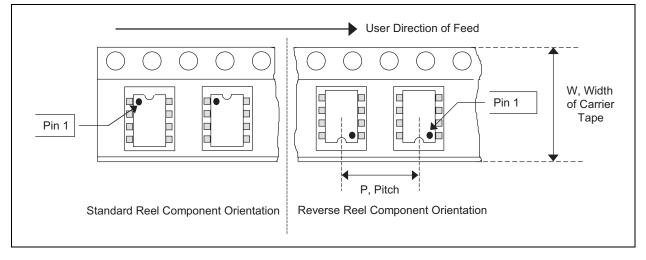


TABLE 6-1: CARRIER TAPE/CAVITY DIMENSIONS

Case	Packag	e	Carrier Dimensions		Cavity Dimensions		•			Output Quantity	Reel Diameter in
Outline	Туре		W mm	P mm	A0 mm	B0 mm	K0 mm	Units	mm		
SL	SOIC .150"	14L	16	8	6.5	9.5	2.1	2600	330		

FIGURE 6-2: SOIC DEVICE



APPENDIX A: REVISION HISTORY

Revision B (February 2007)

- Updated Development Tools section
- · Update packaging outline drawings
- · Updates Product Identification System section.

Revision A (March 2001)

· Initial release of this document

NOTES:		

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X /XX	Exa	mples:	
	nperature Package Range	a) b)	MCP2120-I/SL:	Industrial Temperature, PDIP packaging Industrial Temperature, SOIC package
Device	MCP2120: Infrared Encoder/Decoder MCP2120T: Infrared Encoder/Decoder, Tape and Reel	c)	MCP2120T-I/SL:	lape and Reel, Industrial Temperature, SOIC package
Temperature Range	I = -40×C to+85×C			
Package	P = Plastic DIP (300 mil, Body), 14-lead SL = Plastic SOIC (150 mil, Body), 14-lead			

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Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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