# CY25245

# Frequency-multiplying, Peak-reducing EMI Solution

## Features

- **Cypress PREMIS™ SMARTSPREAD™ family offering**
- **Generates an electromagnetic interference (EMI) optimized clocking signal at the output**
- **Selectable output frequency range**
- **Single 1.25%, 2.5%, 5%, or 10% down or center spread output**
- **Integrated loop filter components**
- **Operates with a 3.3 or 5V supply**
- **Low power CMOS design**
- **Available in 20-pin Small Shrunk Outline Package (SSOP)**

## Key Specifications

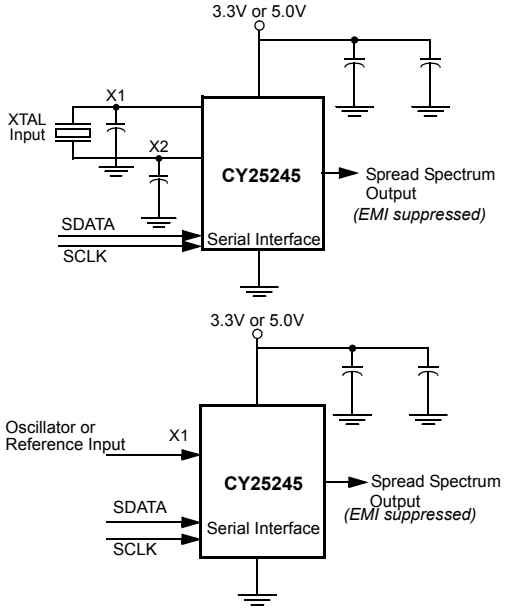
Supply voltages: ..... $V_{DD}$ = 3.3V ± 0.3V or $V_{DD}$ = 5V ± 10%

Frequency range:..... 13 MHz ≤ $F_{in}$ ≤ 166 MHz

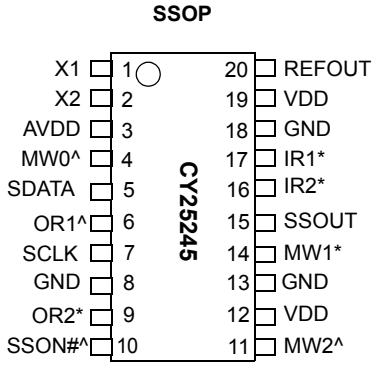
Cycle-to-cycle jitter: ..... 250 ps (max)

Output duty cycle: ..... 40/60% (worst case)

## Simplified Block Diagram




## Pin Configuration[1, 2]




**Notes:**
1. Pins marked with ^ are internal pull-down resistors with weak 250 kΩ.
2. Pins marked with * are internal pull-up resistors with weak 80 kΩ.

## Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|---|---|---|---|
| SSOUT | 15 | O | **Output Modulated Frequency**. Frequency modulated copy of the input clock (SSON# asserted). |
| REFOUT | 20 | O | **Non-modulated Output**. This pin provides a copy of the reference frequency. This output will not have the Spread Spectrum feature enabled regardless of the state of logic input SSON#. |
| X1 | 1 | I | **Crystal Connection or External Reference Frequency Input**. This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock. |
| X2 | 2 | I | **Crystal Connection**. Input connection for an external crystal. If using an external reference, this pin must be left unconnected. |
| SSON# | 10 | I | **Spread Spectrum Control (Active LOW)**. Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor. |
| MW0:2 | 4, 11, 14 | I | **Modulation Width Selection**. When Spread Spectrum feature is turned on, these pins are used to select the amount of variation and peak EMI reduction that is desired on the output signal. MW0:Down, MW1:Up, MW2:Down (see *Table 2*). |
| IR1:2 | 17, 16 | I | **Reference Frequency Selection**. The logic level provided at this input indicates to the internal logic what range the reference frequency is in and determines the factor by which the device multiplies the input frequency. Refer to *Table 3*. These pins have internal pull-up resistors. |
| OR1:2 | 6, 9 | I | **Output Frequency Selection Bits**. These pins select the frequency operation for the output. Refer to *Table 1*. The OR2 pin has an internal pull-up resistor. The OR1 pin has internal pull-down resistors. |
| SCLK | 7 | I | **Clock Pin for SMBus Circuitry**. |
| SData | 5 | I/O | **Data Pin for SMBus Circuitry**. |
| VDD | 12, 19 | P | **Power Connection**. Connected to 3.3V or 5V power supply. |
| AVDD | 3 | P | **Analog Power Connection**. Connected to 3.3V or 5V power supply. |
| GND | 8, 13, 18 | G | **Ground Connection**. Connect all ground pins to the common ground plane. |

**Table 1. Frequency Configuration (Frequencies in MHz)**

| Range of Fin Frequency | | Multiplier Settings | | Output/ Input | Range of Fout | | Required R Settings | | Modulation and Power-down Settings | |
|---|---|---|---|---|---|---|---|---|---|---|
| Min. | Max. | OR2 | OR1 | | Min. | Max. | IR2 | IR1 | MW2 | MW1 |
| 14 | 41.7 | 0 | 1 | 1 | 14 | 41.7 | 0 | 1 | *Table 2* | |
| 14 | 41.7 | 1 | 0 | 2 | 28 | 83.3 | 0 | 1 | *Table 2* | |
| 14 | 41.7 | 1 | 1 | 4 | 56 | 166 | 0 | 1 | *Table 2* | |
| 25 | 83.3 | 0 | 1 | 0.5 | 13 | 41.7 | 1 | 0 | *Table 2* | |
| 25 | 83.3 | 1 | 0 | 1 | 25 | 83.3 | 1 | 0 | *Table 2* | |
| 25 | 83.3 | 1 | 1 | 2 | 50 | 166 | 1 | 0 | *Table 2* | |
| 50 | 166 | 0 | 1 | 0.25 | 13 | 41.7 | 1 | 1 | *Table 2* | |
| 50 | 166 | 1 | 0 | 0.5 | 25 | 83.3 | 1 | 1 | *Table 2* | |
| 50 | 166 | 1 | 1 | 1 | 50 | 166 | 1 | 1 | *Table 2* | |
| Reserved | | 0 | 0 | N/A | N/A | N/A | As Set | As Set | 1 | 0 |
| Power-down Hi-Z | | 0 | 0 | N/A | N/A | N/A | As Set | As Set | 1 | 1 |
| Power-down 0 | | 0 | 0 | N/A | N/A | N/A | As Set | As Set | 0 | 0 |
| Power-down 1 | | 0 | 0 | N/A | N/A | N/A | As Set | As Set | 0 | 1 |

**Table 2. Modulation Width Selection Table**

| EMI Reduction | Modulation Setting | | Bandwith Limit Frequencies as a % Value of Fout | | | |
|---|---|---|---|---|---|---|
| | | | MW0 = 0 | | MW0 = 1 | |
| | MW2 | MW1 | Low | High | Low | High |
| Minimum EMI Control | 0 | 0 | 98.75% | 100% | 99.375% | 100.625% |
| Suggested Setting | 0 | 1 | 97.5% | 100% | 98.75% | 101.25% |
| Alternate Setting | 1 | 0 | 95.0% | 100% | 97.5% | 102.5% |
| Maximum EMI reduction | 1 | 1 | 90.0% | 100% | 95% | 105% |

## Overview

The CY25245 product is one of a series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low-frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram shows a simple implementation.

## Functional Description

The CY25245 uses a phase-locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency.[3] The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

### Frequency Selection With SSFTG

In spread spectrum frequency timing generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (FS2:1 pins), the frequency range can be set (see *Table 2*). Spreading percentage is set with pins MW0:2 as shown in *Table 2*.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentage options are provided.

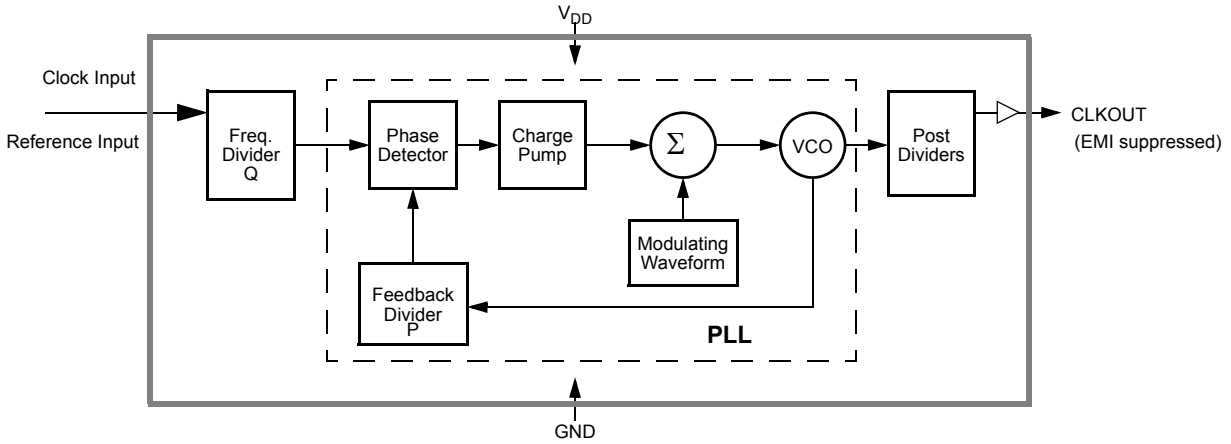



**Figure 1. Functional Block Diagram**

**Note:**
3. For the CY25245, the output frequency is nominally equal to the input frequency.

## Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 2*.

As shown in *Figure 2*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread.

The output clock is modulated with a waveform depicted in *Figure 3*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is as described in *Table 2*. *Figure 3* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

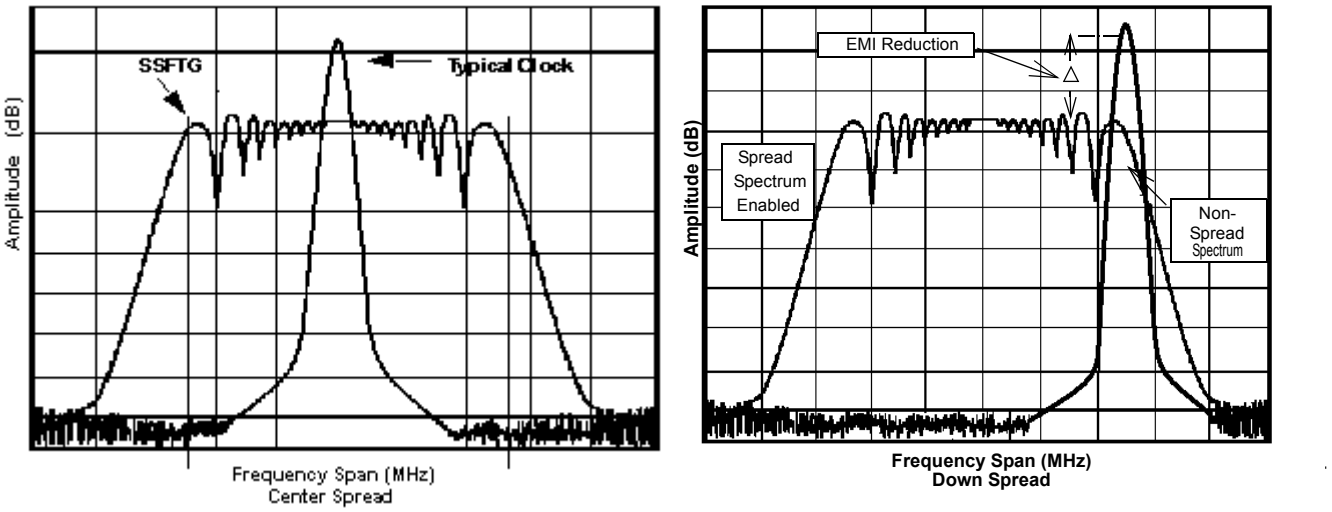



**Figure 2. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**

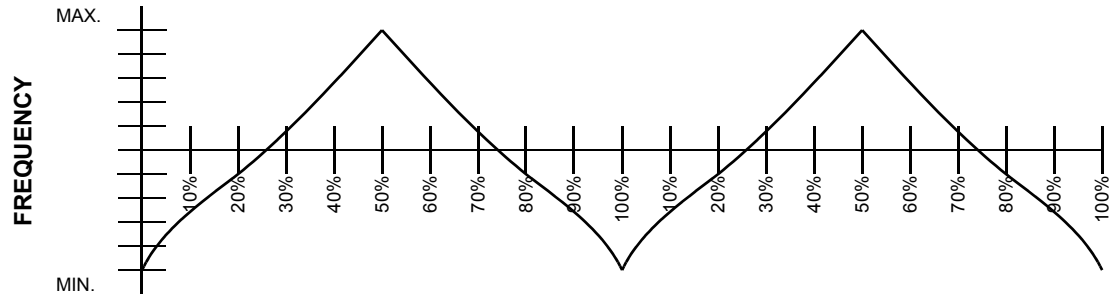



**Figure 3. Typical Modulation Profile**

## Serial Data Interface

The CY25245 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the CY25245 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 3* summarizes the control functions of the serial data interface.

## Operation

Data is written to the CY25245 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 4*.

### Writing Data Bytes

Each bit in Data Bytes 0–7 control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 5* gives the bit formats for registers located in Data Bytes 0–7.

**Table 3. Serial Data Interface Control Functions Summary**

| Control Function | Description | Common Application |
|---|---|---|
| Clock Output Disable | Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW. | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots. |
| CPU Clock Frequency Selection | Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion. | For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation. |
| Spread Spectrum Enabling | Enables or disables spread spectrum clocking. | For EMI reduction. |
| Output three-state | Puts clock output into a high-impedance state. | Production PCB testing. |
| (Reserved) | Reserved function for future device revision or production device testing. | No user application. Register bit must be written as 0. |

**Table 4. Byte Writing Sequence**

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---|---|---|---|
| 1 | Slave Address | 11010010 | Commands the CY25245 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the CY25245 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2 | Command Code | Don’t Care | Unused by the CY25245, therefore bit values are ignored (“don’t care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 3 | Byte Count | Don’t Care | Unused by the CY25245, therefore bit values are ignored (“don’t care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 4 | Data Byte 0 | Refer to *Table 5* | The data bits in Data Bytes 0–7 set internal CY25245 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 5*, Data Byte Serial Configuration Map. |
| 5 | Data Byte 1 | | |
| 6 | Data Byte 2 | | |
| 7 | Data Byte 3 | | |
| 8 | Data Byte 4 | | |
| 9 | Data Byte 5 | | |
| 10 | Data Byte 6 | | |
| 11 | Data Byte 7 | | |

**Table 5. Data Bytes 0–7 Serial Configuration Map**

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|---|---|---|---|---|---|---|
| | Pin No. | Pin Name | | 0 | 1 | |
| **Data Byte 0** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 1** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 2** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 3** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 4** | | | | | | |
| 7 | 16 | IR2 | MSB of Input Range Select | Refer to *Table 1* | | 0 |
| 6 | 17 | IR1 | LSB of Input Range Select | Refer to *Table 1* | | 1 |
| 5 | 9 | OR2 | MSB of Output Range Select | Refer to *Table 1* | | 1 |
| 4 | 6 | OR1 | LSB of Output Range Select | Refer to *Table 1* | | 0 |
| 3 | – | – | Hardware/Software Frequency Select | Hardware | Software | 0 |
| 2 | – | – | Stop Function | Normal | Stop | 0 |

**Table 5. Data Bytes 0–7 Serial Configuration Map** (continued)

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|---|---|---|---|---|---|---|
| | Pin No. | Pin Name | | 0 | 1 | |
| 1 | 10 | SSON# | Spread Spectrum | Spread On | Spread Off | 0 |
| 0 | 4 | MW0 | LSB of Modulation Width Selection | Refer to *Table 2* | | 0 |
| **Data Byte 5** | | | | | | |
| 7 | 11 | MW2 | MSB of Modulation Width Selection | Refer to *Table 2* | | 0 |
| 6 | 14 | MW1 | Modulation Width Selection Bit | Refer to *Table 2* | | 1 |
| 5 | 20 | REFOUT | Output Enable | Disabled | Enabled | 1 |
| 4 | 15 | SSOUT | Output Enable | Disabled | Enabled | 1 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 6** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |
| **Data Byte 7** | | | | | | |
| 7 | – | – | (Reserved) | – | – | 0 |
| 6 | – | – | (Reserved) | – | – | 0 |
| 5 | – | – | (Reserved) | – | – | 0 |
| 4 | – | – | (Reserved) | – | – | 0 |
| 3 | – | – | (Reserved) | – | – | 0 |
| 2 | – | – | (Reserved) | – | – | 0 |
| 1 | – | – | (Reserved) | – | – | 0 |
| 0 | – | – | (Reserved) | – | – | 0 |

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on Any Pin with Respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_B$ | Ambient Temperature under Bias | –55 to +125 | °C |
| $P_D$ | Power Dissipation | 0.5 | W |

## DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 0.3V$[4]

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | | | 18 | 32 | mA |
| $t_{ON}$ | Power-up Time | First locked clock cycle after Power Good | | | 5 | ms |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | Note 4 | –50 | | 50 | µA |
| $I_{IH}$ | Input High Current | Note 4 | –50 | | 50 | µA |
| $I_{OL}$ | Output Low Current | @ 0.4V, $V_{DD} = 3.3V$ | | 15 | | mA |
| $I_{OH}$ | Output High Current | @ 2.4V, $V_{DD} = 3.3V$ | | 15 | | mA |
| $C_I$ | Input Capacitance | | | | 7 | pF |
| $R_P$ | Input Pull-Up Resistor | | | 250 | | kΩ |
| $Z_{OUT}$ | Clock Output Impedance | | | 25 | | Ω |

## DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5V \pm 10\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | | | 30 | 50 | mA |
| $t_{ON}$ | Power-up Time | First locked clock cycle after Power Good | | | 5 | ms |
| $V_{IL}$ | Input Low Voltage | | | | $0.15V_{DD}$ | V |
| $V_{IH}$ | Input High Voltage | | $0.7V_{DD}$ | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V |
| $I_{IL}$ | Input Low Current | Note 4 | –50 | | 50 | µA |
| $I_{IH}$ | Input High Current | Note 4 | –50 | | 50 | µA |
| $I_{OL}$ | Output Low Current | @ 0.4V, $V_{DD} = 5V$ | | 24 | | mA |
| $I_{OH}$ | Output High Current | @ 2.4V, $V_{DD} = 5V$ | | 24 | | mA |
| $C_I$ | Input Capacitance | | | | 7 | pF |
| $R_P$ | Input Pull-up Resistor | | | 250 | | kΩ |
| $Z_{OUT}$ | Clock Output Impedance | | | 25 | | Ω |

**Note:**
4. Inputs OR1:2 and IR1:2 have a pull-up resistor, Input SSON# has a pull-down resistor.

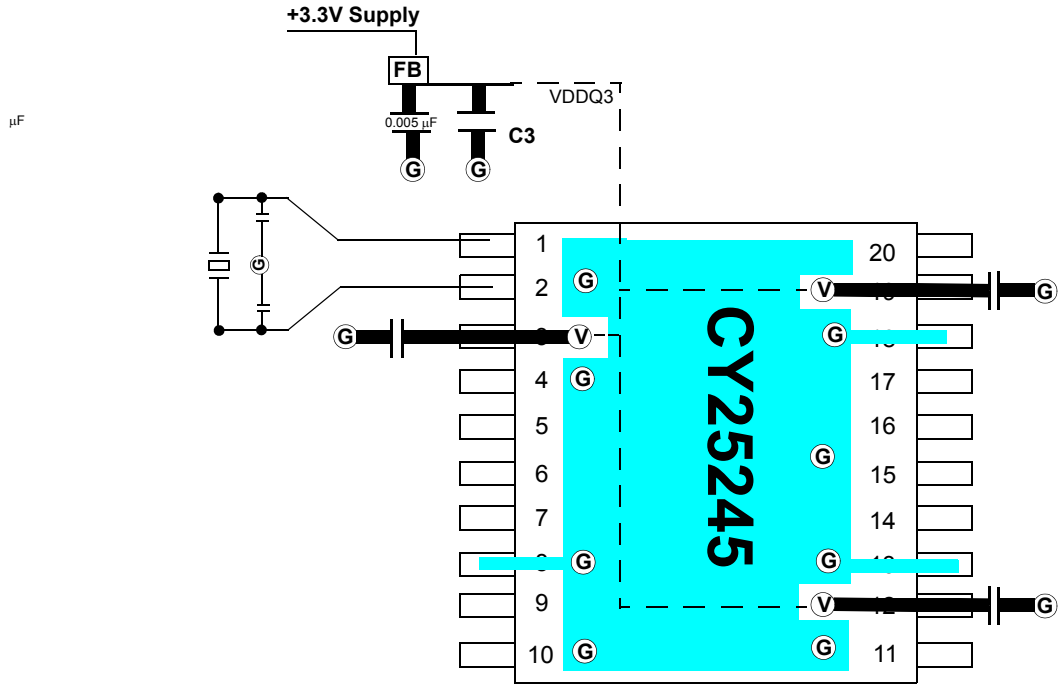
## AC Electrical Characteristics: $T_A$ = 0°C to +70°C, $V_{DD}$ = 3.3V ±0.3V or 5V±10%

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | Input Clock | 14 | | 166 | MHz |
| $f_{OUT}$ | Output Frequency | Spread Off | 13 | | 166 | MHz |
| $t_R$ | Output Rise Time | 15-pF load, 0.8V–2.4V | | 2 | 5 | ns |
| $t_F$ | Output Fall Time | 15-pF load, 2.4V–0.8V | | 2 | 5 | ns |
| $t_{OD}$ | Output Duty Cycle | 15-pF load | 40 | | 60 | % |
| $t_{ID}$ | Input Duty Cycle | | 40 | | 60 | % |
| $t_{JCYC}$ | Jitter, Cycle-to-cycle | | | 250 | 300 | ps |

## Ordering Information

| Ordering Code | Package Type | Product Flow |
|---|---|---|
| CY25245PVC | 20-pin Plastic SSOP | Commercial, 0°C to 70°C |
| CY25245PVCT | 20-pin Plastic SSOP —Tape and Reel | Commercial, 0°C to 70°C |
| **Lead-free** | | |
| CY25245OXC | 20-pin Plastic SSOP | Commercial, 0°C to 70°C |
| CY25245OXCT | 20-pin Plastic SSOP —Tape and Reel | Commercial, 0°C to 70°C |

## Layout Example




**Ceramic Caps C1 = 10–22 µF C2 = 0.005 µF**

**FB = Vishay ILB1206 – 300 (300Ω @ 100 MHz) or TDK ACB2012L-120 or Murata BLM21B601**

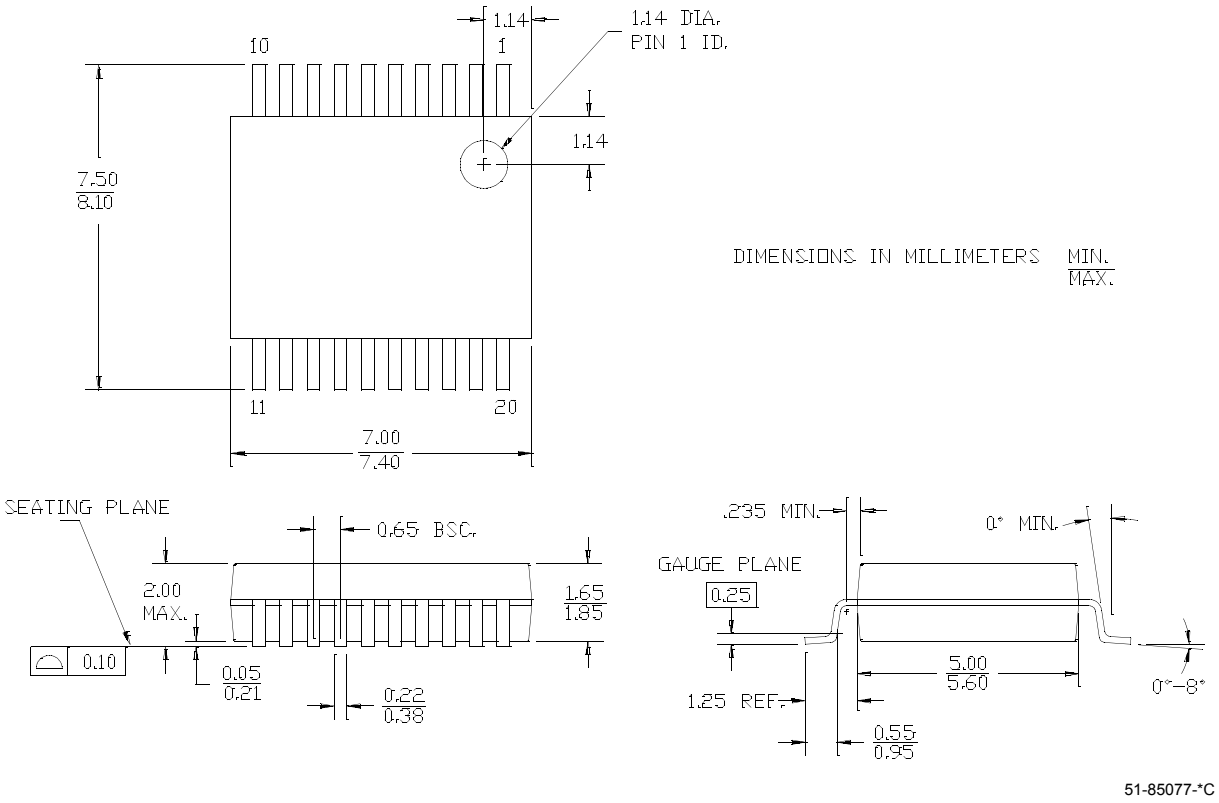
**(G) = VIA to GND plane layer (V) =VIA to respective supply plane layer**

**Note:** Each supply plane or strip should have a **ferrite bead and capacitors**

All bypass caps = 0.1 µF ceramic.

## Package Drawing and Dimension

**20-pin (5.3 mm) Shrunk Small Outline Package O20**

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## Document History Page

| Document Title: CY25245 Frequency-multiplying, Peak-reducing EMI Solution<br>Document Number: 38-07124 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 109865 | 11/13/01 | IKA | New data sheet |
| *A | 122550 | 01/08/03 | RGL | Added SMARTSPREAD™ in the features area |
| *B | 318273 | See ECN | RGL | Added Lead-free devices |

Общество с ограниченной ответственностью «МосЧип»
Адрес: 107023, г.Москва, Семеновский переулок, д.6, офис 409

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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Распределительные склады, находящиеся в России, Европе и в Китае, позволяют нам оперативно поставить необходимые компоненты в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям ISO 9001:2011

**Офис по работе с юридическими лицами:**

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