



# Microprocessor-Compatible 12-Bit D/A Converter

## AD567

### FEATURES

- Single Chip Construction
- Double-Buffered Latch for 8-Bit  $\mu$ P-Compatibility
- Fast Settling Time: 500ns max to  $\pm 1/2$ LSB
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature:  $1/2$ LSB max (AD567K)
- Guaranteed for Operation with  $\pm 12$ V or  $\pm 15$ V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs
- Low Cost

### PRODUCT DESCRIPTION

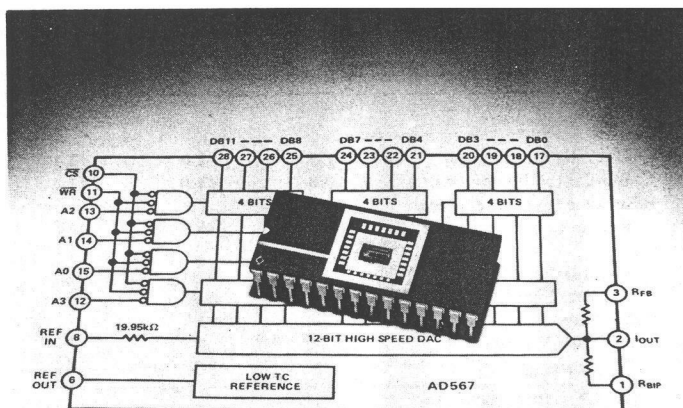
The AD567 is a complete high speed 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD567 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD567 is trimmed at the wafer level and is specified to  $\pm 1/4$ LSB maximum linearity error (K grade) at  $25^{\circ}\text{C}$  and  $\pm 1/2$ LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD567 is thus well suited for wide temperature range performance with  $\pm 1/2$ LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is  $10\text{ppm}/^{\circ}\text{C}$ .

The AD567 is available in three performance grades. The AD567J and K are specified for use over the 0 to  $+70^{\circ}\text{C}$  temperature range and are available in either a 28-pin hermetically-



sealed, ceramic DIP or a 28-pin molded plastic DIP (N package). The AD567S grade is specified for the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range and is available in the ceramic package.

### PRODUCT HIGHLIGHTS

1. The AD567 is a complete current output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a  $\pm 1\%$  maximum error. The reference voltage is also available for external application.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for an A/D converter. The resistors are matched to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current switch design\* provides high dc accuracy and an optimally-damped settling characteristic. Output current settling time is 500 nanoseconds maximum to  $\pm 1/2$ LSB.
6. The single-chip construction makes the AD567 inherently more reliable than multichip hybrid designs. The AD567S grade with guaranteed linearity and monotonicity over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range is especially recommended for high reliability needs in harsh environments. The unit is available processed to MIL-STD-883, Level B.

\*Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.

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# SPECIFICATIONS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = +12V or +15V, V<sub>EE</sub> = -12V or -15V, unless otherwise specified)

MODEL	AD567J			AD567K			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DATA INPUTS<sup>1</sup></b> (Pins 10-15 and 17-28) TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
<b>RESOLUTION</b>							
			12			12	Bits
<b>OUTPUT</b>							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)							
	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R <sub>2</sub> = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance							
		25			25		pF
Compliance Voltage							
T <sub>min</sub> to T <sub>max</sub>	-1.5		+10	-1.5		+10	V
<b>ACCURACY</b> (error relative to full scale) +25°C							
		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.
T <sub>min</sub> to T <sub>max</sub>		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S.
<b>DIFFERENTIAL NONLINEARITY</b> +25°C							
T <sub>min</sub> to T <sub>max</sub>		±1/2	±3/4		±1/4	±1/2	LSB
		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
<b>TEMPERATURE COEFFICIENTS</b> With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
<b>TEMPERATURE RANGE</b>							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
<b>POWER REQUIREMENTS</b>							
V <sub>CC</sub> , +11.4 to +16.5V dc		3	5		3	5	mA
V <sub>EE</sub> , -11.4 to -16.5V dc		-17	-25		-17	-25	mA
<b>POWER SUPPLY GAIN SENSITIVITY<sup>2</sup></b>							
V <sub>CC</sub> = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V <sub>EE</sub> = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
<b>PROGRAMMABLE OUTPUT</b>							
RANGE (see Figures 1, 2, 3)							
		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
<b>EXTERNAL ADJUSTMENTS</b>							
Gain Error with Fixed 50Ω Resistor for R <sub>2</sub> (Figure 2)							
		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R <sub>1</sub> (Figure 3)							
		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
<b>REFERENCE INPUT</b>							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
<b>REFERENCE OUTPUT</b>							
Voltage							
	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)							
	0.1	1.0		0.1	1.0		mA
<b>POWER DISSIPATION</b>							
		300	495		300	495	mW
<b>PRICE (100+)</b>							
		AD567JN	\$12.95		AD567KN	\$17.95	
		AD567JD	\$14.95		AD567KD	\$22.95	

## NOTES

<sup>1</sup>The digital input specifications are guaranteed but not tested over the operating temperature range.

<sup>2</sup>The power supply gain sensitivity is tested in reference to a V<sub>CC</sub>, V<sub>EE</sub> of ±15V dc ±10%.

Specifications subject to change without notice.

MODEL	AD567SD/AD567SD/883B			UNITS
	MIN	TYP	MAX	
<b>DATA INPUTS<sup>1</sup></b> (Pins 10–15 and 17–28)				
TTL or 5 Volt CMOS				
Input Voltage				
Bit ON Logic "1"	+2.0		+5.5	V
Bit OFF Logic "0"			+0.7	V
Logic Current (each bit)				
Bit ON Logic "1"		+120	+300	$\mu$ A
Bit OFF Logic "0"		+35	+100	$\mu$ A
<b>RESOLUTION</b>			12	Bits
<b>OUTPUT</b>				
Current				
Unipolar (all bits on)	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	$\pm$ 0.8	$\pm$ 1.0	$\pm$ 1.2	mA
Resistance (exclusive of span resistors)				
	6k	8k	10k	$\Omega$
Offset				
Unipolar		0.01	0.05	% of F.S.
Bipolar (Figure 3, R <sub>2</sub> = 50 $\Omega$ fixed)		0.05	0.15	% of F.S.
Capacitance				
Compliance Voltage		25		pF
T <sub>min</sub> to T <sub>max</sub>	-1.5		+10	V
<b>ACCURACY</b> (error relative to full scale) +25°C				
		$\pm$ 1/4	$\pm$ 1/2	LSB
		(0.006)	(0.012)	% of F.S.
T <sub>min</sub> to T <sub>max</sub>		$\pm$ 1/2	$\pm$ 3/4	LSB
		(0.012)	(0.018)	% of F.S.
<b>DIFFERENTIAL NONLINEARITY</b>				
+25°C		$\pm$ 1/2	$\pm$ 3/4	LSB
T <sub>min</sub> to T <sub>max</sub>	MONOTONICITY GUARANTEED			
<b>TEMPERATURE COEFFICIENTS</b>				
With Internal Reference				
Unipolar Zero		1	2	ppm/°C
Bipolar Zero		5	10	ppm/°C
Gain (Full Scale)		15	30	ppm/°C
Differential Nonlinearity		2		ppm/°C
<b>TEMPERATURE RANGE</b>				
Operating	-55		+125	°C
Storage	-65		+150	°C
<b>POWER REQUIREMENTS</b>				
V <sub>CC</sub> , +11.4 to +16.5V dc		3	5	mA
V <sub>EE</sub> , -11.4 to -16.5V dc		-17	-25	mA
<b>POWER SUPPLY GAIN SENSITIVITY<sup>2</sup></b>				
V <sub>CC</sub> = +11.4 to +16.5V dc		3	10	ppm of F.S./%
V <sub>EE</sub> = -11.4 to -16.5V dc		15	25	ppm of F.S./%
<b>PROGRAMMABLE OUTPUT RANGES</b> (see Figures 1, 2, 3)				
		0 to +5		V
		-2.5 to +2.5		V
		0 to +10		V
		-5 to +5		V
		-10 to +10		V
<b>EXTERNAL ADJUSTMENTS</b>				
Gain Error with Fixed 50 $\Omega$				
Resistor for R2 (Figure 2)		$\pm$ 0.1	$\pm$ 0.25	% of F.S.
Bipolar Zero Error with Fixed 50 $\Omega$ Resistor for R1 (Figure 3)				
Gain Adjustment Range (Figure 2)	$\pm$ 0.25	$\pm$ 0.05	$\pm$ 0.15	% of F.S.
Bipolar Zero Adjustment Range	$\pm$ 0.15			% of F.S.
<b>REFERENCE INPUT</b>				
Input Impedance	15k	20k	25k	$\Omega$
<b>REFERENCE OUTPUT</b>				
Voltage				
	9.90	10.00	10.10	V
Current (available for external loads)				
	0.1	1.0		mA
<b>POWER DISSIPATION</b>				
		300	495	mW
<b>PRICE</b> (100+)				
		AD567SD	\$59.00	
		AD567SD/883B	\$68.00	

Specifications subject to change without notice.

## TIMING SPECIFICATIONS

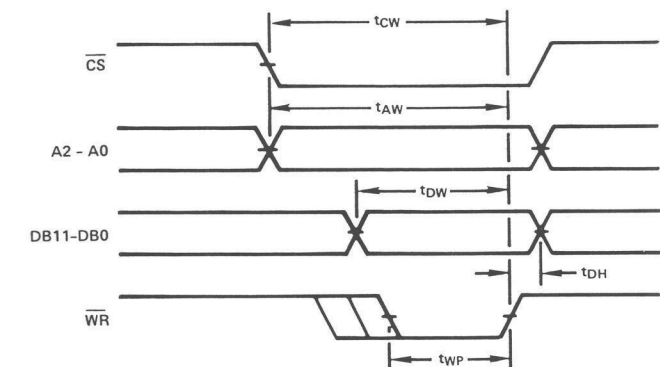
(All Models,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +12\text{V}$  or  $+15\text{V}$ ,  $V_{EE} = -12\text{V}$  or  $-15\text{V}$ )

Symbol	Parameter	Min	Typ	Max	
$t_{DW}$	Data Valid to End of $\overline{WR}$	50	—	—	ns
$t_{CW}$	$\overline{CS}$ Valid to End of $\overline{WR}$	100	—	—	ns
$t_{AW}$	Address Valid to End of $\overline{WR}$	100	—	—	ns
$t_{WP}$	Write Pulse Width	100	—	—	ns
$t_{DH}$	Data Hold Time	0	—	—	ns
$t_{SETT}$	Output Current Settling Time	—	400	500	ns

## TIMING DIAGRAMS

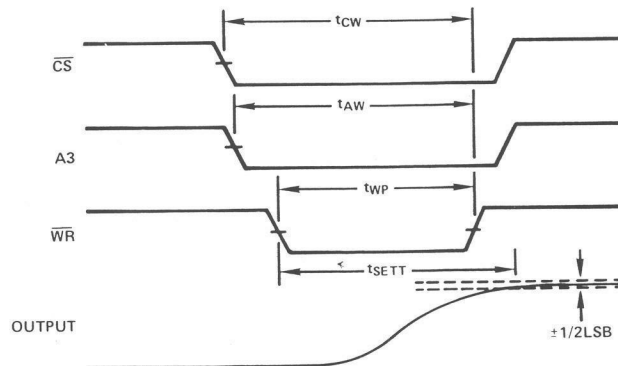
### WRITE CYCLE #1

(Load First Rank from Data Bus;  $A_3 = 1$ )



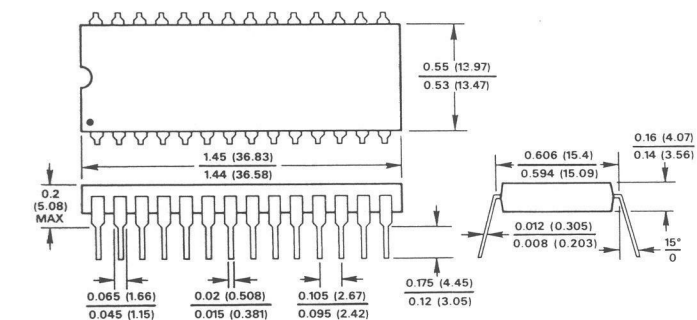
### WRITE CYCLE #2

(Load Second Rank from First Rank;  $A_2, A_1, A_0 = 1$ )



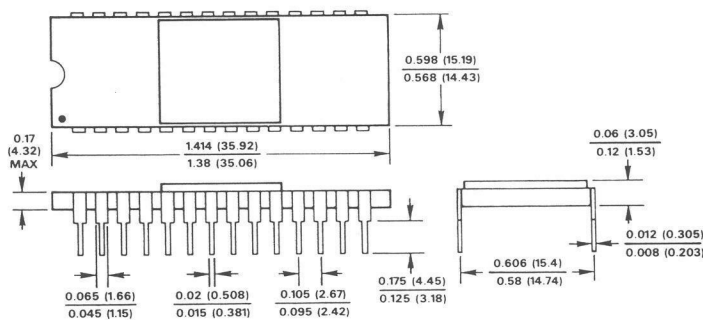
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

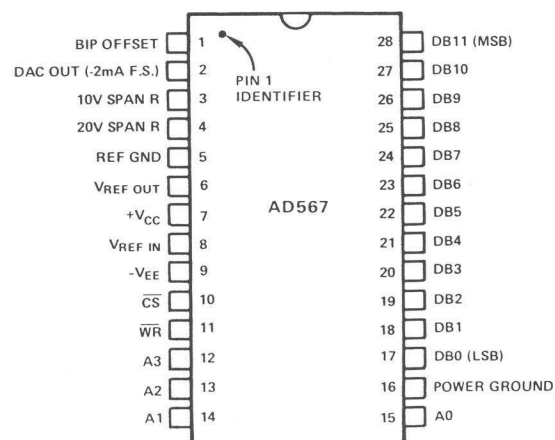
28-Pin Plastic DIP (N Package)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
LEADS ARE GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

28-Pin Ceramic DIP (D Package)

## PIN CONNECTIONS TOP VIEW



## AD567 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	GAIN T.C. MAX
AD567JN	Plastic	Com	±1/2LSB	50ppm/°C
AD567KN	Plastic	Com	±1/4LSB	20ppm/°C
AD567JD	Ceramic	Com	±1/2LSB	50ppm/°C
AD567KD	Ceramic	Com	±1/4LSB	20ppm/°C
AD567SD	Ceramic	Mil	±1/2LSB	30ppm/°C
AD567SD/883B	Ceramic	Mil	±1/2LSB	30ppm/°C



## THE AD567 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

**RELATIVE ACCURACY:** Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. - 1LSB) for any bit combination. The AD567 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K version and 1/2LSB for the J and S.

**MONOTONICITY:** A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of input. All versions of the AD567 are monotonic over their full operating temperature range.

**DIFFERENTIAL NONLINEARITY:** Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB =  $10\text{V} \times 1/4096 = 2.44\text{mV}$ ). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD567K has a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% ( $100^\circ\text{C} \times 1.0\text{ppm}/^\circ\text{C}$ ) of error. The resulting error could then be as much as 0.01% + 0.006% (initial error, 1/4LSB) = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD567 are 100% tested for monotonicity over the full operating temperature range.

### ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L; AD517L; AD741L; AD301AL; AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within  $\pm 1/2\text{LSB}$  (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within  $\pm 2\text{LSB}$  (0.05%).

The AD544 is recommended for buffered voltage-output applications which require fast settling time to  $\pm 1/2\text{LSB}$ . The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

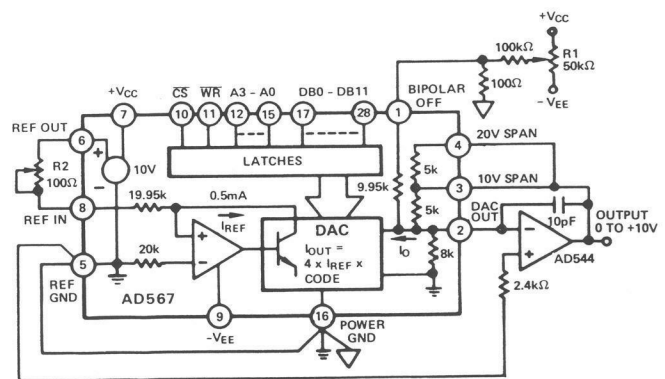


Figure 1. 0 to +10V Unipolar Voltage Output

### FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 1, should be grounded if not used for trimming.

#### STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 1 should be connected to pin 5.

#### STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 3 to the op amp output.

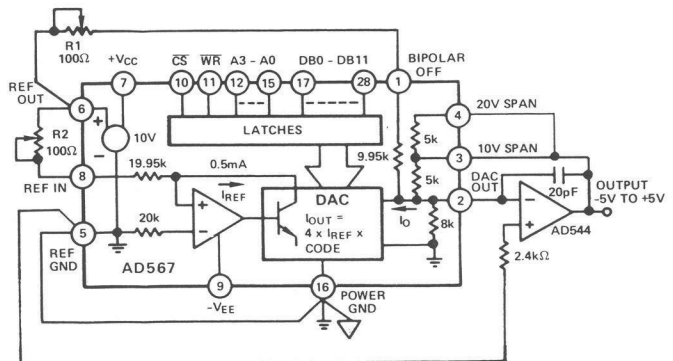


Figure 2. ±5V Bipolar Voltage Output

### FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

#### STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

#### STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.





Figure 8 shows an addressing scheme for use with an AD567 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to  $\overline{CS}$ . The two LSBs of the address bus are connected as shown to the AD567 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

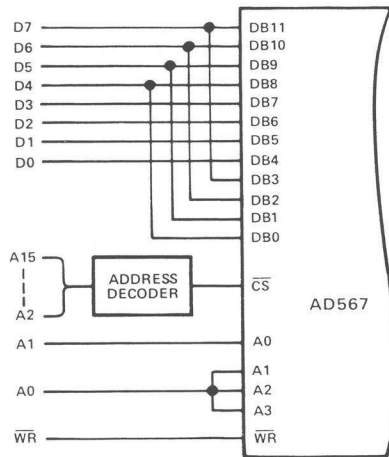


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD567 still occupies two adjacent locations in the processor's memory map.

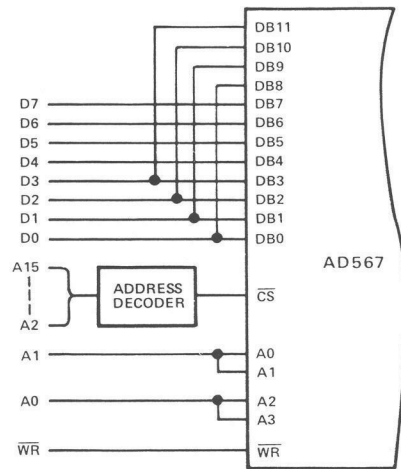


Figure 9. Right-Justified 8-Bit Bus Interface

#### USING MULTIPLE AD567 DACS IN 8-BIT SYSTEMS

Many applications use multiple digital-to-analog converters driven from the same data bus. For example, automatic test equipment systems often require all analog outputs to be produced simultaneously. Vector-scan graphic systems require that the X and Y coordinates of the stroke endpoints be updated simultaneously. The AD567 can be used with a very simple address decoder to perform this function, as shown in Figure 10. The 74LS139 two-line to four-line decoder and one inverter provide a set of distinct address pulses which assign the registers of the two DACs to a block of consecutive memory locations. In this circuit, write operations to addresses X000 and X001 load the first rank registers of one DAC in a right-justified data format. Addresses X010 and X011 load the first rank of another DAC, also in a right-justified format. A write to any address from X100 to X111 will load the second rank registers of both DACs simultaneously from their respective first rank registers.

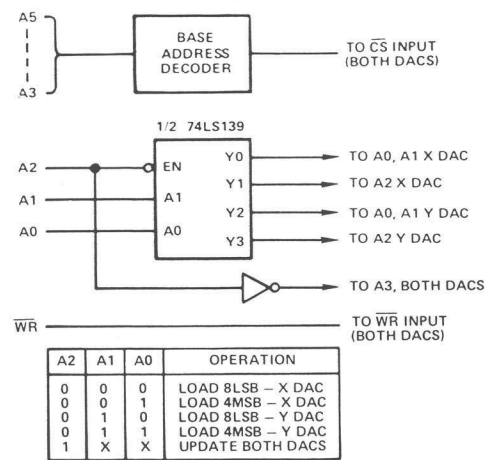


Figure 10. Addressing for Two DACs (Right-Justified) on 8-Bit Bus

#### USING THE AD567 WITH 12- AND 16-BIT BUSES

The AD567 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines ( $\overline{A0}$  through  $\overline{A3}$ ) are tied to low, and the latch is enabled by  $\overline{CS}$  and  $\overline{WR}$  going low. The AD567 thus occupies a single memory location.

This configuration renders the second rank register transparent, using the first rank of registers as the data latch. The  $\overline{CS}$  input can be driven from an active-low decoded address, and  $\overline{WR}$  can be the system  $\overline{WR}$  signal. It should be noted that any data bus activity during the period when  $\overline{CS}$  and  $\overline{WR}$  are both active will cause activity at the AD567 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

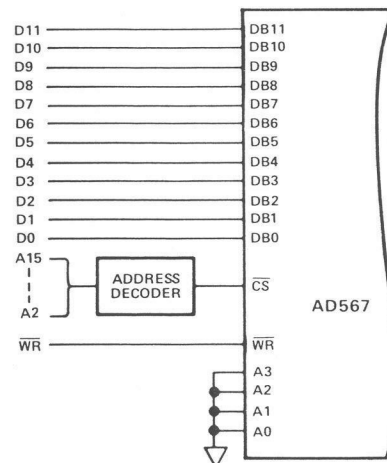


Figure 11. Connections for 12- and 16-Bit Bus Interface

#### DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 12. The input line can be modeled as a 30kΩ resistance connected to a -0.7V rail, in parallel with a 5pF capacitance to ground.

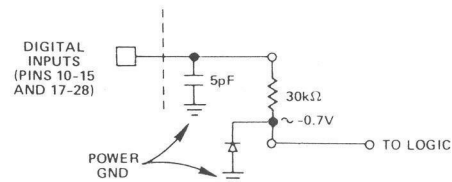


Figure 12. Equivalent Digital Input Circuit

## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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