

## Features

- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - 25-ns, 30-ns and 45-ns access times
  - Internally organized as 2048K × 8 (CY14X116L), 1024K × 16 (CY14X116N), 512K × 32 (CY14X116S)
  - Hands-off automatic STORE on power-down with only a small capacitor
  - STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
  - RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Sleep mode operation
- Low power consumption
  - Active current of 75 mA at 45 ns
  - Standby mode current of 650 μA
  - Sleep mode current of 10 μA
- Operating voltages:
  - CY14B116X: V<sub>CC</sub> = 2.7 V to 3.6 V
  - CY14E116X: V<sub>CC</sub> = 4.5 V to 5.5 V
- Industrial temperature: -40 °C to +85 °C
- Packages
  - 44-pin thin small-outline package (TSOP II)
  - 48-pin thin small-outline package (TSOP I)
  - 54-pin thin small-outline package (TSOP II)
  - 60-ball fine-pitch ball grid array (FBGA) package
  - 165-ball fine-pitch ball grid array (FBGA) package
- Restriction of hazardous substances (RoHS) compliant

## ■ Offered speeds

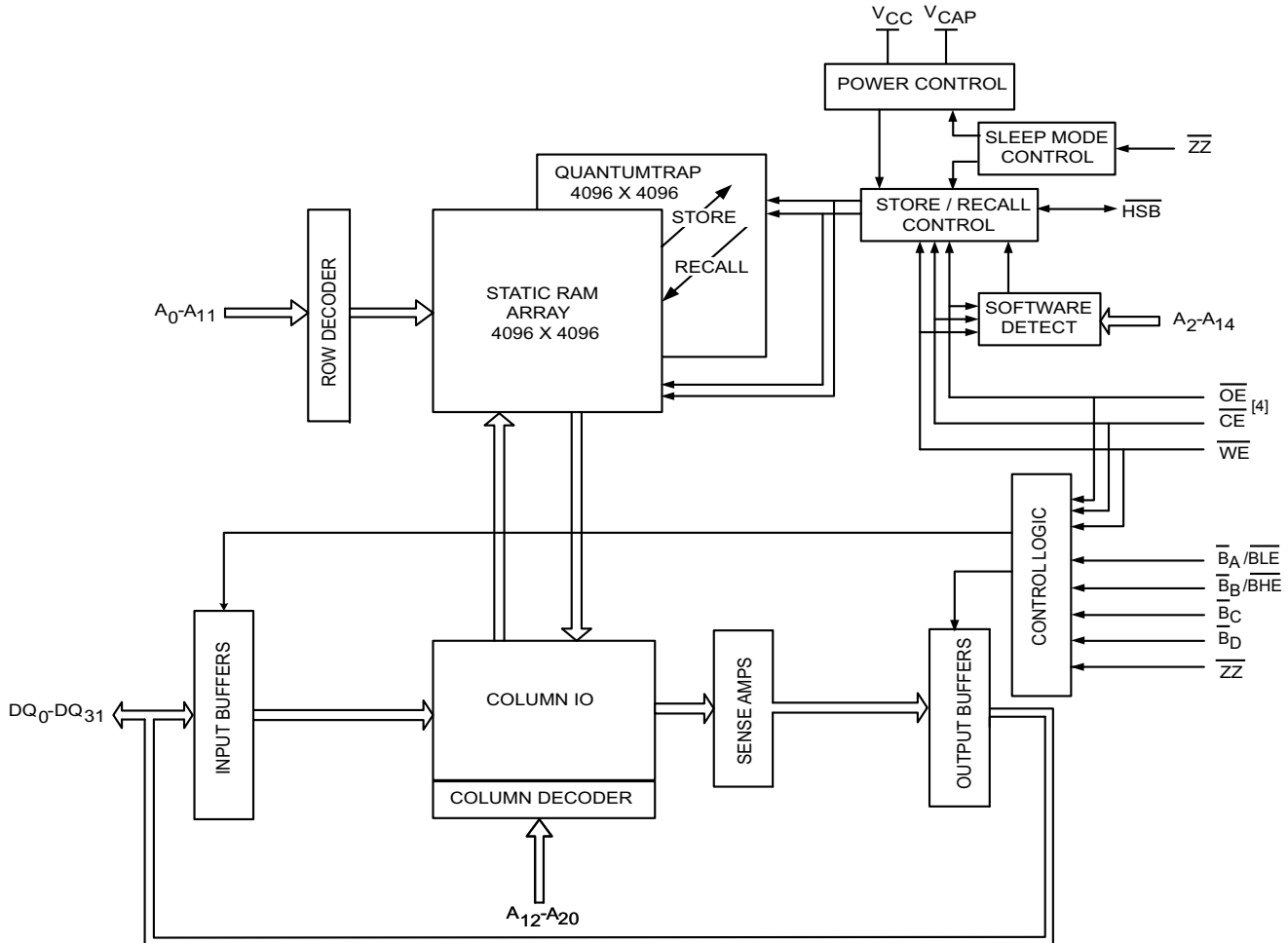
- 44-pin TSOP II: 25 ns and 45 ns
- 48-pin TSOP I: 30 ns and 45 ns
- 54-pin TSOP II: 25 ns and 45 ns
- 60-ball FBGA: 25 ns
- 165-ball FBGA: 25 ns and 45 ns

## Functional Description

The Cypress CY14X116L/CY14X116N/CY14X116S is a fast SRAM, with a nonvolatile element in each memory cell. The memory is organized as 2048K bytes of 8 bits each or 1024K words of 16 bits each or 512K words of 32 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data residing in the nonvolatile elements do not change when data is written to the SRAM. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click [here](#).

Logic Block Diagram<sup>[1, 2, 3]</sup>



Notes

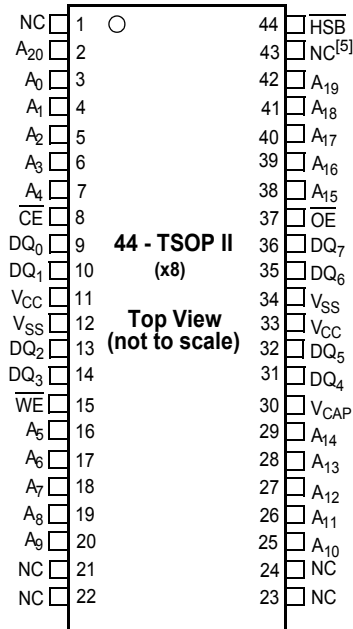
1. Address A<sub>0</sub>–A<sub>20</sub> for ×8 configuration, address A<sub>0</sub>–A<sub>19</sub> for ×16 configuration and address A<sub>0</sub>–A<sub>18</sub> for ×32 configuration.
2. Data DQ<sub>0</sub>–DQ<sub>7</sub> for ×8 configuration, data DQ<sub>0</sub>–DQ<sub>15</sub> for ×16 configuration and data DQ<sub>0</sub>–DQ<sub>31</sub> for ×32 configuration.
3. BLE, BHE are applicable for ×16 configuration and BA, BB, BC, BD are applicable for ×32 configuration only.
4. TSOP II package is offered in single CE. TSOP I and BGA packages are offered in dual CE options. In this datasheet, for a dual CE device, CE refers to the internal logical combination of CE<sub>1</sub> and CE<sub>2</sub> such that when CE<sub>1</sub> is LOW and CE<sub>2</sub> is HIGH, CE is LOW. For all other cases CE is HIGH.

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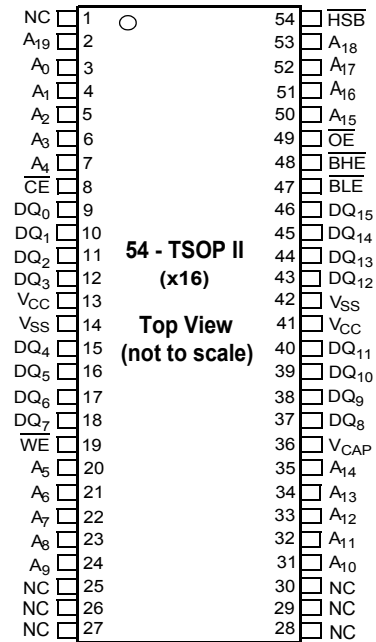
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**Pinouts**

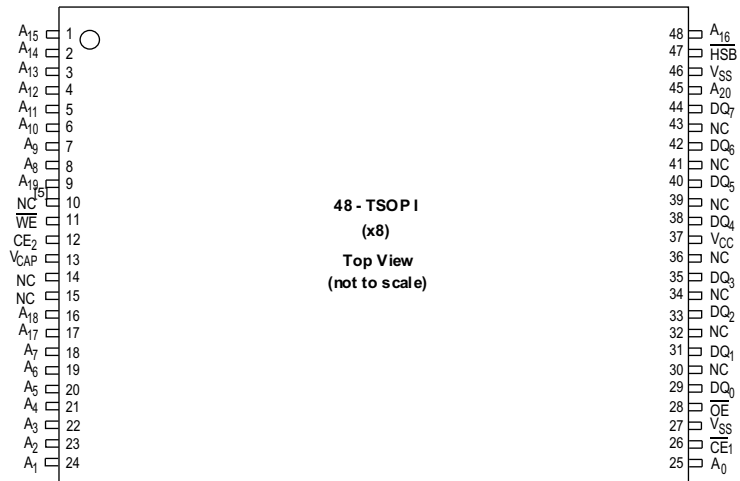
**Figure 1. Pin Diagram: 44-Pin TSOP II (x8)**



**Figure 2. Pin Diagram: 54-Pin TSOP II (x16)**



**Figure 3. Pin Diagram: 48-Pin TSOP I (x8)**

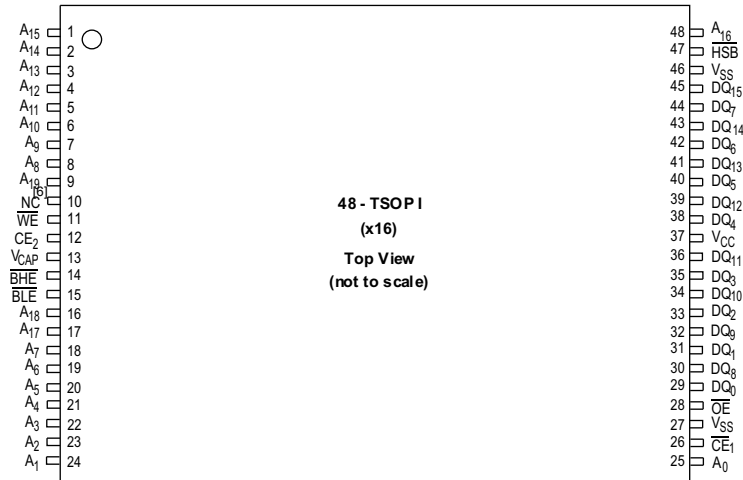


**Note**

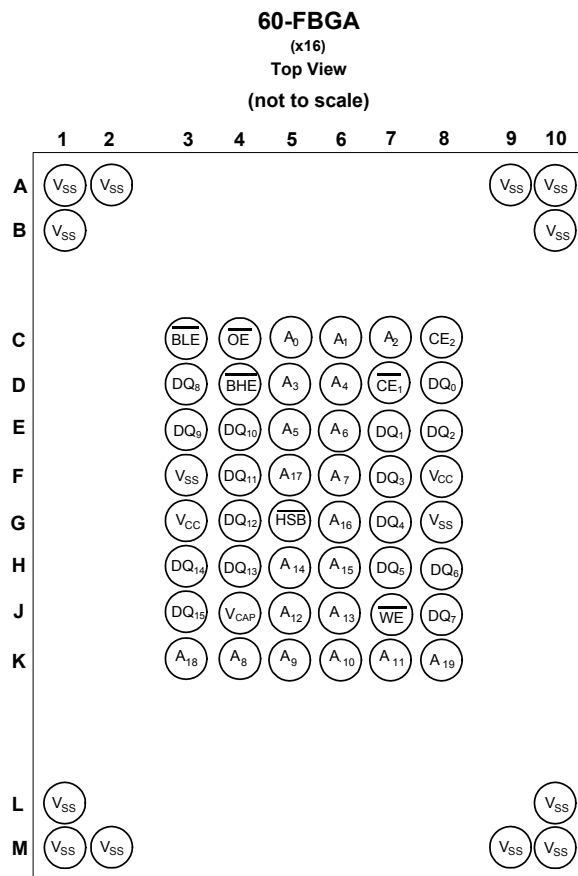
5. Address expansion for 32-Mbit. NC pin not connected to die.

**Pinouts** (continued)

**Figure 4. Pin Diagram: 48-Pin TSOP I (x16)**



**Figure 5. 60-ball FBGA pinout (x 16)**



**Note**  
 6. Address expansion for 32-Mbit. NC pin not connected to die.

**Pinouts** (continued)

**Figure 6. Pin Diagram: 165-Ball FBGA (×16)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A <sub>6</sub>	A <sub>8</sub>	$\overline{WE}$	$\overline{BLE}$	$\overline{CE}_1$	NC	$\overline{OE}$	A <sub>5</sub>	A <sub>3</sub>	NC
<b>B</b>	NC	DQ <sub>0</sub>	DQ <sub>1</sub>	A <sub>4</sub>	$\overline{BHE}$	CE <sub>2</sub>	NC	A <sub>2</sub>	NC	NC	NC
<b>C</b>	$\overline{ZZ}$	NC	NC	V <sub>SS</sub>	A <sub>0</sub>	A <sub>7</sub>	A <sub>1</sub>	V <sub>SS</sub>	NC	DQ <sub>15</sub>	DQ <sub>14</sub>
<b>D</b>	NC	DQ <sub>2</sub>	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
<b>E</b>	NC	V <sub>CAP</sub>	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	DQ <sub>13</sub>	NC
<b>F</b>	NC	DQ <sub>3</sub>	NC	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>12</sub>
<b>G</b>	$\overline{HSB}$	NC	NC	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	NC
<b>H</b>	NC	NC	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
<b>J</b>	NC	NC	NC	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	DQ <sub>8</sub>	NC
<b>K</b>	NC	NC	DQ <sub>4</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	NC
<b>L</b>	NC	DQ <sub>5</sub>	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>9</sub>
<b>M</b>	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	DQ <sub>10</sub>	NC
<b>N</b>	NC	DQ <sub>6</sub>	DQ <sub>7</sub>	V <sub>SS</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	V <sub>SS</sub>	NC	NC	NC
<b>P</b>	NC	NC	NC	A <sub>13</sub>	A <sub>19</sub>	NC	A <sub>18</sub>	A <sub>12</sub>	NC	DQ <sub>11</sub>	NC
<b>R</b>	NC	NC	A <sub>15</sub>	NC	A <sub>17</sub>	NC	A <sub>16</sub>	NC <sup>[7]</sup>	A <sub>14</sub>	NC	NC

**Figure 7. Pin Diagram: 165-Ball FBGA (×32)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A <sub>6</sub>	A <sub>8</sub>	$\overline{WE}$	$\overline{B}_A$	$\overline{CE}_1$	$\overline{B}_C$	$\overline{OE}$	A <sub>5</sub>	A <sub>3</sub>	NC
<b>B</b>	NC	DQ <sub>0</sub>	DQ <sub>1</sub>	A <sub>4</sub>	$\overline{B}_B$	CE <sub>2</sub>	$\overline{B}_D$	A <sub>2</sub>	NC	NC	DQ <sub>31</sub>
<b>C</b>	$\overline{ZZ}$	NC	DQ <sub>4</sub>	V <sub>SS</sub>	A <sub>0</sub>	A <sub>7</sub>	A <sub>1</sub>	V <sub>SS</sub>	NC	DQ <sub>27</sub>	DQ <sub>26</sub>
<b>D</b>	NC	DQ <sub>2</sub>	DQ <sub>5</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	DQ <sub>30</sub>
<b>E</b>	NC	V <sub>CAP</sub>	DQ <sub>6</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	DQ <sub>25</sub>	DQ <sub>29</sub>
<b>F</b>	NC	DQ <sub>3</sub>	DQ <sub>7</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>24</sub>
<b>G</b>	$\overline{HSB}$	NC	DQ <sub>12</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>28</sub>
<b>H</b>	NC	NC	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
<b>J</b>	NC	NC	DQ <sub>13</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	DQ <sub>20</sub>	DQ <sub>19</sub>
<b>K</b>	NC	NC	DQ <sub>8</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>18</sub>
<b>L</b>	NC	DQ <sub>9</sub>	DQ <sub>14</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	NC	DQ <sub>21</sub>
<b>M</b>	NC	NC	DQ <sub>15</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	DQ <sub>22</sub>	DQ <sub>17</sub>
<b>N</b>	NC	DQ <sub>10</sub>	DQ <sub>11</sub>	V <sub>SS</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	V <sub>SS</sub>	NC	NC	DQ <sub>16</sub>
<b>P</b>	NC	NC	NC	A <sub>13</sub>	NC	NC	A <sub>18</sub>	A <sub>12</sub>	NC	DQ <sub>23</sub>	NC
<b>R</b>	NC	NC	A <sub>15</sub>	NC	A <sub>17</sub>	NC	A <sub>16</sub>	NC <sup>[7]</sup>	A <sub>14</sub>	NC	NC

**Note**

7. Address expansion for 32-Mbit. NC pin not connected to die.

## Pin Definitions

Pin Name	I/O Type	Description
A <sub>0</sub> – A <sub>20</sub>	Input	Address inputs. Used to select one of the 2,097,152 bytes of the nvSRAM for the ×8 configuration.
A <sub>0</sub> – A <sub>19</sub>		Address inputs. Used to select one of the 1,048,576 words of the nvSRAM for the ×16 configuration.
A <sub>0</sub> – A <sub>18</sub>		Address inputs. Used to select one of the 524,288 words of the nvSRAM for the ×32 configuration.
DQ <sub>0</sub> – DQ <sub>7</sub>	Input/Output	<b>Bidirectional data I/O lines for the ×8 configuration.</b> Used as input or output lines depending on operation.
DQ <sub>0</sub> – DQ <sub>15</sub>		<b>Bidirectional data I/O lines for the ×16 configuration.</b> Used as input or output lines depending on operation.
DQ <sub>0</sub> – DQ <sub>31</sub>		<b>Bidirectional data I/O lines for ×32 configuration.</b> Used as input or output lines depending on operation.
$\overline{\text{WE}}$	Input	<b>Write Enable input, Active LOW.</b> When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{\text{CE}}$	Input	<b>Chip Enable input in TSOP II package, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{CE}}_1, \text{CE}_2$		<b>Chip Enable input in FBGA package.</b> The device is selected and a memory access begins on the falling edge of $\overline{\text{CE}}_1$ (while $\text{CE}_2$ is HIGH) or the rising edge of $\text{CE}_2$ (while $\overline{\text{CE}}_1$ is LOW).
$\overline{\text{OE}}$	Input	<b>Output Enable, Active LOW.</b> The Active LOW $\overline{\text{OE}}$ input enables the data output buffers during read cycles. Deasserting $\overline{\text{OE}}$ HIGH causes the I/O pins to tristate.
$\overline{\text{BLE}}/\overline{\text{B}}_A$ <sup>[8]</sup>	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>7</sub> –DQ <sub>0</sub> .
$\overline{\text{BHE}}/\overline{\text{B}}_B$ <sup>[8]</sup>	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>15</sub> –DQ <sub>8</sub> .
$\overline{\text{B}}_C$ <sup>[8]</sup>	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>23</sub> –DQ <sub>16</sub> .
$\overline{\text{B}}_D$ <sup>[8]</sup>	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>31</sub> –DQ <sub>24</sub> .
$\overline{\text{ZZ}}$ <sup>[9]</sup>	Input	<b>Sleep Mode Enable.</b> When the $\overline{\text{ZZ}}$ pin is pulled LOW, the device enters a low-power Sleep mode and consumes the lowest power. Since this input is logically AND'ed with $\overline{\text{CE}}$ , $\overline{\text{ZZ}}$ must be HIGH for normal operation.
V <sub>CC</sub>	Power Supply	<b>Power supply inputs to the device.</b>
V <sub>SS</sub>	Power Supply	<b>Ground for the device.</b> Must be connected to ground of the system.
$\overline{\text{HSB}}$	Input/Output	<b>Hardware STORE Busy (HSB).</b> When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, $\overline{\text{HSB}}$ is driven HIGH for a short time (t <sub>HHD</sub> ) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V <sub>CAP</sub>	Power Supply	<b>AutoStore capacitor.</b> Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	NC	<b>No Connect.</b> Die pads are not connected to the package pin.

### Notes

- $\overline{\text{BLE}}$ ,  $\overline{\text{BHE}}$  are applicable for ×16 configuration and  $\overline{\text{B}}_A$ ,  $\overline{\text{B}}_B$ ,  $\overline{\text{B}}_C$ ,  $\overline{\text{B}}_D$  are applicable for ×32 configuration only.
- Sleep mode feature is offered in 165-ball FBGA package only.

## Device Operation

The CY14X116L/CY14X116N/CY14X116S nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) automatically at power-down, or from the nonvolatile cell to the SRAM (the RECALL operation) on power-up. Both the STORE and RECALL operations are also available under software control. Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14X116L/CY14X116N/CY14X116S supports infinite reads and writes to the SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the [Truth Table For SRAM Operations on page 24](#) for a complete description of read and write modes.

### SRAM Read

The CY14X116L/CY14X116N/CY14X116S performs a read cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW, and  $\overline{WE}$ ,  $\overline{ZZ}$ , and  $\overline{HSB}$  are HIGH. The address specified on pins  $A_0$ – $A_{20}$  or  $A_0$ – $A_{19}$  or  $A_0$ – $A_{18}$  determines which of the 2,097,152 data bytes or 1,048,576 words of 16 bits or 524,288 words of 32 bits each are accessed. Byte enables ( $\overline{BLE}$ ,  $\overline{BHE}$ ) determine which bytes are enabled to the output, in the case of 16-bit words and byte enables ( $\overline{B_A}$ ,  $\overline{B_B}$ ,  $\overline{B_C}$ ,  $\overline{B_D}$ ) determine which bytes are enabled to the output, in the case of 32-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of  $t_{AA}$  (read cycle 1). If the read is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at  $t_{ACE}$  or at  $t_{DOE}$ , whichever is later (read cycle 2). The data output repeatedly responds to address changes within the  $t_{AA}$  access time without the need for transitions on any control input pins. This remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or  $\overline{WE}$  or  $\overline{HSB}$  is brought LOW.

### SRAM Write

A write cycle is performed when  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{HSB}$  is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until  $\overline{CE}$  or  $\overline{WE}$  goes HIGH at the end of the cycle. The data on the common I/O pins  $DQ_0$ – $DQ_{31}$  is written into the memory if it is valid  $t_{SD}$  before the end of a  $\overline{WE}$ -controlled write or before the end of a  $\overline{CE}$ -controlled write. The Byte Enable inputs ( $\overline{BLE}$ ,  $\overline{BHE}$ ) determine which bytes are written, in the case of 16-bit words and Byte Enable inputs ( $\overline{B_A}$ ,  $\overline{B_B}$ ,  $\overline{B_C}$ ,  $\overline{B_D}$ ) determine which bytes are written, in the case of 32-bit words. Keep  $\overline{OE}$  HIGH during the entire write cycle to avoid data bus contention on the common I/O lines. If  $\overline{OE}$  is left LOW, the internal circuitry turns off the output buffers  $t_{HZWE}$  after  $\overline{WE}$  goes LOW.

### AutoStore Operation (Power-Down)

The CY14X116L/CY14X116N/CY14X116S stores data to the nonvolatile QuantumTrap cells using one of the three storage operations. These three operations are: Hardware STORE, activated by the  $\overline{HSB}$ ; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of nvSRAM and is enabled by default on the CY14X116L/CY14X116N/CY14X116S.

During normal operation, the device draws current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part automatically disconnects the  $V_{CAP}$  pin from  $V_{CC}$  and a STORE operation is initiated with power provided by the  $V_{CAP}$  capacitor.

**Note** If the capacitor is not connected to the  $V_{CAP}$  pin, AutoStore must be disabled using the soft sequence specified in the section [Preventing AutoStore on page 12](#). If AutoStore is enabled without a capacitor on the  $V_{CAP}$  pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM.

**Figure 8. AutoStore Mode**

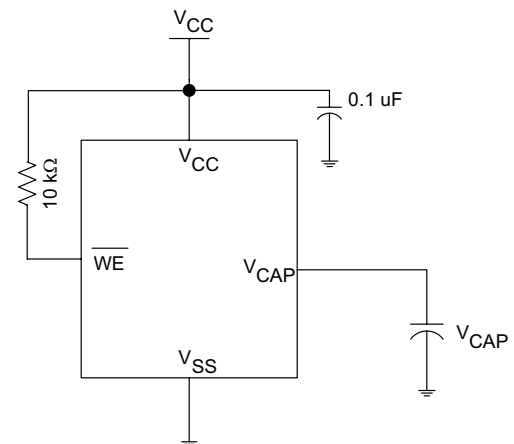


Figure 8 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for the automatic STORE operation. Refer to [DC Electrical Characteristics on page 13](#) for the size of the  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to  $V_{V_{CAP}}$  by a regulator on the chip. A pull-up resistor should be placed on  $\overline{WE}$  to hold it inactive during power-up. This pull-up resistor is only effective if the  $\overline{WE}$  signal is in tristate during power-up. When the nvSRAM comes out of power-up-RECALL, the host microcontroller must be active or the  $\overline{WE}$  held inactive until the host microcontroller comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place (which sets a write latch) since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.



### Hardware STORE ( $\overline{\text{HSB}}$ ) Operation

The CY14X116L/CY14X116N/CY14X116S provides the  $\overline{\text{HSB}}$  pin to control and acknowledge the STORE operations. The  $\overline{\text{HSB}}$  pin is used to request a Hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven LOW, the device conditionally initiates a STORE operation after  $t_{\text{DELAY}}$ . A STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver (an internal 100-k $\Omega$  weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

**Note** After each Hardware and Software STORE operation,  $\overline{\text{HSB}}$  is driven HIGH for a short time ( $t_{\text{HHHD}}$ ) with standard output high current and then remains HIGH by an internal 100-k $\Omega$  pull-up resistor.

SRAM write operations that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means are given time ( $t_{\text{DELAY}}$ ) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH. If the write latch is not set,  $\overline{\text{HSB}}$  is not driven LOW by the device. However, any of the SRAM read and write cycles are inhibited until  $\overline{\text{HSB}}$  is returned HIGH by the host microcontroller or another external source.

During any STORE operation, regardless of how it is initiated, the device continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for  $t_{\text{LZHSB}}$  time after the  $\overline{\text{HSB}}$  pin returns HIGH. Leave the  $\overline{\text{HSB}}$  unconnected if it is not used.

### Hardware RECALL (Power-Up)

During power-up or after any low-power condition ( $V_{\text{CC}} < V_{\text{SWITCH}}$ ), an internal RECALL request is latched. When  $V_{\text{CC}}$  again exceeds the  $V_{\text{SWITCH}}$  on power-up, a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete. During this time, the  $\overline{\text{HSB}}$  pin is driven LOW by the  $\overline{\text{HSB}}$  driver and all reads and writes to nvSRAM are inhibited.

### Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. A Software STORE cycle is initiated by executing sequential  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read cycles from six specific address locations in exact order. During the

STORE cycle, the previous nonvolatile data is first erased, followed by a store into the nonvolatile elements. After a STORE cycle is initiated, further reads and writes are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Otherwise, the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with  $\overline{\text{CE}}$ -controlled reads or  $\overline{\text{OE}}$ -controlled reads, with  $\overline{\text{WE}}$  kept HIGH for all the six read sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled.  $\overline{\text{HSB}}$  is driven LOW. After the  $t_{\text{STORE}}$  cycle time is fulfilled, the SRAM is activated again for the read and write operation.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, perform the following sequence of  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read operations:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

### Sleep Mode

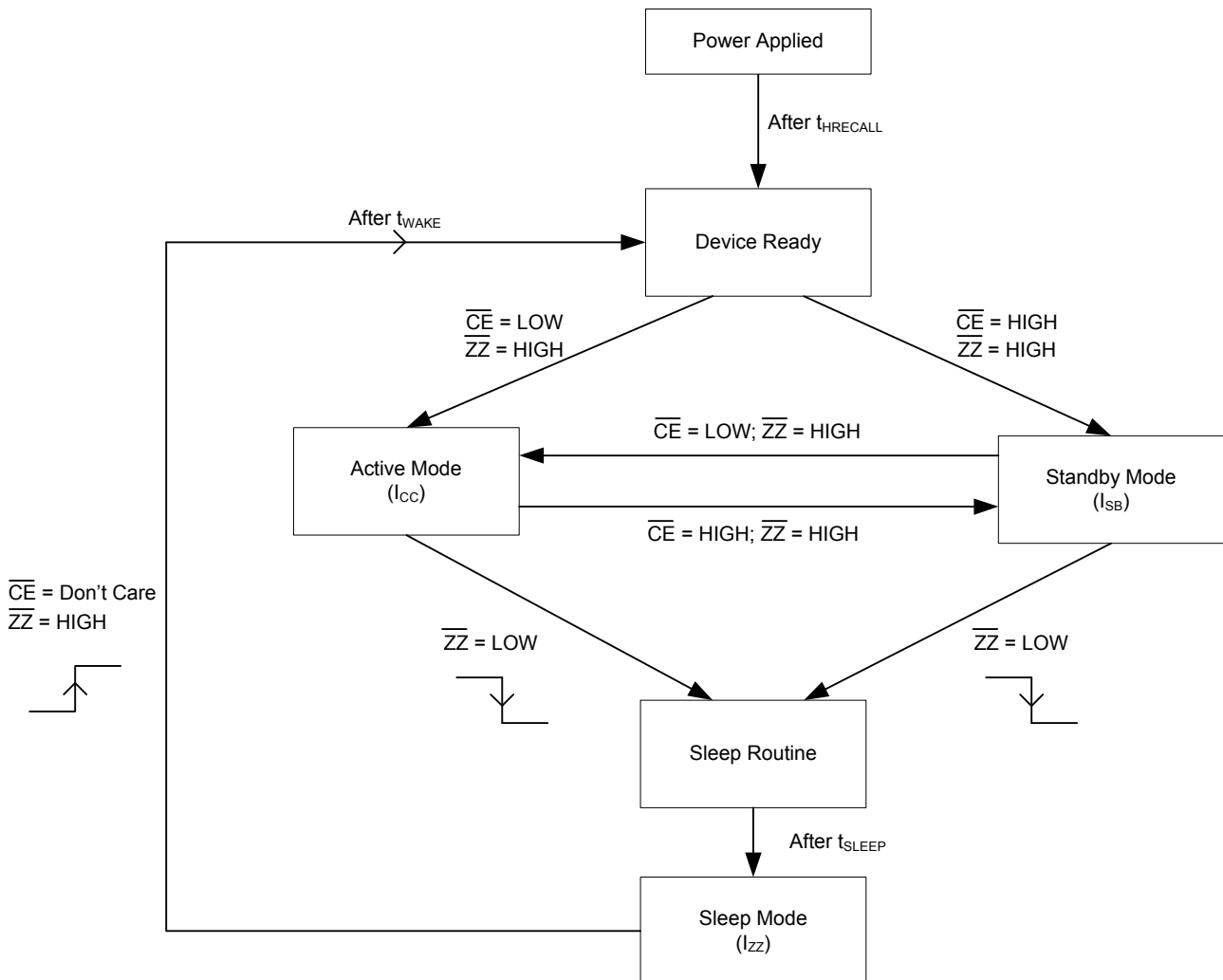
In Sleep mode, the device consumes the lowest power supply current ( $I_{ZZ}$ ). The device enters a low-power Sleep mode after asserting the  $\overline{ZZ}$  pin LOW. After the Sleep mode is registered, the nvSRAM does a STORE operation to secure the data to the nonvolatile memory and then enters the low-power mode. The device starts consuming  $I_{ZZ}$  current after  $t_{SLEEP}$  time from the instance when the sleep mode is initiated. When the  $\overline{ZZ}$  pin is LOW, all input pins are ignored except the  $\overline{ZZ}$  pin. The nvSRAM is not accessible for normal operations while it is in sleep mode.

When the  $\overline{ZZ}$  pin is de-asserted (HIGH), there is a delay  $t_{WAKE}$  before the user can access the device. If sleep mode is not used, the  $\overline{ZZ}$  pin should be tied to  $V_{CC}$ .

**Note** When nvSRAM enters sleep mode, it initiates a nonvolatile STORE cycle, which results in losing one endurance cycle for every Sleep mode entry unless data has not been written to the nvSRAM since the last nonvolatile STORE/RECALL operation.

**Note** If the  $\overline{ZZ}$  pin is LOW during power-up, the device will not be in Sleep mode. However, the I/Os are in tristate until the  $\overline{ZZ}$  pin is de-asserted (HIGH).

**Figure 9. Sleep Mode ( $\overline{ZZ}$ ) Flow Diagram**



**Table 1. Mode Selection**

$\overline{CE}^{[10]}$	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}, \overline{BHE} / \overline{B}_A, \overline{B}_B, \overline{B}_C, \overline{B}_D^{[11]}$	$A_{15} - A_0^{[12]}$	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active <sup>[13]</sup>
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active <sup>[13]</sup>
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{CC2}^{[13]}$
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active <sup>[13]</sup>

**Notes**

10. The TSOP II package is offered in single  $\overline{CE}$ . TSOP I, and BGA packages are offered in dual  $\overline{CE}$  options. In this datasheet, for a dual  $\overline{CE}$  device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{CE}$  for the single chip enable device;  $\overline{CE}_1$  and  $\overline{CE}_2$  for the dual chip enable device).
11.  $\overline{BLE}$ ,  $\overline{BHE}$  are applicable for the  $\times 16$  configuration and  $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$ ,  $\overline{B}_D$  are applicable for the  $\times 32$  configuration only.
12. While there are 21 address lines on the CY14X116L (20 address lines on the CY14X116N and 19 address lines on the CY14X116S), only 13 address lines ( $A_{14}-A_2$ ) are used to control software modes. The remaining address lines are don't care.
13. The six consecutive address locations must be in the order listed.  $\overline{WE}$  must be HIGH during all six cycles to enable a nonvolatile operation.

### Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of  $\overline{CE}$  or  $\overline{OE}$  controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of  $\overline{CE}$  or  $\overline{OE}$  controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual software STORE operation must be performed to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

### Data Protection

The CY14X116L/CY14X116N/CY14X116S protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and write operations. The low-voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ . If the CY14X116L/CY14X116N/CY14X116S is in a write mode at power-up (both  $\overline{CE}$  and  $\overline{WE}$  are LOW), after a RECALL or STORE, the write is inhibited until the SRAM is enabled after  $t_{LZHSB}$  ( $\overline{HSB}$  to output active). This protects against inadvertent writes during power-up or brownout conditions.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Maximum accumulated storage time	
At 150 °C ambient temperature .....	1000 h
At 85 °C ambient temperature .....	20 Years
Maximum junction temperature .....	150 °C
Supply voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	
CY14B116X: .....	-0.5 V to +4.1 V
CY14E116X: .....	-0.5 V to +7.0 V
Voltage applied to outputs in high-Z state .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Input voltage .....	-0.5 V to V <sub>CC</sub> + 0.5 V

Transient voltage (<20 ns) on any pin to ground potential .....	-2.0 V to V <sub>CC</sub> + 2.0 V
Package power dissipation capability (T <sub>A</sub> = 25 °C) .....	1.0 W
Surface mount lead soldering temperature (3 Seconds) .....	+260 °C
DC output current (1 output at a time, 1s duration) .....	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch-up current .....	> 140 mA

## Operating Range

Product	Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
CY14B116X	Industrial	-40 °C to +85 °C	2.7 V to 3.6 V
CY14E116X			4.5 V to 5.5 V

## DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[14]</sup>	Max	Unit	
V <sub>CC</sub>	Power supply		CY14B116X	2.7	3.0	3.6	V
			CY14E116X	4.5	5.0	5.5	V
I <sub>CC1</sub>	Average V <sub>CC</sub> current	Values obtained without output loads (I <sub>OUT</sub> = 0 mA)	t <sub>RC</sub> = 25/30 ns	-	-	95	mA
			t <sub>RC</sub> = 45 ns	-	-	75	mA
I <sub>CC2</sub>	Average V <sub>CC</sub> current during STORE	All inputs don't care, V <sub>CC</sub> = V <sub>CC</sub> (max). Average current for duration t <sub>STORE</sub>	-	-	10	mA	
I <sub>CC3</sub>	Average V <sub>CC</sub> current at t <sub>RC</sub> = 200 ns, V <sub>CC</sub> (Typ), 25 °C	All inputs cycling at CMOS Levels. Values obtained without output loads (I <sub>OUT</sub> = 0 mA).	-	50	-	mA	
I <sub>CC4</sub> <sup>[15]</sup>	Average V <sub>CAP</sub> current during AutoStore cycle	All inputs don't care. Average current for duration t <sub>STORE</sub>	-	-	6	mA	
I <sub>SB</sub>	V <sub>CC</sub> standby current	CE ≥ (V <sub>CC</sub> - 0.2 V). V <sub>IN</sub> ≤ 0.2 V or ≥ (V <sub>CC</sub> - 0.2 V). 'Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	t <sub>RC</sub> = 25/30 ns	-	-	650	μA
			t <sub>RC</sub> = 45 ns	-	-	500	μA
I <sub>ZZ</sub>	Sleep mode current	All inputs are static at CMOS Level	-	-	10	μA	
I <sub>Ix</sub> <sup>[16]</sup>	Input leakage current (except HSB)	V <sub>CC</sub> = V <sub>CC</sub> (max), V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA	
	Input leakage current (for HSB)	V <sub>CC</sub> = V <sub>CC</sub> (max), V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-100	-	+1	μA	

### Notes

14. Typical values are at 25 °C, V<sub>CC</sub> = V<sub>CC</sub>(Typ). Not 100% tested.

15. This parameter is only guaranteed by design and is not tested.

16. The HSB pin has I<sub>OUT</sub> = -2 uA for V<sub>OH</sub> of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V<sub>OH</sub> and V<sub>OL</sub> are valid. This parameter is characterized but not tested.

## DC Electrical Characteristics (continued)

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[14]</sup>	Max	Unit
I <sub>OZ</sub>	Off state output leakage current	$V_{CC} = V_{CC}(\text{Max}), V_{SS} \leq V_{OUT} \leq V_{CC}, \overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BLE}, \overline{BHE}/\overline{B_A}, \overline{B_B}, \overline{B_C}, \overline{B_D} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	-1	-	+1	μA
V <sub>IH</sub>	Input HIGH voltage		2.0	-	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage		V <sub>SS</sub> - 0.5	-	0.8	V
V <sub>OH</sub>	Output HIGH voltage	I <sub>OUT</sub> = -2 mA	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OUT</sub> = 4 mA	-	-	0.4	V
V <sub>CAP</sub> <sup>[17]</sup>	Storage capacitor	Between V <sub>CAP</sub> pin and V <sub>SS</sub>	19.8	22.0	82.0	μF
V <sub>V<sub>CAP</sub></sub> <sup>[18, 19]</sup>	Maximum voltage driven on V <sub>CAP</sub> pin by the device	V <sub>CC</sub> = V <sub>CC</sub> (max)	-	-	5.0	V

## Data Retention and Endurance

Over the [Operating Range](#)

Parameter	Description	Min	Unit
DATA <sub>R</sub>	Data retention	20	Years
NV <sub>C</sub>	Nonvolatile STORE operations	1,000,000	Cycles

## Capacitance

In the following table, the capacitance parameters are listed.<sup>[19]</sup>

Parameter	Description	Test Conditions	Max (All packages except 60-FBGA and 165-FBGA)	Max (60-FBGA package and 165-FBGA package)	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (Typ)	8	10	pF
C <sub>IO</sub>	Input/Output capacitance		8	10	pF
C <sub>OUT</sub>	Output capacitance		8	10	pF

## Thermal Resistance

In the following table, the thermal resistance parameters are listed.<sup>[19]</sup>

Parameter	Description	Test Conditions	44-TSOP II	48-TSOP I	54-TSOP II	60-FBGA	165-FBGA	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	44.6	35.6	41.1	21	15.6	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		2.4	2.33	4.6	3	2.9	°C/W

### Notes

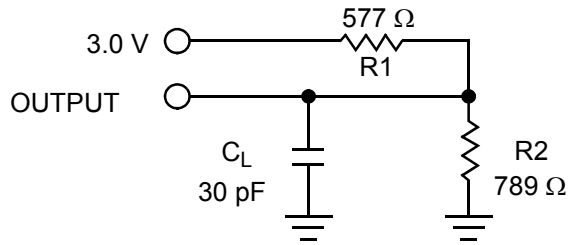
17. Min V<sub>CAP</sub> value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V<sub>CAP</sub> value guarantees that the capacitor on V<sub>CAP</sub> is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits.

18. Maximum voltage on V<sub>CAP</sub> pin (V<sub>V<sub>CAP</sub></sub>) is provided for guidance when choosing the V<sub>CAP</sub> capacitor. The voltage rating of the V<sub>CAP</sub> capacitor across the operating temperature range should be higher than the V<sub>V<sub>CAP</sub></sub> voltage

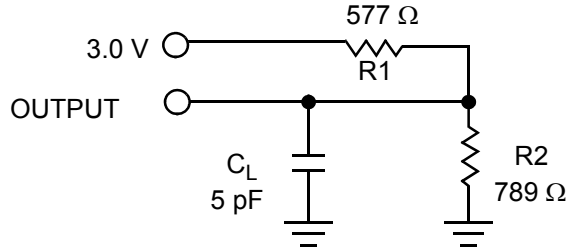
19. These parameters are only guaranteed by design and are not tested.

**Figure 10. AC Test Loads and Waveforms**

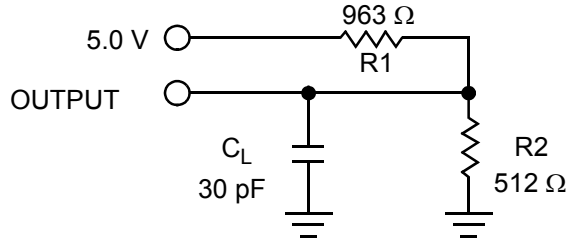
For 3 V (CY14B116X):



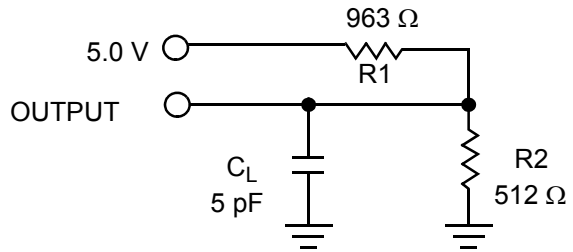
For Tristate specs



For 5 V (CY14E116X):



For Tristate specs



**AC Test Conditions**

	<b>CY14B116X</b>	<b>CY14E116X</b>
Input pulse levels	0 V to 3 V	0 V to 3 V
Input rise and fall times (10%–90%)	≤3 ns	≤3 ns
Input and output timing reference levels	1.5 V	1.5 V

## AC Switching Characteristics

Over the [Operating Range](#)<sup>[20]</sup>

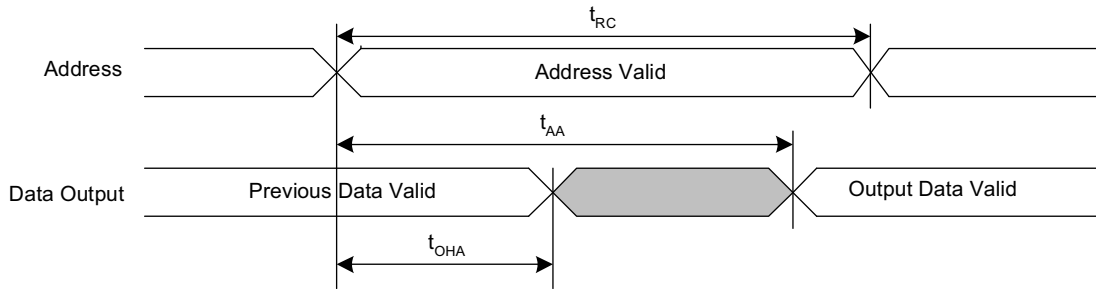
Parameters		Description	25 ns		30 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	Min	Max	
<b>SRAM Read Cycle</b>									
t <sub>ACE</sub>	t <sub>ACS</sub>	Chip enable access time	–	25	–	30	–	45	ns
t <sub>RC</sub> <sup>[22]</sup>	t <sub>RC</sub>	Read cycle time	25	–	30	–	45	–	ns
t <sub>AA</sub> <sup>[23]</sup>	t <sub>AA</sub>	Address access time	–	25	–	30	–	45	ns
t <sub>DOE</sub>	t <sub>OE</sub>	Output enable to data valid	–	12	–	14	–	20	ns
t <sub>OHA</sub> <sup>[23]</sup>	t <sub>OH</sub>	Output hold after address change	3	–	3	–	3	–	ns
t <sub>LZCE</sub> <sup>[24]</sup>	t <sub>LZ</sub>	Chip enable to output active	3	–	3	–	3	–	ns
t <sub>HZCE</sub> <sup>[21, 24]</sup>	t <sub>HZ</sub>	Chip disable to output inactive	–	10	–	12	–	15	ns
t <sub>LZOE</sub> <sup>[24]</sup>	t <sub>OLZ</sub>	Output enable to output active	0	–	0	–	0	–	ns
t <sub>HZOE</sub> <sup>[21, 24]</sup>	t <sub>OHZ</sub>	Output disable to output inactive	–	10	–	12	–	15	ns
t <sub>PU</sub> <sup>[24]</sup>	t <sub>PA</sub>	Chip enable to power active	0	–	0	–	0	–	ns
t <sub>PD</sub> <sup>[24]</sup>	t <sub>PS</sub>	Chip disable to power standby	–	25	–	30	–	45	ns
t <sub>DBE</sub>		Byte enable to data valid	–	12	–	14	–	20	ns
t <sub>LZBE</sub> <sup>[24]</sup>		Byte enable to output active	0	–	0	–	0	–	ns
t <sub>HZBE</sub> <sup>[21, 24]</sup>		Byte disable to output inactive	–	10	–	12	–	15	ns
<b>SRAM Write Cycle</b>									
t <sub>WC</sub>	t <sub>WC</sub>	Write cycle time	25	–	30	–	45	–	ns
t <sub>PWE</sub>	t <sub>WP</sub>	Write pulse width	20	–	24	–	30	–	ns
t <sub>SCE</sub>	t <sub>CW</sub>	Chip enable to end of write	20	–	24	–	30	–	ns
t <sub>SD</sub>	t <sub>DW</sub>	Data setup to end of write	10	–	14	–	15	–	ns
t <sub>HD</sub>	t <sub>DH</sub>	Data hold after end of write	0	–	0	–	0	–	ns
t <sub>AW</sub>	t <sub>AW</sub>	Address setup to end of write	20	–	24	–	30	–	ns
t <sub>SA</sub>	t <sub>AS</sub>	Address setup to start of write	0	–	0	–	0	–	ns
t <sub>HA</sub>	t <sub>WR</sub>	Address hold after end of write	0	–	0	–	0	–	ns
t <sub>HZWE</sub> <sup>[21, 24, 25]</sup>	t <sub>WZ</sub>	Write enable to output disable	–	10	–	12	–	15	ns
t <sub>LZWE</sub> <sup>[24]</sup>	t <sub>OW</sub>	Output active after end of write	3	–	3	–	3	–	ns
t <sub>BW</sub>		Byte enable to end of write	20	–	24	–	30	–	ns

### Notes

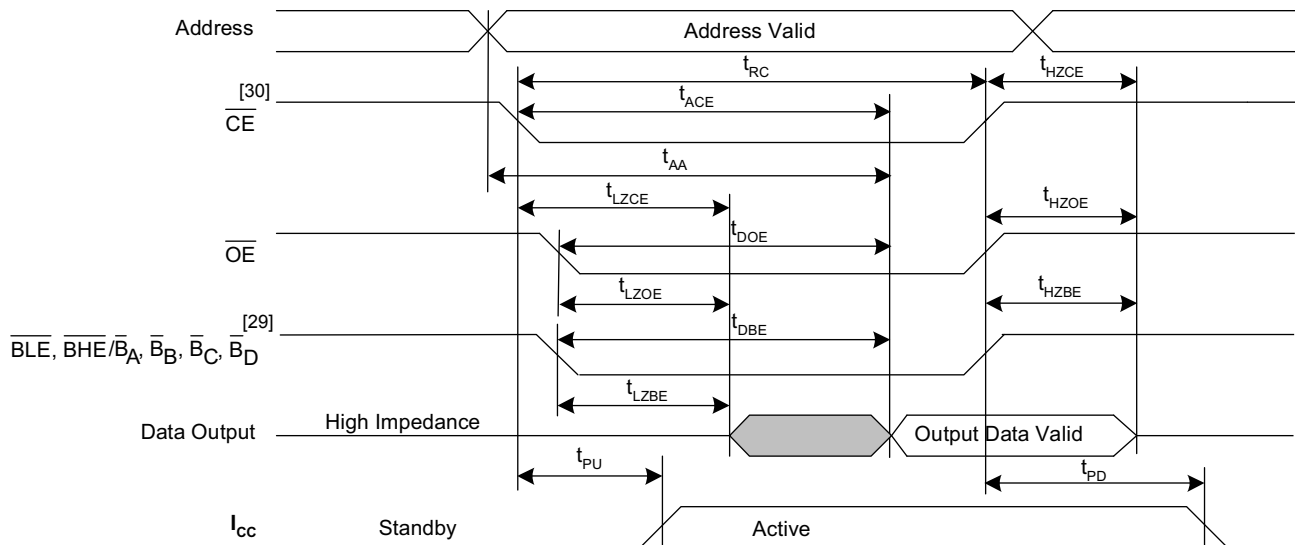
20. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of V<sub>CC</sub>/2, input pulse levels of 0 to V<sub>CC</sub>(Typ), and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance as shown in [Figure 10](#).
21. t<sub>HZCE</sub>, t<sub>HZOE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF. Transition is measured ±200 mV from the steady state output voltage.
22. WE must be HIGH during SRAM read cycles.
23. Device is continuously selected with CE, OE and BLE, BHE/B<sub>A</sub>, B<sub>B</sub>, B<sub>C</sub>, B<sub>D</sub> LOW.
24. These parameters are only guaranteed by design and are not tested.
25. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.



**Figure 11. SRAM Read Cycle 1: Address Controlled**<sup>[26, 27, 28]</sup>



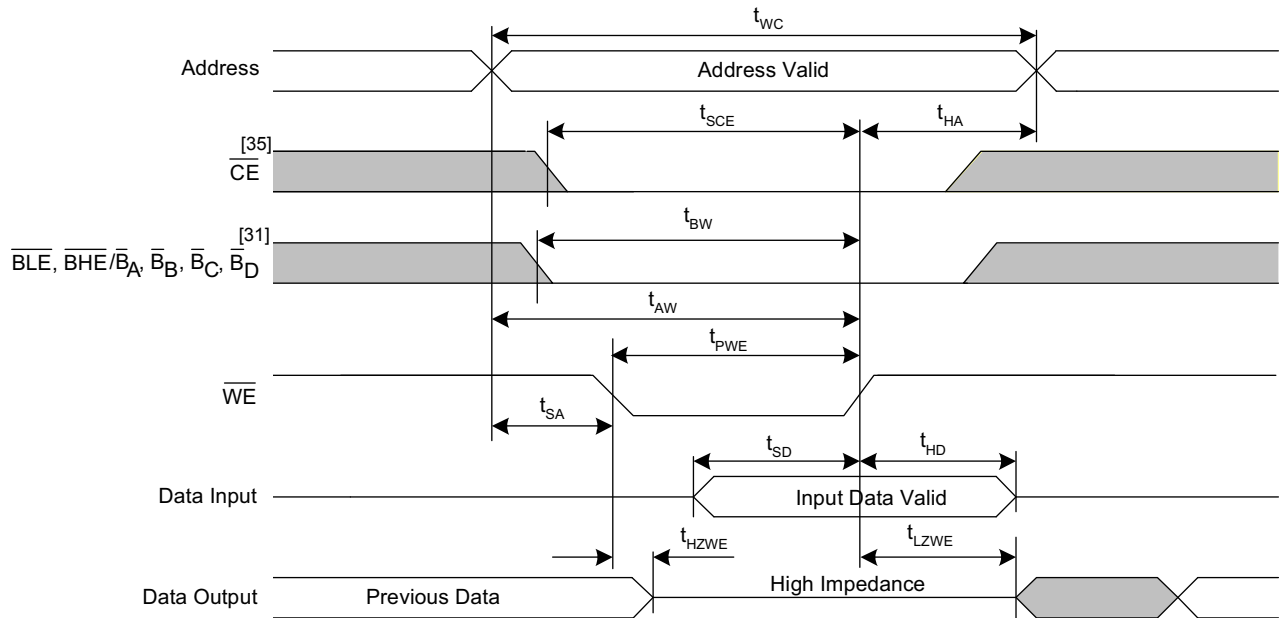
**Figure 12. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled**<sup>[26, 28]</sup>



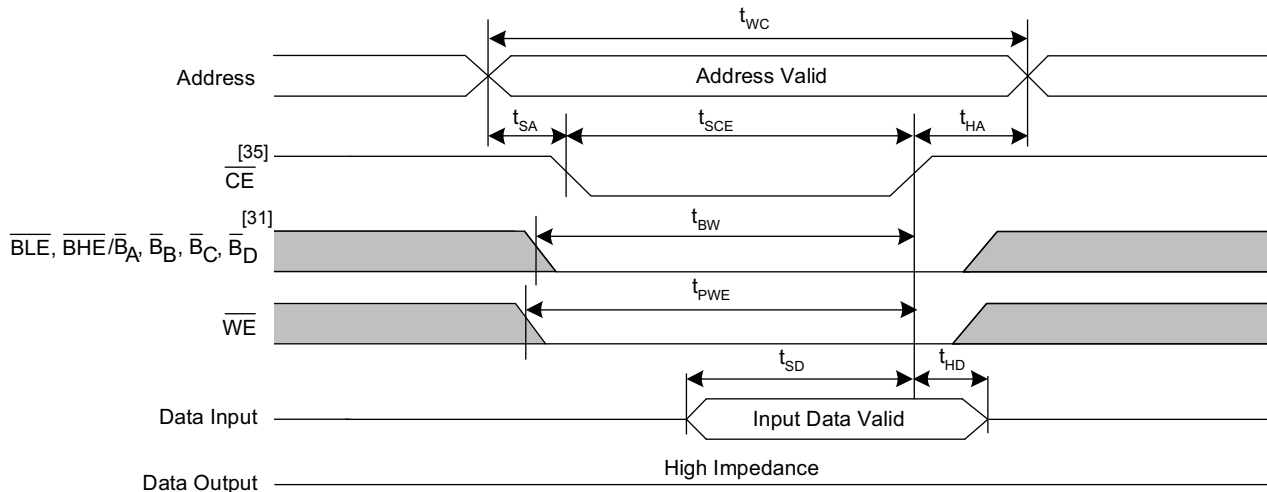
**Notes**

26.  $\overline{WE}$  must be HIGH during SRAM read cycles.
27. Device is continuously selected with  $\overline{CE}$ ,  $\overline{OE}$  and  $\overline{BLE}$ ,  $\overline{BHE}/\overline{B_A}$ ,  $\overline{B_B}$ ,  $\overline{B_C}$ ,  $\overline{B_D}$  LOW.
28.  $\overline{HSB}$  must remain HIGH during Read and Write cycles.
29.  $\overline{BLE}$ ,  $\overline{BHE}$  are applicable for the  $\times 16$  configuration and  $\overline{B_A}$ ,  $\overline{B_B}$ ,  $\overline{B_C}$ ,  $\overline{B_D}$  are applicable for the  $\times 32$  configuration only.
30. TSOP II package is offered in single  $\overline{CE}$  and BGA package is offered in dual  $\overline{CE}$  options. In this datasheet, for a dual  $\overline{CE}$  device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{CE}$  for the single chip enable device;  $\overline{CE}_1$  and  $\overline{CE}_2$  for the dual chip enable device).

**Figure 13. SRAM Write Cycle 1:  $\overline{\text{WE}}$  Controlled**<sup>[32, 34, 36]</sup>



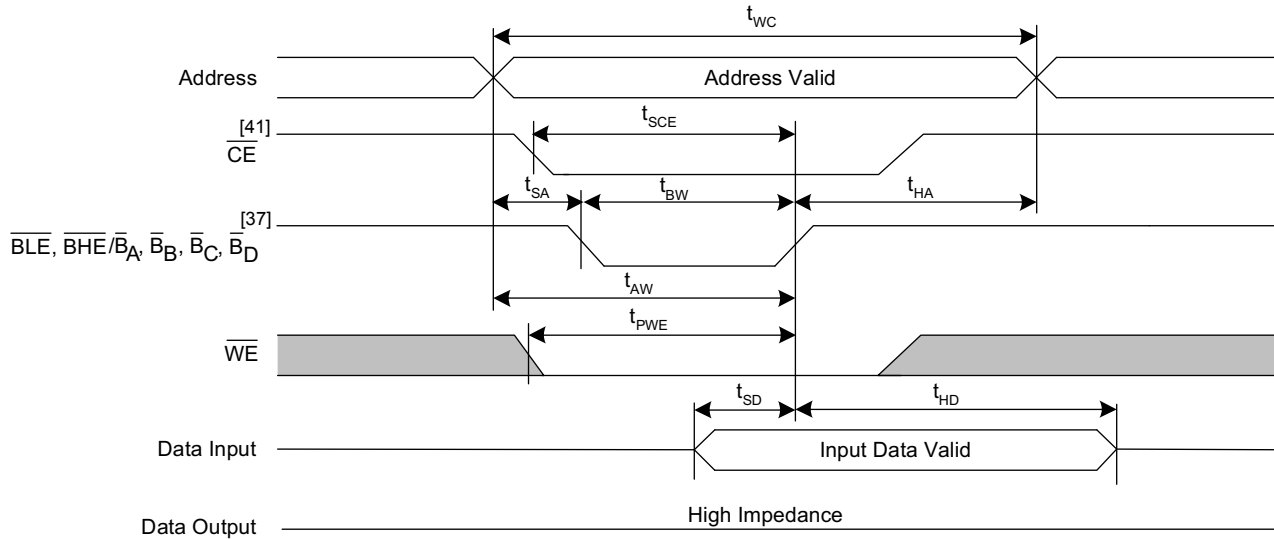
**Figure 14. SRAM Write Cycle 2:  $\overline{\text{CE}}$  Controlled**<sup>[32, 34, 36]</sup>



**Notes**

31.  $\overline{\text{BLE}}$ ,  $\overline{\text{BHE}}$  are applicable for the  $\times 16$  configuration and  $\overline{\text{B}}_A$ ,  $\overline{\text{B}}_B$ ,  $\overline{\text{B}}_C$ ,  $\overline{\text{B}}_D$  are applicable for the  $\times 32$  configuration only.
32. If  $\overline{\text{WE}}$  is LOW when  $\overline{\text{CE}}$  goes LOW, the outputs remain in the high impedance state.
33.  $\overline{\text{WE}}$  must be HIGH during SRAM read cycles.
34. HSB must remain HIGH during Read and Write cycles.
35. TSOP II package is offered in single  $\overline{\text{CE}}$ . TSOP I and BGA packages are offered in dual  $\overline{\text{CE}}$  options. In this datasheet, for a dual  $\overline{\text{CE}}$  device,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{\text{CE}}$  for the single chip enable device;  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  for the dual chip enable device).
36.  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  must be  $\geq V_{IH}$  during address transitions.

Figure 15. SRAM Write Cycle 3:  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ / $\overline{\text{B}}_{\text{A}}$ ,  $\overline{\text{B}}_{\text{B}}$ ,  $\overline{\text{B}}_{\text{C}}$ ,  $\overline{\text{B}}_{\text{D}}$  Controlled<sup>[38, 39, 40]</sup>



**Notes**

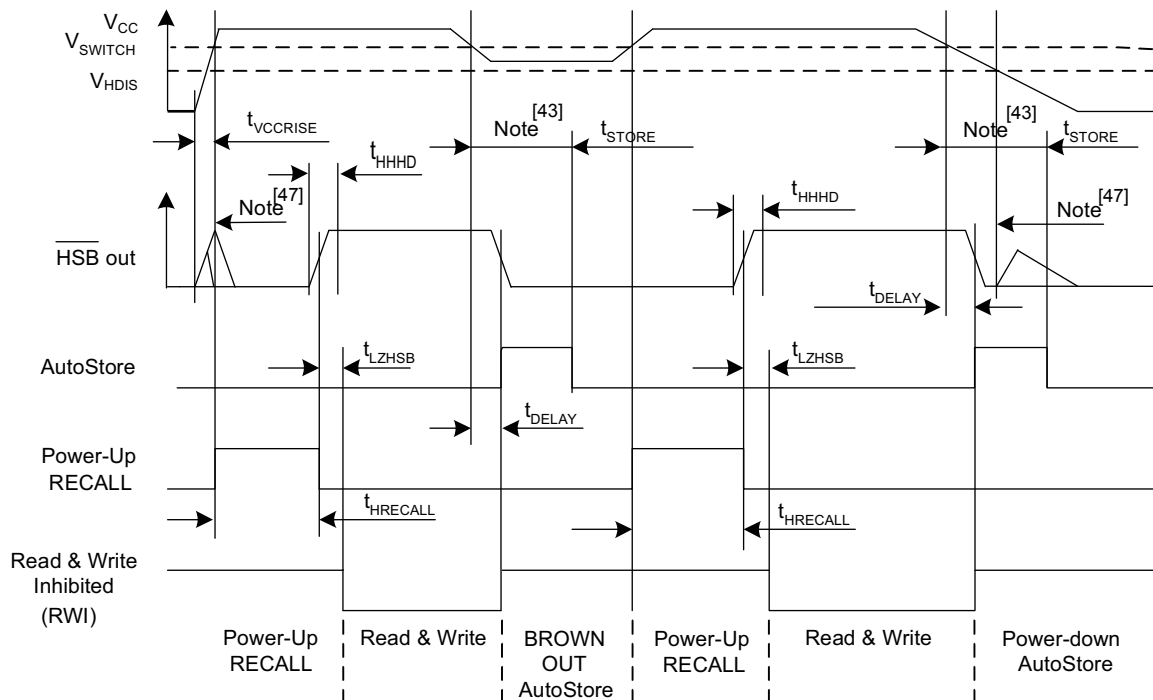
- 37.  $\overline{\text{BLE}}$ ,  $\overline{\text{BHE}}$  are applicable for the  $\times 16$  configuration and  $\overline{\text{B}}_{\text{A}}$ ,  $\overline{\text{B}}_{\text{B}}$ ,  $\overline{\text{B}}_{\text{C}}$ ,  $\overline{\text{B}}_{\text{D}}$  are applicable for the  $\times 32$  configuration only.
- 38. If  $\overline{\text{WE}}$  is LOW when  $\overline{\text{CE}}$  goes LOW, the outputs remain in the high impedance state.
- 39.  $\overline{\text{HSB}}$  must remain HIGH during Read and Write cycles.
- 40.  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  must be  $\geq V_{\text{IH}}$  during address transitions.
- 41. TSOP II package is offered in single  $\overline{\text{CE}}$ . TSOP I and BGA packages are offered in dual  $\overline{\text{CE}}$  options. In this datasheet, for a dual  $\overline{\text{CE}}$  device,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{\text{CE}}$  for the single chip enable device;  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$  for the dual chip enable device).

## AutoStore/Power-Up RECALL Characteristics

Over the [Operating Range](#)

Parameter	Description	Min	Max	Unit	
$t_{HRECALL}$ [42]	Power-Up RECALL duration	–	30	ms	
$t_{STORE}$ [43]	STORE cycle duration	–	8	ms	
$t_{DELAY}$ [44, 45]	Time allowed to complete SRAM write cycle	–	25	ns	
$V_{SWITCH}$	Low-voltage trigger level	CY14B116X	–	2.65	V
		CY14E116X	–	4.40	V
$t_{VCCRRISE}$ [45]	$V_{CC}$ rise time	150	–	$\mu$ S	
$V_{HDIS}$ [45]	$\overline{HSB}$ output disable voltage	–	1.9	V	
$t_{LZHSB}$ [45]	$\overline{HSB}$ to output active time	–	5	$\mu$ S	
$t_{HHHD}$ [45]	$\overline{HSB}$ HIGH active time	–	500	ns	

Figure 16. AutoStore or Power-Up RECALL [46]



### Notes

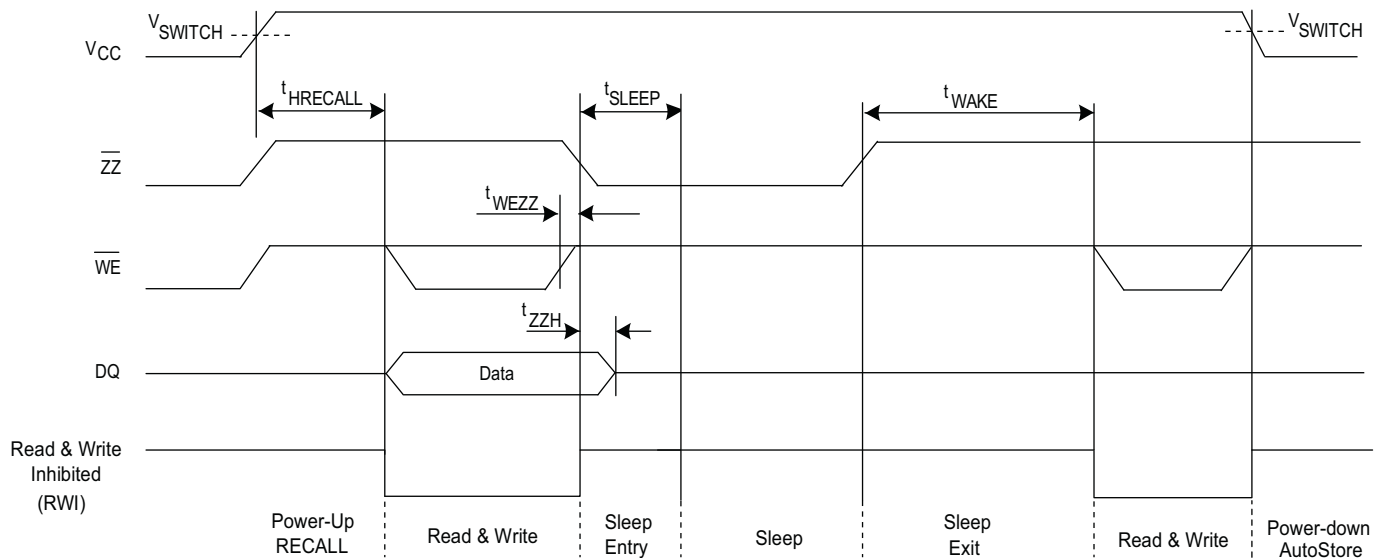
42.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
43. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
44. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time  $t_{DELAY}$ .
45. These parameters are only guaranteed by design and are not tested.
46. Read and Write cycles are ignored during STORE, RECALL, and while  $V_{CC}$  is below  $V_{SWITCH}$ .
47. During power-up and power-down,  $\overline{HSB}$  glitches when  $\overline{HSB}$  pin is pulled up through an external resistor.

## Sleep Mode Characteristics

Over the [Operating Range](#)

Parameter	Description	Min	Max	Unit
$t_{WAKE}$	Sleep mode exit time ( $\overline{ZZ}$ HIGH to first access after wakeup)	–	30	ms
$t_{SLEEP}$	Sleep mode enter time ( $\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	8	ms
$t_{ZZL}$	$\overline{ZZ}$ active LOW time	50	–	ns
$t_{WEZZ}$	Last write to sleep mode entry time	0	–	$\mu$ s
$t_{ZZH}$	$\overline{ZZ}$ active to DQ Hi-Z time	–	70	ns

Figure 17. Sleep Mode<sup>[48]</sup>



**Note**

48. Device initiates sleep routine and enters into Sleep mode after  $t_{SLEEP}$  duration.

## Software Controlled STORE and RECALL Characteristics

Over the [Operating Range](#)<sup>[49, 50]</sup>

Parameter	Description	25 ns		30 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{RC}$	STORE/RECALL initiation cycle time	25	–	30	–	45	–	ns
$t_{SA}$	Address setup time	0	–	0	–	0	–	ns
$t_{CW}$	Clock pulse width	20	–	24	–	30	–	ns
$t_{HA}$	Address hold time	0	–	0	–	0	–	ns
$t_{RECALL}$	RECALL duration	–	600	–	600	–	600	$\mu$ s
$t_{SS}$ [51, 52]	Soft sequence processing time	–	500	–	500	–	500	$\mu$ s

Figure 18.  $\overline{CE}$  and  $\overline{OE}$  Controlled Software STORE and RECALL Cycle<sup>[50]</sup>

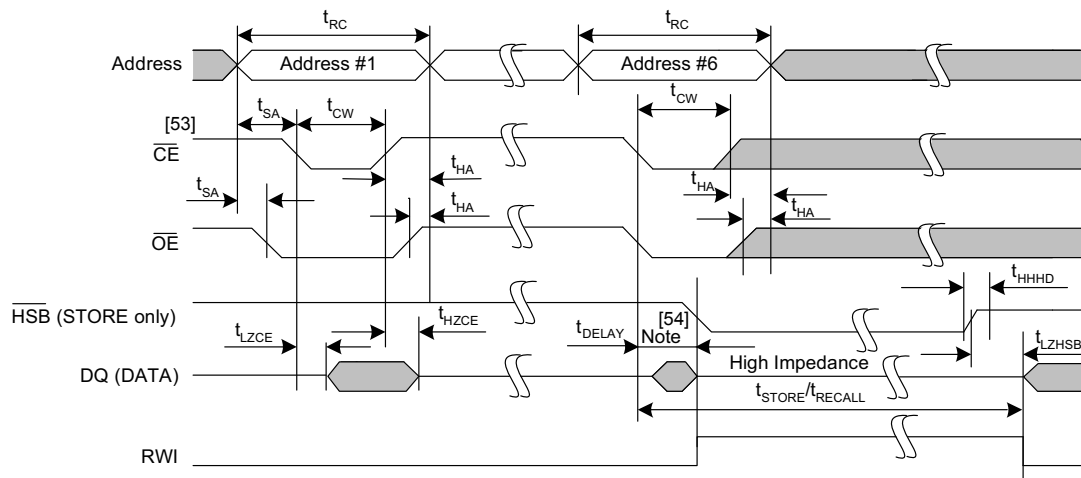
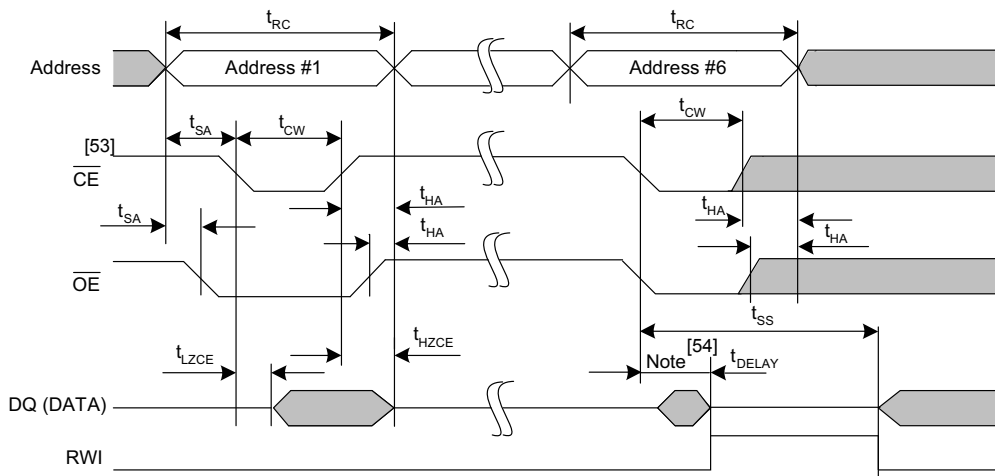


Figure 19. AutoStore Enable and Disable Cycle



### Notes

49. The software sequence is clocked with  $\overline{CE}$  controlled or  $\overline{OE}$  controlled reads.

50. The six consecutive addresses must be read in the order listed in [Table 1](#).  $\overline{WE}$  must be HIGH during all six consecutive cycles.

51. This is the amount of time it takes to take action on a soft sequence command.  $V_{CC}$  power must remain high to effectively register command.

52. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

53. TSOP II package is offered in single  $\overline{CE}$ . TSOP I and BGA packages are offered in dual  $\overline{CE}$  options. In this datasheet, for a dual  $\overline{CE}$  device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{CE}$  for the single chip enable device;  $\overline{CE}_1$  and  $\overline{CE}_2$  for the dual chip enable device).

54. DQ output data at the sixth read may be invalid since the output is disabled at  $t_{DELAY}$  time.

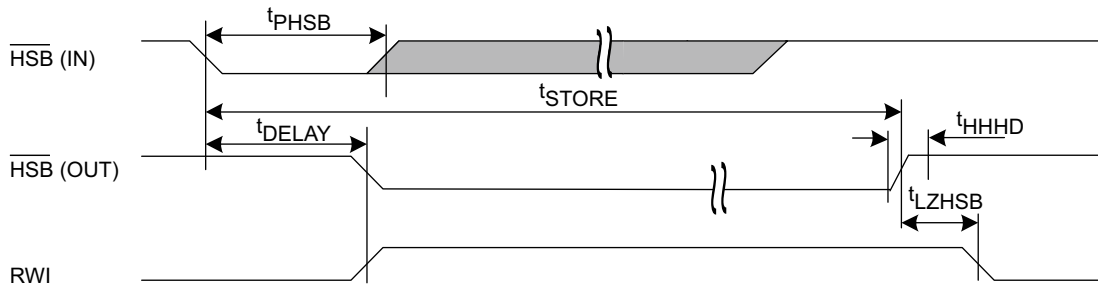
## Hardware STORE Characteristics

Over the [Operating Range](#)

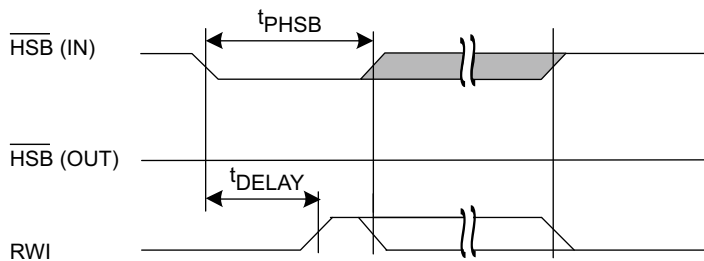
Parameter	Description	Min	Max	Unit
$t_{DHSB}$	HSB to output active time when write latch not set	–	25	ns
$t_{PHSB}$	Hardware STORE pulse width	15	–	ns

Figure 20. Hardware STORE Cycle<sup>[55]</sup>

### Write Latch set

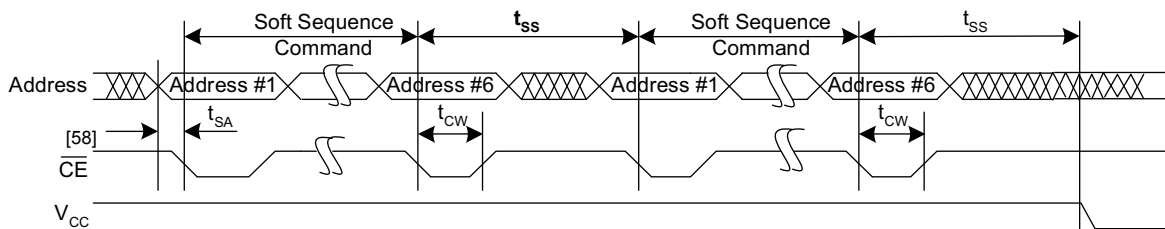


### Write Latch not set



HSB pin is driven HIGH to  $V_{CC}$  only by internal 100 K $\Omega$  resistor, HSB driver is disabled  
SRAM is disabled as long as HSB (IN) is driven LOW.

Figure 21. Soft Sequence Processing<sup>[56, 57]</sup>



### Notes

55. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
56. This is the amount of time it takes to take action on a soft sequence command.  $V_{CC}$  power must remain high to effectively register command.
57. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
58. TSOP II package is offered in single  $\overline{CE}$ . TSOP I and BGA packages are offered in dual  $\overline{CE}$  options. In this datasheet, for a dual  $\overline{CE}$  device,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$  such that when  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ( $\overline{CE}$  for the single chip enable device;  $\overline{CE}_1$  and  $\overline{CE}_2$  for the dual chip enable device).

### Truth Table For SRAM Operations

HSB should remain HIGH for SRAM Operations.

#### For ×8 Configuration

Single chip enable option (44-pin TSOP II package)

CE	WE	OE	Inputs and Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ <sub>0</sub> –DQ <sub>7</sub> )	Read	Active
L	H	H	High-Z	Output disabled	Active
L	L	X	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> )	Write	Active

#### For ×8 Configuration

Dual chip enable option (48-pin TSOP I package)

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Inputs and Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	High-Z	Deselect/Power-down	Standby
L	H	H	L	Data out (DQ <sub>0</sub> –DQ <sub>7</sub> )	Read	Active
L	H	H	H	High-Z	Output disabled	Active
L	H	L	X	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> )	Write	Active

#### For ×16 Configuration

Single chip enable option (54-pin TSOP II package)

CE	WE	OE	BLE	BHE	Inputs and Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	X	X	H	H	High-Z	Output disabled	Active
L	H	L	L	L	Data out (DQ <sub>0</sub> –DQ <sub>15</sub> )	Read	Active
L	H	L	L	H	Data out (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Read	Active
L	H	L	H	L	Data out (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Read	Active
L	H	H	X	X	High-Z	Output disabled	Active
L	L	X	L	L	Data in (DQ <sub>0</sub> –DQ <sub>15</sub> )	Write	Active
L	L	X	L	H	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Write	Active
L	L	X	H	L	Data in (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Write	Active



**For ×16 Configuration**

Dual chip enable option (48-pin TSOP I package and 165-ball FBGA package)

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	H	X	X	H	H	High-Z	Output disabled	Active
L	H	H	L	L	L	Data out (DQ <sub>0</sub> –DQ <sub>15</sub> )	Read	Active
L	H	H	L	L	H	Data out (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Read	Active
L	H	H	L	H	L	Data out (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Read	Active
L	H	H	H	X	X	High-Z	Output disabled	Active
L	H	L	X	L	L	Data in (DQ <sub>0</sub> –DQ <sub>15</sub> )	Write	Active
L	H	L	X	L	H	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Write	Active
L	H	L	X	H	L	Data in (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Write	Active

**For ×32 Configuration**

Dual chip enable option (165-ball FBGA package)

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	DQ <sub>0</sub> –DQ <sub>7</sub>	DQ <sub>8</sub> –DQ <sub>15</sub>	DQ <sub>16</sub> –DQ <sub>23</sub>	DQ <sub>24</sub> –DQ <sub>31</sub>	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	deselect/ Power down	Standby
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	deselect/ Power down	Standby
L	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected	Active
L	H	H	L	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	Active
L	H	H	L	L	H	H	H	Data out	High-Z	High-Z	High-Z	Read	Active
L	H	H	L	H	L	H	H	High-Z	Data out	High-Z	High-Z	Read	Active
L	H	H	L	H	H	L	H	High-Z	High-Z	Data out	High-Z	Read	Active
L	H	H	L	H	H	H	L	High-Z	High-Z	High-Z	Data out	Read	Active
L	H	L	X	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	Active
L	H	L	X	L	H	H	H	Data in	High-Z	High-Z	High-Z	Write	Active
L	H	L	X	H	L	H	H	High-Z	Data in	High-Z	High-Z	Write	Active
L	H	L	X	H	H	L	H	High-Z	High-Z	Data in	High-Z	Write	Active
L	H	L	X	H	H	H	L	High-Z	High-Z	High-Z	Data in	Write	Active
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Output disabled	Active

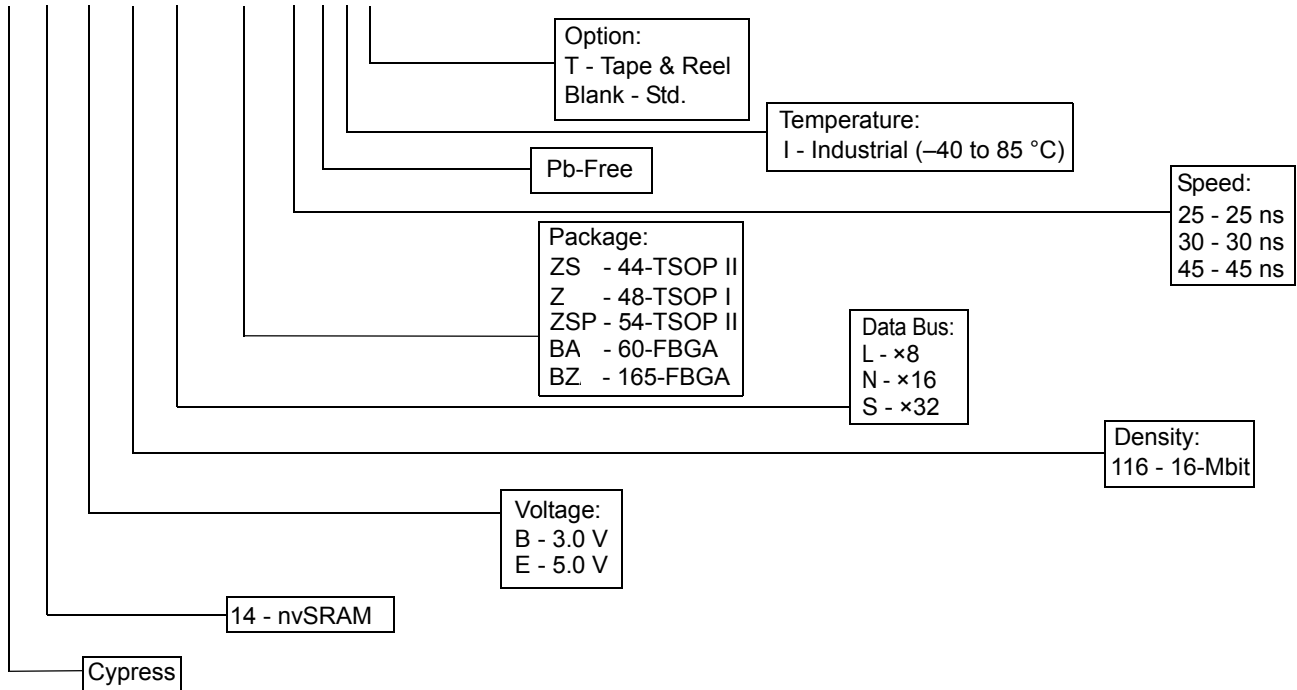
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B116L-ZS25XI	51-85087	44-pin TSOP II	Industrial
	CY14B116L-ZS25XIT	51-85087	44-pin TSOP II	
	CY14E116L-ZS25XI	51-85087	44-pin TSOP II	
	CY14E116L-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B116N-ZSP25XI	51-85160	54-pin TSOP II	
	CY14E116N-ZSP25XI	51-85160	54-pin TSOP II	
	CY14B116N-BA25XI	002-00193	60-ball FBGA	
	CY14B116N-BA25XIT	002-00193	60-ball FBGA	
	CY14B116N-BZ25XI	51-85195	165-ball FBGA	
	CY14B116N-BZ25XIT	51-85195	165-ball FBGA	
	CY14B116S-BZ25XI	51-85195	165-ball FBGA	
	CY14B116S-BZ25XIT	51-85195	165-ball FBGA	
	CY14E116S-BZ25XI	51-85195	165-ball FBGA	
	CY14E116S-BZ25XIT	51-85195	165-ball FBGA	
30	CY14B116L-Z30XI	51-85183	48-pin TSOP I	
	CY14B116L-Z30XIT	51-85183	48-pin TSOP I	
	CY14E116L-Z30XI	51-85183	48-pin TSOP I	
	CY14E116L-Z30XIT	51-85183	48-pin TSOP I	
	CY14B116N-Z30XI	51-85183	48-pin TSOP I	
	CY14B116N-Z30XIT	51-85183	48-pin TSOP I	
	CY14E116N-Z30XI	51-85183	48-pin TSOP I	
	CY14E116N-Z30XIT	51-85183	48-pin TSOP I	
45	CY14B116L-ZS45XI	51-85087	44-pin TSOP II	
	CY14B116L-ZS45XIT	51-85087	44-pin TSOP II	
	CY14E116L-ZS45XI	51-85087	44-pin TSOP II	
	CY14E116L-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B116L-Z45XI	51-85183	48-pin TSOP I	
	CY14B116L-Z45XIT	51-85183	48-pin TSOP I	
	CY14E116L-Z45XI	51-85183	48-pin TSOP I	
	CY14E116L-Z45XIT	51-85183	48-pin TSOP I	
	CY14B116N-Z45XI	51-85183	48-pin TSOP I	
	CY14B116N-Z45XIT	51-85183	48-pin TSOP I	
	CY14B116N-ZSP45XI	51-85160	54-pin TSOP II	
	CY14B116N-ZSP45XIT	51-85160	54-pin TSOP II	
	CY14E116N-Z45XI	51-85183	48-pin TSOP I	
	CY14E116N-Z45XIT	51-85183	48-pin TSOP I	
	CY14B116N-BZ45XI	51-85195	165-ball FBGA	
	CY14B116N-BZ45XIT	51-85195	165-ball FBGA	
CY14B116S-BZ45XI	51-85195	165-ball FBGA		
CY14B116S-BZ45XIT	51-85195	165-ball FBGA		

All parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

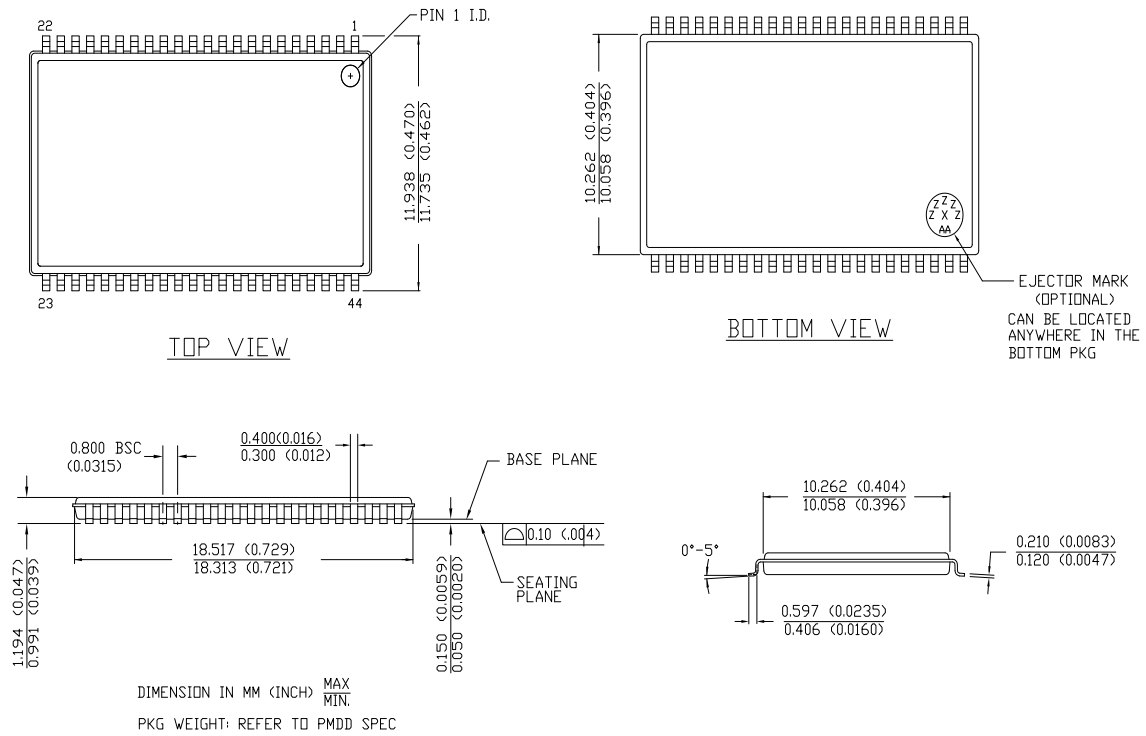
**Ordering Code Definitions**

**CY14 B 116 L - ZS 25 X I T**



Package Diagrams

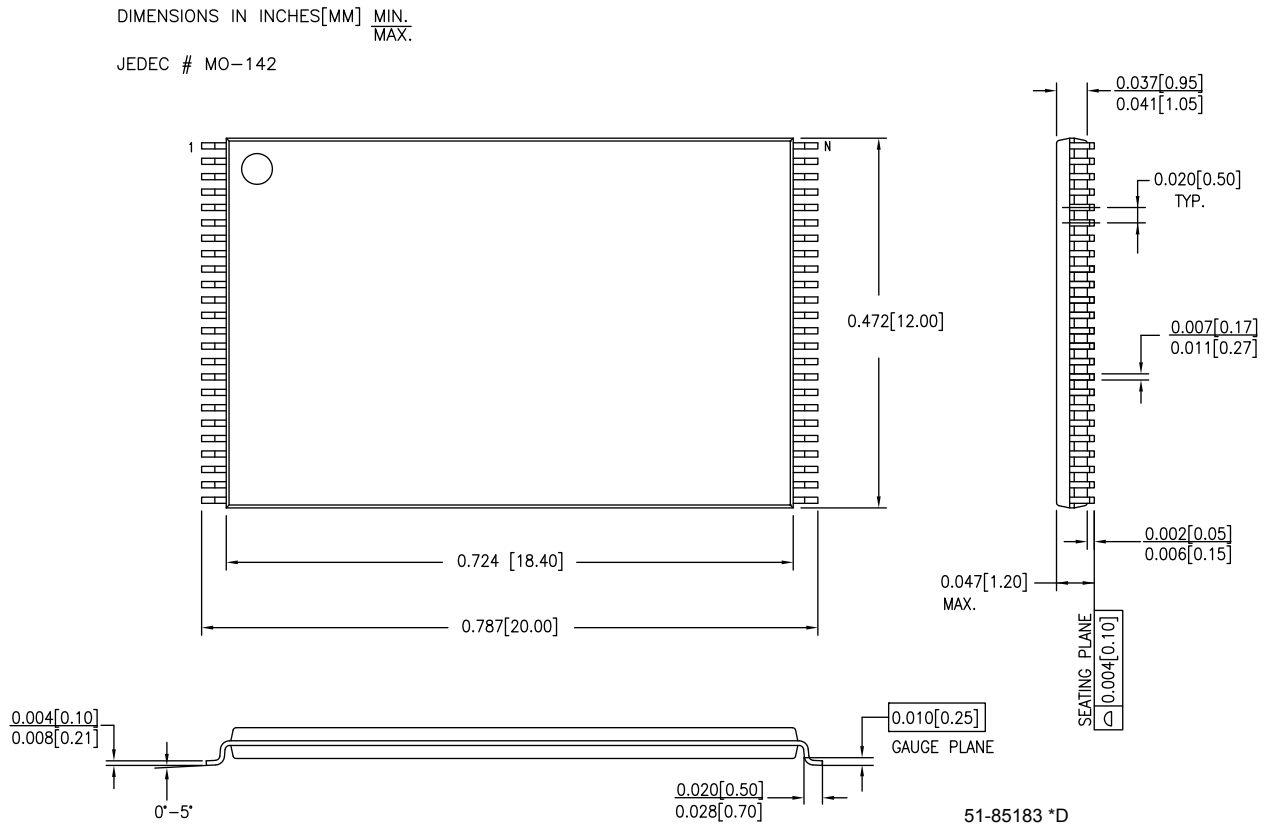
Figure 22. 44-pin TSOP II Package Outline, 51-85087



51-85087 \*E

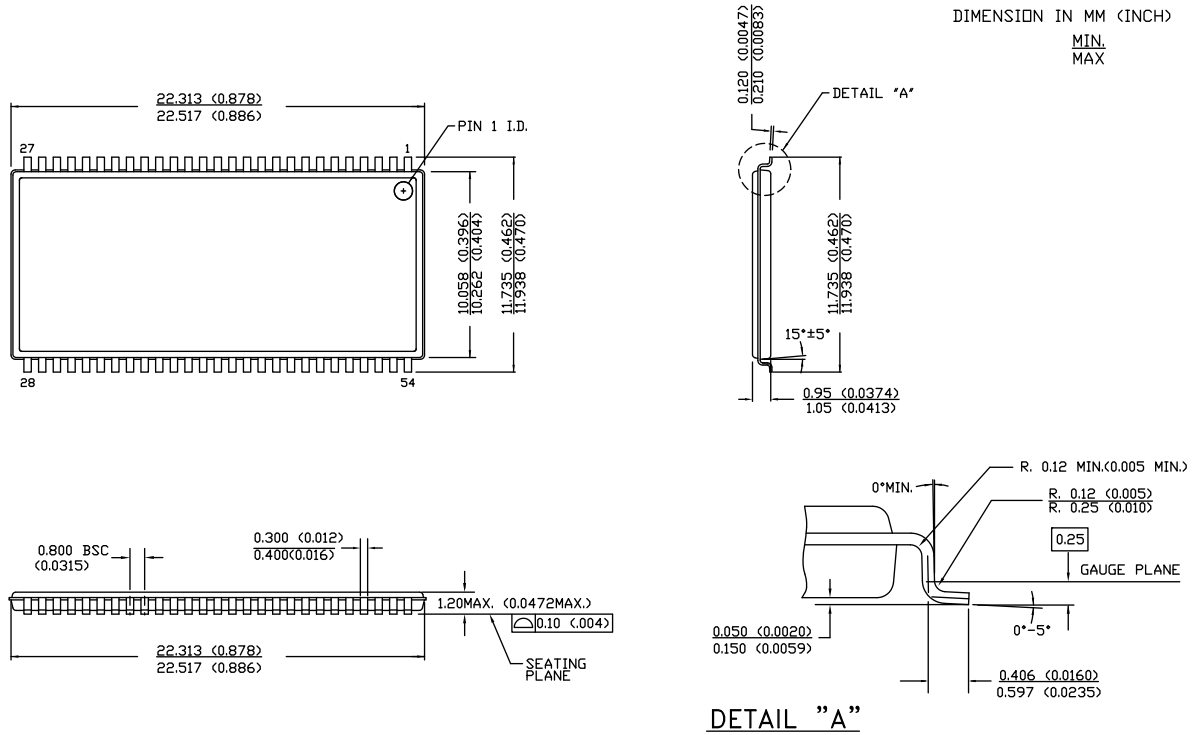
**Package Diagrams** (continued)

**Figure 23. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183**



**Package Diagrams** (continued)

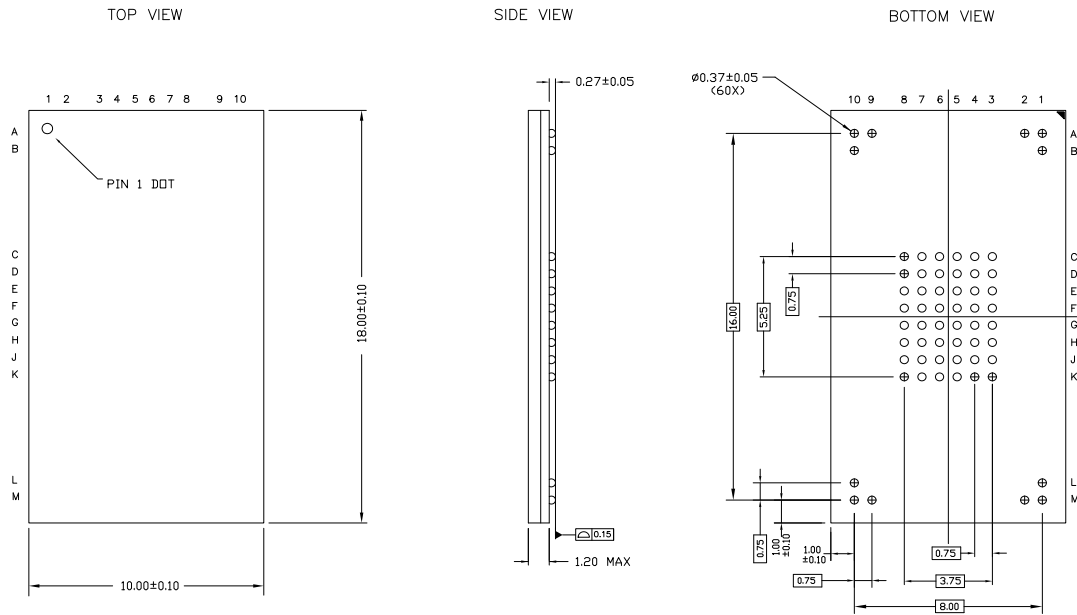
**Figure 24. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160**



51-85160 \*E

**Package Diagrams** (continued)

**Figure 25. 60-ball FBGA (10 × 18 × 1.2 mm) BK60B Package Outline, 002-00193**



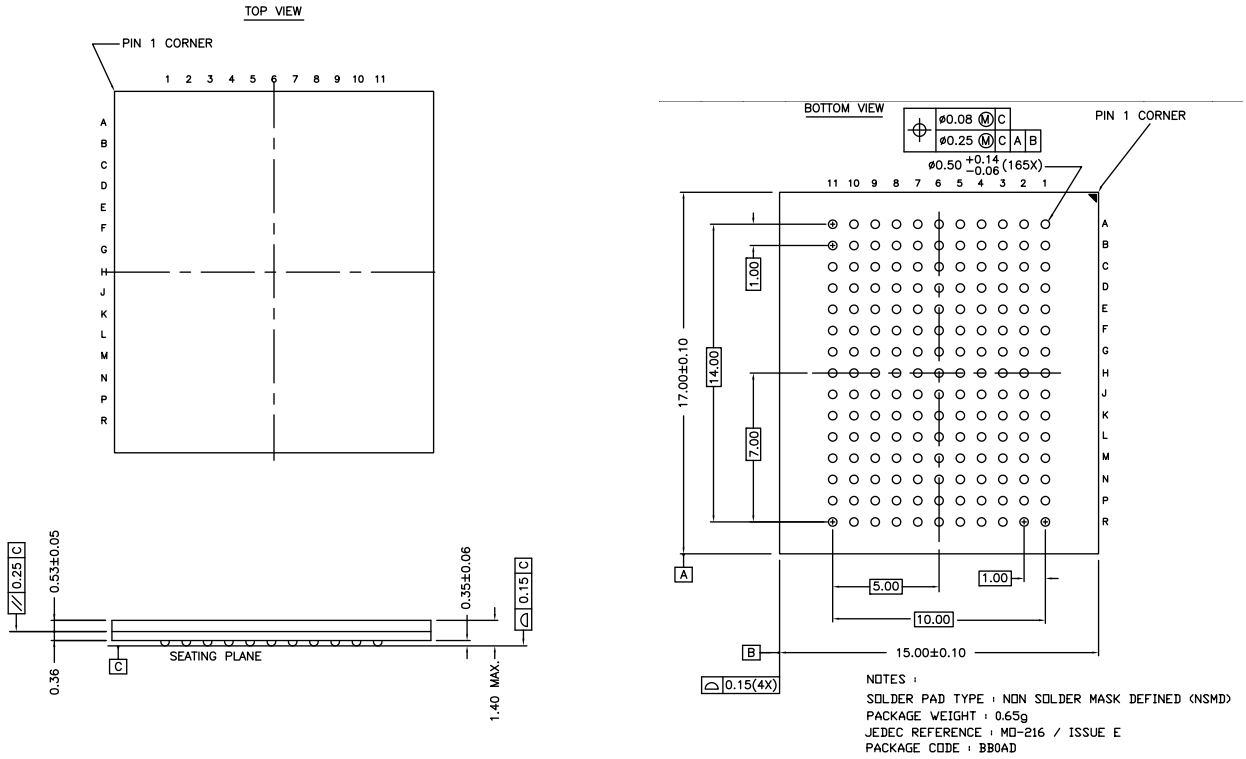
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC : PUB 95, DESIGN GUIDE 4.5

002-00193 \*\*

**Package Diagrams** (continued)

**Figure 26. 165-ball FBGA (15 × 17 × 1.40 mm (0.50 Ball Diameter)) Package Outline, 51-85195**



51-85195 \*D



## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JESD	JEDEC Standards
nvSRAM	nonvolatile Static Random Access Memory
RoHS	Restriction of Hazardous Substances
RWI	Read and Write Inhibited
TSOP II	Thin Small Outline Package

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees celsius
Hz	hertz
Kbit	kilobit
kHz	kilohertz
kΩ	kilohm
μA	microampere
mA	milliampere
μF	microfarad
Mbit	megabit
MHz	megahertz
μs	microsecond
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

All errata for this product are fixed, effective date code 1431 (YY=14, WW=31). For more information, refer to datasheet 001-67793 Rev. \*J, or contact Cypress Technical Support at <http://www.cypress.com/support>.

**Document History Page**

Document Title: CY14B116L/CY14B116N/CY14B116S/CY14E116L/CY14E116N/CY14E116S, 16-Mbit (2048K × 8/1024K × 16/512K × 32) nvSRAM				
Document Number: 001-67793				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3186783	GVCH	03/02/2011	New datasheet.
*A	3202367	GVCH	03/22/2011	Updated <a href="#">DC Electrical Characteristics</a> (Changed maximum value of I <sub>SB</sub> parameter from 3 mA to 500 µA).
*B	3459888	GVCH	12/09/2011	<p>Changed status from “Advance” to “Preliminary”.</p> <p>Updated <a href="#">Pinouts</a> (Updated <a href="#">Figure 6</a> and <a href="#">Figure 7</a>).</p> <p>Updated <a href="#">Pin Definitions</a> (Updated ZZ pin description).</p> <p>Updated <a href="#">DC Electrical Characteristics</a> (Changed maximum value of I<sub>CC1</sub> parameter from 70 mA to 95 mA for t<sub>RC</sub> = 25 ns, changed maximum value of I<sub>CC1</sub> parameter from 50 mA to 75 mA for t<sub>RC</sub> = 45 ns, changed typical value of I<sub>CC3</sub> parameter from 35 mA to 50 mA, changed maximum value of I<sub>CC4</sub> parameter from 10 mA to 6 mA, changed maximum value of I<sub>SB</sub> parameter from 500 µA to 650 µA, added V<sub>CAP</sub> parameter values for CY14C116X, changed minimum value of V<sub>CAP</sub> parameter from 20 µF to 19 µF, changed typical value of V<sub>CAP</sub> parameter from 27 µF to 22 µF respectively, added <a href="#">Note 16</a> and referred the same note in V<sub>CAP</sub> parameter).</p> <p>Updated <a href="#">Thermal Resistance</a> (Added values).</p> <p>Updated <a href="#">AC Switching Characteristics</a> (Added <a href="#">Note 20</a> and referred the same note in Parameters column).</p> <p>Updated <a href="#">AutoStore/Power-Up RECALL Characteristics</a> (Changed maximum value of t<sub>HRECALL</sub> parameter from 40 ms to 60 ms for CY14C116X, changed maximum value of t<sub>HRECALL</sub> parameter from 20 ms to 30 ms for CY14B116X/CY14E116X, changed maximum value of t<sub>WAKE</sub> parameter from 40 ms to 60 ms for CY14C116X, changed maximum value of t<sub>WAKE</sub> parameter from 20 ms to 30 ms for CY14B116X/CY14E116X).</p> <p>Updated <a href="#">Software Controlled STORE and RECALL Characteristics</a> (Changed maximum value of t<sub>RECALL</sub> parameter from 300 µs to 600 µs, changed maximum value of t<sub>SS</sub> parameter from 200 µs to 500 µs).</p> <p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p> <p>Updated <a href="#">Package Diagrams</a> (To current revision).</p>
*C	3510173	GVCH	01/27/2012	<p>Updated <a href="#">Ordering Information</a> (Removed CY14E116N-ZS25XI and added CY14B116N-Z25XI part number).</p> <p>Updated in new template.</p>
*D	3733467	GVCH	09/14/2012	<p>Updated <a href="#">Device Operation</a> (Added <a href="#">Figure 9</a> under <a href="#">Sleep Mode</a>).</p> <p>Updated <a href="#">Maximum Ratings</a> (Changed “Ambient temperature with power applied” to “Maximum junction temperature”).</p> <p>Updated <a href="#">DC Electrical Characteristics</a> (Added V<sub>V<sub>CAP</sub></sub> parameter and its details, added <a href="#">Note 18</a> and referred the same note in V<sub>V<sub>CAP</sub></sub> parameter, also referred <a href="#">Note 19</a> in V<sub>V<sub>CAP</sub></sub> parameter).</p> <p>Updated <a href="#">Capacitance</a> (Changed maximum value of C<sub>IN</sub> and C<sub>OUT</sub> parameters from 7 pF to 11.5 pF).</p> <p>Added <a href="#">Sleep Mode</a> and <a href="#">Figure 17</a> (Corresponding to SLEEP Mode).</p> <p>Updated <a href="#">Package Diagrams</a> (spec 51-85087 (Changed revision from *D to *E)).</p>

**Document History Page** (continued)

Document Title: CY14B116L/CY14B116N/CY14B116S/CY14E116L/CY14E116N/CY14E116S, 16-Mbit (2048K × 8/1024K × 16/512K × 32) nvSRAM Document Number: 001-67793				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*E	4198509	GVCH	01/23/2014	<p>Updated <a href="#">Features</a>:  Removed 2.5 V operating range voltage support.  Added 54-pin TSOP II package related information.  Updated <a href="#">Logic Block Diagram</a>  Updated <a href="#">Device Operation</a>:  Updated <a href="#">AutoStore Operation (Power-Down)</a>:  Removed sentence "The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress."  Updated <a href="#">DC Electrical Characteristics</a>:  Updated Test Conditions of I<sub>SB</sub> parameter and also updated the corresponding values.  Changed maximum value of V<sub>IH</sub> parameter from "V<sub>CC</sub> + 0.3 V" to "V<sub>CC</sub> + 0.5 V".  Updated V<sub>CAP</sub> value from 20 uF to 19.8 uF.  Added Note 20.  Updated <a href="#">Capacitance</a>:  Changed maximum value of C<sub>IN</sub> and C<sub>OUT</sub> parameters from 11.5 pF to 8 pF.  Updated <a href="#">Sleep Mode</a>:  Changed maximum value of t<sub>ZZH</sub> parameter from 20 ns to 70 ns.  Updated <a href="#">Figure 9</a> and <a href="#">Figure 17</a> for more clarity.  Updated <a href="#">Truth Table For SRAM Operations</a> for more clarity.  Updated <a href="#">Ordering Information</a> (Updated part numbers).  Updated <a href="#">Package Diagrams</a>:  Added 54-pin TSOP II package related information (<a href="#">Figure 24</a>).</p>
*F	4303589	GVCH	03/20/2014	<p>Updated <a href="#">Thermal Resistance</a>:  Updated values of <math>\Theta_{JA}</math> and <math>\Theta_{JC}</math> parameters.  Updated to new template.  Completing Sunset Review.</p>
*G	4366689	GVCH	05/01/2014	<p>Updated <a href="#">Device Operation</a>:  Updated <a href="#">Sleep Mode</a>:  Updated description.  Updated <a href="#">Maximum Ratings</a>:  Added Note 14 and referred the same note in "Static discharge voltage".  Updated <a href="#">DC Electrical Characteristics</a>:  Removed "RTC running on backup power supply" in test conditions of I<sub>ZZ</sub> parameter.  Updated <a href="#">AC Switching Characteristics</a>:  Added Note 25 and referred the same note in t<sub>HA</sub> parameter.  Updated <a href="#">Ordering Information</a> (Updated part numbers (Added Part numbers namely CY14B116N-ZSP45XI, CY14B116N-ZSP45XIT, CY14E116S-BZ25XI and CY14E116S-BZ25XIT)).  Added Errata.</p>
*H	4409843	GVCH	06/17/2014	<p>Updated <a href="#">DC Electrical Characteristics</a>:  Updated maximum value of V<sub>V<sub>CAP</sub></sub> parameter to 5.0 V for CY14B116X and CY14E116X.</p>

**Document History Page** (continued)

Document Title: CY14B116L/CY14B116N/CY14B116S/CY14E116L/CY14E116N/CY14E116S, 16-Mbit (2048K × 8/1024K × 16/512K × 32) nvSRAM				
Document Number: 001-67793				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*I	4417851	GVCH	06/24/2014	Updated <a href="#">DC Electrical Characteristics</a> : Added footnote 15 and referred the same note in I <sub>CC4</sub> parameter. Updated <a href="#">Capacitance</a> : Changed maximum value of C <sub>IN</sub> and C <sub>OUT</sub> parameters from 8 pF to 10 pF for 165-ball FBGA package. Added C <sub>IO</sub> parameter. Updated <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> : Added package code for 48-TSOP I package.
*J	4432183	GVCH	07/07/2014	Updated <a href="#">DC Electrical Characteristics</a> : Changed maximum value of V <sub>CAP</sub> parameter from 120.0 μF to 82.0 μF
*K	4456803	ZSK	07/31/2014	Removed Errata section. Added a note at the end of the document mentioning when the errata items were fixed.
*L	4562106	GVCH	11/05/2014	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end. Updated <a href="#">Package Diagrams</a> : spec 51-85160 – Changed revision from *D to *E.
*M	4616093	GVCH	01/07/2015	Changed status from Preliminary to Final. Updated <a href="#">Package Diagrams</a> : spec 51-85183 – Changed revision from *C to *D.
*N	5364155	GVCH	22/07/2016	Added 60-ball FBGA package related information in all instances across the document. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> : Added spec 002-00193 **. spec 51-85195 – Changed revision from *C to *D. Updated to new template.



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