DESCRIPTION

Demonstration Circuit DC787A-A and DC787A-B showcase the LTC4252C-1 and LTC4252C-2 Hot Swap controllers in an AdvancedTCA application. The DC787A-A uses the LTC4252C-1 with latch off after an overcurrent fault condition, while the DC787A-B uses the LTC4252C-2 with auto retry. Included on board is the connection sense circuitry, zero volt transient reservoir capacitor management, opto isolator to drive a 1mA-input 48V brick, input clamping and snubbing, thermal layout for ORing diodes, input and return fuses, LEDs to indicate the presence of various voltages and signals, high voltage layout rules and printed nomenclature to facilitate integration into a working system.

A distinct line of demarcation runs the length of the board, separating high voltage −48V referred potentials from return. Thermal layout around the ORing diodes achieves adequate cooling without the need for connector mass, air flow, or heat sinks. 93mil turret holes accommodate up to 12 gauge wires for in-situ testing.

Design files for this circuit board are available. Call the LTC factory.

Table 1.

Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Nominal Input Voltage		48V
Maximum Input Voltage		100V
Minimum Output Current		5.6A
Minimum Shutdown Voltage	Iin<10mA, excluding LED current	32V

QUICK START PROCEDURE

Board Layout

The top of the board contains the core Hot Swap controller and associated components, along with fuses and LEDs. Also on top are the "B" side ORing diodes and all connection turrets. The large turrets may be removed to permit installation of 12 gauge or smaller wire. None of the turrets are swaged.

The bottom of the board contains ATCA-specific components (connection sense and zero volt transient reservoir capacitor circuits) and the LED current limiting resistors. Also on the bottom are the "A" side ORing diodes, the LTC4252C supply bypass capacitor, and R2, a zero ohm jumper.

The ORing diodes are expected to carry a full load of approximately 5A. With 600mV forward drop, this amounts to 3W dissipation per diode. Since only one of two ORing diodes conducts at a time, they share the same thermal layout, at least as far as the pinout permits. D1 and D2 are sandwiched at the tabs (cathode), whereas D10 and D11 can only share the anode leads. Thus D1 and D2 have superior thermal efficiency and operate ≈10°C cooler at full power.

In a real application air flow, heatsinks, the connector and the availability of multiple power and ground planes dominate the configuration and thermal efficacy of the layout. Holding the tab to a maximum temperature of ≈90°C is very conservative according to Diodes, Inc. In the case of DC787A the tab temperature of D10 or D11 reaches 90°C with the board laying flat on a bench with no air flow. D1 and D2 run 10°C cooler owing to the conjoined tabs and expansive return metal.

Circuit Notes

DC787A provides at least 5.5A under all conditions, implying that 200W is consumable down to 36.4V. Undervoltage lockout has been skewed as low as possible, brushing up against the 32V ATCA minimum limit in order to maximize the amount of energy that can be extracted from the zero volt transient reservoir capacitors. Thus the circuit will continue to supply power at a voltage lower than where 200W is available. If you connect a constant power load and gradually reduce the input voltage, the LTC4252C circuit breaker could trip before the UV pin cuts off the power. This condition is reset by pulsing UV low or by cycling power to the circuit.

The fuse ratings are skewed with 10A on return and 7A on input. Current limiting and voltage spacing on the ENABLE pins is guaranteed by 1206 resistors R5, R6, R9 and R10. EARLY pins are not needed by the LTC4252C.

Operation

Simply connect power to A, B, or both, and short the associated ENABLE pins to simulate the backplane and activate the LTC4252C. The jumper allows selection of either an opto isolator output (collector and emitter are available at C and E turrets), or direct examination of PWRGD#. If the opto is selected, LED D6 is also in line and you get a visual indication of the condition of PWRGD#.

D5 shows the presence of voltage on the reservoir capacitor, which is attached to the "Zero Volt Transient Reservoir Capacitor" turrets. D7 and D8 indicate at least some input on A and B, ahead of the fuses and diodes. Under normal operation D7 and D8 should light up any time voltage is present, and D5 and D6 light up when the LTC4252C turns on. D6 (PWRGD#) stays lit in overvoltage conditions. PWRGD# is reset only by an undervoltage condition, or by dropout on the VIN pin of the LTC4252C. Thus overvoltage transients will not punch a hole in the PWRGD# signal. Since UV essentially monitors the output voltage during an input dropout event, PWRGD# remains asserted during these intervals.

Note that the PWRGD# LED D6 is dim compared to the others because it is running only 2mA.

In summary, when power is applied and the associated ENABLE is activated, the output will turn on. First D7 and D8 light up, then D5 and D6 follow. If the full 3,800µF reservoir is present, D5 will light up gradually. If the output is overloaded, the LTC4252C current limits for somewhere between 1.8ms and 6.5ms. If the overload is still present after this interval, the circuit latches off. Reset is affected by extracting the card.

Converting to Normal −48V Applications

To disable the ATCA circuits, simply leave off the reservoir capacitors, and remove D12 (D4 becomes superfluous). If you want to do a more thorough job, remove R5, R6, R9, R10, R11, Q1, Q2, D4, and D12.

If diode ORing is unnecessary on the return side, simply attach −48RTN to the circuit board at terminal −48RTN OUT, thereby bypassing D1, D2, F1 and F2. Removing D1 and D2 is difficult because of thermal relief and multiple pins. If you must remove the diodes, use two Weller WTCPT soldering irons equipped with PTE8 (800°C) tips.

Connecting a conventional short pin is easy once D1 and D2 are bypassed: removing R2 gives access to the top of the UV/OV divider networks.

NOTE: The top mark code for the LTC4252CCMS-1 is LTGFC, while that of the LTC4252CCMS-2 is LTGFD.

ENABLE Detection

Q1 and Q2 detect the ENABLE pins, irrespective of the input voltage. One peculiar condition may raise eyebrows in some circles. Suppose supply A is present but its RTN side fuse (F1) is blown. Now suppose supply B fails open circuit. This reverse Vbeos Q1 because its base is held at RTN A (+48) while its emitter is pulled to −48V by D1, the load and the LTC4252C circuitry. The same could happen to Q2. In fact, both transistors reverse Vbeo if both F1 and F2 fail. The current is limited to ≈48V/10kΩ, but damage is cumulative. In a bench experiment a transistor was reverse Vbeod with 50mA for 15 minutes, and β was observed to degrade ≈10%. The potential for junction damage is remote given the limited current and unlikeliness of a RTN fuse failure. Nevertheless, if this is cause for concern diode clamps can be added across the base-emitter junctions of Q1 and Q2 to avoid this condition.

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