

1. General description

Planar passivated four quadrant triac in a SOT1292 (IITO3P) package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$). It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- High current TRIAC
- Low thermal resistance
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Insulated tab rated at 2500 V rms

3. Applications

- High current / high surge applications
- High power / industrial controls -- e.g. heating, motors, lighting

4. Quick reference data

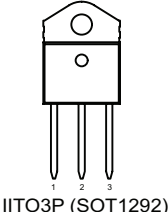
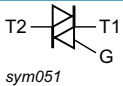
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
Absolute maximum rating				
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 105\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	40	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4 ; Fig. 5	400	A
		full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(init)} = 25\text{ °C}$;	440	A
T_j	junction temperature		150	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+$ $T_j = 25\text{ °C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-$ $T_j = 25\text{ °C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-$ $T_j = 25\text{ °C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G+$ $T_j = 25\text{ °C};$ Fig. 7	-	-	70	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ °C};$ Fig. 9	-	-	80	mA
V_T	on-state voltage	$I_T = 56.6\text{ A}; T_j = 25\text{ °C};$ Fig. 10	-	1.2	1.5	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ °C}; (V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	750	-	-	V/ μ s
		$V_{DM} = 536\text{ V}; T_j = 150\text{ °C}; (V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 125\text{ °C}; I_{T(RMS)} = 20\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ gate open circuit	20	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 150\text{ °C}; I_{T(RMS)} = 20\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ gate open circuit	10	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>IITO3P (SOT1292)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA41-800B	IITO3P	plastic single-ended through-hole package; isolated heatsink mounted; 1 mounting hole; 3-lead TO3P	SOT1292

7. Marking

Table 4. Marking codes

Type number	Marking codes
BTA41-800B	BTA41-800B

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 105^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	40	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$; $T_{j(\text{init})} = 25^\circ\text{C}$; Fig. 4 ; Fig. 5	400	A
		full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(\text{init})} = 25^\circ\text{C}$;	440	A
I^2t	I^2t for fusing	$t_p = 10\text{ms}$; sine wave	800	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 150\text{mA}$	150	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t_p = 20\mu\text{s}$	8	A
P_{GM}	peak gate power	$t_p = 20\mu\text{s}$	40	W
$P_{G(AV)}$	average gate power	over any 20 ms period	1	W
T_{stg}	storage temperature		-40 to 150	$^\circ\text{C}$
T_j	junction temperature		150	$^\circ\text{C}$

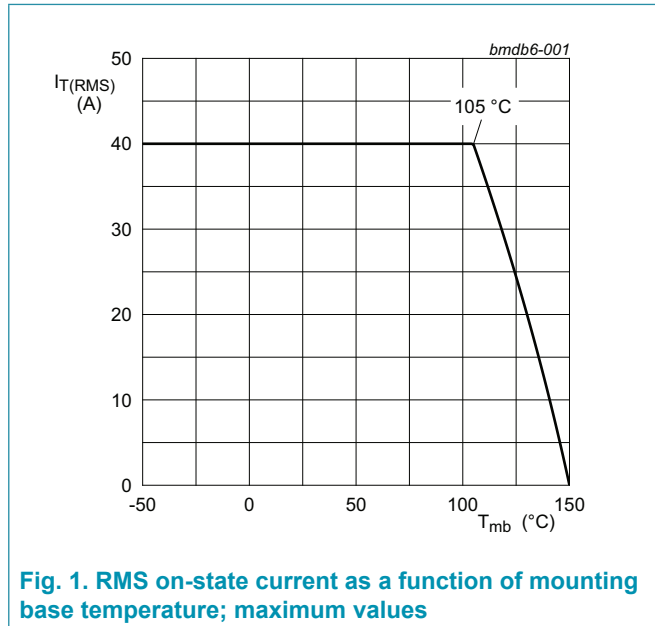


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

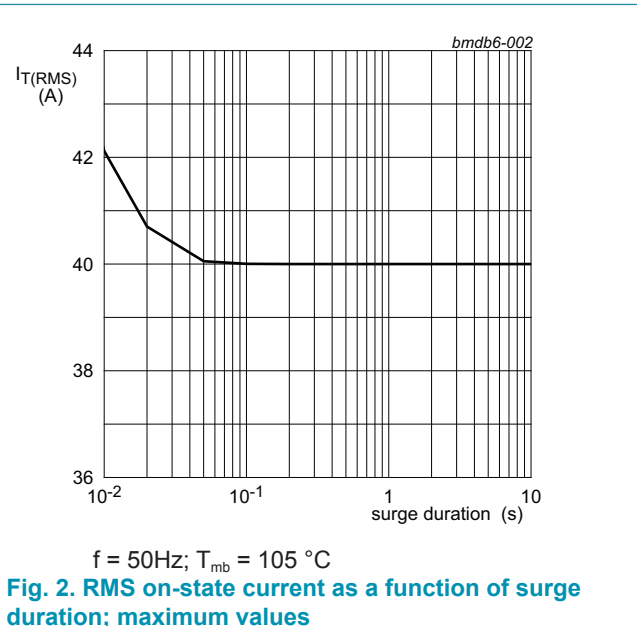


Fig. 2. RMS on-state current as a function of surge duration; maximum values
 $f = 50\text{Hz}$; $T_{mb} = 105^\circ\text{C}$

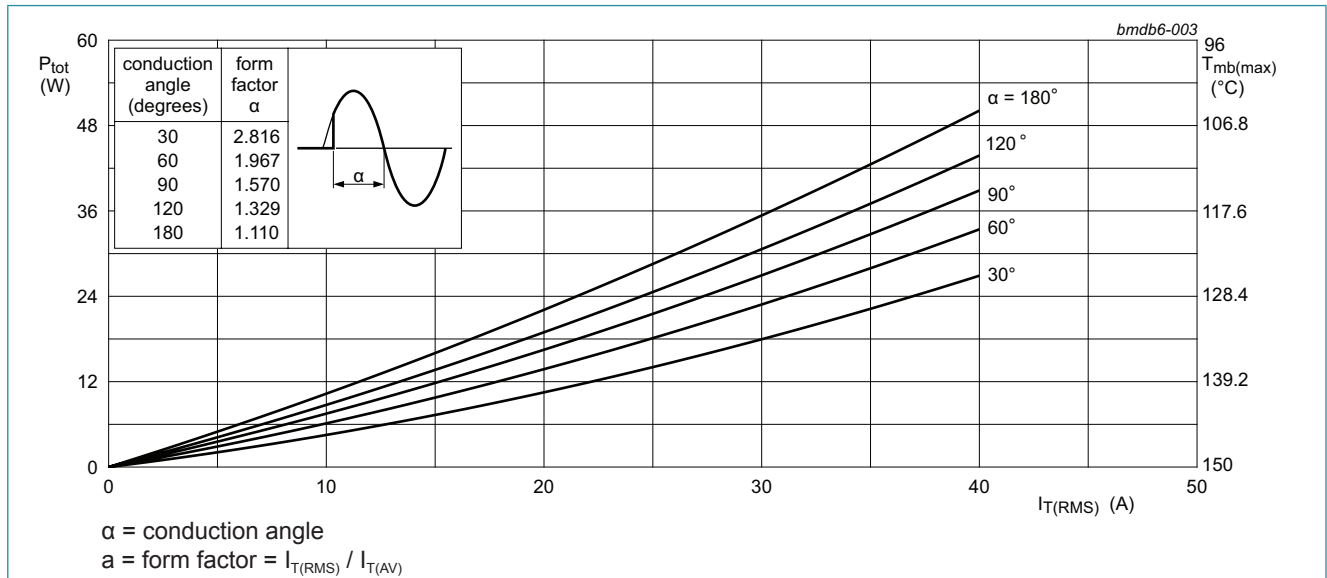


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

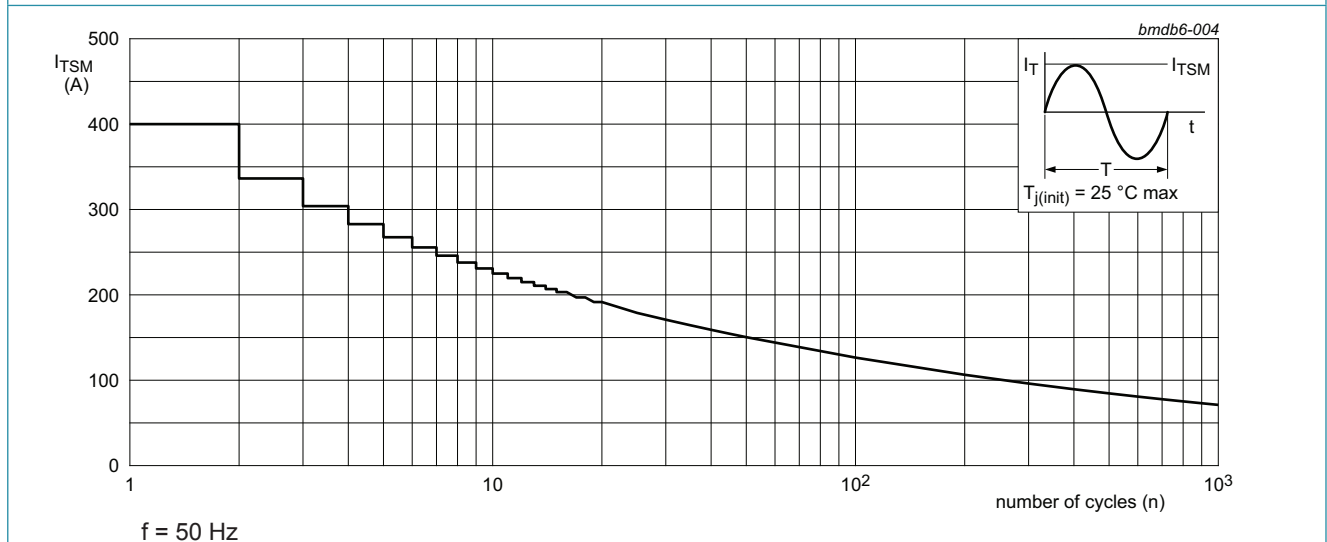


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

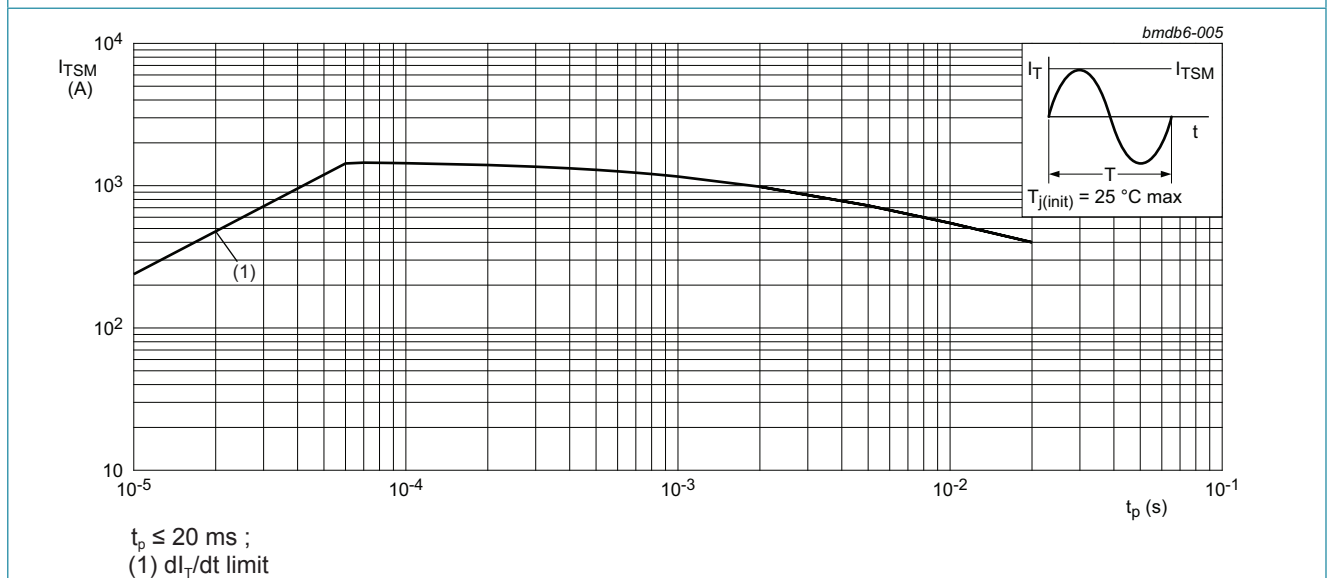


Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

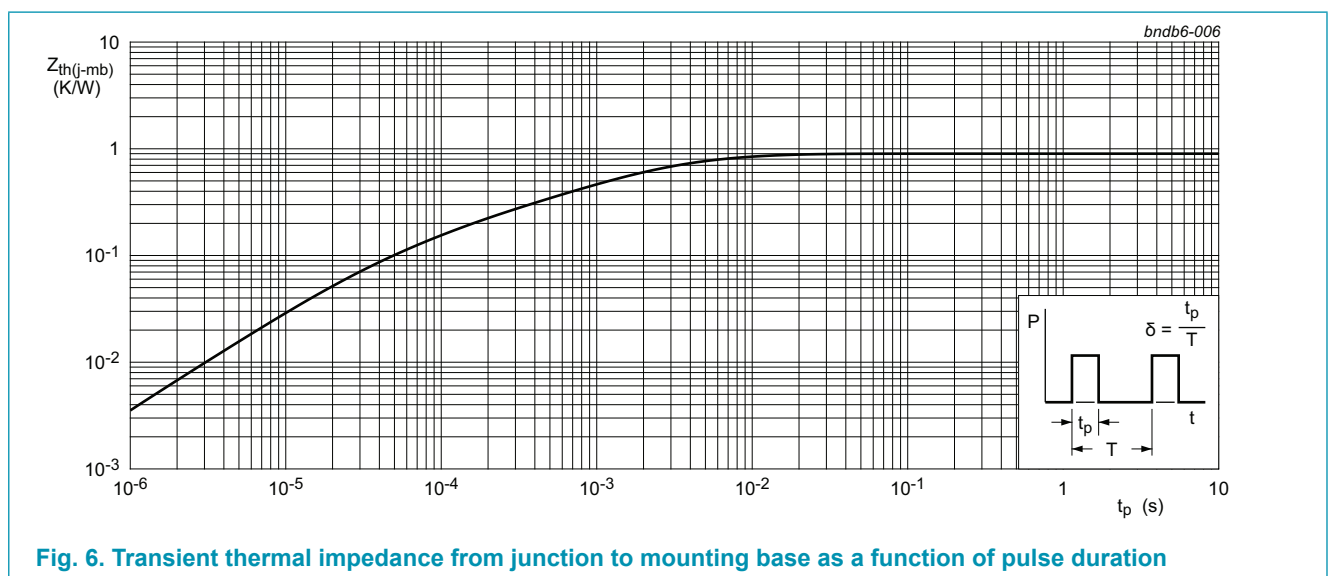


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Isolation characteristics

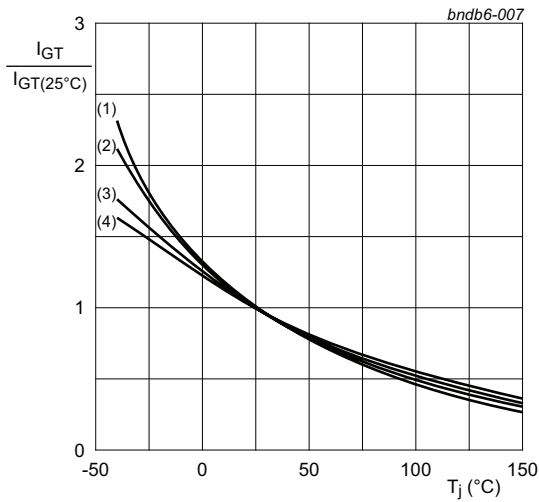
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminal to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T _h = 25 °C	-	-	2500	V

11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	-	-	70	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	100	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	160	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	100	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	100	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	80	mA
V_T	on-state voltage	$I_T = 56.6\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.8	1.3	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 150\text{ °C}$; Fig. 11	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$	-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 150\text{ °C}$	-	-	2.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	750	-	-	V/ μs
		$V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 20\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit	20	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 20\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit	10	-	-	A/ms



- (1) T2- G+
- (2) T2- G-
- (3) T2+ G-
- (4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

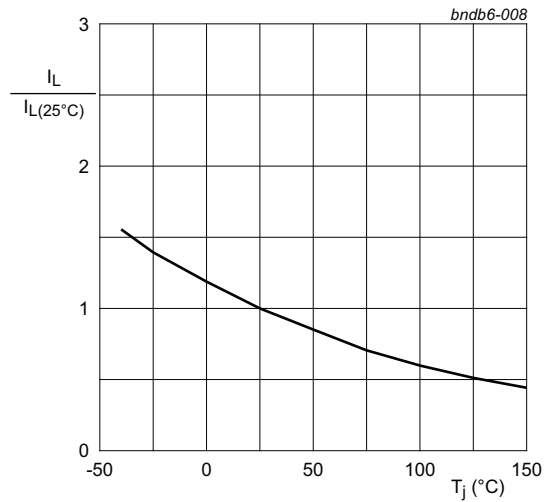


Fig. 8. Normalized latching current as a function of junction temperature

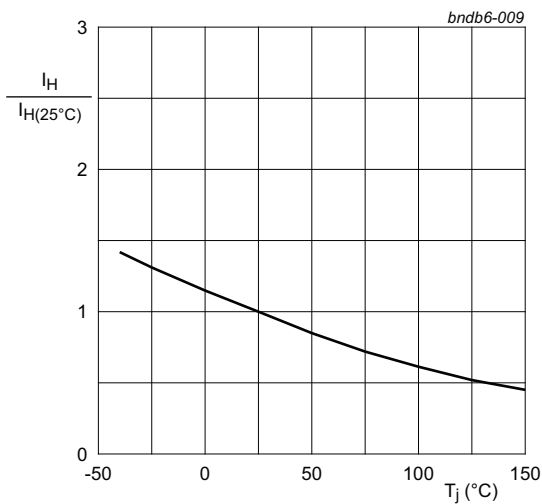
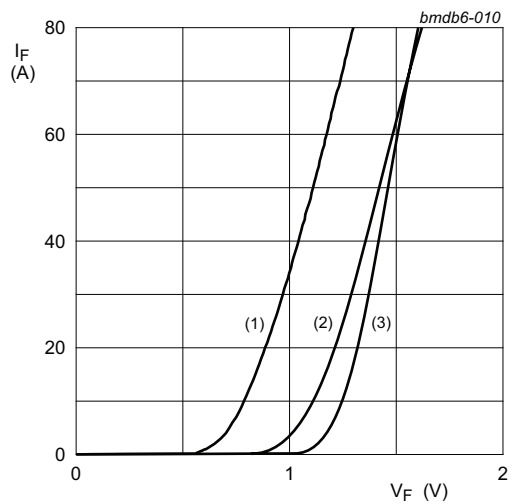


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.063 \text{ V}$; $R_s = 0.0074 \ \Omega$

- (1) $T_j = 150 \ ^{\circ}\text{C}$; typical values
- (2) $T_j = 150 \ ^{\circ}\text{C}$; maximum values
- (3) $T_j = 25 \ ^{\circ}\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

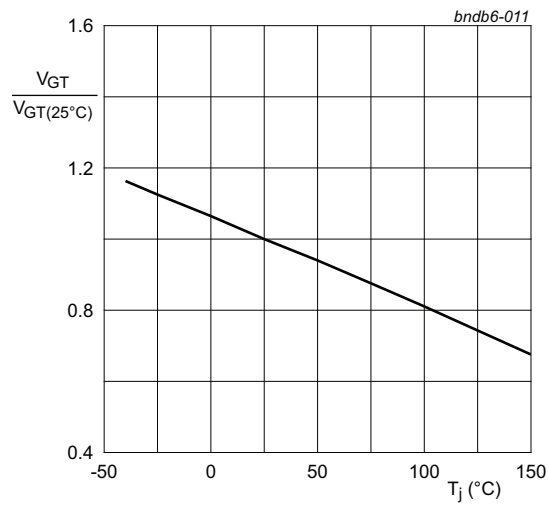
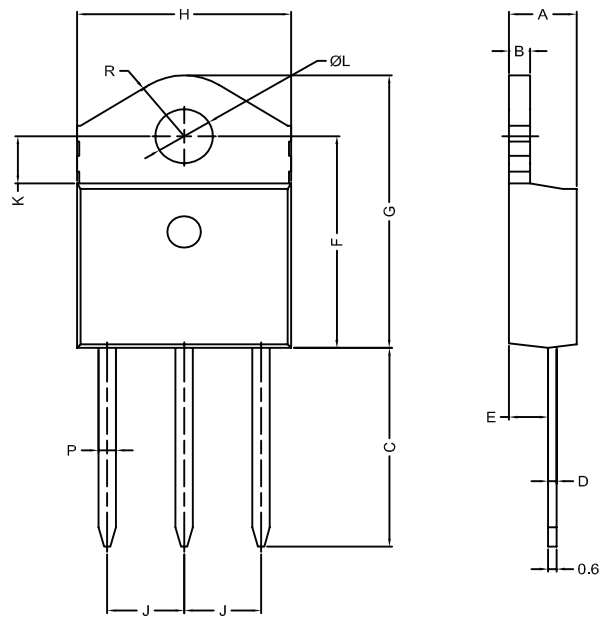


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended through-hole package; isolated heatsink mounted; 1 mounting hole; 3-lead TO3P

SOT1292



Unit		A	B	C	D	E	F	G	H	J	K	L	P	R
mm	min	4.75	1.45	14.35	0.50	2.70	15.80	20.40	15.10	5.40	3.40	4.08	1.20	4.6
	max	4.95	1.55	15.60	0.70	2.90	16.50	21.10	15.50	5.65	3.65	4.17	1.40	(typ)

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT1292		-				

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 10 July 2017

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