

μPA2812T1L

P-channel MOSFET

−30 V, −30 A, 4.8 mΩ

R07DS0762EJ0101

Rev.1.01

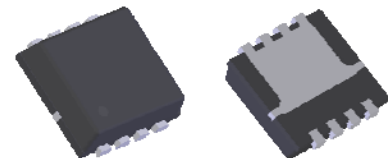
May 28, 2013

Description

The μPA2812T1L is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DS} = -30\text{ V}$ ($T_A = 25^\circ\text{C}$)
- Low on-state resistance
— $R_{DS(on)} = 4.8\text{ m}\Omega$ MAX. ($V_{GS} = -10\text{ V}$, $I_D = -30\text{ A}$)
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader
- Pb-free and Halogen free



8-pin HVSON(3333)

Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2812T1L-E2-AT *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (3333) typ. 0.028 g

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DS}	−30	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GS}	±20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	±30	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±120	A
Total Power Dissipation *2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	3.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T3}	52	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current *3	I_{AS}	25	A
Single Avalanche Energy *3	E_{AS}	62	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	2.4	°C/W

Notes: *1. $PW \leq 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

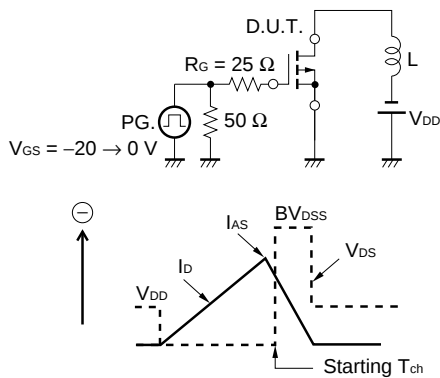
*3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -15\text{ V}$, $R_G = 25\text{ }\Omega$, $V_{GS} = -20 \rightarrow 0\text{ V}$, $L = 100\text{ }\mu\text{H}$

Electrical Characteristics (T_A = 25°C)

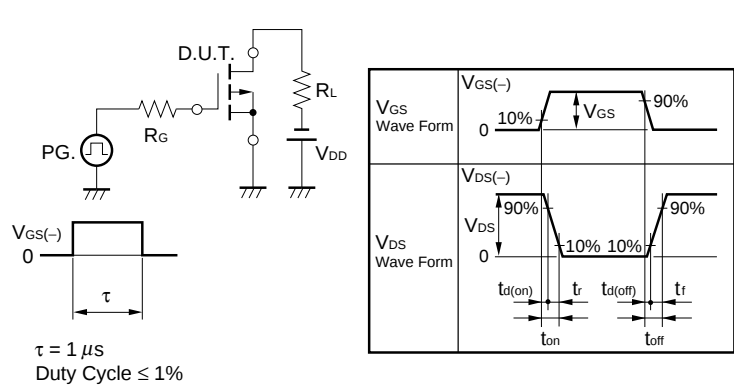
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μA	V _{DS} = -30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate Cut-off Voltage	V _{GS(off)}	-1.0		-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance *1	y _{fs}	8.0			S	V _{DS} = -10 V, I _D = -15 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		3.8	4.8	mΩ	V _{GS} = -10 V, I _D = -30 A
	R _{DS(on)2}		6.4	9.9	mΩ	V _{GS} = -4.5 V, I _D = -15 A
Input Capacitance	C _{iss}		3740		pF	V _{DS} = -10 V,
Output Capacitance	C _{oss}		1775		pF	V _{GS} = 0 V,
Reverse Transfer Capacitance	C _{rss}		1500		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		24		ns	V _{DD} = -15 V, I _D = -15 A, V _{GS} = -10 V, R _G = 10 Ω
Rise Time	t _r		53		ns	
Turn-off Delay Time	t _{d(off)}		176		ns	
Fall Time	t _f		252		ns	
Total Gate Charge	Q _G		100		nC	V _{DD} = -24 V,
Gate to Source Charge	Q _{GS}		11		nC	V _{GS} = -10 V,
Gate to Drain Charge	Q _{GD}		48		nC	I _D = -30 A
Body Diode Forward Voltage *1	V _{F(S-D)}		0.85		V	I _F = 30 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		196		ns	I _F = 30 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		297		nC	

Note: *1. Pulsed

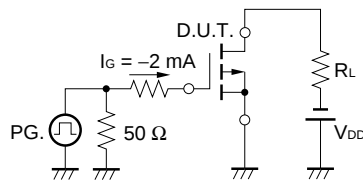
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

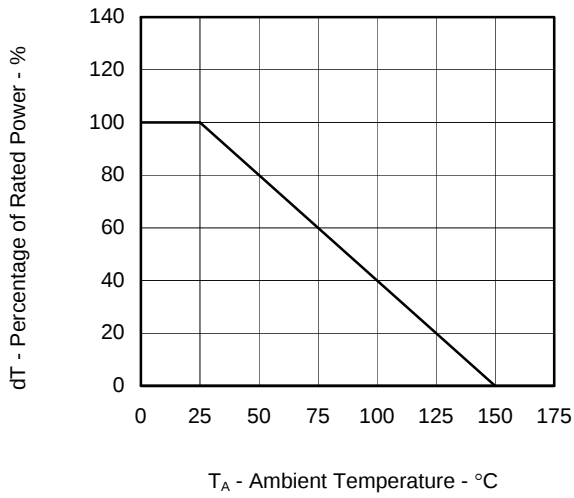


TEST CIRCUIT 3 GATE CHARGE

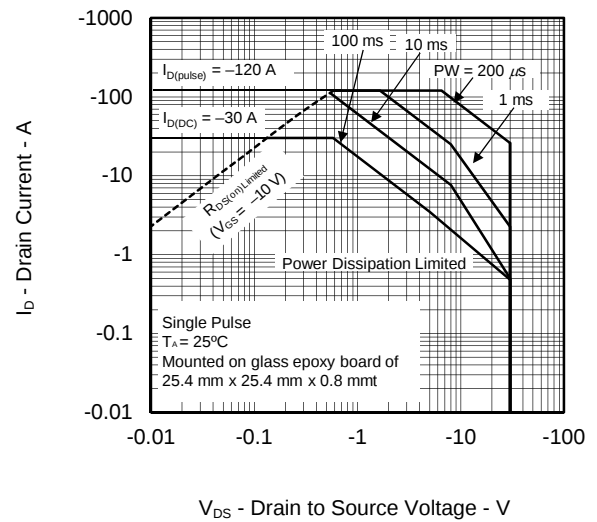


Typical Characteristics ($T_A = 25^\circ\text{C}$)

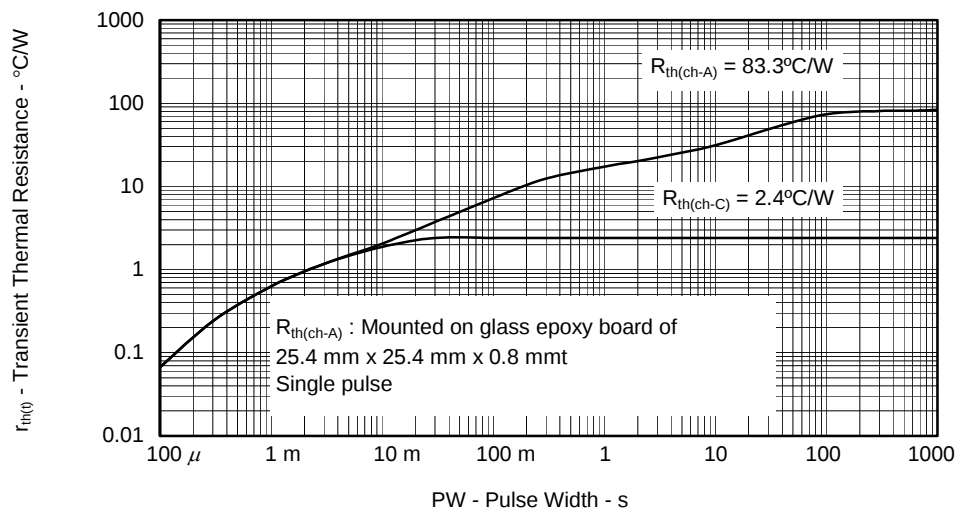
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



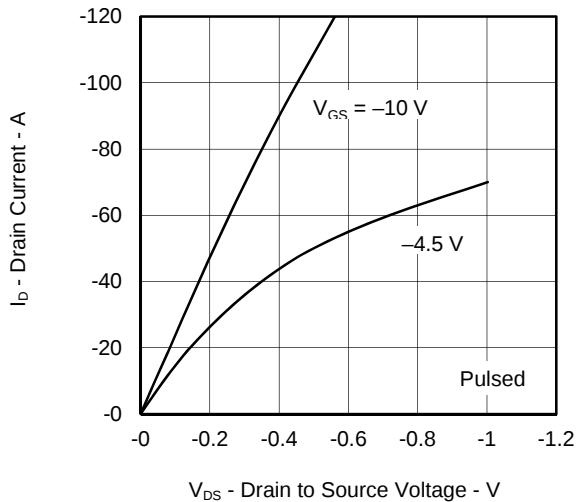
FORWARD BIAS SAFE OPERATING AREA



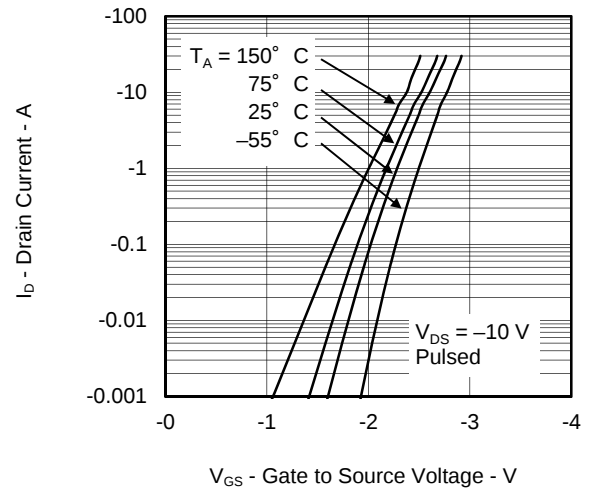
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



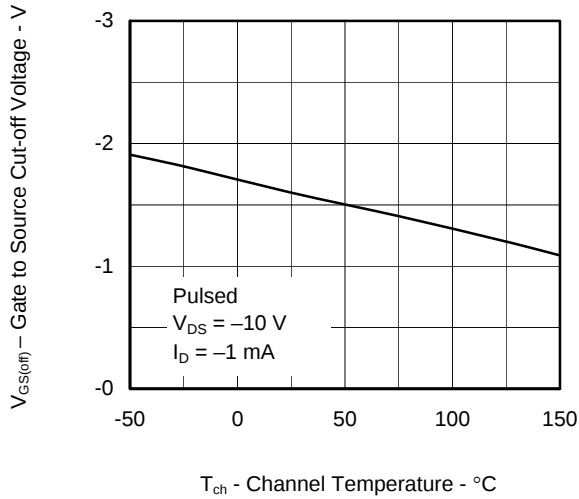
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



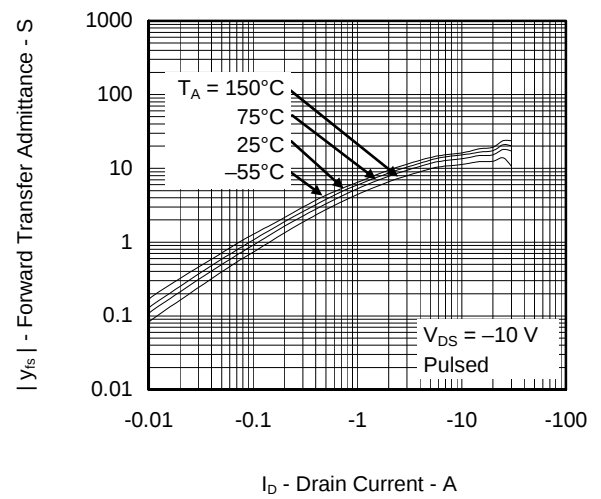
FORWARD TRANSFER CHARACTERISTICS



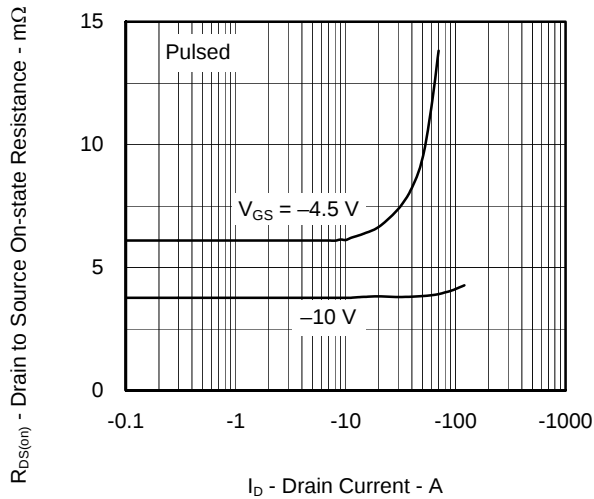
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



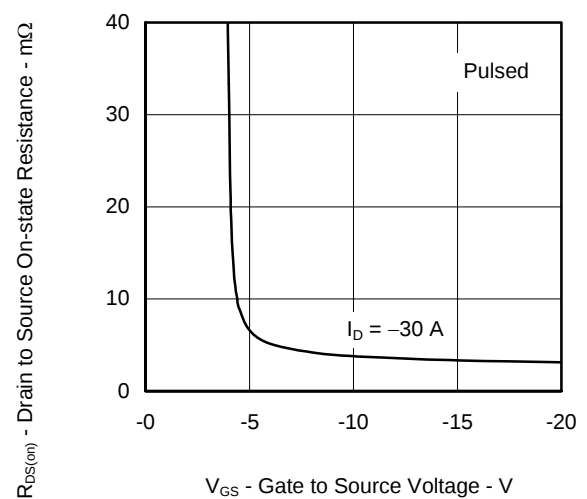
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



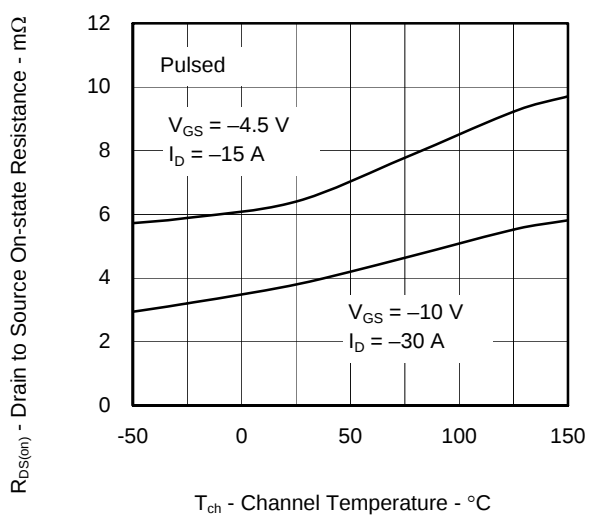
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



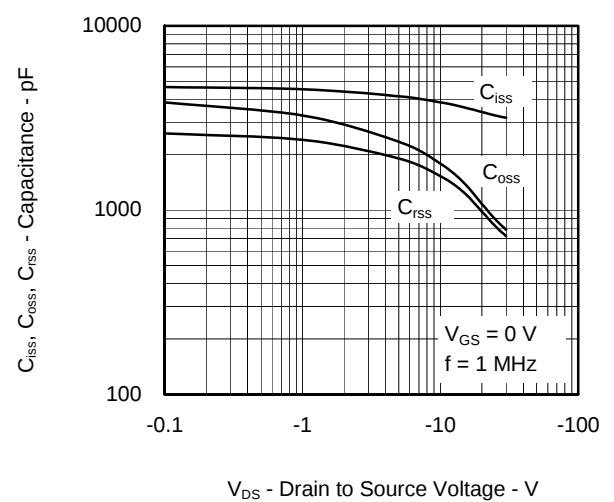
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



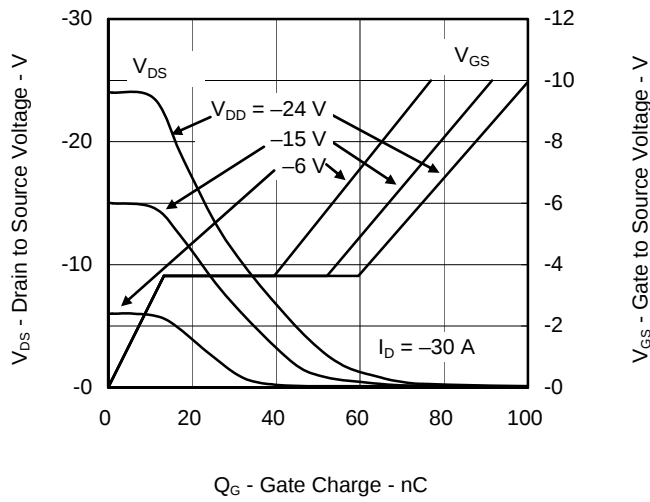
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



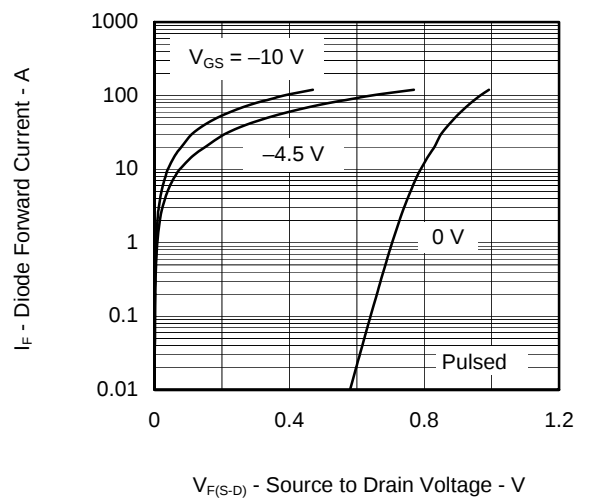
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

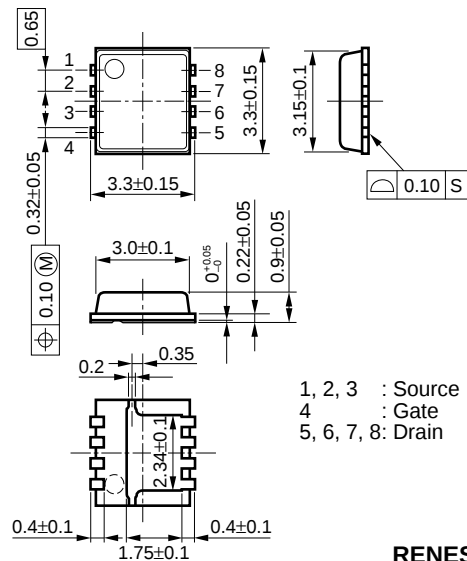


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



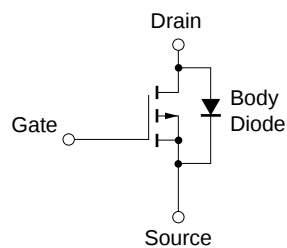
Package Drawings (Unit: mm)

8-pin HVSON (3333)



RENESAS Package code : PVS0008JD-A

Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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